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Preprint

This is the submitted version of a paper presented at *21st International Conference on Optical MEMS and Nanophotonics, OMN 2016, 31 July 2016 through 4 August 2016*.

Citation for the original published paper:

Niklaus, F., Fischer, A C. (2016)

Heterogeneous 3D integration of MOEMS and ICs.

In: *International Conference on Optical MEMS and Nanophotonics* IEEE Computer Society

<https://doi.org/10.1109/OMN.2016.7565909>

N.B. When citing this work, cite the original published paper.

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Heterogeneous 3D Integration of MOEMS and ICs

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Abstract— Heterogeneous integration of micro-opto-electromechanical systems (MOEMS) and integrated circuits (ICs) allows the combination of high-quality optical and photonic MOEMS materials such as monocrystalline silicon (Si) with standard CMOS-based electronic circuits in order to realize complex optical systems. In this paper, we will present examples of such heterogeneous optical systems, including CMOS-integrated SiGe bolometer arrays and CMOS-integrated Si micro-mirror arrays.

Keywords— Wafer-level heterogeneous 3D integration; MEMS; MOEMS; CMOS; IC; micro-mirror arrays; bolometer arrays;

I. INTRODUCTION

This paper presents state-of-the-art wafer-level heterogeneous 3D integration technologies that are suitable to realize high-performance MOEMS devices. Wafer-level heterogeneous 3D integration is defined within this paper as wafer-to-wafer joining, processing and interconnecting materials as well as components that are formed by different base technologies. Heterogeneous 3D integration technologies enable the combination of high-performance MOEMS, MEMS and NEMS materials on top of standard IC wafers. That way, complex systems that are not possible to manufacture with other micro-manufacturing techniques, such as monolithic integration with inherently stringent limitations on material combinations and processing temperature, can be realized.

II. WAFER-LEVEL HETEROGENEOUS 3D INTEGRATION OF MOEMS AND IC TECHNOLOGY

Heterogeneous 3D integration technologies for MOEMS and IC technology can be placed in two broad categories: (1) heterogeneous integration using via-first processes as exemplified in Fig. 1a) and (2) heterogeneous integration using via-last processes as exemplified in Fig. 1b). In heterogeneous integration using via-first processes, vias that establish the mechanical and electrical contacts between components on the different substrates are defined during the bonding process. In heterogeneous integration using via-last processes, the devices are first bonded to each other and the vias defined thereafter. Decoupling MOEMS and CMOS processing enables the use of high-performance MOEMS materials with processing conditions that are not affected by limitations in terms of material compatibility and temperature budget posed by CMOS processing. Both heterogeneous 3D integration approaches enable the realization of MOEMS devices from virtually any solid material directly on top of CMOS electronics.

Fig. 1. a) Example of heterogeneous 3D integration using a via-first process. b) Example of heterogeneous 3D integration using a via-last process.

Both, via-first and via-last heterogeneous 3D integration platforms are being actively developed and commercially exploited [1, 2]. An early example of employing a via-first process is a 32×32 monocrystalline silicon mirror array with individual mirror dimensions of $1 \times 1 \text{ mm}^2$ [3]. Examples of heterogeneous MOEMS and IC 3D integration by via-last processes have been proposed for the realization of infrared bolometer arrays [4] as well as tilting [5] and piston-type [6, 7] micro-mirror arrays. In this paper, we present examples of such via-last integration processes for the realization of SiGe bolometer arrays for infrared imaging applications and monocrystalline silicon micro-mirror arrays for spatial light modulators used in maskless lithography applications.

III. INFRARED BOLOMETER IMAGING ARRAYS

Infrared imaging, often referred to as thermal imaging, is quickly spreading beyond its initial defense-related applications into areas as thermography, medical imaging, industrial process control, person detection/counting, automotive and consumer products. We have developed infrared microbolometer focal plane arrays utilizing monocrystalline silicon/silicon-germanium (Si/SiGe) quantum-well thermistors that are heterogeneously integrated on top of pre-fabricated CMOS-based read-out integrated circuit wafers [4]. These microbolometer arrays consist of 384×288 pixels with a

pixel pitch of 25 μm . As indicated in Fig. 2, the microbolometer current path through the thermistor material is vertical to the thermistor surface through the Si/SiGe quantum-well layers. To achieve a high temperature coefficient of resistance (TCR), low doped, wide and Ge-rich quantum well layers with a measured TCR of $-2.9\%/K$ have been used.

Fig. 2. a) Simplified illustration of a single microbolometer pixel, including the hidden contact legs as well as the via posts serving as interconnection between the thermistor and the bolometer legs. b) Schematic cross-section of the microbolometer with current path through the Si/SiGe quantum-well thermistor. The trench separates the highly doped Si between the upper contacts. c) Tilted SEM image of the microbolometer array. d) Video image frame taken with a fully integrated and packaged Si/SiGe quantum-well infrared microbolometer focal plane array.

The high-performance monocrystalline Si/SiGe quantum-well thermistor material cannot be directly deposited on top of the CMOS wafer since the epitaxial deposition process requires a monocrystalline silicon seed layer and exceeds allowed process temperatures for CMOS electronic circuits. Therefore, the Si/SiGe thermistor material is deposited on an SOI wafer, which is subsequently transferred to a preprocessed CMOS substrate using a via-last heterogeneous integration process.

IV. MONOCRYSTALLINE SILICON MICRO-MIRROR ARRAYS

Spatial light modulators (SLMs) and micro-mirror arrays have been used for more than a decade in video projection systems. In general, SLMs enable the modulation of phase, amplitude, and polarization of light. Micro-mirror arrays have been employed for applications including laser-pulse shaping, phase aberration correction, wave-front control, optical switching, mask writing, and maskless lithography applications. For the latter two applications, the requirements in terms of optical and mechanical quality on micro-mirror arrays are very high. We demonstrated the first high-resolution SLM chip with one million tilting micro-mirrors made of monocrystalline silicon that are integrated on analog high-voltage CMOS driving electronics [5]. The SLM employs 2048×512 micromirrors with a pitch of 16 μm . The silicon mirror membranes are 340 nm thick and are located at a very well defined distance of 700 nm from the corresponding electrodes on the underlying CMOS circuits. The mirror vias have a diameter of 2 μm , and the mirror hinges are 600 nm wide.

Fig. 3. a) Packaged one-megapixel monocrystalline-silicon micromirror array. b) SEM image of the SLM depicting the micromirrors that were individually deflected to different tilting angles by the underlying high-voltage CMOS electronics.

The monocrystalline Si micro-mirrors exhibit an excellent surface roughness below 1-nm root mean square, do not show any imprinting behavior, and operate drift free. A fully packaged one-megapixel SLM is shown in Fig. 3a) and an SEM image depicting a selection of tilted micro-mirrors from an array is shown in Fig. 3b).

V. CONCLUSIONS

Wafer-level heterogeneous 3D integration technologies allow the combination of a variety high-performance materials and sub-systems to realize advanced MOEMS devices. Thus, compromises in the material selection can be avoided and the same real estate on the chip can be used very efficiently both for the MOEMS devices and the integrated circuits. These features enable complex system solutions with high integration densities and high performances. As a consequence, the overall dimensions and ultimately the manufacturing cost of the MOEMS solutions can be reduced.

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