<http://www.diva-portal.org>

Preprint

This is the submitted version of a paper presented at *18th European Conference on Power Electronics and Applications (EPE), SEP 05-09, 2016, GERMANY*.

Citation for the original published paper:

Jahn, I., Townsend, C D., de la Parra, H Z. (2016)

Model-Predictive Modulation Strategy for a Hybrid Si-SiC Cascaded H-Bridge Multi-Level Converter

In: *2016 18TH EUROPEAN CONFERENCE ON POWER ELECTRONICS AND APPLICATIONS (EPE'16 ECCE EUROPE)* IEEE

European Conference on Power Electronics and Applications

<https://doi.org/10.1109/EPE.2016.7695434>

N.B. When citing this work, cite the original published paper.

Permanent link to this version:

<http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-197012>

Model-Predictive Modulation Strategy for a Hybrid Si-SiC Cascaded H-Bridge Multi-Level Converter

I.Jahn*, C.D. Townsend and H. Zelaya de la Parra

ABB Corporate Research

SE-72178 Västerås, Sweden

*KTH Royal Institute of Technology

SE-10044 Stockholm, Sweden

Mail: ilka@kth.se, christopher.townsend@se.abb.com, hector.zelaya@se.abb.com

URL: <http://new.abb.com/>

Keywords

<<Silicon>>, <<Silicon Carbide (SiC)>>, <<Multilevel converters>>, <<STATCOM>>, << Modulation strategy>>

Abstract

This paper analyses new model-predictive modulation strategies applied to hybrid Silicon Silicon-Carbide cascaded H-bridge (CHB) converters. The analysis identifies a suitable ratio of Silicon to Silicon-Carbide cells and the appropriate modulation strategy applied to this topology concept. The evaluation is based on semiconductor losses and harmonic performance.

1. Introduction

Increased integration of renewable energy sources, e.g. off-shore/on-shore wind or PV leads to new challenges regarding compliance with grid codes e.g. IEEE Standard 519 [1]. Grid code compliance can be accomplished by means of static compensators (STATCOMs) that compensate the reactive power demand of the line and furthermore provide active filtering and mitigate voltage flicker. The STATCOM is synchronized to the grid voltage, produces a controllable three-phase voltage output and injects currents depending on the compensation requirements. State-of-the-art STATCOMS are based on CHB voltage source converters and use silicon (Si) power devices. Recent and expected developments of silicon carbide (SiC) power devices however have triggered investigations of their use in STATCOMs, and other high-power grid-connected converter applications such as PV, wind energy systems and battery energy storage. SiC devices offer superior characteristics compared to Si material, specifically lower switching losses and lower conduction losses in case of high voltage class devices.

A hybrid combination of semiconductor devices could exploit the advantages of SiC (low switching loss and lower conduction loss in high voltage classes) within a CHB STATCOM converter while simultaneously maintaining the benefits of Si devices (lower cost and less conduction loss in lower voltage classes). A multi-level concept with different voltage classes was first presented in [2]. Use of SiC converter cells has also been suggested in [3].

The aim of this work is to identify the optimal hybrid Si-SiC combination with regard to Si-SiC cell ratio and SiC voltage class. This is done in correspondence with a suitable modulation strategy that optimizes the STATCOM loss while ensuring good harmonic performance. For this investigation, the converter configuration is varied by changing the number and voltage class of SiC cells. The utilized modulation strategies inherently account for variations in Si-SiC cell ratio and SiC voltage class.

2. Silicon Carbide

The main advantages of SiC are the following: SiC has a ten times higher critical electrical field strength compared to Si which allows semiconductor designers to build ten times thinner devices for the same blocking voltage [4]. Thinner devices facilitate faster switching, because charge carriers can be swept out more quickly during turn-off [5]. For this reason, SiC devices have lower switching losses and are therefore able to operate at higher frequencies compared to Si devices. Furthermore, SiC has a 1000 times smaller area-related resistivity which has an impact on on-state losses [4]. It has to be kept in mind that due to inherent physical properties, the knee voltage of an ideal pn junction at $T = 300 \text{ K}$ in SiC ($V_{knee,SiC} = 2.77 \text{ V}$) is much higher compared to Si ($V_{knee,Si} = 0.65 \text{ V}$) for the same doping [5]. This is important when considering conduction losses for low voltage class devices as the impact of the decreased on-state resistance on conduction losses is counteracted by the permanent knee voltage offset. Lower conduction losses in SiC devices however become more visible for higher voltage class devices where resistivity loss plays a more important role. The knee voltage increases with blocking capability both for Si and SiC power devices.

3. Hybrid Si-SiC CHB STATCOM Topology, Dimensioning, Current Control

The hybrid Si-SiC CHB STATCOM topology as shown in Figure 1 consists of two different H-bridge cell types. One cell type contains Si IGCTs with $V_{block} = 4.5 \text{ kV}$ which will be referred to as the “reference cell”. The other cell type consists of SiC MOSFETs and can change in voltage level depending on the device voltage class. During the analysis, the topology is varied by gradually replacing reference cells with SiC cells of different voltage level until the converter consists only of SiC cells.

The investigated STATCOM has a nominal power $S_{nom} = 100 \text{ MVA}$ and a nominal output voltage $V_{AC,nom} = 33 \text{ kV}$. The grid short circuit current ratio at the point of common coupling is 10 p.u. for all test cases. The semiconductor parameters are scaled based on theoretical data provided by semiconductor manufacturers for 60 A chips. The chip data consists of the knee voltage, on-state resistance as well as turn-on/turn-off energies. A sufficient number of chips are paralleled to conduct the peak converter arm current. The nominal cell voltage V_{cell} is de-rated to 60% of the semiconductor’s blocking voltage V_{block} for two reasons: First, the parasitic inductance in the DC-link causes voltage over-shoot during switching events from which the semiconductor has to be protected. Second, voltage de-rating is necessary to limit cosmic ray failures [5].

The summation of H-bridge capacitor voltages in one converter arm ($V_{DC,nom}$) is regulated such as to synthesize the peak grid voltage plus arm inductance voltage drop plus a control margin (due to possible dynamic changes in reference current) and a safety margin as shown in equation 1.

$$\begin{aligned} V_{DC,nom} &= \sqrt{2} \cdot V_{AC,nom} \cdot (1 + \Delta_{Larm} + \Delta_{control} + \Delta_{safety}) \\ &= \sqrt{2} \cdot V_{AC,nom} \cdot (1 + 0.14 + 0.1 + 0.1) = \sqrt{2} \cdot V_{AC,nom} \cdot 1.34 \end{aligned} \quad (1)$$

Depending on the voltage class of the SiC cell replacing the reference Si IGCT cell, a different number of cells $N_{cell,SiC}$ is required, as shown in Table I. The total voltage must satisfy $V_{DC,nom} = N_{cell,Si} \cdot V_{cell,Si} + N_{cell,SiC} \cdot V_{cell,SiC}$.

The cell capacitors in the reference case are dimensioned to limit the voltage ripple to $\pm 10\%$ of the nominal cell voltage. This corresponds to a capacitance of $C_{ref} = 6.35 \text{ mF}$ or a capacitor time constant of $\tau_{ref} = 16 \text{ ms}$. When SiC cells are introduced, the cell capacitances in the hybrid combination are changed to account for cell voltage classes and number of cells.

The arm reactance X_{Arm} is used as a means to shape the converter output current by controlling the voltage difference across it. A value of $X_{Arm} = 0.14 \text{ p.u.}$ has shown to be adequate for use in delta-connected CHB converters. Its value is chosen mainly to limit the converter arm current in case of short

circuit. A small connection inductance of $X_{filter} = 0.01 \text{ p.u.}$ is used to smoothen the converter output current and limit fault currents in the event of a fault at the output converter terminals.

The current controller used in the investigated delta CHB STATCOM was implemented in the dq-reference frame [6]. As commonly done in current controllers, the error between commanded signal and resulting signal is controlled to zero by means of PI-controllers. These PI-controllers are tuned according to the actual converter configuration, thus taking into account the cell capacitances, cell voltages and cell numbers. The current controller furthermore compensates for diverging total arm DC voltages by circulating a zero sequence current component. This approach can also compensate for negative sequence grid current [7].

Fig. 1: STATCOM design overview

Table I: Cell configurations (reference cell / SiC MOSFET cell)

SiC share of $V_{DC,nom}$	reference cell / 1.7 kV SiC	reference cell / 3.3 kV SiC	reference cell / 4.5 kV SiC	reference cell / 6.5 kV SiC	reference cell / 10 kV SiC	reference cell / 13 kV SiC	reference cell / 15 kV SiC	reference cell / 20 kV SiC	reference cell / 25 kV SiC
0%	23/0	23/0	23/0	23/0	23/0	23/0	23/0	23/0	23/0
25%	18/15	17/8	18/6	18/4	19/2	18/2	17/2	14/2	18/1
50%	12/30	12/16	12/12	12/8	12/5	12/4	10/4	10/3	12/2
75%	7/45	6/24	6/18	6/12	6/8	6/6	3/6	6/4	7/3
100%	0/63	0/32	0/23	0/17	0/11	0/8	0/7	0/6	0/5

4. Previous Model Predictive Modulation

The proposed modulation strategy has been developed by adapting the model predictive modulation scheme described in [8]. The scheme in [8] applies two adjacent voltage levels within each control period for each phase arm. The voltage levels are time weighted to achieve the time integral of the voltage reference. The scheme selects switching devices to provide the voltage step during each control period by evaluating a cost function shown in (2). Here, every leg within each H-bridge cell is associated with an error value that is updated at the beginning of each control interval.

$$\begin{aligned} ERR_{leg} = & \alpha_1(V_{cap} - V_{cap,avg}) \cdot \text{sign}(i_{arm}) + \alpha_2(E_{loss} - E_{loss,avg}) \\ & + \alpha_3(E_{diff} - E_{diff,avg}) \end{aligned} \quad (2)$$

with $E_{diff} = E_{up} - E_{low}$

The first model within the cost function (2) associates each cell leg with an error value based on capacitor voltage balance. The second model adds an error associated with the total accumulated loss energy E_{loss} in each leg, utilizing a loss model that estimates device losses by interpolating theoretical semiconductor data. The third part of the cost function is required to eliminate a possible loss disparity between upper and lower switches in a cell leg. The scaling factors can be used to prioritize the impact of different cost models on the overall cost function and thus switching decision.

The obtained cell leg error values are sorted and the cell leg with the lowest error is scheduled for the next switching action. All other cells maintain their state from the previous control interval. If insertion of more than one cell is required to achieve the reference converter output voltage, the cell with the second lowest error value is scheduled next and so on. As mentioned the scheme applies two adjacent voltage levels in each phase leg in order to achieve the time integral of the voltage reference. In doing so, unnecessary switching actions are avoided by scheduling the on-time (d) of the cell to be switched at the beginning of the interval if the cell was previously in on-state. If the cell was previously in off-state, the cell is turned on after (1-d).

5. Proposed Model Predictive Modulation of Hybrid Si-SiC CHB STATCOM

The modulation strategy summarized above has been extended in this paper for use with two cell types, one consisting of Si devices, the other of SiC devices [9]. Again, the next switching action is based on evaluation of the cost function in (2). Throughout all simulations, the scaling factors are kept at $\alpha_1 = 1$, $\alpha_2 = 1 \cdot 10^{-5}$ and $\alpha_3 = 1 \cdot 10^{-5}$.

The proposed modulation does not specifically favor a switching action in a certain cell type within the model responsible for maintaining capacitor voltage balance. This is because each measured capacitor voltage is normalized with respect to its desired nominal value, meaning cells using different semiconductor voltage classes can be evaluated and compared using relative values. The loss models are implemented with the semiconductor's actual incurred loss energy E_{loss} that is then weighted with regard to the average incurred loss $E_{loss,avg}$ in a cell leg. For the average loss, it is distinguished between the two semiconductor types meaning that for the Si cells, the average loss value $E_{loss,avg,Si}$ is calculated only from Si cells. For the average SiC losses $E_{loss,avg,SiC}$, only SiC cells are taken into account. This approach was chosen to equalize losses among a certain type of cell instead of trying to equalize them between Si and SiC cells.

Three modulation variants were developed: "Full Freedom", "SiC in peaks" and "SiC in zero crossings" as shown in Figure 2. All modulation variants choose the next switching action based on the system cost function shown in (2). The two latter variants however introduce constraints, so that the SiC cells are utilized in a certain part of the voltage waveform only. This is achieved as follows: In general, the modulation strategy maintains the switching states from the previous control interval unless a cell is scheduled for switching based on its error value. Now, the cells that are supposed to be utilized in voltage

peaks are excluded from this principle by manual re-initialization to a disconnected state at the beginning of each control interval. Disconnected cells do not contribute to the converter output voltage. The modulation strategy will then only re-insert the disconnected cells once all other cells do not cover the required output voltage, which occurs in voltage peaks. For “SiC in peaks”, all SiC cells are manually set to a disconnected state at the beginning of each control interval. For “SiC in zero crossings”, this is done for all Si cells so that they are switched in voltage peaks instead of the SiC cells.

Fig. 2: Converter output voltage for proposed modulation strategies with twelve Si cells ($V_{cell} = 2.7 \text{ kV}$) and two SiC cells ($V_{cell} = 15 \text{ kV}$)

The modulation variants were chosen to compare three approaches: The “Full Freedom” variant bases its switching decision on internal cost function models only, similar to the previously proposed scheme. “SiC in peaks” was developed to test the impact on losses of utilizing the high switching frequency capability of SiC devices in voltage peaks. The opposite approach “SiC in zero crossings” aims at best utilizing low SiC switching loss characteristics in voltage zero crossings.

The loss incurred in any switching device increases as a function of the instantaneous current in the phase arm where the switching event occurs. In reactive power applications switching of a cell at voltage zero crossings corresponds to when the current is near its peak due to the 90° phase shift between voltage and current. Therefore, the advantage of utilizing SiC cells with low switching losses is more pronounced when the SiC cells are switched during times when switching loss would otherwise be high.

Switching SiC cells in a certain part of the voltage waveform also has an impact on THD especially when higher voltage class SiC cells are being used. SiC cells in voltage peaks must then be switched at a higher frequency to maintain a constant harmonic performance while synthesizing the desired time integral of the reference voltage. This effect is less pronounced for the “SiC in zero crossings” variant especially if higher voltage class SiC cells are utilized in voltage zero crossings. This is due to the desired step in voltage being closer in magnitude to the step in voltage created by switching one high voltage cell. As a consequence this suppresses switching actions of Si cells during current peaks (voltage zero crossings) which is advantageous in terms of losses as Si switching losses are higher compared to SiC. Furthermore Si switching actions now occur in voltage peaks for the “SiC in zero crossings” modulation variant which is favorable as they occur at low currents.

6. Implementation Aspects and Evaluation Criteria

Simulations of all cell combinations and proposed modulation strategy variants were executed in MATLAB/Simulink for a simulation time of 1 second. The investigated delta CHB STATCOM converter and modulation strategy were implemented as M-functions. The execution time step was $t_{exe} = 0.1 \mu\text{s}$.

6.1 Loss Model

The semiconductors’ conduction and switching energies were accumulated during execution according to equation (3) and (4). The accumulated energy was updated every $t_{exe} = 0.1 \mu\text{s}$ in the model. A linear dependency of the turn-on and turn-off losses on the device current was assumed. As the switched capacitor voltages were assumed balanced, no voltage correction factor was introduced for switching losses.

$$E_{cond} = t_{exe} \cdot (V_{knee} \cdot i_{arm} + R_{on} \cdot i_{arm}^2) \quad (3)$$

$$E_{on} = E_{ref,on,60A} \cdot \frac{i_{arm}}{60A}, \quad E_{off} = E_{ref,off,60A} \cdot \frac{i_{arm}}{60A} \quad (4)$$

The total accumulated conduction and switching energies in the CHB STATCOM were then divided by the simulation time of 1 s to obtain power values and further divided by the total converter power S_{nom} to obtain relative loss values. The relative loss values were scaled with regard to the reference case. The reference case therefore has losses of 1 p.u.

6.2 Harmonic Content

Propagation of harmonics from a grid-connected converter into the grid is unwanted as harmonics have negative effects on general power quality. Though harmonics cannot be avoided completely, they must be minimised.

The total harmonic distortion of the voltage waveform is defined according to equation (6). The limit for the considered CHB converter with $V_{AC,nom} = 33 \text{ kV}$ is $THD_{V,max} = 5\%$ according to IEEE standard 519 [7]. The THD values were measured for V_{ab} at the STATCOM PCC from $t = 0.5 \text{ s}$ to 1 s simulation time. Only harmonics up to the 150th are considered.

$$THD_V = \frac{\sqrt{\sum_{n=2}^{n_{max}} (V_n)^2}}{V_1} \quad [10] \quad (6)$$

In addition to voltage harmonics, current harmonics have to be considered because they cause extra losses in transformers, cables and rotating machines. These extra losses increase stress and lead to premature aging. In case of a mainly inductive load with small resistivity, the load current harmonics can be approximated with equation (7)

$$I_n \cong \frac{V_n}{n \cdot \omega_1 \cdot L} \quad [10] \quad (7)$$

The total harmonic distortion of the current waveform is defined according to equation (6-6) and can be simplified by inserting (8).

$$THD_I = \sqrt{I_0^2 + \sum_{n=2}^{n_{max}} (I_n)^2} = \frac{1}{\omega_1 \cdot L} \sqrt{\sum_{n=2}^{n_{max}} \left(\frac{V_n}{n}\right)^2} \quad [10] \quad (8)$$

By normalizing this expression (9) with respect to $\frac{V_1}{\omega_1 \cdot L}$, the weighted THD can be obtained according to (9).

$$WTHD = \frac{\sqrt{\sum_{n=2}^{n_{max}} \left(\frac{V_n}{n}\right)^2}}{V_1} \quad [10] \quad (9)$$

As all harmonics are weighted by their harmonic order n , the larger order harmonics have less impact on WTHD than lower order harmonics. Still, the normalization factor may change as V_1 changes. To overcome this, a constant normalization factor i.e. V_{DC} , can be chosen. The corresponding WTHD0 value is calculated with equation (10).

$$WTHD0 = \frac{\sqrt{\sum_{n=2}^{n_{max}} \left(\frac{V_n}{n}\right)^2}}{V_{DC}} \quad [10] \quad (10)$$

7. Results

7.1 Losses and Harmonic Content

The obtained full load losses and THD at the PCC are shown in Figure 3 and 4.

Fig. 3: Full load losses for configurations with SiC MOSFET cells

The losses were scaled with regard to the reference case. The reference case has losses of 1 p.u. In general, the introduction of SiC MOSFET cells leads to decreased total losses compared to the reference case. The lowest total losses occur for certain cell combinations with use of “SiC in zero crossings” modulation strategy. In anticipation of the THD results discussed later, the loss value for a (12/5) converter configuration with twelve Si IGCT cells ($V_{block} = 4.5 \text{ kV}$) and five SiC MOSFET cells ($V_{block} = 10 \text{ kV}$) is denoted with an arrow for the “SiC in zero crossings” modulation strategy.

In this case, full-load losses are decreased to 0.72 p.u., thus by 28%. The reason for this is that the SiC cells are switched in voltage zero crossings (current peaks). This is advantageous in terms of device switching losses as switching losses are smaller in SiC devices compared to Si devices. Furthermore, the number of switching actions of Si cells with comparatively high switching losses are avoided when the current is high. As SiC devices have lower switching losses than Si devices, the fact that higher voltage class SiC devices are being used, is not detrimental in terms of switching losses.

Fig. 4: THD at PCC for configurations with SiC MOSFET cells (plots are turned for better visibility)

The reference case has a THD of 1.95%. Modulation mode “SiC in zero crossings” results in the same or lower THD compared to the other two modulation strategies for high voltage class SiC devices. This is marked with an ellipse. As discussed previously, this is due to the fact that the high voltage cells are utilized where the required rate of change in the output voltage waveform is highest i.e. during voltage zero crossings. For the voltage class of the investigated CHB converter, the THD limit of $THD_{V,max} = 5\%$ is given in IEEE standard 519 [1]. It is not exceeded except for 100% SiC configurations with

devices above blocking voltage of $V_{block} = 20 \text{ kV}$. Again, the THD value for a (12/5) converter configuration with five SiC MOSFET cells ($V_{block} = 10 \text{ kV}$) is denoted with an arrow for the “SiC in zero crossing” modulation strategy. Even though high voltage cells are used, the THD of 1.94% is comparable to the reference case. Also, the individual voltage harmonics of the (12/5) converter configuration are below the limit of 3% [1]. Increasing the switching frequency of the SiC MOSFET cells could further improve the harmonic performance if desired.

7.2 Weighted THD

The WTHD0 results for the investigated hybrid CHB STATCOM are shown in Figure 5. There is no important difference between the three modulation modes. The WTHD0 values are in the range of 2.9%. A slight decrease in WTHD0 can be observed for a CHB STATCOM consisting of 100% SiC cells with 20 kV or 25 kV MOSFETs. This is due to the total DC voltage V_{DC} being slightly higher in those two cases than for the other cell combinations. With discrete high cell voltage steps, the desired $V_{DC,nom}$ is not met exactly, but instead exceeded slightly.

Fig. 5: WTHD0 at PCC for configurations with SiC MOSFET cells

7.3 Low-Load Losses

Although being relatively small, low-load losses are of interest in high power converters because they can be required to operate in idle mode for long periods. In case of STATCOMs for example, penalties can be enforced if the STATCOM consumes too much energy while not contributing to grid stability. The losses of the investigated hybrid CHB STATCOM for a low load of 5% are shown in Figure 7. Again, the values were scaled with regard to the reference case in full load (1 p.u. losses). The reference case has low-load losses of 0.012 p.u. The loss value for a (12/5) converter configuration with twelve Si IGCT cells ($V_{block} = 4.5 \text{ kV}$) and five SiC MOSFET cells ($V_{block} = 10 \text{ kV}$) is denoted with an arrow for the “SiC in zero crossings” modulation strategy. The low-load losses are further decreased to 0.008 p.u. which corresponds to a decrease by 33% compared to the low-load losses of the reference case.

Fig. 7: Low-load losses for configurations with SiC MOSFET cells

7.4 Capacitor Voltage Ripple

Depending on the modulation variant utilized, a different capacitor ripple can be observed for the same CHB STATCOM dimensioning. The ripple is shown in Figure 6 for a configuration with twelve Si IGCTs with $V_{block} = 4.5 \text{ kV}$ ($V_{cell} = 2.7 \text{ kV}$) and two SiC MOSFETs with $V_{block} = 25 \text{ kV}$ (cell: 15 kV). This corresponds to a configuration in which 50% of $V_{DC,nom}$ is covered with high-voltage SiC cells. The converter output waveforms are shown in Figure 2.

The capacitor voltage behavior can be explained by the constraint to use a certain set of cells in voltage peaks or zero crossings respectively. As the STATCOM is mainly operating in inductive mode, the current is lagging by 90° . Use of a cell in voltage zero crossings therefore implies use during current peak which causes a larger voltage ripple. The opposite behavior occurs when a cell is used in voltage peaks. Depending on the modulation strategy utilized and the corresponding capacitor voltage ripple, capacitor dimensioning can be optimized.

Fig. 6: Capacitor voltage for proposed modulation strategies with twelve Si cells ($V_{cell} = 2.7 \text{ kV}$) and two SiC cells ($V_{cell} = 15 \text{ kV}$)

8. Discussion

A hybrid model predictive modulation strategy has been investigated for use with a hybrid CHB STATCOM consisting of silicon and silicon carbide cells. This modulation strategy offers three modes, i.e. “Full Freedom”, “SiC in voltage peaks” and “SiC in voltage zero crossings”. All modulation strategy variants choose the next switching action based on a system cost function. The two latter modulation strategies introduce additional constraints, so that a certain type of cell is utilized in a certain part of the voltage waveform only.

These modulation strategies were demonstrated and analyzed in simulations for a hybrid CHB STATCOM with $S_{nom} = 100 \text{ MVA}$ and $V_{AC,nom} = 33 \text{ kV}$. The CHB STATCOM consisted of different combinations of Si and SiC cells. In total, 37 cell combinations were investigated. The high number of test cases required generic dimensioning of cell capacitors as well as automatic tuning of the current controller gains. The values were changed in correspondence with cell voltage and cell number, which is sufficient. Once the most interesting cell combination is identified, controller tuning and capacitor design

can however be further optimized. For capacitor sizing, the chosen modulation variant can then also be taken into account because it influences the capacitor voltage ripple.

The reference case consisting only of Si IGCTs of $V_{block} = 4.5 \text{ kV}$ has 1 p.u. full load losses, and a voltage THD at the PCC of 1.95%. The most promising CHB STATCOM dimensioning replaces 50% share of the nominal phase-leg voltage with SiC MOSFETs cells of $V_{block} = 10 \text{ kV}$ and $V_{cell} = 6 \text{ kV}$. This translates into a (12/5) cell configuration where the first number indicates the number of utilized Si IGCTs ($V_{block} = 4.5 \text{ kV}$) and the second number the number of utilized SiC MOSFETs ($V_{block} = 10 \text{ kV}$). If switched with “SiC in voltage zero crossings” modulation strategy, this configuration offers full load losses of 0.72 p.u. and a voltage THD of 1.94%. Losses are thus decreased by 28% whereas THD is in the same range as the reference case. Furthermore, for this cell combination, low-load losses are decreased by 32% compared to the reference case. WTHD0 is not affected by the chosen cell combination. New degrees of freedom for capacitor dimensioning are offered by choosing a certain modulation strategy.

9. Conclusion

The “SiC in zero crossings” modulation variant is favorable because it takes advantage of low SiC switching losses in voltage zero crossings (current peaks) when switching loss would be high in Si devices. Also, switching actions are further suppressed because high-voltage SiC cells are used when the voltage gradient of the desired waveform is highest. This is furthermore advantageous in terms of harmonic performance.

When using “SiC in zero crossings” modulation strategy in hybrid Si-SiC CHB STATCOM, losses can be decreased while the harmonic performance can be maintained. The most promising dimensioning in this analysis replaces 50% share of the nominal phase-leg voltage with SiC MOSFETs cells of $V_{block} = 10 \text{ kV}$.

References

- [1] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Standard 519, 2014.
- [2] M.D. Manjrekar, P. Steimer and T.A. Lipo, “Hybrid Multilevel Power Conversion System: a competitive solution for high power applications,” *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834-841, May/Jun. 2000.
- [3] Y. Koyama et al., “System fault test of SiC device applied 6.6kV transformerless D-STATCOM,” in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015.
- [4] M. Bakowski, “Tutorial: SiC Power Devices: Status and Prospects,” in *International SiC Power Electronics Applications Workshop (ISiCPEAW)*, Stockholm, 2015.
- [5] J. Lutz et al., *Semiconductor Power Devices – Physics, Characteristics, Reliability*, Berlin Heidelberg: Springer, 2011.
- [6] A. Yazdani and R. Iravani, “Space Phasors and Two-Dimensional Frames,” in *Voltage-Sourced Converters in Power Systems – Modeling, Control, and Applications*, Hoboken, NJ: Wiley & Sons, Inc., 2010.
- [7] E. Behrouzian, M. Bongiorno and H. Zelaya de la Parra, “Investigation of Negative Sequence Injection Capability in H-bridge Multilevel STATCOM,” in *2014 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, Lappeenranta, 2014.
- [8] C. Townsend et al., “Heuristic Model Predictive Modulation for High-Power Cascaded Multi-Level Converters,” *IEEE Trans. Ind. Electron.*, early access, 2016.
- [9] I. Jahn, “Analysis of Modulation Strategies for Future STATCOMs,” unpublished, M.Sc. thesis, Institute for High Voltage Technology, RWTH Aachen University, 2015.
- [10] D.G. Holmes and T.A. Lipo, “Harmonic Distortion,” in *Pulse Width Modulation for Power Converters, Principles and Practice*, Piscataway, NJ: IEEE Press, 2003.