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A 96.4 dB High-Pass Delta-Sigma Modulator with Dynamic Biasing and Tree-Structured DEM

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Abstract—This paper presents a switched-capacitor high-pass delta-sigma modulator that can directly convert a chopper modulated signal to the digital domain. Low power consumption is achieved by employing inverter-based amplifiers and dynamic biasing in the first amplifier with relaxed slew-rate requirements as a result of the multi-bit quantization. The mismatch errors in the switched-capacitor DAC are first-order noise shaped by a tree-structured dynamic element matching encoder. Schematic level simulations show that the high-pass modulator achieves a peak SNDR of 96.4 dB and a SFDR of 101 dBc over a bandwidth of 300 Hz. The total estimated power consumption of the modulator is 19.56 μ W leading to a figure-of-merit of 0.6 pJ/conv.

I. INTRODUCTION

High-pass delta-sigma analog-to-digital converter (HP $\Delta\Sigma$ ADC) can be obtained from its low-pass counterpart by translating the zeros of the noise transfer function (NTF) from DC to half of the sampling frequency, $f_s/2$, without losing the order of the NTF. HP $\Delta\Sigma$ ADCs were mainly investigated for CMOS RF direct-conversion and low-IF receivers due to their ability to process narrow-band signals located above the DC offset and flicker noise corner [1]. However, the impact of the clock jitter in those applications is substantially high and the folding of the image frequency, due to adjacent channels, is a challenging problem to solve. Although HP $\Delta\Sigma$ ADCs have not been relatively successful in radio applications, their immunity to flicker noise makes them interesting in neural recording interfaces.

This paper presents a multi-bit second order switched-capacitor (SC) HP $\Delta\Sigma$ modulator architecture for a neural recording interface (NRI), as shown in Fig. 1. A very power-efficient $\Delta\Sigma$ ADC is obtained by employing inverter-based amplifiers [2] and by using dynamic biasing in the first amplifier [3]. Additionally, the amplifier nonlinearity effects are reduced by adopting multi-bit quantization [4]. In order to circumvent the matching limitations of the digital-to-analog converter (DAC), a first-order tree-structured dynamic element matching (DEM) encoder is selected [5], synthesized and its effectiveness is verified through simulations.

II. HIGH-PASS $\Delta\Sigma$ MODULATOR ARCHITECTURE

A. Architecture Overview

The HP $\Delta\Sigma$ modulator targeting a NRI intended for electrocorticography is shown in Fig. 1. The NRI consists of an anti-aliasing filter and a buffer in the front-end, and a decimator

Fig. 1. A high-resolution HP $\Delta\Sigma$ modulator for neural recording interfaces.

and digital signal processing in the back-end. Due to the low frequency range of the neural signals of interest (up to 300 Hz) and the level of amplitudes (up to 150 μ V), the flicker noise and common-mode noise can pose a serious issue for accurate measurements. A common way to reduce their impact in a NRI is to use chopper modulation [6]. Therefore, it can be very advantageous to use a HP $\Delta\Sigma$ ADC for signal processing in such a system. Another common issue in a NRI is the presence of electrode offset (up to 300 mV) at the electrode-tissue interface. However, the large dynamic range between the information carrying neural signals and the electrode offset will not be an issue provided that the HP $\Delta\Sigma$ ADC has enough resolution (approximately 16-bits) to resolve the small changes around the electrode offset.

A high resolution $\Delta\Sigma$ modulator is usually limited by the thermal noise and not by the aggressiveness of the NTF, so a second-order NTF is sufficient to achieve the targeted resolution. A feedforward architecture is selected to implement the NTF due to its relaxed requirements on the analog blocks [4]. The OSR together with the sampling capacitor C_{s1} of the first high-pass filter (HPF₁) set the thermal noise level. The signal-to-noise-ratio (SNR) can be calculated as in [7]:

$$\text{SNR} \approx 10 \log \left[\frac{v_{in}^2}{2} / \left(\frac{2kT}{C_{s1} \cdot \text{OSR}} \frac{b_1 + 1}{b_1} \right) \right], \quad (1)$$

where v_{in} is the amplitude of the input signal, which is determined by the application, b_1 is the gain coefficient of the HPF₁ shown in Fig. 1 and the factor 2 is due to the differential implementation. An OSR of 256 is selected to provide sufficient noise-shaping, while C_{s1} of 13 pF results in an SNR of 98 dB ($\approx$ 16 bits). A multi-bit quantizer substantially relaxes the linearity requirements of the analog blocks by reducing the output voltage swing. Initially, a 16 level (4-bit)

TABLE I
MINIMUM REQUIREMENTS FOR THE HP $\Delta\Sigma$ MODULATOR

Clock req.	OTAs req.	Caps. req. [pF]
$f_s = 153.6$ kHz	DC gain > 40 dB	$C_{s1} = 13.2$
OSR = 256	GBW > 308 kHz	$C_{int1} = 21.1$
jitter _{SD} < 4.5 ns	SR > 42 kV/s	$C_{int2} = 2.1, C_{s2} = 1.3$

flash ADC was chosen to ensure that the modulator is limited by the thermal noise and not by the quantization noise. After determining the maximum stable amplitude from behavioral simulation, the number of levels in the flash ADC was reduced to 11. A tree-structured DEM encoder with 10 unit elements is selected to linearize the multi-bit SC DAC. The minimum requirements for the modulator and its critical analog building blocks, which are given in Table I, are also determined from behavioral simulations. According to Table I, simple inverter-based amplifiers can be used to implement the HPFs.

B. High-Pass Filters

The SC HPFs are the core building blocks of a $\text{HP}\Delta\Sigma$ modulator. The implementation of the HPF_1 is depicted in Fig. 2, while the HPF_2 is similar but with the scaled down sampling capacitor and constant biasing. The only difference from the parasitic-insensitive SC integrator is that the integrating capacitors C_{int1} are alternated around the amplifier at the chopping frequency, $f_s/2$, to produce the high-pass transfer function [8]. The HPF_1 is often the most power consuming block of the whole modulator due to the large capacitive load. The equivalent load, in the integration phase, $C_{eq,int1}$, and the sampling phase, $C_{eq,s1}$, respectively, at the amplifier output of the HPF_1 , can be calculated as follows [7]:

$$C_{eq,int1} \approx C_{s1} + C_{par1} + C_{L1} \left(1 + \frac{C_{s1} + C_{par1}}{C_{int1}} \right) \quad (2)$$

$$C_{eq,s1} \approx C_{par1} + (C_{L1} + C_{s2}) \left(1 + \frac{C_{par1}}{C_{int1}} \right), \quad (3)$$

where C_{s1} (13.2 pF) and C_{s2} (1.32 pF) are the sampling capacitors of the first and second HPF respectively, C_{par1} is the parasitic capacitance seen on the input terminals of the OTA_1 (≈ 1.71 pF), C_{int1} is the integrating capacitor and C_{L1} (≈ 4.24 pF) is the load capacitance at the output terminals. From (2) and (3), the values of $C_{eq,int1} \approx 22.4$ pF and $C_{eq,s1} \approx 7.9$ pF are calculated. Therefore, the equivalent load drops by approximately a factor of three in the sampling phase, implying that the load-compensated OTA_1 is wasting power due to constant biasing current. Furthermore, the amplifier noise contribution is also dependent on $C_{eq,int1}$ [7], and is given by:

$$\overline{v_{n,ota_1}^2} \approx \frac{1}{b_1^2} \frac{2kT}{\text{OSR} \cdot \beta \cdot C_{eg,int1}}, \quad (4)$$

where β is the feedback factor given by:

$$\beta = C_{int1}/(C_{int1} + C_{s1} + C_{par1}). \quad (5)$$

By comparing (4) and (1), we can observe that the amplifier noise has approximately the same contribution as the sampling

Fig. 2. a) Implementation of the HPF_1 , b) the schematic of the OTA_1 .

noise of C_{s1} . Additionally, the noise is independent of OTA_1 's transconductance. Thus we can conclude that it is possible to reduce the power consumption by dynamically adjusting the biasing current of the first amplifier without compromising the noise, slew-rate (SR) or the gain-bandwidth (GBW) performance.

Dynamic biasing can be implemented by reconfiguring the mirroring ratio of the tail current sources as depicted in Fig. 2b. The top current source consists of two transistors MP_1 and MP_2 , which are sized such that MP_2 is twice the size of MP_1 and the same applies for the bottom current source. At the start of the sampling phase, the signal S_d rises and disconnects the drain terminals of transistors MP_2 and MN_2 from the top and bottom current source, respectively, while the gate voltage potential is approximately the same since only the current mirroring ratio changed. The $HP\Delta\Sigma$ modulator performance will not be affected by dynamic biasing, provided that the DC offset at the output of the first amplifier, which is caused by mismatches in different biasing conditions, does not change significantly the DC operating point of the next amplifier.

C. Feedforward Addition and Flash ADC

The adder block in front of the flash ADC is implemented as a differential SC voltage adder as shown in Fig. 3a. The required OTA_2 is also implemented with inverter-based amplifiers, but with constant biasing. The 11 level flash ADC is

Fig. 3. a) Implementation of the adder block, b) the pre-amplifier and the c) regenerative latch.

implemented with 10 comparators, consisting of a preamplifier and a regenerative latch as given in Fig. 3b and Fig. 3c.

D. Tree-Structured DEM with 10 Unit Elements

The tree-structured DEM technique offers certain advantages compared to other linearization techniques [5]: i) it is not as susceptible to generating spurious tones in the signal-band, ii) it can be implemented with an arbitrary number of DAC levels and iii) the required digital logic is relatively simple and it introduces only the combinational network delay.

A first-order noise-shaping tree-structured DEM encoder is selected considering the targeted accuracy for the $\text{HP}\Delta\Sigma$ modulator. The encoder operates on the thermometer code of the 11 level flash ADC and generates 10 control signals denoted by $\text{DAC}(i,i)$ ($i=1,2,\dots,10$) as shown in Fig. 4. The output of the flash ADC is split into two thermometer codes $\text{D}_{out+}<4:0>$ and $\text{D}_{out-}<4:0>$, where the two codes represent the positive and the negative quantized values of the differential input signal. The $\text{D}_{out+}<4:0>$ and $\text{D}_{out-}<4:0>$ are then combined using five logic OR gates, which compresses the number of wires from 10 to 5 while the information about the sign is retained in $\text{D}_{out+}<0>$. The quantized signal is then down-converted to DC by toggling the $\text{D}_{out+}<0>$ bit at the sampling rate. The "compressed" thermometer code is converted into a binary number using a hardware-efficient Waller-adder. The resulting sum is taken for FFT calculations.

The switching of the DEM encoder is here briefly explained and the reader is referred to [5] for more details. Depending on the value of the input $c[u,w]$, the switching block has two possible outputs which are decided by the noise-shaping sequence of that block $S(u,v,w)$. In both cases, the sum of the outputs has to be equal to the input value $c[u,w]$ so that the number conservation rule is satisfied. During start-up, a reset signal configures all the shift-registers to their unique switching sequences.

Fig. 4. Diagram of the tree-structured DEM encoder.

Fig. 5. Implementation of the switching block S(1,4,10).

Fig. 6. Automatically generated layout of the DEM encoder.

The first block S(1,4,10), which is depicted in Fig. 5, is the most complicated, while the complexity of other switching blocks reduces with each level of the tree. The mathematical operations in a switching block were implemented using look-up-tables (LUTs). The number of switching blocks in each branch was made similar so that the propagation delay would be approximately equal throughout the tree. The encoder contains a total of 180 instances, consumes approximately 1 μA and occupies an area of $117 \times 135 \mu\text{m}^2$ as shown in Fig. 6.

III. SIMULATION RESULTS

The HP $\Delta\Sigma$ modulator was designed in a 0.18 μm CMOS technology with a 1.8 V supply for the analog and 1.2 V for the

TABLE II
PERFORMANCE SUMMARY OF DEM ENCODERS USED IN MULTI-BIT $\Delta\Sigma$ M

	[9]	[10]	⁽¹⁾ this work
Technology [μm]	0.18	0.5	0.18
Digital supply [V]	1.5	3.3	1.2
Digital clock [MHz]	81.92	3.072	0.1536
BW _{ADC} [Hz]	5000	24000	300
f_{signal} [Hz]	833	1500	75
FFT	2048	N/A	4096
SFDR [dBc]	90	105.6	⁽³⁾ 101
P _{digital} [μW]	80	4400	1.2
Area [mm^2]	0.0676	⁽²⁾ 1.04	0.0158

- 1) based on the schematic level simulation results
2) based on an estimation from the die photograph
3) based on the mean value over process and device mismatch

Fig. 7. Down-converted PSD of a 4096-point FFT with a Hanning window.

digital blocks. The first HPF consumes $4.6 \mu\text{A}$ when dynamic biasing is used, compared to $6 \mu\text{A}$ when constant biasing is used. The second HPF consumes $1.8 \mu\text{A}$, while $1 \mu\text{A}$ is needed in the SC voltage adder. The total power consumption of the flash ADC is $2.8 \mu\text{A}$, mostly due to the pre-amplifiers' static power dissipation.

A performance summary of the DEM encoders used in multi-bit $\Delta\Sigma$ modulators is given Table II. Even though the DEM encoder was only synthesized, the results in Table II demonstrate that in this work competitive power and area consumption is achieved. Moreover, post-layout simulation of the DEM encoder did not show any significant change in its performance compared to post-route reports.

The down-converted power spectral density (PSD) of the transient-noise simulations are shown in Fig. 7. The nominal simulation results show a peak SNDR of 98 dB, which in the worst case sample deteriorates by 2.6 dB. The transient-noise simulation results, with the device and process mismatch enabled, show a mean SNDR of 96.4 dB and a SFDR of 101 dB, as it can be seen in Fig. 8. Due to the large computational time and the required numerical accuracy the number of Monte Carlo runs is limited.

The HP $\Delta\Sigma$ modulator total estimated power dissipation is $19.56 \mu\text{W}$, which results in a $0.6 \text{ pJ/conversion-step}$ Walden figure-of-merit, $\text{FOM}_{\text{Walden}}$, calculated as:

$$\text{FOM}_{\text{Walden}} [\text{pJ/conv}] = \frac{\text{Total power}}{2 \cdot \text{BW}_{\text{ADC}} \cdot 2^{(\text{SNDR}-1.76)/6.02}} \quad (6)$$

Fig. 8. Histogram of the SNDR and SFDR over process and device mismatch for a 4096-point FFT with a Hanning window.

IV. CONCLUSION

A multi-bit second-order SC HP $\Delta\Sigma$ modulator has been presented. A power-aware design methodology has been applied to reduce the power consumption of the first amplifier without deteriorating the performance. Additionally, a first-order tree-structured dynamic element matching encoder has been employed to linearize the multi-bit feedback SC DAC. The schematic level Monte Carlo simulations show that the HP $\Delta\Sigma$ modulator achieves a peak SNDR of 96.4 dB over a bandwidth of 300 Hz, while consuming $19.56 \mu\text{W}$. The achieved results demonstrate that the proposed HP $\Delta\Sigma$ modulator is a feasible and power-efficient solution for NRIs.

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