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Through Silicon Vias with Invar Metal Conductor for High-Temperature Applications

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Abstract—Through silicon vias (TSVs) are key enablers of 3D integration technologies which, by vertically stacking and interconnecting multiple chips, achieve higher performances, lower power and a smaller footprint. Copper is the most commonly used conductor to fill TSVs; however, copper has a high thermal expansion mismatch in relation to the silicon substrate. This mismatch results in a large accumulation of thermomechanical stress when TSVs are exposed to high temperatures and/or temperature cycles, potentially resulting in device failure.

In this paper, we demonstrate 300 μm long, 7:1 aspect ratio TSVs with Invar as a conductive material. The entire TSV structure can withstand at least 100 thermal cycles from -50°C to 190°C and at least one hour at 365°C , limited by the experimental setup. This is possible thanks to matching coefficients of thermal expansion (CTE) of the Invar via conductor and of silicon substrate. This results in thermomechanical stresses that are one order of magnitude smaller compared to copper TSV structures with identical geometries, according to finite element modelling. Our TSV structures are thus a promising approach enabling 2.5D and 3D integration platforms for high-temperature and harsh-environment applications.

Index Terms—TSV, CTE, 3D packaging, FEM, spin-on glass, thermal reliability

I. INTRODUCTION

Moore's law has been driving an exponential increase of the complexity of silicon chips since 1965. This has been mostly obtained by downscaling the size of MOS transistors and by increasing the number of transistors per chip. However, scaling of silicon devices is about to reach fundamental physical limits, and the economic costs associated with the establishment of the next generation manufacturing infrastructure are becoming prohibitive [1]. Therefore, reducing transistor dimensions needs to be combined with alternative approaches in order to continue increasing the integration density of microelectronics. Among these approaches, 3D integration represents a key solution. 3D integrated systems consist of multiple chips that are fabricated separately and then stacked and vertically interconnected. An important advantage of 3D

integration is that it enables the integration of heterogeneous technologies in a single package, including digital, analog, RF, power electronics and micro and nano electro-mechanical system (MEMS/NEMS) devices [2]. Moreover, 3D integration allows the reduction of die footprint and interconnection delays as compared to 2D device implementations [3]. Among vertical integration techniques, 2.5D integration is also gaining importance. 2.5D integration relies on interposers to redistribute fine-pitch pads on silicon chips to a larger-pitch array of pads on the package substrate [4].

In both 2.5D and 3D integration technologies, the vertical interconnections between the stacked chips can be realized by utilizing through silicon vias (TSVs). A single TSV typically consists of a hole in a silicon substrate made by e.g. deep reactive ion etching (DRIE), a coating consisting of a thin insulating layer (e.g. silicon dioxide or silicon nitride deposited by chemical vapour deposition, CVD) on the inner sidewall of the hole, possibly combined with a diffusion barrier layer, and an electroplated conductive metal core (e.g. copper) filling the hole [5]. However, there is a large mismatch in the coefficients of thermal expansion (CTEs) between silicon ($2.55 \text{ ppm}/^\circ\text{C}$ at 25°C) and copper ($16.6 \text{ ppm}/^\circ\text{C}$ at 25°C) [6,7], which results in thermomechanical stress accumulation, especially at the interfaces between the materials. For large numbers of thermal cycles during the lifetime of TSV structures, this stress accumulation can cause delamination and cohesive crack growth, which can in turn result in failure of the electrical contacts [8,9]. Most electronic devices are exposed to numerous thermal cycles during their operating life for different reasons. Frequent on/off switching causes alternating Joule heating of transistors and interconnects. Some harsh environments are intrinsically characterized by more or less frequent and extreme thermal cycles. For instance, devices for automotive applications placed near the engine or in the transmission system can be subjected to cycles between -40°C and 200°C , multiple times per day [10]. In other applications, sensors and electronics need to operate in environments constantly at high temperature with very limited space available [11]. Such applications would benefit from the reduction of die footprint enabled by 2.5D and 3D integration of MEMS sensors and readout electronics. For example, the oil and gas industry requires the measurement of tilt and vibrations in drilling tools with environmental temperatures of up to 200°C [12,13]. In aerospace technology, intelligent propulsion systems rely on continuous monitoring and adjustment of combustion conditions, which requires the use of electronics and sensors that are working above temperature of 300°C and

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up to 600 °C [14].

To the best of our knowledge, no TSV architectures that are specifically designed for harsh environments have been proposed yet, and no complete TSV structures, including pads and interconnects, have been reported under thermal cycles wider than -65 °C to 150 °C [15]. Single TSVs without pads and interconnects have been characterized at temperatures between 25 °C and 425 °C where copper pumping, i.e. protrusion of the metal core of the via several microns above the substrate surface, occurred after only three cycles [16]. Air has been proposed as insulating layer to reduce thermomechanical stresses in copper-filled TSVs [17]. Air-gap TSVs on a thinned 50 µm thick silicon wafer proved to be stable after up to 90 thermal cycles between -65 °C and 150 °C [18]. Such an approach could be ultimately combined with the approach presented here to further reduce thermomechanical stresses at extreme temperatures.

Another problem of copper-filled TSVs is the increase of the global effective CTE of the silicon interposer with copper TSVs, which can be significantly larger than the CTE of silicon chips without copper TSVs [4]. As a result, the interposer will expand and contract more than the silicon chips during temperature cycling, which can result in fatigue loading on the solder joints, possibly leading to failure. This demands additional design rules that pose constraints on the interposer thickness and on the pitch of the solder bumps [4], or mandates an underfill [4,19] with additional process steps, thus involving additional costs [10].

Even if no thermomechanical failure occurs, stress in the silicon areas surrounding TSVs can induce mobility variations through the piezoresistive effect in silicon. Such variations can be as large as 50% for p-MOSFETs [20] and thus require the definition of keep-away-zones around the TSVs with dimensions on the order of 10-20 µm [1], or even larger in the case of analog circuits where high precision matching of the device properties of the silicon transistors is required [21].

In the present work, a TSV structure exhibiting very low thermomechanical stresses is proposed. The key element of this structure is the use of Invar alloy as via metal fill. Invar is a Ni-Fe alloy containing 36% of nickel, featuring an extremely low CTE that is well matched to the CTE of silicon. Invar is a ferromagnetic material that is commercially available in wire form; thus, it is compatible with magnetic assembly, a low-cost fabrication technique for realizing very high aspect-ratio TSVs with inherently void-free metal cores [22,23].

We provide a detailed description of the fabrication and characterization of Invar TSVs [24]. The fabricated Invar TSVs are temperature cycled between -50 °C and 190 °C for 100 times. Furthermore, their tolerance to elevated temperatures up to 365 °C is evaluated. The electrical resistances of the TSVs are used as an indicator of their performance in the temperature cycling experiments. In addition, we use CTE data at different temperatures to model the thermomechanical mismatch strain between via metal and substrate for different via materials, and we show that Invar offers the best thermomechanical match over a wide temperature range, compared to copper or tungsten. The improved CTE match is expected to increase the reliability of single TSVs but also of multi-chip stacks, by re-

ducing the effective CTE of a silicon wafer with TSVs and thus potentially reducing the fatigue loading on the solder bumps. We also use finite-element (FE) simulations to estimate the stress distribution in Invar-based TSVs and in the surrounding silicon at various temperatures. The stress distribution in an Invar TSVs is compared to the stress distribution in a copper-based TSV structure described in literature [9]. We show that the use of Invar reduces the cracking probability and the carrier mobility drifts in the silicon region surrounding the TSV.

II. TSV STRUCTURE, MATERIALS AND THERMAL MODEL

Fig. 1: Cross-sectional schematic of a generic TSV structure, indicating the terminology used in this paper.

Figure 1 introduces the terminology and the structure that is discussed in the present paper. It consists of a cylindrical metal element embedded in a silicon substrate. An insulating layer provides electrical insulation between the conducting metal via and the substrate. Two sets of materials for two different TSV structures have been compared:

- A novel structure based on Invar as via conductor in combination with Filmtronics 400F spin-on glass (SOG) and a thin layer of SiO₂ as via insulator.
- A reference structure based on copper as via conductor in combination with SiO₂ as via insulator.

In this paper, the stress and strain free reference temperature T_r is defined as the temperature at which the geometrical dimensions of all the elements of the model correspond to the nominal design and at which no thermal stresses are present. For the Invar TSV model, T_r is set to 250 °C which, in the realized demonstrator device, was the highest temperature used to solidify the SOG liner and therefore fix the TSV geometry. For the copper TSV model, the plating temperature of 50 °C reported for the copper TSV structures [9] is used as reference temperature T_r . Tungsten has been proposed [25,26] as a better CTE-matched alternative to copper (tungsten CTE is 4.42 ppm/°C at 20 °C [27]) and is included in the following discussion as a reference material. However, high stress in

deposited tungsten makes it susceptible to delamination which limits the maximum metal thickness to the order of a few microns and restricts the use of tungsten to small-diameter disk-shaped vias or to ring-shaped (annular) vias [25,26,28]. Thus, for fully metal-filled via holes, the use of tungsten is limited to blind vias or vias in very thin substrates. Tungsten T_r is set to 440 °C based on its typical CVD temperature [25].

The CTE at a temperature T can be defined either as mean CTE

$$\bar{\alpha}_{T_r}(T) = \epsilon_{T_r}(T) \frac{1}{T - T_r} = \frac{L(T) - L(T_r)}{L(T_r)} \cdot \frac{1}{T - T_r} \quad (1)$$

or instantaneous CTE

$$\alpha_{T_r}(T) = \frac{d\epsilon_{T_r}(T)}{dT} = \frac{1}{L(T_r)} \cdot \frac{dL(T)}{dT}, \quad (2)$$

where $\epsilon_{T_r}(T)$ is the strain caused by a temperature change from T_r to T and $L(T)$ is the length of an object at temperature T . Instantaneous CTE depends on the choice of T_r [29] and relationship $\alpha_{T_{r2}}(T) = \alpha_{T_{r1}}(T)L(T_{r1})/L(T_{r2})$ is obtained by writing Equation 2 twice for reference temperatures T_{r1} and T_{r2} . Substituting $L(T_{r2}) = L(T_{r1}) + L(T_{r1}) \int_{T_{r1}}^{T_{r2}} \alpha_{T_{r1}}(T) dT$ and cancelling common terms leads to equation

$$\alpha_{T_{r2}}(T) = \alpha_{T_{r1}}(T) \frac{1}{1 + \int_{T_{r1}}^{T_{r2}} \alpha_{T_{r1}}(T) dT}, \quad (3)$$

which is used to change T_r to the relevant fabrication temperature. Equation

$$\alpha_{T_r}(T) = \bar{\alpha}_{T_r}(T) + (T - T_r) \frac{d\bar{\alpha}_{T_r}(T)}{dT} \quad (4)$$

gives conversion from one CTE type to another [30].

The CTEs of the TSV substrate [6] and the metal conductor [7,27,31,32] materials are shown in Table I and are plotted in Figure 2 as a function of temperature. The CTE functions of all evaluated conductor materials were modified using Equation 3 so that their reference temperatures T_r match those originating from fabrication methods as discussed above. Silicon T_r in Table I and Figure 2 is set to 50 °C, matching the case of the copper TSV. Changes in silicon CTE with different T_r are minimal and therefore are not shown. Invar CTE data [32] in the temperature range from 100 °C to 900 °C has been given as mean CTE values which were fitted with a 3rd order piecewise polynomial and converted to instantaneous form using Equation 4. An interpolating line was used to bridge the gap between available Invar CTE datasets in the temperature range from 26.85 °C to 100 °C.

In an ideal structure with a single TSV and no insulating layer, all the stresses in the TSV structure are proportional to the mismatch strain ϵ_m [33] defined as

$$\epsilon_{m,T_r}(T) = \int_{T_r}^T [\alpha_{C,T_r}(T) - \alpha_{S,T_r}(T)] dT, \quad (5)$$

where α_C and α_S are the CTEs of the conductor and the substrate, respectively. Therefore, $\epsilon_{m,T_r}(T)$ can be considered as a quantitative indication of the thermal mismatch between the via conductor and the substrate. Figure 3 shows the mismatch strains $\epsilon_{m,T_r}(T)$ of Invar, copper and tungsten when used as TSV conductors in a silicon substrate. To

Fig. 2: CTEs of silicon, copper, Invar and tungsten versus temperature.

calculate these values, silicon T_r was changed to match that of the relevant TSV fabrication temperature of each conductor material. Compared to copper, Invar shows a significantly improved CTE matching with the silicon substrate. Similarly, Invar is better matched to silicon than tungsten at temperatures below 277 °C and at this temperature copper's mismatch strain is over 16 times higher than Invar's.

Fig. 3: Mismatch strains $\epsilon_{m,T_r}(T)$ as defined in Equation 5 plotted for Invar, copper and tungsten as TSV conductors in a silicon substrate.

III. THERMO-MECHANICAL SIMULATION

COMSOL 5 was used for FE simulation of the TSV structures. By taking advantage of the symmetries of a single via structure, a 2D axisymmetric model of half of the wafer thickness was simulated. Boundary conditions and model geometry are summarized in Figure 4 and Table III. As discussed in Section IV, the via conductor is insulated from the substrate by a thin layer of thermal SiO_2 coated with spin-on glass. However, the SiO_2 layer has been neglected in the FE model

Material	Range	Constants with related function (temperatures in Kelvins)			
		C_0	C_1	C_2	C_3
Silicon [6]		$\alpha_{50^\circ C}(T) \cdot 10^6 = C_0 + C_1 \cdot T + C_2 \cdot T^2 + C_3 \cdot T^3$			
	120 K $\leq$ T $\leq$ 1500 K	3.7245	5.8793×10^{-3}	1.2398×10^2	5.5473×10^{-4}
Copper [7]		$\alpha_{50^\circ C}(T) \cdot 10^6 = C_0 + C_1 \cdot T + C_2 \cdot T^2 + C_3 \cdot T^3$			
	66 K $\leq$ T $\leq$ 243 K	-6.5956	2.6026×10^{-1}	-1.0672×10^{-3}	1.5452×10^{-6}
	243 K $\leq$ T $\leq$ 800 K	1.1499×10^1	2.4334×10^{-2}	-2.8798×10^{-5}	1.4730×10^{-8}
Tungsten [27]		$\alpha_{440^\circ C}(T) \cdot 10^6 = C_0 + C_1 \cdot T + C_2 \cdot T^2 + C_3 \cdot T^3$			
	160 K $\leq$ T $\leq$ 235 K	2.2456×10^{-1}	3.9742×10^{-2}	-1.3535×10^{-4}	1.6637×10^{-7}
	235 K $\leq$ T $\leq$ 330 K	1.7326	2.0480×10^{-2}	-5.3389×10^{-5}	5.0202×10^{-8}
	330 K $\leq$ T $\leq$ 550 K	3.3464	5.8046×10^{-3}	-8.9309×10^{-6}	5.2497×10^{-9}
	550 K $\leq$ T $\leq$ 1800 K	4.1517	1.4151×10^{-3}	-9.4918×10^{-7}	4.1678×10^{-10}
Invar instantaneous		$\alpha_{250^\circ C}(T) \cdot 10^6 = C_0 + C_1 \cdot T + C_2 \cdot T^2 + C_3 \cdot T^3$			
	80 K $\leq$ T $\leq$ 300 K [31]	1.0083	1.6778×10^{-2}	-5.9149×10^{-5}	3.5151×10^{-9}
	300 K $\leq$ T $\leq$ 373.15 K	2.0448	-4.1050×10^{-3}	0	0
	373.15 K $\leq$ T $\leq$ 623.15 K	1.3446×10^2	-9.0985×10^{-1}	1.9556×10^{-3}	-1.2845×10^{-6}
	623.15 K $\leq$ T $\leq$ 1173.15 K	-7.0770×10^1	2.8979×10^{-1}	-3.0907×10^{-4}	1.0854×10^{-7}
Invar mean *		$\bar{\alpha}_{25^\circ C}(T) \cdot 10^6 = C_0 + C_1 \cdot T + C_2 \cdot T^2 + C_3 \cdot T^3$			
	373.15 K $\leq$ T $\leq$ 623.15 K	4.8297×10^1	-2.8932×10^{-1}	5.5651×10^{-4}	-3.2135×10^{-7}
	623.15 K $\leq$ T $\leq$ 1173.15 K	-3.6034×10^1	1.1667×10^{-1}	-9.4999×10^{-5}	2.7154×10^{-8}

* Curve fitted to CTE values from Harada *et al.* [32]. The first data point value of 11.18 was interpreted to be a typographical error and 1.18 was used instead on the basis of other datasets and figures in the same source.

TABLE I: Functions for instantaneous CTEs of silicon, copper, tungsten and Invar together with the mean CTE of Invar. Number of digits does not represent the precision of the values.

since its effect on the simulation results proved to be negligible compared to the effects from the thicker spin-on glass layer.

Fig. 4: Geometrical model used in the FE simulation (not to scale). Radial and shear stress are plotted along lines A and B in Figure 8 and 9. Where not specified, free boundary conditions are applied on the model boundaries.

The geometrical parameters of the Invar TSV has been chosen to be as similar as possible to the geometry of a copper-based TSV reference structure whose thermomechanical performance has been studied both numerically and experimentally [9]. However, while the reference copper structure has been characterized between -55 °C and 125 °C, the novel

Material	Young's Modulus (GPa)	Poisson's ratio	CTE (ppm/°C)
Silicon dioxide	71.4 [9]	0.16 [9]	0.5 [9]
400F SOG	71.4 [9]	0.16 [9]	3 [34]
Invar	138 [35]	0.28 [35]	Table I
Silicon	130.91 [9]	0.28 [9]	Table I
Copper	73 [36]	0.3 [9]	Table I

TABLE II: Material properties used in the FE simulation. Young's modulus and Poisson ratio of 400F spin-on glass have been assumed to be the same as for SiO₂; the parameters of the spin-on glass have in general a very limited influence on the results given the small thickness of the layers compared to the overall structure.

Invar structure has been evaluated in a wider temperature range between -50 °C and 190 °C. The parameters used for the properties of the materials in the simulation are summarized in Table II. All materials are considered to have linear elastic properties. Indeed, an analysis of the von Mises stress distributions generated in the thermomechanical simulations (not shown here) revealed that no plastic deformation should occur according to the von Mises criterion, with the yield stress of electroplated copper and Invar being 233 MPa [36] and 291 MPa [37], respectively.

Modelling of stress-distributions can provide insights on two issues that are known to affect copper-based TSVs, namely alteration of the charge carrier mobility in the silicon region surrounding the via and cracks onset and propagation. Comparisons between simulated stress distributions and analysis of cross-sections of TSVs after thermal cycling have shown a strong correlation between cracking and regions with high

Parameter	Value (μm)
r_{via}	22.5
$t_{ins,via}$	2.0
$t_{ins,top}$	2.0
w_{Si}	43.0
t_{wafer}	300.0

TABLE III: Geometrical parameter values used in the simulation (c.f. Figure 4).

stress concentrations [9,38]. Figure 5 summarizes the fracture modes that have been identified in TSVs at the interfaces between different materials [9,33,38]. In previous works, one critical location in particular appeared to be the Cu/SiO₂ interface at the top surface, where high shear stress is likely to induce mode II interfacial fractures [9]. Cu/SiO₂ interfacial cracks also appeared in the via sidewalls [9,38] and they are attributed to shear stress which, during cooling, is combined with high tensile stress. This occurs because the copper tends to contract to a larger extent than the substrate: the two effects thus contribute to a mixed mode I and II fracture [33].

Fig. 5: Overview of the fracture modes occurring in TSVs under thermal loading. Mode I fractures are due to radial tensile stress, mode II fractures are due to shear stress [39].

The correlation between cracking and stress concentration is coherent with fracture mechanics considerations. Indeed, Equations 6 and 7 apply for strain energy release rates in a multilayered structure [40]:

$$G_I \propto \sigma^2 \quad (6)$$

$$G_{II} \propto \tau^2 \quad (7)$$

where G_I , G_{II} , σ and τ are the mode I and mode II strain energy release rates, the normal and the shear stress ahead of the crack tip respectively. A number of failure criteria have been proposed, but, in general, failure is expected to occur when G_I and G_{II} are large enough so that a combination of them exceeds a certain threshold, which depends on the materials and on their bonding energies [41].

The copper TSVs reported in [9] have been subjected to 4500 thermal cycles between -55 °C and 125 °C. Cracks and delaminations appeared in a large number of TSVs, especially along the SiO₂/Cu interface and radially, from the SiO₂/Si

interface towards the substrate. However, electrical failure did not occur, and fracture mechanical analysis revealed that catastrophic crack propagation in the copper or in the substrate bulk should not be expected under the above conditions [9]. Nevertheless, the presence of cracks in the TSV structure can potentially lead to critical failures under more extreme thermal cycling, such as the ones which can occur in automotive and other harsh environment applications [10], or if more complex structures, such as multilayered interconnects, are present. Moreover, a crack breaking the insulating layer could lead to current leakage and copper diffusion in the substrate [38]. Hermeticity in MEMS packages could also be compromised by cracks in the substrate caused by the TSV structures. Therefore, the shear and the radial stress values in the copper TSV reference structure at -55 °C and 125 °C, will be considered as representative of a potential failure situation.

Fig. 6: Shear stress τ distribution. Top row: Invar TSV. Bottom row: Copper TSV. Left column: -55 °C. Right column: 125 °C. identical colour scales have been used in all columns. The absolute value of the peak shear stress in the Invar TSV is 1.7 times and 3.9 times lower than in the copper TSV at -55 °C and 125 °C, respectively.

Figure 6 and Figure 7 show a comparison of the distribution of radial and shear stress at -55 °C and 125 °C for the copper TSV and the Invar TSV respectively. To be consistent, stresses in the two structures have been compared at the

Fig. 7: Radial stress σ_r distribution. Top row: Invar TSV. Bottom row: Copper TSV. Left column: -55 °C. Right column: 125 °C. identical colour scales have been used in all columns. The absolute value of the peak radial stress in the Invar TSV is 1.9 times and 3.3 times lower than in the copper TSV at -55 °C and 125 °C, respectively.

same temperatures, even if the Invar TSV was evaluated at a minimum temperature of -50 °C due to limitations in our experimental setup. However, simulations show that stresses at -50 °C and at -55 °C in the Invar TSV differ by less than 1%. The location of the high-stress regions is coherent with the expectations based on published data [9,38,42], namely the conductor/insulator interface close to the surface and in the central part of the via along the wafer thickness. A quantitative comparison of the stress levels in these critical regions in the two TSV structures will be performed in the following paragraphs. However, it should be noted that stress levels in the Invar structure are barely noticeable if identical colour scales are used for the copper and the Invar structures, as shown in Figure 6 and Figure 7.

The simulated shear stresses along the conductor/insulator interface for both TSVs are shown in Figure 8. Even if the temperature interval for the Invar structure is increased to between -50 °C and 190 °C, peak shear stresses are in all cases at least five times smaller than the ones present in the

Fig. 8: Shear stress along the conductor/insulator interface (line A in Figure 4) for the Invar and copper TSVs at the lowest and highest temperatures respectively. Stresses in the Invar TSV at 300 °C and 365 °C, at which the structure has been evaluated in a long-term high-temperature exposure experiment, are also shown.

copper structures in the temperature range from -55 °C to 125 °C. It is not until the temperature reaches 365 °C that the stresses in the Invar TSV becomes comparable to the stresses in the copper TSV at 125 °C.

Fig. 9: Radial stress at the location 200 nm below the top silicon surface (line B in Figure 4) for the Invar and copper TSVs at the lowest and highest temperatures respectively. Stresses in the Invar TSV at 300 °C and 365 °C, at which the structure has been evaluated in a long-term high-temperature exposure experiment, are also shown. For this plot, w_{Si} has been increased to 500 μm and data has been truncated at $w_{Si}/2$ to eliminate the unrealistic stress due to the peeling of the top oxide at the edge of the wafer.

As highlighted in Figure 9, similar considerations can be formulated when comparing the radial stress close to the Si/top SiO₂ interface, where stresses can affect carrier mobility and might require a keep-away-zone for transistors around the TSVs. Assuming a biaxial stress state in this region, it can be shown that, because of the piezoresistivity of silicon, the maximum relative mobility variation for a transistor chan-

nel oriented along a [110] direction is $\sigma_r \sqrt{\Pi_{xxx}^2 + \Pi_{xyy}^2}$ [20]. With the piezoresistive coefficients in Table IV, if the maximum tolerable mobility variation is 5%, then pMOS and nMOS transistors should not be placed where radial stress is higher than ≈ 50 MPa and ≈ 140 MPa, respectively. Therefore, according to Figure 9, a keep-away-zone of about 20 μm must be defined for the copper via. In contrast, using the same assumptions, the Invar via does not require any keep-away-zone as the mobility variation over the extended temperature range from -50 $^{\circ}\text{C}$ to 190 $^{\circ}\text{C}$ would always be less than 3%.

Doping	Π_{xxx} (Pa^{-1})	Π_{xyy} (Pa^{-1})
n	-3.16×10^{-10}	-1.76×10^{-10}
p	7.18×10^{-10}	-6.63×10^{-10}

TABLE IV: Piezoresistive coefficients of silicon [20].

IV. INVAR TSV FABRICATION AND CHARACTERIZATION

Invar TSV structures were fabricated and characterized in order to demonstrate their ability to withstand large temperature variations as suggested by simulations. Therefore, Invar wire (California Fine Wire Co., USA) with a diameter of 45 μm was cut to rods with a nominal length of 320 μm using a similar dicing-saw cutting method as described by Fischer *et al.* [22]. The only notable difference was the addition of an etch step (30 s in 3.5 M FeCl_3) between wire cutting and releasing the wires from a wafer supporting them during the wire cutting. The etching step removes burr defects created by the dicing saw at the ends of the rods during cutting. Figure 10 summarizes the steps involved in the TSV manufacturing by magnetic assembly [22,23]. A 300 μm thick double-sided-polished p-type silicon wafer with (100) crystal orientation was thermally oxidized. Holes with a diameter of 55 μm and a pitch of 350 μm were created in the topside SiO_2 masking layer using reactive ion etching (see Figure 10a). Deep reactive ion etching (DRIE) of silicon using the Bosch process was performed to form the via holes. The SiO_2 membrane on the backside of the wafer was used as an etch-stop layer for the DRIE process. Another thermal oxidation step created a 0.5 μm thick SiO_2 layer on the side walls of the via holes while the topside SiO_2 reached the final thickness of 1.6 μm (see Figure 10b). The Invar rods were placed on the substrate and pulled into the via holes by moving a magnet underneath the wafer (see Figure 10c). The yield of the magnetic assembly was not part of this study but previous works show that a 100% filling yield can be achieved by tuning the magnetic assembly parameters and by using an excess amount of wires compared to the number of via holes [22]. The assembly process has been projected to be scalable to wafer level while retaining 100% yield by moving an array of magnets underneath the wafer [43]. A several millimetres thick layer of spin-on glass (400F, Filmtronics Inc., USA) was drop-casted on the substrate surface. Air in the gaps between the Invar rods and the sidewalls of the via holes was removed by exposing the substrate to a vacuum of 0.2 bar for 10 minutes. This allowed the SOG to fill the gaps without trapping voids. The

SOG was baked on a hotplate at steps of 80 $^{\circ}\text{C}$, 150 $^{\circ}\text{C}$, and 250 $^{\circ}\text{C}$ in an ambient air atmosphere. Each temperature was sustained for one minute and the wafer was kept on the hotplate while the temperature was increased between the baking steps. The wafer was left to cool slowly on the hotplate after baking in order to prevent SOG cracking (see Figure 10d). The protruding ends of the Invar rods and the excess SOG were ground away. The SiO_2 membranes on the backside of the substrate were opened by reactive ion etching (see Figure 10e). A metallization consisting of 50 nm thick TiW and 0.5 μm thick Au were sputtered on both sides of the substrate and subsequently patterned using femtosecond laser ablation in order to form TSV pairs in which individual TSVs are connected in series (see Figure 10f). The wafer was diced and five chips, each containing multiple TSV pairs, were mounted on ceramic dual in-line chip carriers using high-temperature glue (930-4, Epoxy Technology Inc., USA). TSV pairs were contacted to the package using gold ball/stitch wire bonding (see Figure 10g). TSV, pad and wire bonding can be identified in the SEM image in Figure 10h. A cross-sectional SEM image of two TSVs is shown in Figure 10i. The result of laser patterning is visible on the top metallization, whereas the bottom metallization connects the two TSVs in series. The material layout and the void-free SOG filling of the TSVs is shown in the inset of Figure 10i, obtained after polishing the cross section.

Changes in the electrical resistance of the TSVs were used as an indicator for possible TSV deterioration in response to temperature-induced stresses. Two-point resistance measurements were used and therefore the measured resistances include the resistances from the wire bonds and the package leads. Two-point resistance measurements were deemed a reasonable compromise allowing a larger amount of TSV pairs to be evaluated. In addition, resistances of four TSV pairs were measured using four-point measurements after the chip had been exposed to all temperature treatments discussed in the following. The lowest resistance value obtained for a TSV pair with a four-point measurement was 569 m Ω , giving a nominal resistance value of 284.5 m Ω for a single TSV. The measured four-point value includes the Invar rods, the contact resistances between the Invar rods and the surface metallization on both sides of the wafer as well as the resistance from the backside metallization contacting the two TSVs. The electrical resistivity of Invar is between 750 n $\Omega \cdot \text{m}$ and 850 n $\Omega \cdot \text{m}$ [44], resulting in a theoretical resistance of between 141 m Ω and 160 m Ω for the Invar core of a single TSV. The measured value is consistent with the expected value, especially when the contact resistances between the surface metallization and the Invar TSV are taken into account. It should be noted that the resistivity of Invar is about one order of magnitude larger than that of copper or tungsten but is five orders of magnitude smaller than the resistivity of heavily doped polysilicon, another material which has been proposed for low-stress TSVs [45].

The TSVs were temperature cycled between -50 $^{\circ}\text{C}$ and 190 $^{\circ}\text{C}$ for 100 complete cycles with one cycle typically taking 66 min. Resistances of 51 TSV pairs were measured at room temperature before cycling, then after 65 cycles

Fig. 10: Process flow of TSV fabrication using magnetic assembly: a) silicon dioxide patterning, b) etching of through silicon holes, c) magnetic assembly of Invar rods, d) gap fill by SOG using drop casting and vacuum treatment, e) front side planarization together with patterning of back-side contact openings, and f) metallization with patterning and wire bonding to g) a ceramic chip carrier. h) Top SEM image of two TSVs with respective pads and wire bonds. i) Cross-sectional SEM image of two TSVs connected in series via backside metallization. Inset: upper corner of a TSV after polishing the cross section.

Fig. 11: Horizontal axis shows the resistance of a TSV pair before temperature cycling. The vertical axis shows the largest change in resistance of each TSV pair either after 65 cycles or after 100 cycles.

and then again after a total of 100 cycles. For each TSV pair, Figure 11 shows the resistance before cycling and its largest change either after 65 or 100 cycles, whichever is larger. One TSV pair with an initial resistance of $2.052\ \Omega$ failed before 65 cycles and, therefore, is not included in the figure. As it can be seen in Figure 11, TSV pairs with a low initial resistance show minimal resistance changes during cycling. The pairs with the initial resistance below an arbitrary $1.6\ \Omega$ limit show a maximum resistance increase of $6\ \text{m}\Omega$ and a maximum decrease of $35\ \text{m}\Omega$ compared to their initial value. The observed resistance decrease could be attributed

to metal annealing at high temperatures during cycling. In this case, TSV stability could possibly be further improved by adding an annealing step at the end of the TSV fabrication sequence. The large resistance increases for TSV pairs with high initial resistances could be explained by a poor electric contact quality between the surface metallization and the Invar TSV core making these TSVs more sensitive to temperature-induced stresses.

In order to establish a thermal budget for the proposed TSVs, temperature cycling as described above was complemented by further testing at elevated temperatures. One chip containing 11 TSV pairs was heated up to $300\ ^\circ\text{C}$, kept at this temperature for one hour, cooled down to room temperature, heated up to $365\ ^\circ\text{C}$, kept at this temperature for one hour, and cooled down again. Heating to $300\ ^\circ\text{C}$ took 11 minutes and heating to $365\ ^\circ\text{C}$ took 18 minutes. After each high-temperature exposure, the chip was left to cool down slowly for over one and half hours on a switched-off hotplate. Thereafter, two-point measurements were carried out at room temperature to extract the TSV resistances. The temperature of $365\ ^\circ\text{C}$ is the maximum our experimental setup can apply and does not necessarily represent the highest tolerable temperature of the proposed TSV structure. Figure 12a shows the resistances of these 11 TSV pairs after each thermal treatment. Figure 12b shows a close-up of the TSV pairs with lower initial resistance, indicating stable resistances as a response to temperature cycling and exposure to elevated temperatures of $300\ ^\circ\text{C}$ and $365\ ^\circ\text{C}$.

A separate sample was prepared to characterize capacitive properties of the proposed TSV structure. Laser ablation has been used to define pads connected to individual TSVs on the top metallization and to isolate TSVs on the bottom metallization. The capacitance between pairs of adjacent TSVs

Fig. 12: Measured resistances of 11 TSV pairs in one chip after temperature cycling and after subsequent exposure to elevated temperatures of 300 °C and 365 °C. Each line represents a TSV pair. a) All pairs; b) A close-up of the TSV pairs with low resistance TSV.

has been measured with a probe station connected to a Keithley 4200A-SCS measurement system (1 MHz signal with 100 mV RMS amplitude and no DC bias), on the pristine samples and after thermal treatment as discussed in the following paragraph. To minimize the impact of the capacitance between pads and probes, the capacitances of two additional couples of pads with the same size and separation but without the corresponding TSV in the substrate have been measured, averaged together and subtracted from all the measurements. The resulting capacitance corresponds to the series of the two capacitors composed of one TSV and the substrate.

The capacitances between 10 pairs of adjacent TSVs before and after one thermal cycle between -50 °C and 190 °C, after a one hour exposure to a temperature of 300 °C and an additional one hour exposure to a temperature of 365 °C, are shown in Figure 13. Across samples, there is a relevant variability due to the difficulty of precisely controlling the thickness of the spin-on glass along the TSV length. However, all TSV pairs show a capacitance variation of less than 17% after one thermal cycle and the exposure to a temperature of 300 °C and 8 pairs out of 10 also after the exposure to a temperature of 365 °C.

Fig. 13: Capacitances between 10 pairs of adjacent TSVs, measured before and after a temperature cycle and subsequent exposure to elevated temperatures of 300 °C and 365 °C. Each line represents a TSV pair.

V. CONCLUSIONS

An innovative TSV structure with Invar as via conductor has been investigated as a solution to enable 2.5D and 3D integration in applications where the device is subjected to temperatures of up to 365 °C and temperature cycles from -50 °C to 190 °C. Invar features a CTE that is better matched to silicon compared to copper, resulting in a lower mismatch strain over wide temperature ranges, without the fabrication and design limitations of tungsten. Furthermore, FE simulations indicate that, in the critical regions where cracks are most likely to occur, thermomechanical stresses in an Invar TSV are at least five times smaller than in a copper-based TSV with the same geometry in a narrower temperature range. Lower stresses result in improved reliability due to a reduction of the probability of cracking and in a reduction of the keep-away-zone for transistors surrounding the TSV due to the lower carrier mobility variation induced by piezoresistivity in silicon.

An array of Invar TSV pairs has been fabricated by magnetic assembly and has been exposed to 100 thermal cycles between -50 °C and 190 °C. One TSV pair out of 51 failed, and 42 TSVs showed resistance increases of less than 6 mΩ. 11 TSV pairs have been subsequently exposed to 300 °C and 365 °C for one hour at each temperature without resulting in any TSV device failure. Capacitive measurements have been performed on 10 TSV pairs before and after one thermal cycle between -50 °C and 190 °C and exposures to 300 °C and 365 °C for one hour at each temperature. All TSV pairs showed a capacitance variation of less than 17% after a thermal cycle and the exposure to a temperature of 300 °C, and 8 out of 10 also after the final exposure to a temperature of 365 °C.

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