Potential of Ultra-High Voltage Silicon Carbide Semiconductor Devices

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Abstract—In this paper, the theoretical performance of ultra-high voltage Silicon Carbide (SiC) based devices are investigated. The SiC semiconductor device conduction power loss and switching power loss are predicted and compared with different modeling approaches, for SiC metal-oxide semiconductor field-effect transistors (MOSFETs) up to 20 kV and SiC gate turn-off (GTO) thyristors and SiC insulated-gate bipolar transistors (IGBTs) up to 50 kV. A parameter sensitivity analysis has been performed to observe the device power loss under various operating conditions, for instance current density, temperature and charge carrier lifetime. Also, the maximum allowed current density and maximum switching frequency for a maximum chip power dissipation limit of 300 W/cm² are investigated. The simulation results indicate that the SiC MOSFET has the highest current capability up to approximately 15 kV, while the SiC IGBT is suitable in the range of 15 kV to 35 kV, and thereafter the SiC GTO thyristor supersedes the loss performance from 35 kV to 50 kV.

Keywords—Silicon Carbide; 4H-SiC; Ultra-High Voltage Device; SiC MOSFET; SiC GTO thyristor; SiC IGBT

I. INTRODUCTION

Efficient electrical energy transmission across long distances is enabled by high power electronic technologies such as high-voltage direct current transmission (HVDC) and flexible ac transmission systems (FACTS). Traditionally, silicon (Si) based thyristors have been used for current controlled HVDC. Similarly, Si insulated-gate bipolar transistors (IGBTs) have been the main choice for voltage-source converter based HVDC [1]. The introduction of MMC topologies had a significant impact on several power electronic applications, mainly due to the reduction of converter losses in comparison to two or three level VSC [1]. SiC based semiconductor devices are now acknowledged to offer better efficiency performance, along with reduction in the overall system cost over a wide span of power electronics applications, compared to leading horse Si counterparts, thanks to the superior physical properties of the SiC material in comparison to Si [2]. Furthermore, this material enables converter designs with relaxed cooling system requirements and smaller passive components. This facilitates more compact designs and thereby higher power densities. The main advantage of SiC based semiconductor devices is the strong electric breakdown field strength, about 10 times higher than that of Si, which enables

semiconductor device designs with reduced drift region thicknesses but with higher blocking voltage capabilities, in comparison to Si counterparts [2]. In order to realize devices with very high blocking voltages, the SiC crystal growth process must offer a sufficiently high quality, so as to grow thick epitaxial layers with low material defect densities. Additionally, it is a challenge to manufacture thick SiC epitaxial layers with sufficiently high charge carrier lifetimes that should provide sufficient conductivity modulation in the drift region of bipolar devices. It is predicted that carrier lifetimes of 2 μ s, 5 μ s, and 10 μ s are required to ensure sufficient conductivity modulation of SiC devices with blocking voltage ratings of 10 kV, 15 kV and 20 kV, respectively [3]. The relatively low carrier lifetimes in SiC are explained by the lifetime-killer point-defect center ($Z_{1/2}$), which is due to a carbon monovacancy [4]. Carrier lifetime enhancement processes have been developed to eliminate carbon vacancies [5, 6] and recent studies show charge carrier lifetimes above 20 μ s in high voltage SiC PiN-diodes [7]. The carrier lifetime enhancement processes might be further developed in order to provide futuristic bipolar devices with blocking voltages beyond those of the state-of-the-art research-level devices of today, which are capable of blocking voltages in the range of 12-27 kV [8-12].

The theoretical performance of SiC based semiconductor devices have been predicted by different analytical and empirical models [1, 13-17]. For example, Huang *et al.*, investigated the energy losses of SiC MOSFETs, SiC bipolar junction transistors (BJTs), and SiC GTO thyristors based on a set of analytical equations [13]. The results of the model indicated the total energy losses and maximum switching frequencies of the devices under various operating conditions. Similarly, Nawaz estimated the performance of high voltage SiC MOSFETs, SiC IGBTs, SiC Schottky-barrier diodes (SBDs) and SiC PiN diodes up to blocking voltages of 20 kV [14]. Recently, Chowdhury and Chow presented the results of numerical simulation studies for SiC n- and p- IGBTs with blocking voltages in the range of 15 kV to 25 kV [15]. Wang *et al.*, investigated the feasibility of using high voltage SiC thyristors in HVDC applications [16]. It was concluded that SiC thyristor could greatly reduce the number of devices in series connection along with lower energy loss in comparison to Si thyristors. To the best of author's knowledge, no studies

are presented in the scientific literature for predicting SiC device performance with blocking voltages exceeding 30 kV.

This work aims to predict the performance of ultra-high blocking voltage SiC based semiconductor devices. The objective is to further extend the Huang [13] and Nawaz [14] models towards higher blocking voltages, for instance SiC MOSFETs up to 20 kV and SiC GTO thyristors and SiC IGBTs up to 50 kV. The two models are implemented and the simulation results are compared to the Baliga modeling approach [17]. In this model, both analytical equations and empirical equations have been used to predict the conduction power losses and switching power losses under various operating conditions. The effect of temperature and charge carrier lifetimes have been investigated as well as the maximum allowed current density and switching frequency for a given maximum power dissipation level.

II. MODEL DESCRIPTION

A. General Modeling Approach

The modeling approaches implemented in this study are fully represented in [13-14, 17]. This section presents specific parts of the models for further discussion. Note that the implemented model is based on the assumption that the circuit oriented impact such as gate drivability, gate resistance and stray inductance on the switching characteristics is negligible for the intended device.

The general modeling approach is based on the use of conduction loss and switching loss to extract the total power loss (1) and by that determine the maximum allowed current density and switching frequency (2) for a given maximum power dissipation limit, e.g. $P_{D,MAX}=300 \text{ W/cm}^2$.

$$P_{TOT} = DP_{COND} + f(E_{ON} + E_{OFF}) \quad (1)$$

$$f_{MAX} = \frac{P_{D,MAX} - DP_{COND}}{E_{ON} + E_{OFF}} \quad (2)$$

here D is the duty cycle and f is the frequency. The SiC MOSFET, SiC GTO thyristor and SiC IGBT conduction loss and switching loss are expressed in terms of blocking voltage, V_B , which is related to the drift region doping concentration, N_D , and drift region thickness, W_D [14]. Further, the critical electrical field strength, E_C , is derived according to [14]. Temperature, T , current density, J , and initial carrier lifetimes, τ_{n0} , τ_{p0} , are variables in the model. A relation of $\tau_{n0}=10\tau_{p0}$ is assumed in the model. The carrier lifetimes are modeled according to the Scharfetter relation with power-law temperature dependence [18] and the carrier mobilities are modeled according to the Arora model [19]. The SiC bandgap properties and intrinsic carrier concentration, n_i , is derived according to [20]. The modeling parameters used in the model are presented in Table 1. The theoretical blocking voltage as a function of drift layer doping concentration is presented in Fig 1. The particular drift region doping concentration and drift region width for the theoretical devices used in this model are presented in Fig 2.

TABLE I
MODELING PARAMETERS

Symbol	Parameter name	Value and Unit
D	Duty cycle	0.5
A	Active device area	1 cm ²
ϵ_{SiC}	Permittivity SiC	10.1
ϵ_{SiO_2}	Permittivity SiO ₂	3.9
$v_{sat,p}$	Saturation velocity holes	$2 \times 10^7 \text{ cm/s}$
V_{GH}	MOSFET high gate voltage	20 V
V_{GL}	MOSFET low gate voltage	-5 V
$N_{a,GTO}$	GTO thyristor anode doping concentration	$5 \times 10^{19} \text{ cm}^{-3}$
$N_{a,IGBT}$	IGBT emitter doping concentration	$5 \times 10^{19} \text{ cm}^{-3}$
W_e	IGBT Emitter diffusion length	$3.3 \times 10^{-7} \text{ cm}$
t_{ox}	Oxide layer thickness	$5 \times 10^{-6} \text{ cm}$
g_m	IGBT transconductance	0.3 S
V_G	IGBT gate voltage	20 V
V_{TH}	IGBT threshold voltage	4.36 V
p	Cell pitch	$2 \times 10^{-3} \text{ cm}$
L_{CH}	Channel length	$1 \times 10^{-4} \text{ cm}$
μ_{ni}	Channel mobility	$20 \text{ cm}^2/\text{Vs}$

Fig. 1. Blocking voltage as a function of drift region doping concentration and drift region width.

Fig. 2. Estimated drift region doping concentration and drift region width for the theoretical devices investigated in this model.

B. SiC MOSFET Model

The SiC MOSFET on-state characteristics are mainly given by the sum of resistive elements inherently in the device, for instance the MOS-channel resistance, drift region resistance and substrate resistance. The resistance contribution raised from the drift region is significantly larger than the other contributing resistances (e.g., channel resistance, contact resistance) for SiC MOSFET devices with blocking voltage

capabilities above 1.2 kV [21]. The specific on-state resistance of two modeling approaches, analytically [13] and empirically [14], are implemented in the model. The empirically extracted on-state resistance is based on extracted values of 10 kV and 15 kV SiC MOSFET [22]. The SiC MOSFET switching characteristics are mainly governed by charging and discharging of the gate-source and gate-drain capacitances, in an ideal case. The ideal SiC MOSFET characteristics are derived according to [13,14] which depends on the switching voltage, V_{DS} , peak transconductance, g_m , threshold voltage, V_{TH} , and gate drive upper and lower voltage, V_{GH} , V_{GL} . The switching voltage is assumed to 60 % of the blocking voltage (i.e., $V_{DS}=0.6V_B$). The temperature dependent peak transconductance and threshold voltage parameters are extracted from experimental data of a 10 kV SiC MOSFET [23], as presented in Fig. 3.

The simulated SiC MOSFET performance for Huang and Nawaz modeling approach are presented in Fig. 4. The conduction power loss density are estimated to 30 W/cm² to 60 W/cm² in the range of 10 kV to 20 kV, under the given conditions of $J=15$ A/cm² and $T=300$ K. The main difference between the two models, besides the analytical and empirical approach, is that the change in E_C is accounted by a cubic relation for the $R_{SP,ON}$ in the analytical model [13], in contrast to the empirical model where the E_C is only accounted through the blocking voltage. The switching losses for the ideal SiC MOSFET contributes insignificantly to the total power losses at the switching frequency of $f=150$ Hz.

C. SiC IGBT Model

The conduction losses of bipolar SiC devices are composed of two parts. The first part is the knee-voltage, V_{KNEE} which is close to the built-in potential/bandgap energy of SiC material and the second part is related to the inherent resistive elements in the device, similar to R_{ON} . The prediction of SiC IGBT conduction power loss density is based on extrapolation of the experimental values, similar as in [14]. The characteristics of high voltage state-of-the-art research-level SiC IGBT are used for extraction of V_{KNEE} and R_{ON} parameters, as shown in Fig. 5 [8 - 12]. The analytical conduction power loss density modeling approach by Baliga is implemented for comparison [17]. Here, the SiC IGBT forward voltage drop is modeled as

$$V_{F,IGBT} = V_{Knee} + \frac{pL_{CH}J}{\mu_{ni}C_{OX}(V_G - V_{TH})} \quad (3)$$

$$V_{Knee} = \frac{2kT}{q} \ln \left[\frac{JW}{4qD_a n_i F(W/2L_a)} \right] \quad (4)$$

where, the L_{CH} is the MOS-channel length, μ_{ni} is the channel mobility and p is the cell pitch. V_G is the gate voltage and C_{OX} is the oxide capacitance, determined from the oxide thickness, $C_{OX}=\epsilon_{OX}/t_{OX}$. T is the temperature, q is the elementary charge (1.602×10^{-19} C) and k is the Boltzmann's constant (8.617×10^{-5} eV/K). W is the drift region width, D_a and L_a is the ambipolar diffusion constant and length [17] and the function $F(W/2L_a)$ is determined according to (5-6), [17].

Fig. 3. Temperature dependence of SiC MOSFET peak transconductance and threshold voltage, extracted from the experimental data of a 10 kV SiC MOSFET [23].

Fig. 4. Simulated SiC MOSFET conduction power loss density and switching power loss density. The Huang [13] and Nawaz [14] conduction power loss density modeling approaches are compared. The switching loss power density are predicted by the same set of equations in the two models.

$$F\left(\frac{W}{2L_a}\right) = \frac{(W/2L_a) \tanh(W/2L_a)}{\sqrt{1 - 0.25 \tanh^4(W/2L_a)}} \exp\left(-\frac{qV_M}{2kT}\right) \quad (5)$$

$$V_M = \frac{2kT}{q} \left(\frac{W}{2L_a}\right)^2 \quad \text{for } (W/2L_a) \leq 2 \quad (6a)$$

$$V_M = \frac{3\pi kT}{8q} \exp(W/2L_a) \quad \text{for } (W/2L_a) > 2 \quad (6b)$$

here, V_M represents the voltage drop over the middle region [17]. The switching characteristics of SiC IGBT are mainly governed by the reverse recovery behavior of the free-wheeling diode during turn-on and the charge carrier removal within the IGBT drift region structure. For simplicity, the reverse recovery of the diode is not considered in this model, instead the turn-on energy loss is assumed equal to the turn-off energy loss. The turn-off energy loss is composed of the energy dissipated during the voltage rise phase and the current fall phase, in other words the tail current phase. Nawaz represented this event analytically [14] which also has been implemented

here. Also, the Baliga IGBT turn-off energy loss is implemented for comparison [17] as follows

$$E_{OFF} = J V_{CS} \left(\frac{t_V}{2} + \frac{\tau_{HL,N-Base}}{2} \right) \quad (7)$$

$$t_V = \frac{\epsilon_0 \epsilon_{SiC} p_0 V_{CS}}{W(N_D + p_{SC})J} \quad (8)$$

$$p_{SC} = \frac{J}{qv_{sat,p}} \quad (9)$$

where, V_{CS} is the IGBT switching voltage, t_V is the voltage rise time during turn-off. $\tau_{HL,N-Base}$ is the high level carrier lifetime in the collector layer and p_0 is the plasma density at the collector end of the IGBT device, which is assumed equal as for the Nawaz model, $p_a = p_0$ [14]. $v_{sat,p}$ is the hole saturation velocity.

The simulated SiC IGBT performance for Nawaz and Baliga modelling approach are presented in Fig. 6. The predicted conduction loss ranging from approximately 25 W/cm² to 90 W/cm² for the blocking voltage range of 10 kV to 50 kV, under the given conditions of $J=15$ A/cm², $T=300$ K and $\tau_{n0}=17$ μ s, which results in the ambipolar carrier lifetime of $\tau_a=10$ μ s. The main difference between the two modeling approaches, in the range of 10 kV to 20 kV, is due to the differences in knee voltage, $V_{KNEE} \approx 3.9$ V versus $V_{KNEE} \approx 3.4$ V. In literature, Mizushima *et al.*, has presented a 16 kV IE-n-IGBT with knee voltage characteristics of about 3.4 V [10]. In practice, the knee voltage is mainly determined by the SiC material quality, manufacturing process and the level of conductivity modulation in the drift region which ideally should approach the bandgap energy, $E_{G,SiC}=3.26$ V, for all voltage classes [7, 9-11]. The switching energy loss at $f=150$ Hz, of the SiC IGBT increases rapidly with increasing V_B and is a significant part of the total SiC IGBT losses.

D. SiC GTO Thyristor Model

The SiC GTO thyristor conduction loss follows the same modeling approach as for the SiC IGBT. The conduction losses as determined as (10) in the Huang model [13]. In order to compare the performance of the SiC IGBT and SiC GTO fairly, the same knee voltage model (4-6) is adopted to (10), denoted as ‘‘Mixed model’’. The Huang SiC GTO thyristor conduction loss is determined as

$$P_{COND} = JA \frac{E_G}{q} + JA \frac{3\pi kT}{8q} \exp\left(\frac{3V_B}{2L_a E_C}\right) \quad (10)$$

here, E_G is the bandgap energy of SiC and A is the device area. The SiC GTO thyristor turn-on and turn-off switching energy losses derived according to [13]. The Baliga SiC GTO turn-off loss modeling approach is added as reference. Similar to SiC IGBT, the losses are composed of losses during voltage rise time and the tail current. The W_P region thickness is assumed to 50 % of the W_N region thickness, similar as in [13]. The turn-on energy loss is derived as in [13].

Fig. 5. SiC IGBT knee voltage and specific on-resistance extracted from devices in literature [8-12].

Fig. 6. Simulated SiC IGBT conduction power loss density and switching power loss density.

$$E_{OFF} = E_{OFF,V} + E_{OFF,I} = \frac{qJ_{A,ON}(N_D + p_{SC})(W_P + W_N)^2}{6\epsilon_0 \epsilon_{SiC} \tau_a^2} t_V^3 + \frac{J_{A,D} V_S \tau_a}{2} \quad (9)$$

$$t_V = \sqrt{\frac{2\epsilon_0 \epsilon_{SiC} V_S}{q(N_D + p_{SC})(W_P + W_N)^2}} \tau_a \quad (10)$$

$$p_{SC} = \frac{J_{A,ON}}{qv_{sat,p}} \quad (11)$$

$$J_{A,D} = \frac{D_n J_{A,ON}^2 \tau_a^2}{q L_{nP+} N_{AA} (W_P + W_N)^2} \quad (12)$$

here, $J_{A,ON}$ is the on-state current density and $J_{A,D}$ is the anode current density level at the beginning of the current tail. V_S is the switching voltage, D_n is the diffusion constant of electrons. N_{AA} and L_{nP+} is the doping concentration and the diffusion length of electrons in the P+ region at the anode side of the GTO thyristor.

The simulated SiC GTO thyristor performance for Huang and Baliga modeling approach are presented in Fig. 7. The same operating conditions apply as for SiC IGBT model. The

Fig. 7. Simulated SiC GTO thyristor conduction power loss density and switching power loss density.

Fig. 8. The SiC GTO thyristor turn-on and turn-off switching energy loss and average (α_{AVG}) and maximum current gain (α_{MAX}) factors are studied to explain the decreasing trend of the total switching energy loss.

Mixed model conduction loss modeling approach shows slightly higher conduction losses than compared to the original Huang model. The switching power loss shows on the other hand different trends for increasing blocking voltages. The Baliga model predicts a positive total power loss trend whereas the Huang model predicts a decreasing loss trend. Therefore, the Huang switching characteristics are studied in more detail in Fig. 8. Here, the turn-on losses are increasing with blocking voltage and the turn-off losses, which is a main part of the total losses, shows a decreasing trend. The turn-off loss trend is determined by the average and maximum current gain, α_{AVG} and α_{MAX} [13], which is also presented in Fig. 8. Both α_{AVG} and α_{MAX} decreases for increasing V_B . For low values of τ_a , the first part of the E_{OFF} equation is dominant where the α_{AVG} contributes to decreasing turn-off energy loss. For higher ambipolar carrier lifetimes, the second part of the equation is more dominant and therefore the turn-off energy losses increases with blocking voltage.

III. PARAMETRIC SENSITIVITY ANALYSIS

In order to compare the performance of the SiC MOSFETs, SiC IGBTs and SiC GTO thyristors, the devices are simulated with the same operational conditions for each device type, $J=15 \text{ A/cm}^2$, $T=300 \text{ K}$, $\tau_a=10 \text{ } \mu\text{s}$ and $f=150 \text{ Hz}$. For simplicity, the modeling approach which resulted in the highest loss figures were chosen for comparison, e.g. $P_{COND,H}$ and P_{SW} for SiC MOSFET, $P_{COND,B}$ and $P_{SW,N}$ for SiC IGBT and $P_{COND,Mixed}$ and $P_{SW,B}$ for SiC GTO thyristor. The maximum current

Fig. 9. Maximum current density allowed for a power dissipation limit of $P_{D,MAX}=300 \text{ W/cm}^2$.

Fig. 10. Maximum switching frequency allowed for a power dissipation limit of $P_{D,MAX}=300 \text{ W/cm}^2$.

density and switching frequency allowed at a certain maximum power dissipation limit, e.g. $P_{D,MAX}=300 \text{ W/cm}^2$, is derived and presented in Fig. 9 and Fig. 10. The maximum allowed current density is derived under given conditions of $T=300 \text{ K}$, $\tau_a=10 \text{ } \mu\text{s}$ and $f=150 \text{ Hz}$ and estimates that SiC MOSFET is the most current handling capable device up to approximately 15 kV, whereas the SiC IGBT is more suitable up to about 35 kV and the SiC GTO thyristor up to about 50 kV. Furthermore, it is evident that the SiC MOSFETs is capable to operate at switching frequencies significantly higher than that of SiC IGBTs and SiC GTO thyristors.

Since the study is performed to predict the performance of ultra-high voltage SiC based devices that are not available today, there is a large uncertainty of the modeling parameters and therefore a parametric sensitivity study has been performed. The ambipolar carrier lifetime is one key parameter which enables conductivity modulation and thereby reduces conduction loss but on the other hand increases the switching times and thereby the switching losses. The total power loss density trends are for different current densities, temperatures and ambipolar carrier lifetimes are presented in Fig. 11, Fig. 12 and Fig. 13 respectively. Here, the SiC MOSFET shows strong increase of total power loss density, dominated by the conduction losses for increasing temperature and current density. For increasing temperature, the SiC GTO thyristor shows most increase of total power loss density for lower blocking voltages, ranging 10 kV to 40 kV, while the SiC IGBT shows an increase for higher blocking voltages. For

Fig. 11. Total power loss density of SiC MOSFET, SiC IGBT and SiC GTO thyristor for different current density levels, at room temperature.

Fig. 12. Total power loss density of SiC MOSFET, SiC IGBT and SiC GTO thyristor for different current density levels, at $T=425$ K.

Fig. 13. Total power loss density of SiC IGBT and SiC GTO thyristor for different ambipolar carrier lifetimes, at room temperature.

increasing current densities, the SiC GTO thyristor appears to have a stronger increase of power loss density than for SiC IGBTs. For low ambipolar carrier lifetimes, $\tau_a=5 \mu s$, the SiC GTO thyristor exhibits large conduction losses for $V_B>40$ kV. As the ambipolar carrier lifetime increases, e.g. $\tau_a=20 \mu s$, the conduction losses of the SiC GTO thyristor is decreased which could be noticed by the reduction of total power loss for high blocking voltages, 40-50 kV range. At the same time, the switching energy losses are increased, which is noticeable for SiC GTO thyristors in the range of 10-30 kV.

IV. CONCLUSIONS

In this paper, a set of analytical and empirical equations has been used to predict the performance of ultra-high voltage SiC MOSFETs, SiC IGBTs and SiC GTO thyristors. Different modeling approaches have been implemented, compared and discussed in order to predict the conduction power losses and switching power losses for theoretical SiC devices with blocking voltages ranging from 10 kV to 50 kV. The simulation results indicate that the SiC MOSFET has the largest current handling capability up to 15 kV, whereas the SiC IGBT is more suitable for blocking voltages in the range of 15 to 35 kV and the SiC GTO thyristor is more capable for voltages above 35 kV. Furthermore, the simulation results provide valuable information for future prediction of the potential of ultra-high voltage devices and hence facilitate the design of power converters. Numerical TCAD simulations will now be performed to validate the predicted device performance which is the object of our future research.

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