Potential of Ultra-High Voltage Silicon Carbide Semiconductor Devices

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Abstract—In this paper, the theoretical performance of ultra-high voltage Silicon Carbide (SiC) based devices are investigated. The SiC semiconductor device conduction power loss and switching power loss are predicted and compared with different modeling approaches, for SiC metal-oxide semiconductor field-effect transistors (MOSFETs) up to 20 kV and SiC gate turn-off (GTO) thyristors and SiC insulated-gate bipolar transistors (IGBTs) up to 50 kV. A parameter sensitivity analysis has been performed to observe the device power loss under various operating conditions, for instance current density, temperature and charge carrier lifetime. Also, the maximum allowed current density and maximum switching frequency for a maximum chip power dissipation limit of 300 W/cm² are investigated. The simulation results indicate that the SiC MOSFET has the highest current capability up to approximately 15 kV, while the SiC IGBT is suitable in the range of 15 kV to 35 kV, and thereafter the SiC GTO thyristor supersedes the loss performance from 35 kV to 50 kV.

Keywords—Silicon Carbide; 4H-SiC; Ultra-High Voltage Device; SiC MOSFET; SiC GTO thyristor; SiC IGBT

I. INTRODUCTION

Efficient electrical energy transmission across long distances is enabled by high power electronic technologies such as high-voltage direct transmission (HVDC) and flexible ac transmission systems (FACTS). Traditionally, silicon (Si) based thyristors have been used for current controlled HVDC. Similarly, Si insulated-gate bipolar transistors (IGBTs) have been the main choice for voltage-source converter based HVDC [1]. The introduction of MMC topologies had a significant impact on several power electronic applications, mainly due to the reduction of converter losses in comparison to two or three level VSC [1]. SiC based semiconductor devices are now acknowledged to offer better efficiency performance, along with reduction in the overall system cost over a wide span of power electronics applications, compared to leading horse Si counterparts, thanks to the superior physical properties of the SiC material in comparison to Si [2]. Furthermore, this material enables converter designs with relaxed cooling system requirements and smaller passive components. This facilitates more compact designs and thereby higher power densities. The main advantage of SiC based semiconductor devices is the strong electric breakdown field strength, about 10 times higher than that of Si, which enables

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are presented in the scientific literature for predicting SiC device performance with blocking voltages exceeding 30 kV.

This work aims to predict the performance of ultra-high blocking voltage SiC based semiconductor devices. The objective is to further extend the Huang [13] and Nawaz [14] models towards higher blocking voltages, for instance SiC MOSFETs up to 20 kV and SiC GTO thyristors and SiC IGBTs up to 50 kV. The two models are implemented and the simulation results are compared to the Baliga modeling approach [17]. In this model, both analytical equations and empirical equations have been used to predict the conduction power losses and switching power losses under various operating conditions. The effect of temperature and charge carrier lifetimes have been investigated as well as the maximum allowed current density and switching frequency for a given maximum power dissipation level.

II. MODEL DESCRIPTION

A. General Modeling Approach

The modeling approaches implemented in this study are fully represented in [13-14, 17]. This section presents a specific part of the models for further discussion. Note that the implemented model is based on the assumption that the circuit oriented impact such as gate drivability, gate resistance and stray inductance on the switching characteristics is negligible for the intended device.

The general modeling approach is based on the use of conduction loss and switching loss to extract the total power loss (1) and by that determine the maximum allowed current density and switching frequency (2) for a given maximum power dissipation limit, e.g. \( P_{\text{D,MAX}} = 300 \text{ W/cm}^2 \):

\[
P_{\text{TOT}} = DP_{\text{COND}} + f(E_{\text{ON}} + E_{\text{OFF}})
\]

\[
f_{\text{MAX}} = \frac{P_{\text{D,MAX}} - DP_{\text{COND}}}{E_{\text{ON}} + E_{\text{OFF}}}
\]

here \( D \) is the duty cycle and \( f \) is the frequency. The SiC MOSFET, SiC GTO thyristor and SiC IGBT conduction loss and switching loss are expressed in terms of blocking voltage, \( V_b \), which is related to the drift region doping concentration, \( N_D \), and drift region thickness, \( W_D \) [14]. Further, the critical electrical field strength, \( E_C \), is derived according to [14]. Temperature, \( T \), current density, \( J \), and initial carrier lifetimes, \( \tau_{\text{off}}, \tau_{\text{off}} \), are variables in the model. A relation of \( \tau_{\text{off}} = 10 \tau_{\text{on}} \) is assumed in the model. The carrier lifetimes are modeled according to the Scharfetter relation with power-law temperature dependence [18] and the carrier mobilities are modeled according to the Arora model [19]. The SiC bandgap properties and intrinsic carrier concentration, \( n_i \), is derived according to [20]. The modeling parameters used in the model are presented in Table 1. The theoretical blocking voltage as a function of drift layer doping concentration is presented in Fig 1. The particular drift region doping concentration and drift region width for the theoretical devices used in this model are presented in Fig 2.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter name</th>
<th>Value and Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>Duty cycle</td>
<td>0.5</td>
</tr>
<tr>
<td>A</td>
<td>Active device area</td>
<td>1 cm²</td>
</tr>
<tr>
<td>( \varepsilon )</td>
<td>SiC permittivity</td>
<td>10.1</td>
</tr>
<tr>
<td>( \varepsilon _{\text{SiO2}} )</td>
<td>SiO₂ permittivity</td>
<td>3.9</td>
</tr>
<tr>
<td>( V_{\text{sat}} )</td>
<td>Saturation velocity holes</td>
<td>2×10⁶ cm/s</td>
</tr>
<tr>
<td>( V_{\text{GH}} )</td>
<td>MOSFET high gate voltage</td>
<td>20 V</td>
</tr>
<tr>
<td>( V_{\text{GL}} )</td>
<td>MOSFET low gate voltage</td>
<td>-5 V</td>
</tr>
<tr>
<td>( N_{\text{GTO}} )</td>
<td>GTO thyristor anode doping concentration</td>
<td>5×10¹⁹ cm⁻³</td>
</tr>
<tr>
<td>( N_{\text{IGBT}} )</td>
<td>IGBT emitter doping concentration</td>
<td>5×10¹⁹ cm⁻³</td>
</tr>
<tr>
<td>( W_o )</td>
<td>IGBT Emitter diffusion length</td>
<td>3.3×10⁻⁶ cm</td>
</tr>
<tr>
<td>( t_{\text{ox}} )</td>
<td>Oxide layer thickness</td>
<td>5×10⁻⁶ cm</td>
</tr>
<tr>
<td>( g_m )</td>
<td>IGBT transconductance</td>
<td>0.3 S</td>
</tr>
<tr>
<td>( V_{\text{GG}} )</td>
<td>GTO gate voltage</td>
<td>20 V</td>
</tr>
<tr>
<td>( V_{\text{TH}} )</td>
<td>IGBT threshold voltage</td>
<td>4.36 V</td>
</tr>
<tr>
<td>( p )</td>
<td>Cell pitch</td>
<td>2×10⁻² cm</td>
</tr>
<tr>
<td>( L_{\text{ch}} )</td>
<td>Channel length</td>
<td>1×10⁻⁴ cm</td>
</tr>
<tr>
<td>( \mu_n )</td>
<td>Channel mobility</td>
<td>20 cm²/Vs</td>
</tr>
</tbody>
</table>

![Fig. 1. Blocking voltage as a function of drift region doping concentration and drift region width.](image1)

![Fig. 2. Estimated drift region doping concentration and drift region width for the theoretical devices investigated in this model.](image2)

B. SiC MOSFET Model

The SiC MOSFET on-state characteristics are mainly given by the sum of resistive elements inherently in the device, for instance the MOS-channel resistance, drift region resistance and substrate resistance. The resistance contribution raised from the drift region is significantly larger than the other contributing resistances (e.g., channel resistance, contact resistance) for SiC MOSFET devices with blocking voltage...
The specific on-state resistance of two modeling approaches, analytically [13] and empirically [14], are implemented in the model. The empirically extracted on-state resistance is based on extracted values of 10 kV and 15 kV SiC MOSFET [22]. The SiC MOSFET switching characteristics are mainly governed by charging and discharging of the gate-source and gate-drain capacitances, in an ideal case. The ideal SiC MOSFET characteristics are derived according to [13, 14] which depends on the switching voltage, $V_{DS}$, peak transconductance, $g_m$, threshold voltage, $V_{TH}$, and gate drive upper and lower voltage, $V_{GH}$, $V_{GL}$. The switching voltage is assumed to 60% of the blocking voltage (i.e., $V_{TH}=0.6V_{B}$).

The simulated SiC MOSFET performance for Huang and Nawaz modeling approach are presented in Fig. 4. The conduction power loss density are estimated to 30 W/cm$^2$ to 60 W/cm$^2$ in the range of 10 kV to 20 kV, under the given conditions of $J=15$ A/cm$^2$ and $T=300$ K. The main difference between the two models, besides the analytical and empirical approach, is that the change in $E_C$ is accounted by a cubic relation for the $R_{DS(on)}$ in the analytical model [13], in contrast to the empirical model where the $E_C$ is only accounted through the blocking voltage. The switching losses for the ideal SiC MOSFET contributes insignificantly to the total power losses at the switching frequency of f=150 Hz.

### C. SiC IGBT Model

The conduction losses of bipolar SiC devices are composed of two parts. The first part is the knee-voltage, $V_{Knee}$ which is close to the built-in potential/bandgap energy of SiC material and the second part is related to the inherent resistive elements in the device, similar to $R_{DS(on)}$. The prediction of SiC IGBT conduction power loss density is based on extrapolation of the experimental values, similar as in [14]. The characteristics of high voltage state-of-the-art research-level SiC IGBT are used for extraction of $V_{Knee}$ and $R_{DS(on)}$ parameters, as shown in Fig. 5 [8 - 12]. The analytical conduction power loss density modeling approach by Baliga is implemented for comparison [17]. Here, the SiC IGBT forward voltage drop is modeled as

$$V_{F,IGBT} = V_{Knee} + \frac{pLCHJ}{\mu_n C_{Ox}(V_G - V_{TH})}$$  

(3)

where, the $LCH$ is the MOS-channel length, $\mu_n$ is the channel mobility and $p$ is the cell pitch. $V_G$ is the gate voltage and $C_{Ox}$ is the oxide capacitance, determined from the oxide thickness, $C_{Ox,0}=3.5 \times 10^{-12} F/cm^2$. $T$ is the temperature, $q$ is the elementary charge ($1.602 \times 10^{-19}$ C) and $k$ is the Boltzmann’s constant ($8.617 \times 10^{-5}$ eV/K). $W$ is the drift region width, $D_n$ and $L_o$ is the ambipolar diffusion constant and length [17] and the function $F(W/2L_o)$ is determined according to (5-6), [17].
here. Also, the Baliga IGBT turn-off energy loss is implemented for comparison [17] as follows

\[ E_{OFF} = JV_{CS} \left( t_v + \frac{\tau_{HL,N-Base}}{2} \right) \]  

\[ t_v = \frac{\varepsilon_0 \varepsilon_{SC} p_0 V_{CS}}{W (N_D + p_{SC})} f \]  

\[ p_{SC} = \frac{J}{q v_{sat,p}} \]  

where, \( V_{CS} \) is the IGBT switching voltage, \( t_v \) is the voltage rise time during turn-off, \( \tau_{HL,N-Base} \) is the high level carrier lifetime in the collector layer and \( p_0 \) is the plasma density at the collector end of the IGBT device, which is assumed equal as for the Nawaz model, \( p_n = p_0 \) [14]. \( v_{sat,p} \) is the hole saturation velocity.

The simulated SiC IGBT performance for Nawaz and Baliga modelling approach are presented in Fig. 6. The predicted conduction loss ranging from approximately 25 W/cm² to 90 W/cm² for the blocking voltage range of 10 kV to 50 kV, under the given conditions of \( J=15 \) A/cm², \( T=300 \) K and \( \tau_{n0}=17 \) µs, which results in the ambipolar carrier lifetime of \( \tau_n=10 \) µs. The main difference between the two modeling approaches, in the range of 10 kV to 20 kV, is due to the differences in knee voltage, \( V_{KNEE}=3.9 \) V versus \( V_{KNEE}=3.4 \) V. In literature, Mizushima et al., has presented a 16 kV IEGT with knee voltage characteristics of about 3.4 V [10]. In practice, the knee voltage is mainly determined by the SiC material quality, manufacturing process and the level of conductivity modulation in the drift region which ideally should approach the bandgap energy, \( E_{G,SC}=3.26 \) V, for all voltage classes [7, 9-11]. The switching energy loss at \( f=150 \) Hz, of the SiC IGBT increases rapidly with increasing \( V_B \) and is a significant part of the total SiC IGBT losses.

D. SiC GTO Thyristor Model

The SiC GTO thyristor conduction loss follows the same modeling approach as for the SiC IGBT. The conduction losses as determined as (10) in the Huang model [13]. In order to compare the performance of the SiC IGBT and SiC GTO fairly, the same knee voltage model (4-6) is adopted to (10), denoted as “Mixed model”. The Huang SiC GTO thyristor conduction loss is determined as

\[ P_{COND} = J A E_B \frac{3 \pi k T}{8} q \exp \left( \frac{3 W_B}{2 L_a E_C} \right) \]  

here, \( E_B \) is the bandgap energy of SiC and \( A \) is the device area. The SiC GTO thyristor turn-on and turn-off switching energy losses derived according to [13]. The Baliga SiC GTO turn-off loss modeling approach is added as reference. Similar to SiC IGBT, the losses are composed of losses during voltage rise time and the tail current. The \( W_P \) region thickness is assumed to 50 % of the \( W_N \) region thickness, similar as in [13]. The turn-on energy loss is derived as in [13].
Mixed model conduction loss modeling approach shows slightly higher conduction losses than compared to the original Huang model. The switching power loss shows on the other hand different trends for increasing blocking voltages. The Baliga model predicts a positive total power loss trend whereas the Huang model predicts a decreasing loss trend. Therefore, the Baliga model is more suitable for devices with decreasing blocking voltage. The ambipolar carrier lifetime is one key parameter which enables conductivity modulation and thereby reduces conduction loss but on the other hand increases the switching times and thereby the switching losses. The total power loss density trends are for different current densities, temperatures and ambipolar carrier lifetimes are presented in Fig. 11, Fig. 12 and Fig. 13 respectively. Here, the SiC MOSFET shows strong increase of total power loss density, dominated by the conduction losses for increasing temperature and current density. For increasing temperature, the SiC GTO thyristor up to about 50 kV. Furthermore, it is evident that the SiC MOSFETs is capable to operate at switching frequencies significantly higher than that of SiC IGBTs and SiC GTO thyristors.

Since the study is performed to predict the performance of ultra-high voltage SiC based devices that are not available today, there is a large uncertainty of the modeling parameters and therefore a parametric sensitivity study has been performed. The ambipolar carrier lifetime is one key parameter which enables conductivity modulation and thereby reduces conduction loss but on the other hand increases the switching times and thereby the switching losses. The total power loss density trends are for different current densities, temperatures and ambipolar carrier lifetimes are presented in Fig. 11, Fig. 12 and Fig. 13 respectively. Here, the SiC MOSFET shows strong increase of total power loss density, dominated by the conduction losses for increasing temperature and current density. For increasing temperature, the SiC GTO thyristor shows most increase of total power loss density for lower blocking voltages, ranging 10 kV to 40 kV, whereas the SiC IGBT is more suitable up to about 35 kV and the SiC GTO thyristor up to about 50 kV. Furthermore, it is evident that the SiC MOSFETs is capable to operate at switching frequencies significantly higher than that of SiC IGBTs and SiC GTO thyristors.

III. PARAMETRIC SENSITIVITY ANALYSIS

In order to compare the performance of the SiC MOSFETs, SiC IGBTs and SiC GTO thyristors, the devices are simulated with the same operational conditions for each device type, J=15 A/cm², T=300 K, τa=10 µs and f=150 Hz. For simplicity, the modeling approach which resulted in the highest loss figures were chosen for comparison, e.g. PCOND,H and PSW for SiC MOSFET, PCONDB and PSWN for SiC IGBT and PCONDMixed and PSWB for SiC GTO thyristor. The maximum current density and switching frequency allowed at a certain maximum power dissipation limit, e.g. Pd_MAX=300 W/cm², is derived and presented in Fig. 9 and Fig. 10. The maximum allowed current density is derived under given conditions of T=300 K, τa=10 µs and f=150 Hz and estimates that SiC MOSFET is the most current handling capable device up to approximately 15 kV, whereas the SiC IGBT is more suitable up to about 35 kV and the SiC GTO thyristor up to about 50 kV. Furthermore, it is evident that the SiC MOSFETs is capable to operate at switching frequencies significantly higher than that of SiC IGBTs and SiC GTO thyristors.
IGBTs. For low ambipolar carrier lifetimes, the SiC MOSFETs, SiC IGBTs and SiC GTO thyristors in the range of 10-30 kV. As the ambipolar carrier lifetime increases, e.g. \( \tau_a = 5 \mu s \), the SiC GTO thyristor exhibits large conduction losses for \( V_B > 40 \text{kV} \). The simulation results indicate that the SiC MOSFET has the largest current handling capability up to 15 kV, whereas the SiC IGBT is more suitable for blocking voltages in the range of 15 to 35 kV and the SiC GTO thyristor is more capable for voltages above 35 kV. Furthermore, the simulation results provide valuable information for future prediction of the potential of ultra-high voltage devices and hence facilitate the design of power converters. Numerical TCAD simulations will now be performed to validate the predicted device performance which is the object of our future research.

**Fig. 11.** Total power loss density of SiC MOSFET, SiC IGBT and SiC GTO thyristor for different current density levels, at room temperature.

**Fig. 12.** Total power loss density of SiC MOSFET, SiC IGBT and SiC GTO thyristor for different current density levels, at \( T = 425 \text{K} \).

**Fig. 13.** Total power loss density of SiC IGBT and SiC GTO thyristor for different ambipolar carrier lifetimes, at room temperature.

Increasing current densities, the SiC GTO thyristor appears to have a stronger increase of power loss density than for SiC IGBTs. For low ambipolar carrier lifetimes, \( \tau_a = 5 \mu s \), the SiC GTO thyristor exhibits large conduction losses for \( V_B > 40 \text{kV} \). As the ambipolar carrier lifetime increases, e.g. \( \tau_a = 20 \mu s \), the conduction losses of the SiC GTO thyristor is decreased which could be noticed by the reduction of total power loss for high blocking voltages, 40-50 kV range. At the same time, the switching energy losses are increased, which is noticeable for SiC GTO thyristors in the range of 10-30 kV.

### IV. CONCLUSIONS

In this paper, a set of analytical and empirical equations has been used to predict the performance of ultra-high voltage SiC MOSFETs, SiC IGBTs and SiC GTO thyristors. Different modeling approaches have been implemented, compared and discussed in order to predict the conduction power losses and switching power losses for theoretical SiC devices with blocking voltages ranging from 10 kV to 50 kV. The simulation results indicate that the SiC MOSFET has the largest current handling capability up to 15 kV, whereas the SiC IGBT is more suitable for blocking voltages ranging from 10 kV to 50 kV. Furthermore, the simulation results provide valuable information for future prediction of the potential of ultra-high voltage devices and hence facilitate the design of power converters. Numerical TCAD simulations will now be performed to validate the predicted device performance which is the object of our future research.

### REFERENCES