Towards Monolithic 3D Integration: A Design Flow

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Abstract

Monolithic 3D (M3D) integration is considered as a key enabling technology for the continuation of Moore's Law. To facilitate the study of M3D circuits, a design flow is clearly needed. In this work we discuss the potentials and challenges of this technology and present a design flow for M3D circuits which includes a M3D Process Design Kit (PDK) with parametric extraction capabilities.

Keywords: monolithic (sequential) 3D integration, design flow.

Introduction and Motivation of Work

3D integration technologies show a great potential for increasing the integration density of future ICs. Arguably, the most popular 3D integration technology is Parallel 3D (P3D) which has drawn a lot of attention recently. In P3D integration two wafers can be fabricated separately and then stacked together using Through-Silicon-Vias (TSVs) and micro Bumps. The large size of TSVs, a consequence of the poor alignment between stacked wafers, is the biggest bottleneck of this technology as it can induce a lot of parasitics in a design. On the other hand, in M3D integration, tiers of transistors are sequentially processed on top of other devices. Devices in adjacent tiers can be connected through Monolithic Inter-layer Vias (MIVs) with dimensions similar to the inter-metal vias. Hence, M3D integration can offer fine-grained 3D interconnections, even at transistor level. Until now, two M3D design techniques have been proposed: (1) placing nmos and pmos transistors on different tiers and (2) stacking digital cells [1]. Both of these techniques apply only to digital designs considering a more abstract view of the digital cells. Furthermore, none of them takes into account the inter-tier interconnection parasitics, or the fact that the top tier devices resemble SOIs and not conventional bulk MOSFETs. To deal with this problem and facilitate the detailed analysis of M3D topologies, we propose a design flow that takes into account the unique features of this technology.

Results

To demonstrate our design flow, we have developed a M3D virtual process. The structure of a commercial 150nm process is used as the bottom tier. On top of that we envision a thin Si film where the top tier transistors will be fabricated. Relevant technology parameters have been defined with the collaboration of the electronic devices research group in our department. The latter are characterized through CEA-LETI's UTSOI2.1 model [2], [3]. The effectiveness of these models when it comes to our virtual process is validated though comparisons with TCAD simulations as shown in Fig. 1. As far as the bottom tier MOSFETs are concerned, the native models of the commercial process are employed. Since the interconnection parasitics are of major importance in 3DICs, we have also generated a parasitic extraction flow based on the Cadence QRC toolset. The biggest challenge that we faced lies in QRC Techgen's inability to recognize more than one diffusion layers. To this end, we have modeled the top Si film as a conductor with high sheet resistance. If the thin Si film was modeled as a dielectric instead, Techgen would be unable to account for the top contacts' parasitics (from the top Si to the top

metal 1). As explained in [1], tungsten is preferred over copper for the bottom tier interconnects as it can withstand higher temperatures during the processing of the top tier. To reflect tungsten's higher resistivity, the sheet resistance of the bottom tier metals is set three times larger than the top tier ones. To validate the proposed design flow, a M3D inverter has been designed (schematic entry and layout) and simulated. The 3D view of the layout is presented in Fig. 2. The nmos transistor is placed on top and the pmos in the bottom. The simulation results, which are shown in Fig. 3 and include RC parasitic extraction, suggest that the MIVs parasitics have an insignificant impact on the operation of the inverter even though the signals have to transverse through 6 metal layers.

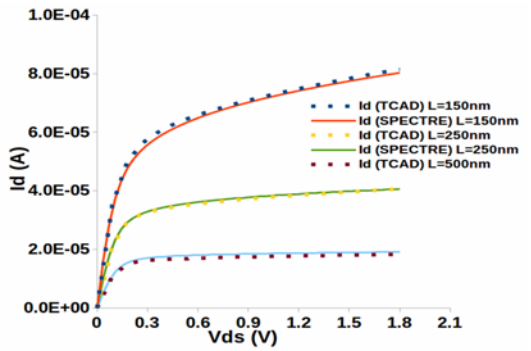

Fig. 1: Comparison between UTSOI2.1 model for the top FETs and TCAD simulations

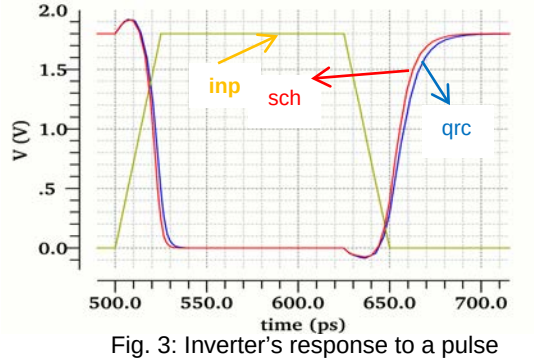

Fig. 3: Inverter's response to a pulse before and after parasitic extraction

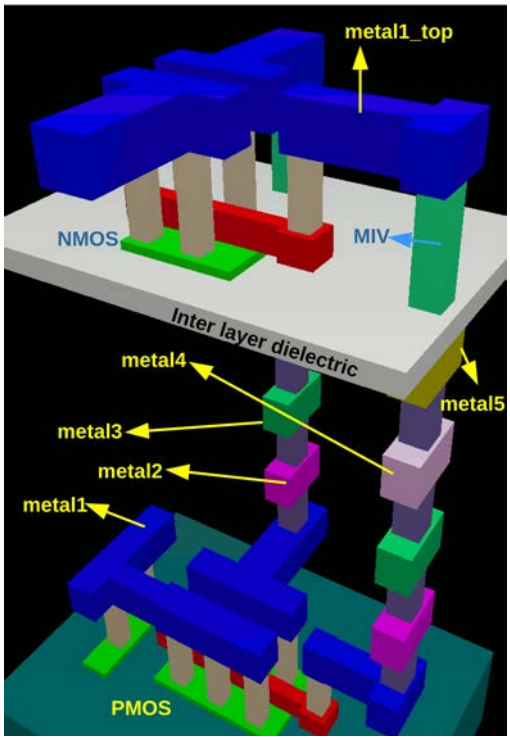

Fig. 2: M3D integration of a CMOS inverter

Conclusions

The presented M3D design flow can be used to explore novel M3D circuits and estimate their performance without the soaring costs of fabrication. Additionally, it can facilitate the investigation and design of complex circuits.

Acknowledgements

This work was supported by the Swedish Foundation for Strategic Research.

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