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Wafer-Level Vacuum Packaging Enabled by Plastic Deformation and Low-Temperature Welding of Copper Sealing Rings with a Small Footprint

Xiaojing Wang, Simon J. Bleiker, Mikael Antelius, Göran Stemme, *Fellow, IEEE*, and Frank Niklaus, *Senior Member, IEEE*

Abstract—Wafer-level vacuum packaging is vital in the fabrication of many MEMS devices and enables significant cost reduction in high-volume MEMS production. In this paper, we propose a low-temperature wafer-level vacuum packaging method based on plastic deformation and low-temperature welding of copper sealing rings with a small footprint. A device wafer with copper ring structures and a cap wafer with corresponding metalized grooves are placed inside a vacuum chamber and pressed together at a temperature of 250 °C, resulting in low-temperature welding of the copper and thus, hermetic sealing of the cavities enclosed by the sealing rings. The vacuum pressure inside the fabricated cavities 146 days after bonding was measured using residual gas analysis (RGA) to be as low as 2.6×10^{-2} mbar. Based on this value, the leak rate is calculated to be smaller than 3.6×10^{-16} mbarL/s using the most conservative assumptions, demonstrating the excellent hermeticity of the seals. Shear testing was used to demonstrate that the seals are mechanically stable with over 90 MPa in shear strength for 5.2 μm -high Cu sealing rings with widths down to 8 μm . The reported method is potentially compatible with CMOS substrates and may be applied to vacuum packaging of 3D heterogeneously integrated MEMS on state-of-the-art CMOS substrates.

Index Terms—vacuum, packaging, MEMS, sealing, copper, hermetic, 3D integration, small footprint, cold welding.

I. INTRODUCTION

VACUUM packaging is crucial for the functionality of a wide variety of MEMS devices such as inertial sensors, resonators, and infrared detectors [1]. Cost considerations for high-volume MEMS production make wafer-level vacuum packaging an advantageous choice compared to component-level packaging [1], [2]. Bonding techniques for wafer-level hermetic sealing of cavities can be categorized into direct bonding, anodic bonding, and intermediate layer bonding [3]. Direct bonding techniques are either conducted at high temperatures [4], making them unsuitable for CMOS substrates, or demanding on surface roughness and preparation of the substrates [5]. For intermediate layer bonding, polymers, glasses,

and metals are used. However, polymers are typically not fully hermetic due to their high permeability to gases and moisture [5], [6]. Glass-based methods, including glass frit bonding and anodic bonding, typically consume comparably large areas for the sealing rings since the sealing structures have to be at least several hundreds of micrometers wide to ensure high bond strength and sufficient hermeticity [7]–[10]. As alternatives, metals have drawn extensive attention as intermediate bonding layers because they provide excellent hermeticity and mechanical strength, while enabling size reduction in the sealing ring area by nearly a hundredfold [7], thus facilitating significant reduction in die size.

Various metal-based wafer-level hermetic packaging methods have been proposed, including solder bonding [11]–[14], eutectic bonding [15]–[18], solid-liquid inter-diffusion (SLID) bonding [13], [19], [20], surface activated bonding (SAB) [21], and thermo-compression bonding [22]–[27]. All these technologies have individual advantages and disadvantages. Drawbacks of solder bonding and eutectic bonding are that the melting of solder metals and alloys can cause reflow problems, and to ensure sufficient hermeticity and bond strength, the sealing ring widths typically are more than 100 μm [13], [14], [16], [18]. For SLID bonding, voids can occur in the intermetallic compound layer, and special care has to be taken in designing the sealing layer thickness and in controlling the temperature ramping during bonding to get uniform and strong bonds [19], [20], [28]. Surface activated bonding enables room temperature sealing [21], [29], but the requirements on surface planarity and surface roughness of the substrates are very high [21], [30]. Thermo-compression bonding typically employs high temperatures of 300 – 450 °C [22]–[27], [31] and high bonding pressures, and has been demonstrated with metals such as gold (Au) [22]–[24], aluminum (Al) [25], [26], and copper (Cu) [27], [31]. However, low bonding temperatures during vacuum packaging are desired to avoid thermally induced damages of MEMS devices and CMOS circuits. To lower the temperature threshold, several low-temperature wafer-level sealing techniques have been investigated using e.g. Al [32], indium (In) [33], Au [34]–[39], and Cu [40], [41] as bonding layers. Localized heating was applied to seal MEMS cavities using Al at room temperature but micro-heaters have to be incorporated in the fabrication of the package [32], thereby significantly increasing process

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X. Wang, S. J. Bleiker, G. Stemme, and F. Niklaus are with the Department of Micro and Nanosystems, KTH Royal Institute of Technology, 100 44, Stockholm, Sweden (e-mail: xiawang@kth.se; bleiker@kth.se; stemme@kth.se; frank.niklaus@ee.kth.se).

M. Antelius is with APR Technologies AB, 745 39, Enköping, Sweden (e-mail: antelius@kth.se).

complexity. Low-temperature hermetic thermo-compression bonding has been investigated using In and Au. However, the reported sealing rings feature relatively large widths, ranging from 60 μm to 200 μm [33], [34], [39], and bonding layers with granular materials [35] or smoothed surfaces [39] have to be prepared by specialized processes. The high ductility of Au enables vacuum sealing based on cold welding of the Au sealing structures [36]–[38]. However, the proposed sealing techniques either rely on reinforcement of the bond strength by additional materials such as epoxy underfill [36], or solder patches [37], or the process is based on wafer bonding in combination with sealing of vent-holes by plastic deformation of Au plugs [38].

Compared to the abovementioned materials, Cu is being increasingly used for metal interconnect layers in state-of-the-art CMOS circuits and for the electrical vias in advanced 3D integrated circuit (IC) technologies [42]. Thus, Cu is a preferred bonding and sealing material for low-temperature vacuum packaging of next generation microsystems as it is compatible with state-of-the-art CMOS circuits and 3D IC fabrication. Furthermore, the excellent mechanical strength of Cu makes it potentially suitable for realizing very narrow sealing rings, resulting in small package sizes. Cu thermo-compression bonding has been reported to achieve wafer-level vacuum sealing at low temperatures [40], [41], but very flat and clean Cu surfaces [40] or additional capping layers [41] have to be prepared in these methods, and the total bonding areas are still relatively large. In another study, ultrasonic Cu bonding was used to seal MEMS cavities at room temperature [43]. However, this method was demonstrated only on die-level and the mechanical and hermetic reliability of the bonding has not been verified.

Here, we present a wafer-level vacuum packaging method based on low-temperature welding of Cu. In this process, a device wafer with Cu rings is pressed together with a cap wafer containing corresponding grooves at a temperature of 250 $^{\circ}\text{C}$. Thereby, the Cu sealing rings are wedged into the grooves and plastically deformed, inducing sealing of the enclosed cavities. The low-temperature welding is based on large-scale plastic deformation of Cu at the bonding interface, thus making this method insensitive to surface roughness. A similar approach has been proposed earlier where protruding Au rings on both wafers were used for cavity sealing [36]. However, this caused considerable problems of breakage of the outer rings due to resulting shear stresses. The strategy in this work differs from previous work in that we have grooves in the cap wafer, hence avoiding the problem of shearing off any of the sealing rings. Furthermore, in our new approach we demonstrate vacuum sealing with Cu sealing rings that are narrower and shorter than the Au rings in [36], thus significantly reducing the sealing ring footprint and process complexity. In this paper, we present the design and the process to realize vacuum cavities using Cu sealing rings. The hermeticity and mechanical strength of the sealed cavities are evaluated. The influence of design variations of the sealing ring structures on the resulting bonding yields is investigated.

Fig. 1. Schematic drawing of our sealing approach. The close-up images indicate evaluated design variations of the sealing ring structures.

TABLE I
KEY DIMENSIONS OF DIFFERENT EVALUATED SEALING STRUCTURE DESIGNS.

Number of annular grooves	1 / 2 / 3
Overlap width of sealing rings	1 μm / 2 μm / 3 μm
Distance between grooves	1.5 μm / 3 μm
Dimension of Cu rings (w $\times$ h)	6 – 21 μm $\times$ 5 μm
Cavity size (l $\times$ w $\times$ h)	4015 μm $\times$ 4015 μm $\times$ 8 μm
Radius of the rounded corners	300 μm
Total number of design variations	15

II. CONCEPT AND FABRICATION

A. Design of metal sealing structures

The sealing concept is illustrated schematically in Fig. 1. The device wafer with the Cu sealing rings is aligned to the cap wafer with the corresponding annular grooves. Next, the wafers are pressed together at a temperature of 250 $^{\circ}\text{C}$. The Cu rings are slightly wider than the grooves and the resulting small overlapping areas of the rings and grooves experience very high localized pressures that exceed the yield strength of Cu (~ 233 MPa) [44] and thus, inducing plastic deformation of the Cu rings. The Cu rings are partially squeezed into the grooves covered by a thin layer of Cu (marked in green color in Fig. 1), resulting in low-temperature Cu-Cu welding and sealing of the enclosed cavities. Low-temperature welding is a solid-state diffusion bonding process, utilizing different mechanisms including plastic deformation, interface diffusion, surface diffusion, and grain boundary diffusion, among which plastic deformation is the dominant mechanism in the initial stage of the bonding [45]. The induced large-scale plastic deformation initiates the Cu-Cu bond formation and facilitates the other subsequent atomic diffusion procedures, which lowers the required bonding temperature to 250 $^{\circ}\text{C}$ or below, compared to conventional thermo-compression bonding (300 – 450 $^{\circ}\text{C}$) [46].

Different design variations of the sealing structures with dif-

Fig. 2. Cross-sectional view of the process flow of the vacuum sealing method. (a) Mold-defined electroplating of Cu rings on the device wafer. (b) Si DRIE of the grooves and cavities and Cu deposition on the cap wafer, followed by alignment of the two wafers. (c) Joining and bonding of the wafers inside a vacuum chamber at a temperature of 250 °C, resulting in sealing of the enclosed cavities. (d) Thinning of the cap wafer to form deflected diaphragms for leak rate testing.

ferent dimensions are incorporated on the same wafer (shown in the close-up drawings in Fig. 1) in order to investigate the bonding and sealing properties for different designs. The simplest case is with only one annular groove in the cap wafer. The major feature changes between the different designs are the overlap width at the edge of the Cu rings on the device wafer, the number of the annular grooves in the cap wafer, and the distance between the grooves. These design variations directly affect the available surface area for the Cu-Cu bond formation. In all cases, there is only one Cu sealing ring surrounding each cavity on the device wafer. The key design parameters and variations of all 15 different designs are listed in Table I. The definitions of the related parameters are shown in Fig. 1.

B. Wafer preparation and bonding process

The fabrication flow of the proposed wafer-level vacuum packaging method is shown in Fig. 2. For the experiments, a single-side polished 500 μm -thick, 100 mm-diameter silicon (Si) wafer with a 100 nm-thick layer of thermal oxide (SiO₂) on top was chosen as the device wafer. The SiO₂ layer insulates the Cu sealing rings from the underlying device substrate to avoid shorting of encapsulated devices. A 10nm/100nm-thick Ti/Cu adhesion/seed layer was deposited on the wafer

by sputtering. The Ti layer also acts as a barrier layer to prevent diffusion of Cu into the Si substrate. Then a 6 μm -high mold for defining the Cu sealing rings was patterned by lithography using AZ9260 photoresist. Thereafter, 5 μm -high Cu rings were electroplated (AAC Microtech AB) using a commercial setup. The thickness of the Cu sealing rings was measured using a profilometer to be $5.2 \mu\text{m} \pm 5\%$ across the whole wafer. Next, the Cu seed layer was removed by wet etching in a 1:10 diluted solution using (NH₄)₂S₂O₈ and 96% H₂SO₄ as etchants, followed by wet etching in 0.25% HF for Ti removal, which also simultaneously removed any thin oxide layer on the surface of electroplated Cu. After this, the wafer was rinsed in DI water and dried in a spin dryer. A cross-section of the resulting structure is depicted in Fig. 2a.

For the cap wafer, a double-side polished 300 μm -thick and 100 mm-diameter Si wafer was prepared as indicated in Fig. 2b. Both the annular grooves corresponding to the Cu rings and the enclosed central square cavities were formed by deep reactive ion etching (DRIE) to a depth of 8 μm in an ICP tool (STS Multiplex). An oxygen plasma treatment was then performed to remove organic residues. This was followed by sputter deposition of a 10 nm/300nm-thick Ti/Cu layer on the surfaces of the grooves for the subsequent Cu to Cu bonding and sealing. If necessary, e.g. for realizing sealed cavities with transparent cap wafers, the Ti/Cu layer can be patterned by an additional dry etching step such that the Ti/Cu layer remains only in the groove areas, thus forming transparent windows over the cavities.

After alignment of the two wafers in a prebond wafer aligner (Suss BA8) using backside alignment marks [5], the wafer stack was clamped together and moved to a wafer bonder (Suss CB8). For the bonding and sealing process, the pressure in the bonder chamber was pumped down to 7×10^{-5} mbar. After 20 minutes of additional pumping, a force of 1 kN was applied to the wafer stack to ensure the relative positions between the two wafers. Then, the wafer chucks pressing the wafers together were heated up to 250 °C with a temperature ramping rate of ~ 3 °C/min. Thereafter, the wafer stack was subject to a force of 20 kN with a force ramping time of 2 minutes from 1 kN to 20 kN. The force was kept constant at 20 kN for 25 minutes. This force corresponds to a local pressure of 550 MPa in the small Cu-Cu overlapping areas at the bonding interfaces, which is around 2.4 times the reported yield strength of electroplated Cu (~ 233 MPa) [44], implying a high probability of plastic deformation of the Cu rings. Thereafter, the wafer chucks were cooled down to 50 °C with a cooling rate of ~ 2 °C/min. Finally, the bonding force was removed and the chamber was vented to atmospheric pressure. In addition to experiments with the above bonding parameters, another bonding test was carried out at room temperature, while all other bonding conditions remained identical. In this experiment, the cap wafer adhered to the device wafer immediately after bonding but detached from the device wafer during subsequent wafer handling, indicating that the resulting Cu-Cu bond was very weak.

In order to evaluate the leak rate of the sealed cavities, the backside of the cap wafer was thinned down in the ICP by Si isotropic etching to create diaphragms over the square cavities,

Fig. 3. Visible diaphragm deflections in three different chips after dicing.

as shown in Fig. 2d. The thicknesses of the diaphragms were measured by cross-sectional optical microscope inspection of the individual cavity dies after dicing and values ranging from $75\ \mu\text{m}$ to $95\ \mu\text{m}$ were obtained across the wafer. This thickness variation was caused by the varying etch rates from the center to the edge of the wafer. The deflection of a diaphragm depends on the thickness of the diaphragm and the pressure difference of atmospheres inside and outside of the enclosed cavity [37]. This approach potentially offers a much lower detection limit for leak rate measurements compared with bubble leak test and helium fine leak test, although at the cost of a longer measurement period [47].

III. RESULTS AND DISCUSSION

A. Results of bonding experiments

After bonding and thinning of the cap wafer, 93 out of the 124 cavities were successfully sealed, which was concluded by observing the deflection of the diaphragms. After four months, all but one of the 93 diaphragms were still deflected, i.e. 92 cavities showed no gross leakage. The failure points of all the leaked cavities were in the Cu-Cu bond interfaces and no cracks or delamination due to thermal stresses was observed. The bonded wafers with the cavities were then diced using a standard dicing saw (*Disco DAD 320*). The visible deflections of the diaphragms of three different chips after dicing are displayed in Fig. 3. The yield of sealed cavities before and after dicing is summarized in Fig. 4. Due to the fact that the sealing ring designs with groove distances of $1.5\ \mu\text{m}$ and $3\ \mu\text{m}$ exhibited almost no difference in surviving the dicing procedure, they are all considered as one type of sealing ring design when calculating the yield values. The original 15 design variations can then be classified as 9 major types, featuring different overlap width (O) at the edge of the Cu rings, and number of grooves (G) in the cap wafer as listed in Fig. 4. For each of the 1-groove designs, 8 samples were evaluated. For all the other designs, either 16 or 20 samples each were evaluated.

It is clear to see in Fig. 4 that after bonding, none of the cavities with the O1G1 design ($1\ \mu\text{m}$ overlap width and 1 groove in the cap wafer) were sealed, indicating that it is not a suitable design. The cavities with all the other designs result in vacuum sealing yields of at least 62.5%, with the O2G2 design reaching a yield of 100% after bonding. In all designs that have $2\ \mu\text{m}$ or $3\ \mu\text{m}$ overlaps, the designs with 2 or 3 grooves seem to work slightly better than the designs with

Fig. 4. Yield of vacuum sealing of cavities with different sealing ring structures before and after dicing. The labels at the horizontal axis indicate the overlap width in micrometers and number of grooves in the cap wafer, e.g. O2G3 means $2\ \mu\text{m}$ overlap width and 3 grooves in the cap wafer. The wide bars represent the corresponding yield values before wafer dicing and the thinner bars inside the wide ones denote the yield values after dicing.

only 1 groove. This could be due to that multi-groove designs provide increased Cu-Cu contact areas compared with 1-groove designs. When comparing the different overlap designs, the $1\ \mu\text{m}$ and $2\ \mu\text{m}$ overlaps tend to provide better yield values than the $3\ \mu\text{m}$ overlap, except for cavities with the O1G1 design, but the difference is not significant. The reason why the O1G1 design easily fails could simply be due to wafer-to-wafer misalignment, since in this design a misalignment of above $1\ \mu\text{m}$ can easily cause leakage into the cavity. The bonded wafers were diced four months after bonding. As can be seen from Fig. 4, there is a notable reduction of yield values after dicing for designs with $1\ \mu\text{m}$ and $2\ \mu\text{m}$ overlaps, with $1\ \mu\text{m}$ -overlap designs resulting in the lowest yield. The designs with $3\ \mu\text{m}$ overlap exhibit the best mechanical stability and hermeticity after dicing, although the absolute yield values are comparable to the designs with $2\ \mu\text{m}$ overlap. This is because a wider overlap between the Cu ring and the edges of the corresponding groove(s) results in a larger Cu bonding area, thus leading to a more stable bond. However, it should be noted that for a larger bonding area, a higher bonding force is needed to reach a given bonding pressure. For individual sealing ring designs, the O2G1 design shows the highest yield of 75% after dicing, although it only consists of an $8\ \mu\text{m}$ -wide and $5.2\ \mu\text{m}$ -high Cu sealing ring.

To evaluate the bonding interfaces, the different sealing structures were cleaved using a dicing saw and inspected using scanning electron microscope (SEM), as shown in Fig. 5. It is clearly visible that the Cu from the sealing ring on the device wafer is wedged into the grooves in the cap wafer, verifying that plastic deformation of Cu has occurred as expected. The displacement of the Cu rings into the grooves ranges from $3.1\ \mu\text{m}$ up to $4.2\ \mu\text{m}$. Cu rings of different widths were compressed from the original $5.2\ \mu\text{m}$ down to $2.5 - 4.2\ \mu\text{m}$ in height and widened by about $2 - 8\ \mu\text{m}$. These variations result from the different dimensions of the sealing ring designs

Fig. 5. Cross-sectional SEM images of different sealing rings and corresponding grooves at the bond interface: (a) is from an O2G1 design. The dashed line indicates the interface between the cap wafer and the device wafer; (b) is from an O3G2 design with a groove distance of 3 μm ; (c) and (d) represent O3G3 designs with different groove distances of 3 μm and 1.5 μm , respectively. In (d) the left groove separation wall is broken.

and the non-uniform distribution of bonding force exerted by the wafer chucks. No reflow behaviour of the Cu sealing rings was observed under SEM inspection. The bonding interface between the two wafers is compact and uniform, ensuring the hermeticity of the bond.

The sample presented in Fig. 5d shows a sealing ring structure with a broken groove separation wall that is 1.2 μm wide. The very thin groove wall broke most likely as a result of shear forces that developed during bonding. The samples with wider groove separation walls of 2.7 μm in width remained intact as can be seen in Fig. 5b and Fig. 5c. The sealing ring design with only one groove and 2 μm overlap offers the smallest footprint, i.e. bond rings which are as narrow as 8 μm , that yielded successfully sealed cavities. However, multi-groove designs resulted in higher yield of sealed cavities after bonding and dicing as compared to sealing ring designs with only one groove. In addition, it should be noted that for multi-groove designs, if the wafer-to-wafer misalignment is slightly larger than the designed overlap width, e.g. 4 μm misalignment during bonding of an O2G3 design (2 μm overlap), the cavities nevertheless can still be sealed. This is because even if the misaligned outer groove is not sealed, the other two grooves still have overlapping areas with the Cu rings to yield plastic deformation and low-temperature welding of Cu. Thus, sealing ring designs with more than one groove do increase the tolerance for wafer-to-wafer misalignment, although at the cost of a larger footprint of the sealing ring structures.

In future work it would be interesting to investigate if it is possible to further reduce the bonding temperature from 250 $^{\circ}\text{C}$ down to room temperature and still obtain reliable bonding and sealing of the Cu sealing ring structures. This may be achieved by increasing the bonding force and thus the

Fig. 6. Measured deflection of a cavity diaphragm by white-light interferometry. The zero-level (red area) refers to the initial flat wafer surface.

resulting bonding pressure on the Cu sealing ring structures.

B. Leak rate evaluation

In order to evaluate the leak rate of the sealed cavities, the deflection changes of the 4015 $\mu\text{m} \times 4015 \mu\text{m}$ cavity diaphragms were monitored over a period of 97 days by white-light interferometry (Veeco Wyko NT9300) [37]. Fig. 6 shows the measured deflection of a typical cavity diaphragm as a result of the pressure difference of the atmospheres inside and outside the cavity. The surrounding red area in Fig. 6 defines the initial flat surface of the wafer.

The deflection in the center of the diaphragm is proportional to the differential pressure [48] and the leak rate L can be derived using the formula [47]:

$$L = \ln \left(\frac{W_{t_1}}{W_{t_2}} \right) \left(\frac{VP_0}{t_2 - t_1} \right) \quad (1)$$

where W_{t_1} and W_{t_2} are the deflections at the time point t_1 and t_2 , respectively. P_0 is the ambient reference pressure outside the package. V is the volume of the sealed cavity, which is calculated to be 0.174 mm^3 under the assumption that no diaphragm deflection is present. Using this value for calculation will lead to a conservative estimation of the leak rate since in practice the cavity volume is smaller due to the deflection of the diaphragm. The deflections of all the cavity diaphragms were recorded immediately after bonding and wafer thinning, and monitored during the following 97 days. The variations of ambient pressure were compensated using data from a nearby weather station. One failure, i.e. one cavity with a gross leak was observed among the 93 sealed cavities during the test period, which was indicated by the deflection of the cavity diaphragm leveling to near 0 μm . The measured deflection variations of 24 randomly selected cavity diaphragms (the same 24 cavities throughout the evaluation period) out of the 93 diaphragms located at different positions on the wafer are plotted in Fig. 7. The flat diaphragms of the leaked cavities provide an indication that there are no significant residual stresses in the diaphragms causing the diaphragm deflections.

The measured deflections of the 24 cavity diaphragms range from 4.15 μm to 8.80 μm , as a result of the thickness difference between the diaphragms. It is clear in Fig. 7 that there is no significant trend of the deflection changes over time since both positive and negative changes were observed

Fig. 7. Cavity diaphragm deflections measured by optical interferometry over a period of 97 days. The data are collected from 24 diaphragms randomly chosen out of the 93 diaphragms located at different positions on the wafer, and have been compensated for varying ambient pressure.

throughout the evaluation period, even after ambient pressure compensation. This means that the deviations of measured deflections are on the same level as the noise of the measurement system, which reflects the detection limit of this measurement. By a conservative calculation using (1) with the smallest deflection value of $4.15 \mu\text{m}$, the cavity volume of 0.174 mm^3 , and the largest measured deflection deviation of $0.27 \mu\text{m}$, the detection limit of this leak rate measurement is determined to be $1.3 \times 10^{-12} \text{ mbarL/s}$. The true leak rates of the sealed cavities should be lower than this value, which is already well below reported values of 10^{-10} to 10^{-8} mbarL/s level using the helium fine leak test for Cu thermo-compression bonding [40], Ni/Sn solder bonding [12], and Au-Sn eutectic bonding [17]. It should be noticed that the diaphragm deflection method is suitable for long-term evaluation of leak rate but not applicable to extract an accurate number of the absolute pressure inside the cavity.

C. Residual gas analysis

In order to obtain the absolute pressures inside the sealed cavities, residual gas analysis (RGA) was conducted (SAES Getters S.p.A, Italy). The measured compositions of the gases and the relevant partial gas pressures in the sealed vacuum cavities with different sealing structures are listed in Table II. Four sealed and diced cavities with different sealing ring designs (O2G1, O2G2, O2G3, and O3G3) were chosen for RGA. Before performing RGA, the internal pressures of the four vacuum cavities were roughly estimated by observing the changes of the diaphragm deflections when placing the cavities in a vacuum chamber. Once the chamber was evacuated to reach a gas pressure of around 1 mbar, the membrane deflections leveled and were no longer visible, indicating that the pressure inside the sealed cavity should be on the order of 1 mbar or below. However, it should be pointed out that the pressure inside the cavity with the O2G1 sealing ring design was measured to be 89 mbar using RGA (not shown in Table II). A possible explanation for this may be that this

TABLE II
RESULTS FROM RESIDUAL GAS ANALYSIS (RGA) OF THREE SEALED VACUUM CAVITIES WITH DIFFERENT SEALING RING DESIGNS.

Gas	O2G2 design		O2G3 design		O3G3 design	
	Pressure (mbar)	Percent (%)	Pressure (mbar)	Percent (%)	Pressure (mbar)	Percent (%)
H ₂	2.9×10^{-2}	63.07	0	0	0	0
CO ₂	1.1×10^{-2}	23.92	0	0	0	0
CO	5.1×10^{-3}	11.09	0	0	0	0
CH ₄	0	0	2.5×10^{-2}	97.66	1.7×10^{-2}	55.77
CHs ^a	6.7×10^{-4}	1.46	4.5×10^{-4}	1.76	7.0×10^{-4}	2.30
Ar	2.1×10^{-4}	0.46	1.3×10^{-4}	0.51	1.2×10^{-2}	39.37
He	0	0	1.8×10^{-5}	0.07	7.8×10^{-4}	2.56
O ₂	0	0	0	0	0	0
N ₂	0	0	0	0	0	0
H ₂ O	0	0	0	0	0	0
Total	4.6×10^{-2}	100.00	2.6×10^{-2}	100.00	3.0×10^{-2}	100.00

^a CHs represents the contribution of light hydrocarbons (C₂H₆ and C₃H₈).

cavity was damaged during handling while performing the RGA.

The pressures inside the other three sealed cavities were all measured to be on the order of 10^{-2} mbar 146 days after bonding as indicated in Table II. Considering that no getter materials have been used, this is an excellent level that is adequate for many MEMS applications such as resonators, gyroscopes, and RF switches [49]. The achieved vacuum pressure is also well below reported data of many other vacuum packaging methods, including PECVD deposition of SiN [49], glass-frit bonding [8] and solid-liquid inter-diffusion bonding [13], which range from 0.3 to 10 mbar without getters. Since the cavity pressure at the time of sealing is not exactly known, comparing the measured cavity pressure 146 days after sealing to absolute vacuum provides a worst-case estimation of the leak rate. Based on the measured pressure of 2.6×10^{-2} mbar after 146 days and by using the formula $L = \Delta PV / \Delta t$, where V is 0.174 mm^3 , a conservative leak rate of $3.6 \times 10^{-16} \text{ mbarL/s}$ is calculated. This conservatively estimated leak rate is smaller than the reported data from cavities based on Au sealing rings [37] and Au bumps [38] by three and two orders of magnitude, respectively. Although the absolute pressure inside the cavity is not as good as the work reported in [38], it should be noted that the significantly smaller cavity volume in the present work yields a higher surface/volume ratio, which makes it more difficult to maintain the vacuum level inside the cavity. Increasing the vacuum pumping time at elevated temperature before joining the wafers could help to achieve lower cavity pressures. In addition, incorporating a getter material in the cavity can further reduce the pressure level inside the sealed cavity, which however typically requires getter activation at temperatures of above 300°C and substantially increases the package cost [50].

The gas compositions in the three cavities are distinct, but none of them reveal trace of N₂ or O₂, which is a clear indication of the excellent hermeticity of the packages. The dominant gases in the cavity with the O2G2 sealing ring design are H₂, CO₂, and CO, which could result from reactions between the water vapor and the metal sealing structures

during vacuum pumping and heating [51]. These gases could have been trapped inside the cavity while sealing and not be fully adsorbed by the inner surfaces of the sealed cavity after cooling. The gas species in the cavities with O2G2 and O2G3 designs are the same, although the proportions of the partial gas pressures are different. CH_4 , C_2H_6 , and C_3H_8 could be desorbed from the electroplated Cu sealing rings as electroplated Cu can contain pockets of organic impurities such as fragments of hydrocarbons [52] that result from additives in the electroplating solution used to achieve better uniformity. Ar is present to a high ratio in the cavity with the O3G3 design. This can be a result of outgassing from the sputtered Cu layer on the cap wafer since Ar is known to be incorporated into metal layers prepared by sputter deposition [53]. The reason why the gas composition differs between cavities can have several causes: Difference of the pumping rates at different positions of the wafer; non-uniform distribution of diffused impurities or pockets of impurities in the electroplated and sputtered Cu; or releasing of gases from Cu regions outside of the bonding frame while the cap of the cavity is broken during RGA.

D. Shear strength testing

To evaluate the robustness of the sealed cavities, the shear strength of the bond between the device substrate and the cap substrate was investigated for different sealing ring designs using a shear tester (PC2400, Dage Ltd, UK). The widths of the tested Cu sealing rings were designed to range from 8 μm to 19 μm . The sealing ring widths were typically widened during bonding to about 10 μm for the 8 μm -wide designs and up to 25 μm for the 19 μm -wide designs (25% – 32% increase). During shear strength testing, two types of failure mechanisms were observed. In the first type, the cap substrate was completely detached from the device substrate, whereas in the second failure type, only parts of the cap substrate were broken away. The measured shear forces range from 32.84 N to 41.94 N, which are very high values considering the small bond areas and footprints of the sealing rings. The measured shear force does not increase significantly with the width of the Cu sealing ring. The fracturing of the cap substrates is likely due to the fact that they are comparably thin and thus, fragile. Only about 42% of the cavities exhibited complete detachment of the cap substrates. The extracted shear strengths of all the 12 tested cavities are above 90 MPa. This excellent shear strength is much higher than the reported shear strengths of 8 MPa using Ni/Sn solder bonding [12], 25 MPa (characteristic shear strength) using Cu-Cu thermo-compression bonding [41], and 28 MPa [13] to 51.7 MPa [17] using Au-Sn eutectic bonding.

Fig. 8 shows top view images of the cap and device substrates (O2G1 sealing ring design) with parts of the Cu sealing ring sheared off during shear testing. In the SEM image, it is clear to see that the Cu ring is stuck into the groove in the cap substrate and detached from the device substrate, which indicates that the shear strength of the bond is higher than the adhesion between the Cu ring and the device substrate. In addition, the Cu ring in the cap substrate maintained an intact line shape after bonding, verifying that no reflow had

Fig. 8. Top image: The cap substrate (O2G1 sealing ring design) is completely detached from the device substrate after shear testing (the first failure type). Bottom image: SEM top view of the area in the cap substrate where the Cu sealing ring is completely detached from the device substrate and embedded into the groove of the cap substrate.

occurred. The excellent bonding strength in combination with the small sealing ring footprint achieved here enables further miniaturization of vacuum packages compared to alternative metal-based vacuum packaging techniques, which use sealing rings that are typically at least 100 μm wide [13], [14], [16], [18], [22], [23], [25], [33], [36], [37], [39].

IV. CONCLUSION

A wafer-level vacuum packaging method based on plastic deformation and low-temperature welding of Cu at 250 $^{\circ}\text{C}$ has been proposed and evaluated. The pressure inside the sealed cavities was measured to be as low as 2.6×10^{-2} mbar and the leak rate is calculated to be better than 3.6×10^{-16} mbarL/s. Cu sealing rings that are 5.2 μm high and as narrow as 8 μm provide hermetic and mechanically stable vacuum sealing of cavities at wafer scale. These cavities can survive wafer dicing to singulate individual dies. The shear strengths of the seals are measured to be above 90 MPa. Sealing ring designs with multi-groove structures tend to exhibit better hermeticity, mechanical stability, and larger wafer-to-wafer misalignment tolerance than designs with only one groove in the cap wafer. The proposed sealing strategy offers reliable, simple, and cost-effective vacuum sealing for a wide range of MEMS applications. Since Cu is an established material used in state-of-the-art ICs and in 3D ICs, this method could enable reliable electrical, mechanical, and hermetic Cu connections in future 3D integrated MEMS and 3D IC components.

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Göran Stemme (F’06) received the M.Sc. degree in electrical engineering and the Ph.D. degree in solid-state electronics from Chalmers University of Technology, Gothenburg, Sweden, in 1981 and 1987, respectively.

In 1981, he joined the Department of Solid State Electronics, Chalmers University of Technology, where he became an Associate Professor (docent) heading the silicon sensor research group in 1990. Since 1991, he has been a Professor at KTH Royal Institute of Technology, Stockholm, Sweden, where

he is the Head of the Department of Micro and Nanosystems, School of Electrical Engineering. His research is devoted to microsystem technology based on micromachining of silicon. He has published more than 300 research journal and conference papers and has more than 22 patent proposals or granted patents.

Dr. Stemme is a member of the Royal Swedish Academy of Sciences (KVA).

Xiaojing Wang received his Bachelor Degree in mechanical engineering from National University of Defense Technology, Changsha, China, in 2013.

After finishing his course studies on Master level, he has been conducting his Ph.D. research in the Department of Micro and Nanosystems, School of Electrical Engineering, KTH Royal Institute of Technology, Stockholm, Sweden, since 2014. Currently he is working on wafer-level vacuum packaging technologies and microsystems for medical applications.

Simon J. Bleiker received the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology, Zurich, Switzerland, in 2012.

He is currently pursuing the Ph.D. degree with the Microsystem Technology Group, Royal Institute of Technology (KTH), Stockholm, Sweden. His current research interests include MEMS integration technology and self-assembly and a European Union funded research project about nanoelectromechanical systems for computation applications.

Frank Niklaus (SM’12) received the M.Sc. degree in mechanical engineering from the Technical University of Munich, Munich, Germany, in 1998, and the Ph.D. degree in MEMS from KTH Royal Institute of Technology, Stockholm, Sweden, in 2002.

He has been a Professor with the Department of Micro and Nanosystems, KTH, since 2013, where he is currently the Head of the Micro and Nanofabrication Group. His current research interests include innovative manufacturing, integration, and packaging technologies for MEMS and nanoelectromechanical

systems.

Mikael Antelius received the M.Sc. degree in chemical engineering from Uppsala University, Uppsala, Sweden, in 2007, and the Ph.D. degree in Micro and Nanosystems from KTH Royal Institute of Technology, Stockholm, Sweden, in 2013.

He is currently at APR Technologies, Enköping, Sweden