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Comparison of Thermal Stress during Short-Circuit in Different Types of 1.2 kV SiC Transistors Based on Experiments and Simulations

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Abstract. The temperature evolution during a short-circuit in the die of three different Silicon Carbide 1200-V power devices is presented. A transient thermal simulation was performed based on the reconstructed structure of commercially available devices. The location of the hottest point in the device is compared. Finally, the analysis supports the necessity to turn-off short-circuit events rapidly in order to protect the device immunity after a fault.

Introduction

The short-circuit (SC) behaviour of three Silicon Carbide (SiC) devices available on the market was investigated in [1]. The present paper compares the evolution in time of the temperature distribution in the chip of 3 different types of 1.2 kV SiC transistors during a short-circuit event. In [2] the maximum junction temperature evolution in time for a SiC MOSFET and a SiC BJT (SJT) has been computed by means of a Cauer model. In contrast, in this work, devices have been de-capsulated in order to reconstruct their structures in Taurus MEDICI [3]. Similar work for the SiC JFET has already been performed in [4]. The temperature distribution in the chip of each device is then simulated based on the experimental short-circuit tests. Moreover, results for a SiC JFET are presented.

Experimental Setup

The measured and simulated structures were SiC MOSFET, SiC BJT and SiC JFET, rated at 1.2 kV. The test circuit is illustrated in Fig. 1, where $V_{dc} = 600 \text{ V}$, $C_{in} = 160 \mu\text{F}$ and $L_{stray} = 10 \text{ nH}$. The drivers used to turn the devices on are adapted to the device type. More informations on the drivers used in this work can be found in [1]. The short circuits experimental results for the SiC MOSFET, SiC BJT and SiC JFET are illustrated in Fig. 2, where the devices are turned into a short-circuit (short-circuit type I) under $V_{ds} = 600 \text{ V}$. The devices under test and their short-circuit peak current $I_{sc,peak}$ and the over-voltage at turn-off are stated in Table 1.

Table 1: Short-circuit behaviour of the devices under test

SiC DUTs	$I_{peak} [\text{A}]$	Overvoltage [V]
SCT2080KE	300	150
UJN1205K	120	200
GA50JT12-247	80	25

Device Structure

To obtain precise information on the device structure, the devices were decapsulated as in [5]. Dimensions of the device structures for simulation were investigated and obtained by scanning electron

Fig. 1: Schematic diagram of the short-circuit test for a discrete device

Fig. 2: Short-circuit behaviour of SiC devices (a) SiC MOSFET, (b) SiC JFET and, (c) SiC BJT

microscopy (SEM) [4]. The structures were further calibrated by comparison of simulated static electrical characteristics – output, gate transfer and blocking characteristics – with the datasheet values. SEM pictures are given in 3, for the SiC MOSFET, SiC JFET and, SiC BJT (SJT). The driving conditions are as in the experiment and the source stray inductance has been measured and is set to 10 nH for the best fit to the measured currents and voltages during the SC tests, see Fig. 3a for the SiC MOSFET, Fig. 3b for the SiC JFET and, Fig. 3c for the SiC BJT respectively. The simulated curves are shown in Fig. 4. It can be seen that they are corresponding to the experimental curves shown in Fig. 2.

Fig. 3: Device structures of the (a) SiC MOSFET, (b) SiC JFET and, (c) SiC BJT

Electro-thermal simulations of SiC MOSFETs, BJTs and normally-On JFETs

The temperature distributions in the SiC JFET, SiC BJT and SiC MOSFET after 500 ns can be observed in Fig. 6a, Fig. 6b, and Fig. 6c, respectively. In the SiC JFET device the hottest area is located in the drift region and also deepest in the structure and farthest away from the top surface compared to the

Fig. 4: Simulated Electrical Short-circuit behaviour of SiC devices (a) SiC MOSFET, (b) SiC JFET and, (c) SiC BJT

SiC BJT and SiC MOSFET. The distance to the surface is $6 \mu m$ and the distance to the trench bottom is $2.5 \mu m$. In the SiC BJT the hottest area is located in the collector region close to the base-collector junction and under the edge of the emitter. The distance to the surface is $4 \mu m$ and $1.5 \mu m$ to the base-collector junction. Finally, in the SiC MOSFET the hottest area is located under the gate and just below the JFET region of the DMOSFET structure. The distance between the hottest area and the surface (and gate-oxide) is $2 \mu m$. This is significantly smaller than for the two other device types. After 500 ns, the maximum temperature values from the simulations are $273^\circ C$, $108^\circ C$ and $136^\circ C$ for SiC MOSFET, SiC JFET and SiC BJT, respectively. After $1 \mu s$ of SC stress the maximum temperatures are $402^\circ C$, $227^\circ C$ and $187^\circ C$. The temperature evolution for a short-circuit event of $1 \mu s$ is shown in Fig. 5. It can be observed that for the SiC MOSFET, the temperature in the die rises significantly higher than for the other devices. This may be critical considering the narrow distance between the hottest point and the surface and gate-oxide. The active device area is 0.071 , 0.141 and 0.096 cm^2 for the SiC JFET, SiC BJT and SiC MOSFET, respectively. Thermal boundary conditions were obtained from the fit to the thermal impedance data for pulse width less than 0.001 sec for each device. The differences between the localization of the hottest region and the simulated maximum temperature values are clearly related to the physics of operation and unit cell design of the different devices. Although for the SiC MOSFET, the oxide layer can withstand higher temperatures than $273^\circ C$, this high temperature can be critical for the encapsulating material or lead to increased gate leakage current due to charge transport over the potential barrier. The latter observations show that it is important to turn-off a short-circuit fault quickly when using SiC MOSFETs since the temperature rise is quicker. The turn-off time can be longer for SiC JFETs and SiC BJTs. The two latter devices are therefore more robust against short-circuit faults.

Fig. 5: Evolution of the max. temperature for a $1 \mu s$ short-circuit event (a) SiC MOSFET, (b) SiC JFET, (c) SiC BJT

Fig. 6: Temperature distribution in the device die after a 500 ns short-circuit event a) SiC MOSFET $T_{max} = 273$ °C, (b) SiC JFET $T_{max} = 108$ °C, (c) SiC BJT $T_{max} = 136$ °C

Summary

The present paper investigated the temperature distribution in the chip of three different SiC devices after 1 μ s of short-circuit fault. The results of the simulations revealed that the SiC MOSFET was the device that requires the fastest turn-off response time in case of a short-circuit since it has both the highest temperature rise after 1 μ s as well as the shortest distance between the hottest point in the die and the surface. Moreover, considering that the oxide-layer may be more sensitive to higher temperature than the surface, limitation of the short-circuit duration is desirable in order to preserve the device immunity. Secondly, although the SiC JFET has a wider distance between the hottest point and the surface than the SiC BJT, the temperature rise in the SiC JFET is approx. 8 % higher after a short-circuit of 1 μ s compared to the SiC BJT. This value increases to 33 % for the SiC MOSFET.

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