On Reliability of SiC Power Devices in Power Electronics

DIANE-PERLE SADIK

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A mes parents, ma soeur Johanna, mon frère Salomon...
A Christine qui garde un œil sur moi au pays des anges...
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Abstract

Silicon Carbide (SiC) is a wide-bandgap (WBG) semiconductor material which has several advantages such as higher maximum electric field, lower ON-state resistance, higher switching speeds, and higher maximum allowable junction operation temperature compared to Silicon (Si). In the 1.2 kV - 1.7 kV voltage range, power devices in SiC are foreseen to replace Si Insulated-gate bipolar transistors (IGBTs) for applications targeting high efficiency, high operation temperatures and/or volume reductions. In particular, the SiC Metal-oxide semiconductor field-effect transistor (MOSFET) – which is voltage controlled and normally-OFF – is the device of choice due to the ease of its implementation in designs using Si IGBTs.

In this work the reliability of SiC devices, in particular that of the SiC MOSFET, has been investigated. First, the possibility of paralleling two discrete SiC MOSFETs is investigated and validated through static and dynamic tests. Parallel-connection was found to be unproblematic. Secondly, drifts of the threshold voltage and forward voltage of the body diode of the SiC MOSFET are investigated through long-term tests. Also these reliability aspects were found to be unproblematic. Thirdly, the impact of the package on the chip reliability is discussed through a modeling of the parasitic inductances of a standard module and the impact of those inductances on the gate oxide. The model shows imbalances in stray inductances and parasitic elements that are problematic for high-speed switching. A long-term test on the impact of humidity on junction terminations of SiC MOSFETs dies and SiC Schottky dies encapsulated in the same standard package reveals early degradation for some modules situated outdoors. Then, the short-circuit behavior of three different types (bipolar junction transistor, junction field-effect transistor, and MOSFET) of 1.2 kV SiC switching devices is investigated through experiments and simulations. The necessity to turn OFF the device quickly during a fault is supported with a detailed electro-thermal analysis for each device. Design guidelines towards a rugged and fast short-circuit protection are derived. For each device, a short-circuit protection driver was designed, built and validated experimentally. The possibility of designing diode-less converters with SiC MOSFETs is investigated with focus on surge current tests through the body diode. The discovered fault mechanism is the triggering of the npn parasitic bipolar transistor. Finally, a life-cycle cost analysis (LCCA) has been performed revealing that the introduction of SiC MOSFETs in already existing IGBT designs is economically interesting. In fact, the initial investment is saved later on due to a higher efficiency. Moreover, the reliability is improved, which is beneficial from a risk-management point-of-view. The total investment over 20 years is approximately 30 % lower for a converter with SiC MOSFETs although the initial converter cost is 30 % higher.

Keywords: Silicon Carbide, Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), Junction Field-Effect Transistor (JFET), Bipolar Junction Transistor (BJT), Reliability, Failure Analysis, Reliability Testing, Short-Circuit Currents, Humidity, Resonant converter, Series-resonant converter (SLR), Base drive circuits, Gate drive circuits, Life-Cycle Cost Analysis (LCCA).
Sammanfattning

Kiselkarbid (SiC) är ett bredbandgapsmaterial (WBG) som har flera fördelar, såsom högre maximal elektrisk fältstyrka, lägre ON-state resistans, högre switch-hastighet och högre maximalt tillåtna arbetstemperatur jämfört med kisel (Si). I spänningsområdet 1,2-1,7 kV förutses att effekthalvedar-komponenter i SiC kommer att ersätta Si Insulated-gate bipolar transistorer (IGBT:er) i tillämpningar där hög verkningsgrad, hög arbetstemperatur eller volymreduktioner eftersträvas. Förstahandsvalet är en SiC Metal-oxide semiconductor field-effect transistor (MOSFET) som är spänningsstyrda och normally-OFF, egenskaper som möjliggör enkel implementering i konstruktioner som använder Si IGBTer.


Nickelord: Kiselkarbid, MOSFETar, JFETar, Bipolär Junction Transistor (BJT), Tillförlitlighet, Robusthet, Felanalys, Tillförlitlighetstestning, Kortslutningsströmmar, Luftfuktighet, Resonansomvandlare, Série-resonansomvandlare (SLR), Basdrivkretsar, Gate-drivkretsar, Felskydd, Livscykelnanalys.
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Stockholm, May 2017
Diane-Perle Sadik
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Chapter 1

Introduction

The motivation behind this doctoral dissertation is given in this chapter. The objectives of this work are presented as well as the main scientific contributions. Appended and related publications are listed.

1.1 Background

Power electronics (PE) is the application of solid-state electronic components with the task to control and convert electric power from one form to another. PE converters are used to convert voltages, currents or frequencies. Such converters can have different power ranges from watts to hundreds of megawatts depending on the application. While the converter topology may vary depending on the application, the targets are often to process power in an efficient manner, safely, and at low cost. Up to recently, semiconductor devices have been made with silicon (Si). One limitation of this technology is the maximum permissible operation temperature. Another limitation is the switching frequency. As a result, research efforts have been targeting so-called "wide band gap" power semiconductors such as silicon carbide (SiC) and galium nitride (GaN). Some properties of these materials compared to Si can be found in Table 1.1.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>SiCv</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap energy [eV]</td>
<td>1.1</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Breakdown electric field [MV/cm²]</td>
<td>0.3</td>
<td>3.5</td>
<td>3.3</td>
</tr>
<tr>
<td>Electron mobility [cm²/V·s]</td>
<td>1500</td>
<td>900</td>
<td>900-2000</td>
</tr>
<tr>
<td>Electron saturation velocity [cm/s]</td>
<td>1·10⁷</td>
<td>2.2·10⁷</td>
<td>2.5·10⁷</td>
</tr>
<tr>
<td>Thermal conductivity [W/cm-K]</td>
<td>1.5</td>
<td>5.0</td>
<td>1.3</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.9</td>
<td>10</td>
<td>8.9</td>
</tr>
</tbody>
</table>
Silicon carbide has undergone a dramatic development during the last two decades. It has a larger bandgap compared with Si, ranging from 2.3 to 3.3 eV. As a consequence, the maximum operation temperature can be higher than for Si. The current status of the metallization, contacts, and packaging limit the temperature of operation. However, the high critical electric field strength allows thinner drift layers required for a given voltage, and higher doping concentrations [1]. As a result, the ON-resistance of unipolar devices can be reduced by almost three order of magnitude as compared to Si. This allows to produce unipolar devices like Schottky diodes and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) up to much higher voltages compared to Si devices. As a consequence unipolar SiC devices are today replacing bipolar rectifiers and IGBTs up to voltages above 3.3 kV. The unipolar SiC devices are characterized by extremely fast switching due to the lack of stored charges. Thus, fast-switching and highly efficient devices can be fabricated such as Schottky diodes, high-voltage PiN diodes, bipolar and unipolar active devices. The devices will be presented in Chapter 2. The reason for late development of SiC technology is that the substrate is much difficult to fabricate than Si substrates. SiC substrates are produced by sublimation growth at temperatures above 2000 °C while Si substrates are grown by crystallization from the melt at much lower temperatures producing crystals with much larger size and better quality. The SiC material has been suffering from various defects such as micropipes and stacking faults. However, effort have been made to develop wafers free from defects and devices with larger areas have been developed. The largest commercially available MOSFET dies are today about 0.3 cm² and still more than three times smaller than Si IGBT dies. The devices developed in SiC are ranging from 600 V to 10 kV. The commercially available devices are rated 600 V, 900 V, 1.2 kV, and 1.7 kV.

At the time this work was initiated, the available SiC devices where the Schottky diode, the Junction Field Effect Transistor (JFET), and the Bipolar Junction Transistor (BJT). The Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) had just been released as the lower quality of the SiO2-SiC interface slowed down the fabrication of a reliable SiC MOSFET devices. Up to now, SiC devices have been far more expensive than corresponding Si devices. However, due to the aforementioned advantages of SiC, great improvements in efficiency can be achieved when replacing Si by SiC. Moreover, SiC will allow the design of converters operating at higher temperatures which reduces the cooling system requirements. Finally, the higher switching speeds allow a size reduction of the passive components. These three aspects may lead to reduced investment costs as well as operating costs. However, reliability is also a key factor when considering the use of a new technology in real applications. The reliability aspects covered in this doctoral thesis are presented in Section 1.2.
1.2 Main Objectives

The main objective of this work is to evaluate the reliability and robustness of state-of-the-art SiC power devices. The following tasks were defined:

- Study of the potential reliability issues still present in the state-of-the-art SiC devices available on the market. The analysis is done both on the die level and on the package device level, but also from a system perspective.
- Investigation of the possibility to parallel connect discrete MOSFET devices
- Modelling of a SiC Power Module package and analysis of the stray inductance impact on the reliability
- Long term testing of SiC MOSFET discrete devices and modules without acceleration factors
- A complete study of the short-circuit behavior of SiC power devices and a solution for protection circuits. A complete analysis of the temperature spread and rise with time in the die during a short-circuit is also presented. This complements the electrical behavioural analysis. Corresponding protection drivers for each of the tested devices are implemented and verified experimentally and in a full converter setup
- An analysis of the reliability and possibility of cost/efficiency improvement when replacing Si IGBT modules with SiC MOSFET modules in a resonant converter application

1.3 Outline of the thesis

Chapter 1 introduces the thesis, provides the background of the technology and reliability aspects and shows the main objectives. It also describes the main scientific contributions.

Chapter 2 introduces several silicon carbide devices and their respective reliability concerns.

Chapter 3 shows the experimental investigation of the possibility to parallel-connect SiC MOSFETs. This includes early overviews static and dynamic performances by pairs as well as implemented in a dc/dc boost converter.

Chapter 4 investigates the impact of parasitic elements in a standard power module package designed for Si IGBTs but populated with SiC MOSFET chips. A finite element model is reconstructed based on the module geometry and material. The model is verified by comparison of experimental measurements on-chip and at the module terminals. Finally, reliability aspects are discussed.

Chapter 5 shows the experimental outcome of 1000 hours long-term testing of SiC MOSFET discrete devices. Two different failure modes are investigated.
Chapter 6 investigates the threshold-voltage behavior of SiC power MOSFET modules when exposed to humid environment.

Chapter 7 gives a complete analysis of the short-circuit behavior of SiC Power devices. A thermal analysis of the temperature spread in the die is done to complement the experimental electrical behaviour. Protection solutions are presented for each device within turn-off times determined by the aforementioned analysis. Finally, different circuit parameters which impact the temperature rise in the die are analyzed by simulations.

Chapter 8 describes the failure mode of SiC Power MOSFET discrete devices and module when subjected to surge current in the reverse direction. This work has been performed experimentally.

Chapter 9 gives a life estimation of a series resonant system using SiC power modules and derives a life-cycle cost analysis.

Chapter 10 draws the conclusions of the work discusses ideas for future work.

1.4 Methodology

The results of this work are mainly observed by experiments but also demonstrated by simulations which match the experimental results. The experimental results are performed by measuring the voltage and current waveforms using voltage probes and Rogowski coils. The long term tests where monitored using the CompactRIO Platform from National Instrument together with the LabView software. For the humidity testing, the monitoring is done with the Keysight Data-logger HP34970A. The parasitic elements of the MOSFET module model where simulated by implementing the module geometry into the ANSYS Q3D software. The temperature distribution in the die was derived by implementing the geometry and design of different decapsulated devices into the Taurus MEDICI software.

1.5 Main Scientific Contributions

This thesis has resulted in the following original scientific contributions:

- Investigations on the parallel connection of two SiC discrete MOSFETs with identical and non-identical characteristics have been performed through static and dynamic tests. It was shown that parallelling SiC MOSFETs can be done without selection criteria. A positive temperature coefficient of the ON-state resistance has been observed when sufficient current is fed through the device with a gate voltage of 24 V.

- The SiC MOSFET module CAS120M12BM2 from Wolfspeed packaged in a 62 mm housing has been reconstructed in ANSYS Q3D. The extracted package parasitic elements have been simulated in LTSPICE in order to investigate the impact of the gate-loop inductance on the gate-source voltage. It was concluded that there is a need for a dedicated package for SiC modules. However,
when used with the recommended gate resistor value and a minimized inductance between the gate-driver and the gate-source terminal of the module, the 62 mm package is reliable.

- For the SiC MOSFET, two 1000 h tests have been performed. It has been shown that the threshold voltage drift when powering-OFF the SiC MOSFET during a prolonged time is not an issue and that the body-diode conduction is not a potential treat for devices from the second generation and forward.

- The impact of humidity of SiC MOSFET modules has been verified in a non accelerated test setup. This type of study has not been done earlier. It has been shown that modules placed outdoors present signs of early degradation of their blocking voltage characteristics.

- The behavior of SiC devices (MOSFETs, BJTs, and JFETs) during the early phase of a short-circuit event has been studied extensively. A gate driver design including a rapid short-circuit protection has been proposed for each device type. This protection has been designed, built and tested successfully for the three device types. An electro-thermal analysis has been performed based on simulations. The simulations have been modelled using the device structure obtained by decapsulation and and scanning electron microscopy by Mietek Bakowski and Jang-Kwon Lim. An extended analysis on the impact of various circuit parameters on the temperature evolution in the die of a SiC MOSFET has been presented. The conclusions are that, when using the full SiC potentials, a fast protection against short-circuit events is required.

- The possibility of building diode-less high-voltage direct-current converters with SiC MOSFET devices has been analyzed. Surge current through the body diode of SiC MOSFET devices has not been linked to bipolar degradation. The failure of the SiC MOSFET when a surge current is flowing in the reverse direction has been linked to a turn-ON of the parasitic npn bipolar transistor. The failure has been observed on devices from different manufacturers and different generations. Moreover, the presence of Schottky diode chips in the module does not prevent the phenomenon from occurring.

- A life-cycle cost analysis has been performed in order to show that replacing Si IGBTs with SiC MOSFETs in a state-of-the-art converter will improve the efficiency and reliability of the system and not cost more than the Si based system. In fact, the cost saving generated by the considerably lower loss generation cover the higher investment cost of the SiC based converter. Additional redundancy in order to improve the reliability and further reducing the losses has been investigated. However, over a lifetime of twenty years, the additional expenses are barely covered and this solution is not economically attractive.
1.6 List of Appended Publications


This paper investigate the possibility of parallel-connecting two discrete SiC MOSFET devices. The static and dynamic aspects are covered in order to investigate the steady-state current sharing and transient current sharing of various selected devices. Finally, a boost converter with two parallel-connected discrete devices was built. For the steady-state test, two devices are randomly selected. The test is performed with three values of shared current $I_{\text{shared}} = I_1 + I_2$ : 10 A, 20 A, and 25 A. The case temperature are measured by a thermal camera and the electrical values $V_{ds}$ and $I_{ds}$ are measured every 2 minutes. A positive temperature coefficient of the on-state resistance $R_{ds,\text{on}}$ could be identified from this test. For the dynamic test, devices are selected with regards to their pre-measured characteristics $V_{th}$ and $R_{ds,\text{on}}$ in order to investigate the behaviour of similar devices and very different devices. As expected, a mismatch in the device characteristics results in different switching losses among the two devices. The ON-state sharing is also deteriorated. The experimental verification in a converter performed via the boost-converter reveals an unbalance in the thermal losses of the two MOSFETs under test.

The main contributions to this manuscript are the construction of the two different experimental setup, electrical and thermal measurements, as well as the verification with the boost converter, and the preparation of the manuscript.


In this work, the impact of the stray inductances of the gate-loop of a commercially available SiC power MOSFET module. The module is reconstructed according to its geometry and materials in the ANSYS Q3D software. The parasitic inductances and capacitances inside the module as well as the resistive elements are extracted. An electrical simulation model is built based on the extracted parameters and including the estimated parasitic elements of the driver and supply
circuits. The model is successfully verified by comparing the experimental waveforms obtained while measuring at the module terminals under a double-pulse test. Moreover, on-chip measurements have been performed. These measurements confirm the validity of the simulation model. Finally, the stresses on the gate oxide during commutation in this module while varying the gate-loop stray inductance and driver gate resistance are addressed. The possible reliability issues resulting from too high stray inductances and/or too low gate-resistance are discussed to conclude this work.

The main contribution to this manuscript are the electrical simulation model, the experimental verification of the simulation model, the analysis of different realistic case scenarios and their impact on the gate-source junction reliability as well as the preparation of the manuscript. The module was reconstructed in ANSYS Q3D by Konstantin Kostov.


This conference paper covers two different reliability issues of the early generations of SiC MOSFETs: the body-diode degradation and the threshold voltage instability. The two tests are performed for over 1000 hours while measurements of key values are carried out every hour. Both test setups were automated. It was found that the continuous conduction of current through the body diode is no longer a problem. The threshold voltage test was performed for negative bias. In this case, it was found also that the drift in threshold voltage was not significant.

The main contribution to this manuscript are the two automated setups, data recorded for a minimum of 1000 hours every hour, the analysis of the obtained results and the preparation of the manuscript.
CHAPTER 1. INTRODUCTION


In this publication, the effect of humidity on SiC power modules is investigated. To do so, four identical full-bridge series resonant converters are built using commercially available SiC power MOSFETs. Two of these converters are operated outdoors while the two others are operated indoors. The setup is monitored and continuously operated for a total of 8000 h. The blocking voltage of all the power modules is measured regularly during the test period.

The main contribution to this manuscript is the replacement of Si IGBT module with SiC MOSFET modules in a resonant converter application, the operation of two converters indoors and two outdoors, the measurement of the blocking voltage during the test period of 8000 h, as well as the data analysis, and the preparation of the manuscript.


In this paper, an update of Publication IV is given where the results from 1700h to 5924h of the test are given. The present paper form is the abstract for the 19th IEEE European Conference on Power Electronics and Applications (EPE). The final paper will contain the full results for 8000 h of operation.

The main contribution to this manuscript is the replacement of Si IGBT module with SiC MOSFET modules in a resonant converter application, the operation of two converters indoors and two outdoors, the measurement of the blocking voltage during the test period of 8000 h, as well as the data analysis, and the preparation of the manuscript.

This paper studies the electrical and thermal behavior of three different types of SiC devices during the early phase of a short-circuit event. It was shown that the short-circuit can be detected by the desaturation technique for all three device types. The differences in behavior between the devices are highlighted. Moreover, the temperature distribution in the die of one of the two investigated SiC MOSFET has been simulated. The analysis supports the need to turn OFF a short-circuit event quickly but with a low turn-OFF speed. Consequently, three short-circuit protection drivers - one for each device type - have been realized and experimentally verified. The short circuit could be detected within 180 ns for all devices and the fault was turned off safely for all devices. The drivers developed permit to safely protect the devices without affecting the switching performances significantly.

The main contributions to this manuscript are the experimental short-circuit setup, the design, realization and verification of the three different gate drivers first in simulation and then on printed-circuit boards, the analysis of the simulated temperature distribution in the MOSFET die, and the preparation of the manuscript. The thermo-electrical simulations were realize by Mietek Bakowski.


This paper compares the temperature distribution in the die of three different types of SiC devices during the early phase of a short-circuit event. A device simulation model was developed by Mietek Bakowski and Jang-Kwon Lim. The dimensions of the devices have been extracted by decapsulation and scanning electron microscopy. The doping levels have been determined by comparison between simulated conduction, transfer, and blocking characteristics with the datasheet values. The thermal boundary conditions are based on the thermal capacitance and thermal resistance values ($C_{th}$ and $R_{th}$) extracted from the transient impedance data curves for the respective device. They are then reconstructed in the Taurus Medici software. The device models are simulated under the same conditions as the
experiments presented in Publication VI. It was found that the simulated curves are corresponding to the experimental ones. The comparison between the different devices reveals that the temperature rise for the SiC MOSFET is higher than for the SiC JFET and SiC BJT. This supports the author’s hypothesis of turning OFF a short-circuit as fast as it can be detected.

The main contributions to this manuscript are the experimental short-circuit setup as well as the comparison of the temperature distribution in different device types based on the simulations provided by Mietek Bakowski, and the preparation of the manuscript.


In this work, ruggedness of the SiC MOSFET body diode with respect to surge currents is investigated. The investigated devices are both discrete devices and modules (with and without integrated Schottky diodes). A test setup was realized such that it was possible to vary the length and the amplitude of the current surge which was a half-sine wave. No bipolar degradation has been observed. All the devices failed when the voltage across their body-diode exceeded a critical value, regardless of the duration of the surge current. An identical behavior was observed for the modules containing Schottky diode chips. The hypothesis of the author is that the failure mechanism of the SiC MOSFETs is the activation of the parasitic npn-transistor leading to a bipolar second breakdown.

The main contribution to this manuscript is the test setup, the experimental work - both performed together with Keijo Jacobs - as well as the preparation of the manuscript. Stefanie Heinig has contributed to the manuscript.
1.7. RELATED PUBLICATIONS


This work investigates the advantages of replacing Si-IGBTs with SiC MOSFET modules in an already existing application. The investigated topology is a load resonant full-bridge converter which constitutes the low-voltage unit of a power supply for an industry application. The analysis shows a non-negligible improvement in reliability and a considerable reduction in losses. The life-cycle cost analysis demonstrates that, even though the investment cost is higher when using SiC, the energy savings compensate for the investment over the product lifetime. Moreover, the total costs for the end user are lower when upgrading to SiC technology. Redundancy for the SiC-based converter is also investigated. The reliability becomes four times higher compared with the initial Si reference case. However, over a 20 year lifetime, the investment costs are too high and are not economically interesting in comparison with the Si technology.

The main contribution to this manuscript is the modelling of the reliability of SiC MOSFET modules and a SiC-based converter topology, the life-cycle cost analysis of three different cases, and the preparation of the manuscript.

1.7 Related Publications

The following list of publications is composed by a variety of work related to SiC devices in various applications. The author of this thesis is a contributor of these works conducted in parallel to this project. In peer-reviewed journals:


In conference proceedings


Chapter 2

SiC Power Devices and Reliability Aspects

2.1 Introduction

Silicon Carbide (SiC) as a material for power devices has attracted much research and development efforts in the last two decades. In contrast to silicon (Si), which has a bandgap energy of 1.1 eV, 4H-SiC has a bandgap energy of 3.2 eV. As a consequence, the maximum permissible operating temperature and breakdown electric field are much higher than for Si. Another advantage of unipolar devices in SiC compared to Si bipolar devices is that much higher switching speeds are possible. This results in lower switching losses and possibilities to increase the switching frequency. Finally, when comparing conduction losses of unipolar devices in SiC with Si IGBTs, it is found that great reduction can be achieved. In fact, almost infinitely low conduction losses can be achieved by increasing the chip area of unipolar SiC power devices. Increasing the chip area of Si IGBT would not pay off in the same way, because of the built-in potential of the Si IGBT. However, since SiC devices have been recently introduced, reliability has to be evaluated. First, the newly introduced devices should be as robust as the Si devices so to be competitive in terms of lifetime. Secondly, due to the inherent possibility to operate at higher temperature, higher blocking voltages compared to the chip thickness, and higher switching frequencies, the SiC devices may have to sustain higher stress compared with their Si counterpart. The material properties of Si and SiC are stated in Table 2.1.

2.2 SiC Power Devices

This work focuses on SiC power devices reliability. Since the beginning of this doctoral work, the SiC power devices have evolved and gone through a couple of generations of development. The devices available on the market nowadays are
Table 2.1: Material properties of Silicon and Silicon Carbide

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap energy [eV]</td>
<td>1.1</td>
<td>3.2</td>
</tr>
<tr>
<td>Breakdown electric field [MV/cm²]</td>
<td>0.3</td>
<td>3.5</td>
</tr>
<tr>
<td>Electron mobility [cm²/V·s]</td>
<td>1500</td>
<td>900</td>
</tr>
<tr>
<td>Electron saturation velocity [cm/s]</td>
<td>1·10⁷</td>
<td>2·10⁷</td>
</tr>
<tr>
<td>Thermal conductivity [W/cm·K]</td>
<td>1.5</td>
<td>5.0</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.9</td>
<td>10</td>
</tr>
</tbody>
</table>

packaged as discrete devices or modules. The devices types currently available on the market are SiC JFETs, SiC BJTs, SiC MOSFETs, and SiC Schottky diodes. These devices are available at different rated voltages from 600 V to 1.7 kV. The current ratings vary from 2.6 A to 325 A. The most popular device types are the SiC Schottky diode and the SiC MOSFET due to their fairly simple implementation as a replacements to Si devices. However, the SiC JFET and the SiC BJT offer advantages and are competitive with the SiC MOSFETs in other ways. The variety of available SiC devices from different manufacturers shows that the SiC technology has matured and is ready to replace Si technology in various applications. Most applications, nevertheless, require high reliability. However, the reliability aspect is necessary in order to convince the different actors to use SiC where Si has proven to be reliable since many year. Being a new technology, SiC cannot easily prove the high robustness claimed by its manufacturers by field experiments only. Therefore, the focus of this work was to investigate different aspects of reliability of SiC devices with regards to material properties (degradation, drifts and stability), device design and packaging (parasitics and humidity), and fault handling (surge current in forward and reverse direction). In the final phase of this project work, the focus has been on determining how fast the investment in SiC devices can be recovered by the savings brought by its advantages (such as energy savings).

SiC Power Diodes

The SiC Schottky diode is by far the most investigated SiC device so far as it is the first device which reached maturity. It was introduced commercially by Infineon Technologies and Cree Inc. in 2001 and 2002, respectively. Today, available SiC Schottky diodes cover the voltage range from 600 V to 1700 V with a current rating per die reaching up to 100 A per die at room temperature (C5D50065D from Wolfspeed). At first, due to their comparably high cost, they have mainly been used in high-end applications like server or telecom power supplies. Later on, they have been introduced in performance-driven applications such as solar power conversion. SiC diodes have near-zero reverse recovery current and are used in combination with Si devices in order to increase the transient slew rates. Hybrid Si-SiC modules are also available on the market. From a reliability point-of-view,
2.2. **SiC POWER DEVICES**

Schottky diodes have been the devices which have the most hours of operation among all SiC devices and have reached very low failure rates. Today, one may even claim that the SiC Schottky diode outperforms many Si devices in several aspects of reliability. In [cite 68], several aspects of reliability of SiC Schottky diodes have been investigated. These aspects include material related, design related, and package related reliability issues. From an over-current and over-voltage handling point-of-view, SiC Schottky diodes are more reliable than most Si devices. The conclusions are that if SiC Schottky diodes are used in conjunction with other SiC devices, the effort for increasing the reliability of the system should not be focused on the SiC Schottky diodes but on the other devices. For this reason, the SiC Schottky diode is not investigated in this work.

**Junction Field-Effect Transistors (JFETs)**

Two different SiC JFET structures have been developed so far. The first type is the Lateral Channel JFET (LCJFET). The second type is the Vertical Trench JFET (VTJFET). The LCJFET is a normally-ON device but the VTJFET can either be normally-ON or normally-OFF [2,3]. The SiC VTJFET, shown in Fig. 2.1, was introduced commercially in 2008 by Semisouth Laboratories. Semisouth Laboratories is no longer existing but other companies such as Infineon and United Silicon Carbide (USCi) are developing SiC JFETs. The normally-ON VTJFET (depletion-mode) has better performance than the normally-OFF (enhancement-mode) version due to its lower ON-resistance and its higher saturation current.

The SiC JFET (as the SiC MOSFET) is able to operate in reverse conduction which allows the device to operate in a bridge leg without a freewheeling diode. The so-called diodeless operation of SiC JFET was proposed by Ållebrand and Nee in 2001 [4]. It was experimentally proven in [5] and [3] for SiC LCJFETs and SiC VTJFETs, respectively.

Due to the normally-On characteristic of the SiC JFET, the design of the gate driver has to be made very carefully in order to avoid shoot-through. In fact, if a gate-driver failure occurs, the device will stay on. Due to this reliability issue, the
SiC JFET is less attractive for industrial and commercial applications. Peftitsis et al. have presented a solution to this problem together with a start-up solution in [6]. The proposed driver is self-powered and handles the short-circuit current at start-up.

**Bipolar Junction Transistors (BJTs)**

4H-SiC BJTs have the following advantages: low on-resistance (i.e., low conduction losses), fast switching, and high-temperature capability [7]. High common-emitter current gain is required since BJTs are current-controlled devices. The SiC BJT is easy to connect in parallel since its ON-resistance has a positive temperature coefficient along with that the current gain decreases with temperature. Parallel-operation of SiC BJTs has been successfully presented in [8] where the realized 6 kW, 200 kHz DC/DC boost converter with 4 parallel-connected discrete SiC BJTs exhibits a total efficiency of 98.23%. However, to improve the current gain of SiC BJTs the surface recombination on the SiC surface has to be suppressed [7,9]. The cross section of a SiC BJT is illustrated in Fig. 2.2.

The main drawback of SiC BJTs is the bipolar nature that requires a constant base current applied to its base. Moreover, the need to have a parallel Schottky diode makes the SiC BJT less attractive compared to the SiC JFET and SiC MOSFET.

![Cross-section of a SiC BJT](image)

**Figure 2.2: Cross-section of a SiC BJT.**

**Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs)**

The SiC MOSFET is the latest SiC power device that was released on the market in 2010 by Cree Inc. (now Wolfspeed). Several issues related to oxide quality, channel mobility, and material defects had slowed down its commercialization. As a normally-OFF and voltage-controlled device, the SiC MOSFET is an excellent candidate for future power electronic applications. Considering the growing interest for this device, this thesis work has focused mainly on reliability aspects concerning the SiC MOSFET.
2.3. RELIABILITY ASPECTS

In the first generations of SiC MOSFETs, the oxide layer of the $SiO_2 - SiC$ interface suffered from poor quality. Another issue was the reliability of the SiC body diode. Both issues are discussed in Section 2.7. After two generations of devices (for ROHM Co., Ltd) and three generations for Wolfspeed, significant improvements are noticeable. The devices available today are the SiC DMOSFET (c.f Figure 2.3) and the SiC trench MOSFET recently introduced by ROHM Co., Ltd. Finally, power modules based on several parallel-connected SiC DMOSFET dies (with or without Schottky diodes in parallel) are available from both manufacturers. Other manufacturers such as Mitsubishi, Infineon, and General Electric (GE) are also developing SiC MOSFET devices. However, most of this work has been performed utilizing devices from Wolfspeed and ROHM Co., Ltd. covering all generations.

Figure 2.3: Cross-section of a SiC DMOSFET.

2.3 Reliability Aspects

In this thesis work, the reliability has been treated from different points of view - from a system point of view as well as a device point of view. From a system point of view, one can design reliable systems when understanding the device failure mechanisms. Therefore, there is a need to analyze the reliability from a device point of view first. In fact, a better understanding of the failure mechanisms and device limits allow the design engineer to "build for reliability". Thus, the designer may have to compromise between performance and reliability. The reliability tests have pointed out several issues and feedbacks to manufacturer certainly helps pushing towards reliable high performance devices. Finally, as all new technology, SiC devices has not been "in the fields" for a long time. Therefore, showing that the early material failures and failure modes have been overcome is also a way to prove the robustness of SiC.

In this work, the focus was on testing different aspect that may compromise the reliability of commercially available SiC MOSFETs for an industrial application. The advantage of SiC MOSFETs in comparison with the other SiC switching
CHAPTER 2. SiC POWER DEVICES AND RELIABILITY ASPECTS

deivces, is the few changes required to replace Si-IGBTs with SiC MOSFETs. Al-
though fewer reliability issues have been noticed for SiC BJTs and Sic JFETs, more
effort with regards to the driver circuits has to be done. In fact, although the JFET
has very low conduction losses in its normally-ON version, the normally-ON char-
acteristics is considered as a potential reliability issue. For the SiC BJT, there is a
need to supply current to the base continuously (driver losses and complexity) and
to have an anti-parallel Schottky diode. Although the SiC MOSFET was the latest
commercially introduced device, it is today the most commercialized device. As a
consequence, the main focus in this work is to investigating whether SiC MOSFETs
are a reliable solution to replace Si-IGBT for the targeted application. However,
Chapter 7 covers the behaviour of all three SiC devices during a short-circuit event
and assess their protection in case of a short-circuit fault.

Another issue that has to be overcome by SiC technology is the comparatively
small chip sizes compared with Si which results in lower current ratings for discrete
devices. Parallel connection of discrete devices or modules populated with several
chips are two ways to overcome this issue. At first, it was not straight forward
that SiC devices could be safely paralleled but this was successfully demonstrated
in [8,10,11] for SiC MOSFETs (c.f Chapter 3), SiC JFETs, and SiC BJTs, respec-
tively. Then the parallel connection of fast-switching devices require low inductive
paths for the current to limit the over-voltages induced by fast current transients.
This is relevant both for the main current paths and the gate connections. As a
consequence, module designs made for Si IGBTs or Si MOSFETs may not be suit-
able for SiC when switching at higher speeds. This is investigated in this work in
Chapter 4.

Another advantage brought by the SiC substrate is the higher temperature
under which the device can operate. However, when introducing SiC, the material
used for the packaging were similar as for Si technology and were not suitable for
high-temperature operation. This is further discussed in Section 2.5. Finally, the
need to be reliable in harsh environment is presented in Section 2.3. Overall, a
better understanding of the failure mechanisms and barriers to the utilization of
the full device potentials lead to research efforts towards the production of devices
with increased reliability and packaging methods using appropriate materials.

The coming subsections will cover an introduction of reliability engineering,
reliability testing, reliability in harsh environment, and failure analysis. The main
purpose is to introduce some notions in order to give a better understanding of the
conducted work and why some methods have been preferred over others.

Reliability Engineering

The purpose of reliability engineering is to provide a guidance on how to
design and build more reliable electronic systems. It is a powerful tool which helps
to ensure that all electronic components are correctly applied, that margins are
adequate, and, that failure mode are prevented during the expected lifetime of the
system. The reliability indicators are the failure rate (FIT - failures in time) for
components and the mean time to failure (MTTF) or mean time between repairs (MTBR) for non-repairable and repairable systems respectively. The FIT rate is the number of times a system fails during $10^9$ hours in operation. The value 1 FIT means one failure in $10^9$ device hours [12]. The elementary relationships between failure rate, failure distribution function, MTTF and MTBR can be found in [13]. The failure rate is defined as

$$\lambda = \frac{n_f}{N t}, \quad (2.1)$$

where $n_f$ is the number of failures; $N$ is the number of components in operation, and $t$ is the monitoring period.

The MTTF value is the mean expected time between two failures and is the reciprocal to the FIT rate. It is calculated as

$$MTTF = \frac{1}{\lambda}. \quad (2.2)$$

In the past, the reliability was only analysed once the product was finished. Nowadays, most companies has understood that the reliability have to be discussed during the design process. This is the context into which this doctoral thesis falls into. The aim of reliability building is to provide A collection of design rules for making a SiC - based product reliable and predictive methods to assess the reliability of the future devices / systems based on design data and models describing the time and stress behaviour of similar products. Therefore, through different focus in this work, a detailed overview of the possible failures modes of SiC devices (in particular SiC MOSFETs) is presented. Design guidelines in order to prevent these failures are also provided. A general understanding of how to design reliable systems with SiC devices is the main outcome of this work. Since power electronic components are composed of a die and a package, one must identify the threats on die-level as well as on the package-level. When a failure risk is identified - through reliability tests - the design guidelines are drawn in order to minimize the risk of failure.

**Reliability Testing**

In reliability testing, two types of reliability data are considered:

- Laboratory tests
- Operational reliability (field data).

The objective of the reliability tests are [12]:

- To ensure general product reliability and quality
- To establish the limits of systems by exposing them to various test conditions
- To ensure process stability and reproducibility of production processes
Laboratory reliability assessment processes are much faster than operational reliability assessment processes and are also good for comparing different devices. These tests are often accelerated which may imply that the accelerating tests do not show the mechanisms dominating in the operating conditions. The laboratory tests can be quantitative or qualitative. Quantitative tests aim to assess reliability indicators for a batch of components in terms of FIT. Qualitative tests (or stress tests) are used to establish the operational limits of the components. The operational limits are translated into failure or drift of a significant electrical parameter. In this work, both qualitative and quantitative tests are considered.

The typical standard tests for Si devices are stated in Table 2.2. Most of these tests are accelerated by application of high temperature. The most popular life-stress relationship used in accelerated life testing is the Arrhenius life-stress model. It relates the failure rate and device junction temperature. Even though a wide range of applications are covered by the standard tests, the superior properties of SiC devices may require specific tests to ensure high reliability under extreme operating conditions [14]. Another solution is to customize the reliability tests with regards to the targeted application. In this work, in a desire to observe failure modes which are not triggered by temperature, no tests are accelerated.
Table 2.2: Standard test conditions for Si MOSFETs, IGBTs, Diodes, and Thyristors.

<table>
<thead>
<tr>
<th>Reliability</th>
<th>Si MOSFETs, IGBTs</th>
<th>Si Diodes, Thyristors</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Temperature Reverse Bias (HTRB)</td>
<td>$1000 \text{ h}$</td>
<td>$1000 \text{ h}$</td>
</tr>
<tr>
<td></td>
<td>$95% \frac{V_{DC(max)}}{V_{CE(max)}}$ $125^\circ\text{C} \leq T_c \leq 145^\circ\text{C}$</td>
<td>$66%$ of voltage class $105^\circ\text{C} \leq T \leq 120^\circ\text{C}$</td>
</tr>
<tr>
<td>High Temperature Gate Bias (HTGB)</td>
<td>$1000 \text{ h}$</td>
<td>not applicable</td>
</tr>
<tr>
<td></td>
<td>$\pm \frac{V_{GS(max)}}{V_{GE(max)}}$ $T_{j(max)}$</td>
<td></td>
</tr>
<tr>
<td>High Humidity &amp; Temperature Reverse Bias (THB)</td>
<td>$1000 \text{ h}$</td>
<td>$1000 \text{ h}$</td>
</tr>
<tr>
<td></td>
<td>$85^\circ\text{C}/85%$ RH $\frac{V_{DS}}{V_{CE}} = 80%$</td>
<td>$85^\circ\text{C}/85%$ RH $\frac{V_{D}}{V_{R}} = 80%$</td>
</tr>
<tr>
<td></td>
<td>$\frac{V_{DS(max)}}{V_{CE(max)}} = \text{max. } 80 \text{ V}$</td>
<td>$\frac{V_{D(max)}}{V_{R(max)}} = \text{max. } 80 \text{ V}$</td>
</tr>
<tr>
<td></td>
<td>$V_{GS}/V_{GE} = 0 \text{ V}$</td>
<td></td>
</tr>
<tr>
<td>High Temperature Storage (HTS)</td>
<td>$1000 \text{ h}$</td>
<td>$1000 \text{ h}$</td>
</tr>
<tr>
<td></td>
<td>$T_{\text{storage(max)}}$</td>
<td>$T_{\text{storage(max)}}$</td>
</tr>
<tr>
<td>Low Temperature Storage (LTS)</td>
<td>$100 \text{ cycles}$</td>
<td>$100 \text{ cycles}$</td>
</tr>
<tr>
<td></td>
<td>$T_{\text{storage(min)}}$</td>
<td>$T_{\text{storage(min)}}$</td>
</tr>
<tr>
<td>Thermal Cycling (TC)</td>
<td>$100 \text{ cycles}$</td>
<td>$100 \text{ cycles}$</td>
</tr>
<tr>
<td></td>
<td>$T_{\text{storage(max)}} - T_{\text{storage(max)}}$</td>
<td>$T_{\text{storage(max)}} - T_{\text{storage(max)}}$</td>
</tr>
<tr>
<td>Power Cycling (PC)</td>
<td>$20,000$ load cycles $\Delta T_j = 100 \text{ K}$</td>
<td>$10,000$ load cycles $\Delta T_j = 100 \text{ K}$</td>
</tr>
<tr>
<td>Vibration</td>
<td>Sinusoidal sweep $5 \text{ g}$ $2 \text{ hours per axis (x,y,z)}$</td>
<td>Sinusoidal Sweep $5 \text{ g}$ $2 \text{ hours per axis (x,y,z)}$</td>
</tr>
<tr>
<td>Mechanical Shock</td>
<td>Half sine pulse $30 \text{ g}$ $3 \text{ times each direction (±x, ±y, ±z)}$</td>
<td>Half sine pulse $30 \text{ g}$ $3 \text{ times each direction (±x, ±y, ±z)}$</td>
</tr>
</tbody>
</table>
When testing a semiconductor device, a faulty component can be defined in various ways. For silicon MOSFETs devices, Semikron [12] defines a component as faulty when the following drift in parameters:

- ON-resistance / saturation voltage : $+ 20\%$ of the value before testing
- Max. change in threshold voltage : $\pm 20\%$ of the limits
- Gate leakage current : $+ 100\%$ above the upper limit
- Drain-source current : $+ 100\%$ above the upper limit.

For Si IGBTs, the failure criteria are:

- Breakdown voltage : $\pm 20\%$ change
- Leakage current ($I_{DSS}$) : $> 500\%$ increase
- Reverse gate leakage current : $> 500\%$ increase
- Forward voltage drop : $> \pm 20\%$ change
- Current gain : $> \pm 20\%$ change.

In conclusion, when testing semiconductor devices one has to specify what are the test criteria and the limits after which the device is considered as 'failed'. In this work, the tests performed are laboratory tests, but no test will be accelerated by high temperature.

**Failure Analysis**

When testing for reliability, it is important to determine, once the device has failed according to different criteria, the root/cause of the failure. Failure analysis is the most important element of the reliability assessment. It aims to identify the failure mechanism and, eventually, to model the dependence of the failure mechanism on stress and technological factors. After the failure symptoms are identified, the failure analyst must discover the root/cause of the failure since it is only after identifying the failure cause that measures can be taken in order to avoid that failure or improve the component(s). Failure analysis is often time consuming and costly. One should also clearly differentiate if a failure is due to manufacturing errors or design deficiencies.
2.3. RELIABILITY ASPECTS

Package and reliability

The package for power electronic semiconductors is either made of plastic (non-hermetic) or of metal or ceramic (hermetic). Nowadays, most of the packages are made of plastic, mainly for economic reasons.

An important factor for the electrical characteristics of the die is the ion contamination due to the moulding material which may lead to the formation of an immersion layer at the surface of the die. The electrical characteristics of the devices are degraded by this process. The package must withstand ambient temperature and are either hermetic or not. When moisture penetrates into the package it can reach the die (corrosion) or it may dilate the moulding material. The package should also withstand the given rated temperature depending on the application.

When used in a final product, the devices can be exposed to different kinds of environmental stress. These stresses are stipulated in EN 60721-3 [12] and illustrated in Fig. 2.4. In order to design a reliable system, one must identify all the environmental conditions that can occur in the field application and include them in the design process of electrical products. This also means that the selection of the suitable power semiconductor devices has to be done accordingly. This also concerns the cooling system and the assembly.

The conditions of storage, transportation to the final place of use, and the conditions during down-time also have to be taken into account and iteratively combined with protection measures against environmental impacts. Finally, the best compromise between the component, circuitry and design complexity must be found while taking into account commercially available semiconductors. The intrinsic semiconductor limits or specific device limits (moisture absorption, temperature limit, ... ) have to be taken into consideration as well.

The circuitry design of power modules consisting of a high number of dies connected in parallel (often in a half-bridge configuration) has to be realized carefully. For Si devices, operation frequency range did not require particularly severe margins with regards to the internal stray inductances and capacitances inside the module housing. For SiC, the possibility of operating at higher frequency requires low-inductive designs when high switching speeds are targeted. Up to recently, the commercially available SiC modules (MOSFETs) where packaged in housing designs for Si IGBT dies. This is assessed in Chapter 4.

The humidity stress on SiC MOSFET power modules discussed in Section 2.4 is investigated in this work in Chapter 6. It has been identified as one of the major environmental impacts for the application considered in this work. High relative humidity combined with temperature can cause corrosion of the semiconductors. The factors affecting corrosion are various. For the substrate, they depend on the structure, the composition, and the moisture absorptivity. For conductors, the nature of the material, the surface roughness, the spacing between two conductors and the conductor configuration affect corrosion. Temperature acts as an increasing factor. Corrosive gases present in the air have an impact on corrosion.
Humidity is a critical parameter for a plastic package. It can be absorbed the moulding compound or at the interconnection between the leads and the plastic package. However, plastic packages are cheaper than metal packages. Moisture needs to be combined with ionic contamination to create corrosion in a package. Thus, the threat for semiconductors is that the moisture reacts with ionic contamination and creates a solution that can chemically react with the metallization. A second threat is that the moisture absorbed by the plastic damages the package itself.

Issues concerning the reaction with the wafer can be avoided by reducing phosphorous levels in passivation because it creates phosphorus acid in contact with oxide, controlling ionic passivation in final wafer processing, and minimizing the presence of cracks by adopting a suitable top layer process. Choosing a top side metallization suiting the present technology (SiC) is also a part of the solution.

In operation, the dissipated power increases the temperature of each component which in particular decreases the relative humidity. Thus, the components that operate intermittently are subject to typical failures caused by humidity and mechanical stress caused by rapid change of temperature (due to different temperature coefficient of the die, the metallisation and of the package). For components operating under the same environmental conditions, if one operates at an over-temperature of 10 °C (due to self-heating), it has been reported that the lifetime may be increased 10 times [13].
2.4 Reliability of SiC Power Devices in Humid and Harsh Environment

Humidity and moisture can deteriorate the ohmic contacts of the SiC semiconductors due to chemical reactions with the metallization when exposed to high temperature and oxygen-rich environments. Very little work has been performed on SiC power transistors operating in humid environments. However, in [15], 4H-SiC MOSFETs with a stable protecting coating for harsh environment applications are presented. The presented solution consists of a stacked ONO gate dielectric and Ti/TiN/Pt/Ti interconnect together with Ti ohmic contacts in combination with a-SiOx/a-SiC coating. Autoclave tests have been successfully completed by those devices up to 220 °C. Power Cycling test up to 700 °C and long term aging up to 600 °C were promising as well. This demonstrates that solutions toward a higher reliability against humidity and moisture are possible and are being investigated. In SiC, compared with Si, the junction terminations (for all device types) are exposed to higher electrical fields while the substrate is thinner. This results in a higher stress. Infineon and Cree have investigated the impact of humidity on SiC Schottky diodes [14,16,17]. The impact of humidity on SiC MOSFETs may be similar to the impact observed on SiC schottky diodes but the author believes that there is still a need to investigate this specifically. Moreover, the deterioration of the oxide layer due to humidity cannot be excluded at this stage. However, this will not be investigated in this work.

SiC devices are, as Si devices, tested when they leave production by the device manufacturers. Doing so, the batches sold commercially are free from defects. The SiC devices are often stressed in a similar manner as Si devices. The two standard tests for humidity are the 85 °C/85 % relative humidity test and the autoclave test [12]. In the 85 °C/85 % test, the devices are exposed to 85 % humidity at 85 °C for a total of 1000 h and under a bias of maximum 80 V [12]. This is a comparably low voltage for high-power applications. For Si IGBTs it was shown that it was obsolete [18] for high-voltage devices as high bias accelerates the humidity-induced degradation significantly. The humidity-induced corrosion mechanisms for power semiconductors are electromechanical migration and aluminum corrosion [19].

In multichip power modules, moisture is able to enter the non-sealed housing. The moisture reaches the chip and its passivation layer through the silicone gel. From this point of view, the most critical region for power semiconductors is the junction termination (see [20] for Si IGBTs). Even though these tests are sufficient for the state-of-the-art industry standard, the author believes that, SiC devices may react in a different way with regards to humidity than Si. First, the electric field applied to its junction termination is considerably higher compared to Si devices. Ion contamination can thus be more severe for SiC than for Si, resulting in an accelerated degradation process. Secondly, the aforementioned tests are 'accelerated' by high temperature. This might trigger fault mechanisms that are not related to humidity but to high temperature. Therefore, a non-accelerated humidity test
has been performed in this work. Accordingly, the test duration has been 1 year (approx 8000 h) instead of the standard of 1000 hours.

### 2.5 Thermal Stability of SiC devices

This section focuses on reliability issues common to all SiC power devices. Even though SiC remains solid up to 2370 °C, the actual maximum temperature of SiC devices is much lower [21–23]. The major limiting factor is the thermal runaway, as described in [24]. At the thermal runaway temperature, the device is no longer capable to block its rated blocking voltage because the intrinsic carrier density becomes higher than the maximum doping level sustaining a given voltage.

The second issue is that SiC-based devices also require other materials for the final product such as the metal for the contacts and the packaging. At first, materials used in Si technology were used when producing SiC-based devices, limiting the use of the whole SiC potential towards high-temperature operation. An example of the difference in maximal temperature among the different elements in the device package is given in Table 2.3. The latter shows that the manufacturing technology has to be adapted to SiC. However, recent efforts are made to address these issues [25].

<table>
<thead>
<tr>
<th>Material</th>
<th>Max. Temperature [°C]</th>
<th>cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Semiconductor</td>
<td>SiC</td>
<td>2730</td>
</tr>
<tr>
<td>Schottky metal</td>
<td>Ti</td>
<td>1668</td>
</tr>
<tr>
<td>Top metallization</td>
<td>Al</td>
<td>660</td>
</tr>
<tr>
<td>Secondary passivation</td>
<td>polyimide</td>
<td>500-620</td>
</tr>
<tr>
<td>Contact Anneal [25]</td>
<td>Ti/Ni</td>
<td>350-500</td>
</tr>
</tbody>
</table>

### 2.6 Reliability of SiC Power Devices against Cosmic Rays

Cosmic rays are high radiation energy that can lead to spontaneous failures in the blocking mode of a device. These particles may collide with the cores of silicon atoms. For Si, the design guidelines are to limit the electric fields at the pn-junction to a safe value with respect to the breakdown electric field. For SiC, these electric fields are approximately ten times higher but the impact ionization rates are lower. However, as the physical volume with high field strength is ten time smaller in SiC compared to Si, the probability of a collision in that zone is smaller. As mentioned in [26], the failure rate for cosmic rays is increased for 600 V SiC devices compared to Si. For the 1200 V devices, the failure rate is decreased. This has been recently confirmed by [27] for 1200 V and 1700 V SiC MOSFETs and SiC Schottky diodes. This reliability issue has not been covered by this thesis work.
mainly due to the fact that Cosmic Rays have not been perceived as an issue for
the targeted applications surrounding this project work but also due to the focus
on other reliability aspects that seemed more relevant at the time of the project
pre-study.

2.7 Reliability of SiC power MOSFETs

The following section covers some aspects of reliability of SiC power MOS-
FETs. The aspects considered here do not cover every failure mode of the SiC
MOSFET. However, they are only visible in SiC MOSFETs (and not common to
all devices). Since the MOSFET is the device which was, and is foreseen to be, the
device of choice when replacing Si IGBTs by SiC switching devices, some of these
issues are investigated in this work.

Reliability of the gate-insulating layer

As oxide is used as gate-insulating layer in SiC power MOSFETs, its reliability
directly affects the reliability of the SiC MOSFET. However, by a combination of
an appropriate oxide growth process and device structure, a high-quality oxide has
been achieved. Recently, Rohm and Cree (Wolfspeed) claimed that their oxide layer
is as reliable as those of Si MOSFETs [28]. The assessed lifetime for a gate-source
voltage of 20 V is ten million hours (Cree/Wolfspeed). However, even with a high-
quality gate insulating layer, there might still remain crystal defects that may cause
initial failure.

The stability of the gate-oxide when exposed to negative bias for a prolonged

time (1000 h) is discussed in Section 2.7 and investigated in Chapter 5.

High junction temperature operation - reliability issue

As a direct consequence of that the development of SiC power devices was
partly based on the existing Si-technology, long-term high junction temperature op-
eration of SiC power MOSFETs may be associated with reliability problems. Several
groups address the issue and some interesting results were presented in [29,30,30,31].
In [29], it was shown that the MOSFET can reach steady-state conditions for junc-
tion temperatures as high as 250 °C which is higher than for comparable SiC JFETs.
This is due to the fact that the channel resistance represents a significant portion of
the total device resistance and that it decreases with increasing temperatures due to
the charge trapping effect in the channel. In [30], five different problems and poten-
tial threats of high-temperature operation are discussed: (1) interlayer dielectric
erosion, (2) aluminum spearing to the poly-Si gate, (3)Ni2Si contact disappearance,
(4) electrode delamination, and (5) gate time-dependent dielectric breakdown. Most
of these reliability issues can be improve by a proper selection of the material used
for the metallization, passivation layers and packaging of SiC MOSFET devices.
High-temperature of operation of the SiC MOSFET is not covered in this work. However, the ruggedness of SiC MOSFETs against surge currents may partly be dependent on the ability of the gate oxide to withstand high temperatures. This aspect is covered in Chapter 7 where a thermo-electrical simulation has been developed. It was shown that the location of the hot-spot during a short-circuit fault is extremely close to the gate oxide. For that reason, it is relevant to ensure that the gate oxide of SiC MOSFETs is resistant to high temperatures, even when high-temperature operation is not targeted.

Stability of the gate threshold voltage

When a continuous positive gate voltage is applied for an extended period of time, electrons can be trapped at the interface between the gate insulating layer and SiC body. This mechanism increases the threshold voltage. The shift for 1.2 kV Rohm devices is 0.2-0.3 V after 1000 hours operating at 100°C and $V_{gs} = 22$ V \[32\]. Once the traps are filled, the threshold is fixed.

When a continuous negative voltage is applied to the gate for an extended period of time the threshold voltage drops due to trapped holes. When $V_{gs} = -10$ V, the deviation from the original threshold is approximately 0.5 V (1.2 kV Rohm devices). However, in normal operation, as the gate voltage alternates between positive and negative bias, charges and discharges make it unlikely to obtain any significant changes in the threshold \[32\].

In this work, the stability of 1.2 kV SiC MOSFETs against negative bias voltage at room temperature is investigated in Chapter 5.

Reliability of body diodes

The reliability of the SiC MOSFET is known to be affected by the degradation caused by the conduction of its body diode \[33\]. If forward current is continuously applied to the body diode, a crystal defect called stacking fault may grow due to the hole-electron recombination energy. These faults are progressively blocking the current path which results in an increased ON-state resistance as well as an increased forward voltage of the body diode. An increase of the leakage current in blocking mode is also observed \[33, 34\]. The increased forward losses and blocking losses affect the thermal design. Moreover, there is also a correlation between degradation of the body diode and an increase of $R_{ds(on)}$. For these reasons, for circuit topologies where the body diode conducts a significant current, it is important to use a device free from stacking faults.

Short-circuit ruggedness

The short-circuit capability of SiC MOSFET devices has been reported in \[35, 36, 36–38\]. The reported reason of failure is that the chip reaches local temperatures beyond the melting point of aluminum. However, the short-circuit robustness might
also depend on the manufacturer and the fabrication process of the devices. It is also reported that the failure is due to gate failure or gate weakness since the gate leakage current increases just before the failure, which is probably due to heat spreading in the device which may lead to the destruction of the gate oxide. Finally, the short-circuit robustness is dependent on the gate-voltage and the voltage across the device during a short-circuit event.

Even though short-circuit robustness of SiC devices has been widely documented, very little has been done on SiC MOSFET protection against short-circuit failure. In this work, the early stages of a short-circuit event have been investigated both with experiments and electro-thermal simulations. The latter are discussed in Chapter 7.

Finally, the effect of repetitive short-circuit events on SiC MOSFETs is described in [38]. The degradations observed are an increase of the ON-state resistance and of the gate leakage current. Chapter 7, provides an extended analysis of the short-circuit behaviour of SiC devices. For SiC MOSFET, an additional analysis describes the effect of the circuit parameters on the heat spread in the device.

Over-voltage capability

The failure modes of the SiC power MOSFET under avalanche conditions are current failure due to the biasing of the parasitic NPN BJT transistor, localized impact ionization, or temperature failure due to thermal runaway. The voltage required to trigger the NPN BJT transistor is of 3 V for SiC MOSFETs (0.7 V for Si). This voltage decreases with an increase of temperature by 2 mV/°K [37]. Unclamped voltage tests show that the SiC MOSFET is very rugged and is able to sustain high avalanche currents.

2.8 Reliability of SiC Power BJTs

SiC BJTs have very low ON-state resistance, short switching times and high temperature capability. As the device is current controlled, the maximum collector current is dictated by the base-current provided by the base-drive circuit. Therefore, losses in the base-drive circuit have to be considered. As a result, the driver design is more complicated for SiC BJTs compared with unipolar SiC devices. This has been considered as an issue from an industrial application point-of-view.

Bipolar Degradation of SiC BJTs

All bipolar devices in SiC can potentially suffer from bipolar degradation. These faults in the SiC crystal structure are activated by the bipolar operation mode and spread through the device. This mechanism is destroying the active area [7]. As a result, under forward bias stress at high current densities, the forward voltage drop $V_{cesat}$ and the current gain are degraded [39]. In [7], A. Lindgren and M. Domeij have presented a 1200 V - 50 A fast-switching BJT free from defects
causing bipolar degradation. The degradation was eliminated by buffer layer design and use of material with a low concentration of basal-plane dislocations (BPD).

Second Breakdown

Si BJTs suffer from second breakdown, which make them unable to withstand short-circuit faults. This issue does not concern SiC BJTs. They have been proven to be free of second breakdown even under high turn-OFF power densities ($3.7 \text{ MW/cm}^2$). This is due to the 100 times higher required current densities for second breakdown in SiC compared to Si [40].

2.9 Reliability of SiC Power JFET

Due to its simplicity, the SiC Power JFET is free from issues related to oxide quality (since it is free from oxide) and from bipolar degradation (as it is a unipolar device). However, the normally-ON version is not favorable for industrial applications for safety reasons. Solutions to the normally-ON problem have been realized in [6, 41].

Another issue brought by the SiC JFET is the so-called "Gate punch-through stability" which can result in a loss of gate control. The two main parameters that should be taken into account in order to control the gate of the SiC JFET are $V_{TO}$ and $V_{PT}$. $V_{TO}$ is the minimum negative gate-to-source voltage required to block the device. $V_{PT}$ is the limit gate-to-source voltage after which the gate current exceeds the gate driver capabilities. [21]. To ensure a safe operation, the difference between $V_{TO}$ and $V_{PT}$ should be large. However, a solution is to increase the negative supply voltage of the driver to a voltage lower than the initial punch-through voltage and to use a gate resistor to limit the current supplied to the gate. This has been realized in [42] with a "so-called" $DR_{p}C$ parallel network. It should be noted that LCJFETs are more prone to this effect since their punch-through voltage is more sensitive than the punch-through voltage of VTJFETs [6].

Short-Circuit ruggedness of SiC JFETs and Repetitive Surge Current and Overvoltage Capability

Analyses of the short-circuit ruggedness of normally-OFF SiC JFETs have been presented in [35], where the surge current under a direct voltage of 400 V and 600 V is investigated, respectively. The devices could withstand a short-circuit for 1.44 ms and 1.17 ms, respectively. The SiC JFET is thus the most robust SiC active device. For normally-ON JFETs, similar results have been presented in [43, 44]. Besides their excellent behavior under short circuit, SiC JFETs are able to have a current limitation regime even at temperatures as high as 350 °C. Also, due to variations of the carrier mobility at higher temperatures, the saturation current is lower for higher temperatures [43]. The SiC JFET can withstand repetitive short-circuits for limited durations of short-circuit events. In [44], repetitive over current
pulses of 200 $\mu$s have been applied under a direct voltage of 540 V. The device failure occurred after 88'336 short-circuit events. The result was a loss of gate control. The degradation indicators where an increase of the ON-state resistance $R_{ds,on}$ and an increase of the internal gate resistance $R_{gs}$.

Avalanche breakdown of SiC JFETs has been investigated in [45] where the avalanche breakdown and energies have been measured for different values of the gate-source voltage. It was observed that there is a dependence of the blocking voltage on the negative gate bias.

2.10 Reliability of SiC Power Diodes

The SiC Schottky diode is by far the most investigated SiC device so far. Many of the devices have already been operating for several years, and the experiences are generally very good. Today, one may even claim that the SiC Schottky diode outperforms many Si devices in several aspects of reliability. In [14], several aspects of reliability of SiC Schottky diodes have been investigated. These aspects include material related, design related, and package related reliability issues. From an over-current and over-voltage handling point-of-view SiC Schottky diodes are more reliable than most Si devices. According to estimations from the number of delivered devices and reported failures, the authors estimated that the 2\textsuperscript{nd} generation of SiC Schottky diodes from Infineon had operated in applications without faults for a total of 25 GHours. The conclusion is that if SiC Schottky diodes are used in conjunction with other SiC devices, the efforts for increasing the reliability of the system should not be focused on the SiC Schottky diodes, but on the other devices. The reliability of SiC Schottky Diodes is not covered in this work. A potential issue is the junction termination that may be sensitive to humidity. This issue is investigated in this work on SiC MOSFET modules containing SiC Schottky dies.

For high-voltage applications, the SiC PiN diode is considered since it can block very high voltages. The degradation of SiC PiN diodes is characterized by a rapid increase in the forward voltage with operation time. This degradation is associated with an increase of stacking faults and their extent in the active region of the device. The production and expansion of these stacking faults in 4H- and 6H-SiC is created by electron-hole recombination. The degradation occurs under forward biasing only because it results in minority carrier injection and in an increase in the rate of electro-hole recombination. This effect is similar to recombination-induced dislocation glide [21]. It is self-limiting and reaches saturation and can also be reversed by annealing.

2.11 Conclusion

A general overview of the presented issues for SiC power devices is presented in Table 2.4. The conclusion from this chapter is that future SiC power devices are likely to be more reliable than state-of-the-art silicon devices. The main reason for
Table 2.4: Key reliability issues for SiC power semiconductor devices.

<table>
<thead>
<tr>
<th>SiC Devices</th>
<th>Key reliability issues</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET</td>
<td>Oxide layer stability</td>
</tr>
<tr>
<td></td>
<td>$V_f$ degradation</td>
</tr>
<tr>
<td></td>
<td>$V_{th}$ stability</td>
</tr>
<tr>
<td></td>
<td>Short-circuit ruggedness</td>
</tr>
<tr>
<td></td>
<td>Humidity</td>
</tr>
<tr>
<td>BJT</td>
<td>Stacking Faults</td>
</tr>
<tr>
<td></td>
<td>Current gain degradation</td>
</tr>
<tr>
<td></td>
<td>Special gate drive</td>
</tr>
<tr>
<td></td>
<td>No reverse conduction</td>
</tr>
<tr>
<td></td>
<td>Humidity</td>
</tr>
<tr>
<td>JFET</td>
<td>Normally-ON</td>
</tr>
<tr>
<td></td>
<td>Special gate drive</td>
</tr>
<tr>
<td></td>
<td>Short-circuit ruggedness</td>
</tr>
<tr>
<td></td>
<td>Humidity</td>
</tr>
<tr>
<td>PiN Diode</td>
<td>Stacking Faults</td>
</tr>
<tr>
<td></td>
<td>Sensitive to material defects</td>
</tr>
<tr>
<td></td>
<td>Humidity</td>
</tr>
<tr>
<td>Schottky Diode</td>
<td>Cosmic Rays</td>
</tr>
<tr>
<td></td>
<td>Humidity</td>
</tr>
</tbody>
</table>

this is that SiC devices have greater margins than silicon devices with respect to all potential failure modes. For currently available SiC devices, i.e. devices that could be purchased and used in this thesis work, the following conclusions have been drawn:

- The short-circuit ruggedness is higher for SiC components than for Si components.
- SiC devices are reportedly rugged against over-voltages.
- SiC devices (>1.2 kV) are expected to be more rugged than Si devices with respect to cosmic ray failure.
- SiC devices have greater margins with regards to high-temperature operation provided that the packaging can withstand these high temperatures.
- The SiC body diode has improved but its reliability still has to be investigated.
- The gate insulating layer may be as reliable for SiC MOSFETs as for Si MOSFETs with a $V_{gs}$ within the datasheet limits.
- The operation in humid environments still has to be investigated.
2.11. CONCLUSION

This work has assessed several of the aforementioned reliability concerns. The parallel connection of SiC MOSFETs is investigated in Chapter 3. The impact of the gate-loop stray inductance on the gate oxide is covered in Chapter 4. Chapter 5 discusses the long-term tests on the body-diode and on the threshold-voltage stability. The operation of SiC power modules (MOSFETs) in humid environment is presented in Chapter 6. The only work covering all the device types is presented in Chapter 7 where the short-circuit behaviour of three types of SiC switching devices (MOSFET, JFET, and BJT) is covered extensively. As the body diode of the SiC MOSFET suggests the possibility to operate in a diode-less manner, an additional work investigating its ruggedness against surge currents is presented in Chapter 8. Finally, a reliability analysis investigating the efficiency improvement and loss reduction when replacing Si IGBTs with SiC MOSFETs has been performed and is presented together with a life-cycle cost analysis in Chapter 9.
Chapter 3

Parallel Connection of SiC MOSFET discrete devices

The information presented in this chapter is based on Publication I.

3.1 Introduction

In recent years a dramatic improvement of both material properties and fabrication processes for silicon carbide (SiC) power semiconductor components has been observed. Currently, several types of power transistors in SiC are available on the market. Common to all these components is that the chip sizes are still small compared to their silicon counterparts. This means that in order to achieve high current ratings, several chips have to be connected in parallel, either as separate components or in a multi-chip module. Several attempts to achieve this have already been presented [46, 47]. However, at the time this work was initiated, many details regarding these issues were still uncertain, especially issues regarding transient mismatches. For SiC junction field effect transistors (JFETs) detailed investigations regarding parallel connection have been presented in [11, 48]. For parallel-connected metal-oxide semiconductor field-effect transistors (MOSFETs) in SiC, however, only little had been presented. One particular point of interest is the fact that the threshold voltage of the SiC MOSFETs available on the market has a negative temperature coefficient. The question is if this property could have adverse effects on static and transient currents sharing. In [49] switching transients of SiC MOSFETs have been presented, and in [50] parallel-connection issues have been treated. The turn-ON transients of paralleled SiC MOSFETs reported in [50] are, however, quite oscillative. It is the opinion of the authors of the present paper that these waveforms could be improved without losing switching speed. This is demonstrated in this work. Additionally, in [50] it is stated that small imbalances in the stray inductances may introduce severe mismatches in the individual currents of parallel-connected SiC MOSFETs. This work, on the contrary, demonstrates that
if the circuit is reasonably symmetrical, very good transient current sharing and low switching energy losses may be obtained, even if the parallel-connected SiC MOSFETs have different characteristics. It has to be noted that the SiC MOSFET parallel connection is done using a standard totem-pole driver. In that sense, no particular design is required for the gate driver, besides minimizing the stray inductance between the devices and the driver - as well as symmetrical paths.

This work presents static current sharing of parallel connected discrete SiC MOSFETs, dynamic current sharing. To conclude this analysis, a dc/dc boost converter has been built with parallel-connected SiC MOSFETs as main switch.

3.2 Methodology

The performance of the parallel connection of two SiC MOSFETs, has been measured. At first, static performance is measured and then a double-pulse test is executed to analyze the switching performance of the parallel-connected MOSFETs. The main parameters of the Cree CMF20120 SiC MOSFET used are listed in Table 3.1. It has to be noted here that this MOSFET device is from the first generation of SiC MOSFETs available for purchase. The static current sharing of

<table>
<thead>
<tr>
<th>$V_{DS}$</th>
<th>$I_{d,max}@25\text{ deg C}$</th>
<th>$I_{d,max}@100\text{ deg C}$</th>
<th>$R_{DS(on)}$</th>
<th>$V_{GS(typ)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1200 V</td>
<td>42 A</td>
<td>24 A</td>
<td>80 m$\Omega$</td>
<td>20 V</td>
</tr>
</tbody>
</table>

the two parallel MOSFETs is investigated by means of a static test. The two MOSFETs under test are mounted on a common heat sink and current is fed through them using a current source. The gate signal is common to both MOSFETs and is supplied by a current-limited voltage source as shown in Fig. 3.1. At regular intervals of 3 minutes $I_1$ and $I_2$, i.e. the currents flowing through M1 and M2, are measured as well as their common drain-source voltage, $V_{DS}$. The case temperatures of M1 and M2 are also measured using an infrared thermal camera. The average case temperatures ($T_1$ and $T_2$) are then derived from the image by using software provided by the manufacturer of the infrared thermal camera, as shown in Fig. 3.2. The test is performed with three values of shared current : 10 A, 20 A, and 25 A. To study the switching performance of the parallel-connected devices, several devices have been sorted with regards to their on-state resistance and their threshold voltage. They have been tested in four different pairs to investigate if the current sharing is still acceptable even with most different device characteristics. In this work, the ON-state resistance is measured at a gate voltage of 24 V. The circuit layout of the double pulse test (DPT) is shown in Fig. 3.3. The driver used is a resistive totem-pole with a gate resistance of $R_g = 0.56\ \Omega$. As the SiC MOSFET used in this study has an internal gate resistor of 5 Ω, the total gate resistance is then of 5.56 Ω. The DPT was performed using a direct voltage of $V_{DC} = 600\ \text{V}$, with an inductance $L = 200\ \mu\text{H}$, and the SiC Schottky diode D
3.2. METHODOLOGY

SDP30S120 from Cree. The gate driver was supplied with -5 V and 24 V. In order to validate the safe realization of the parallel connection in steady-state operation, a dc/dc boost converter is built. The converter has a nominal input power of 6 kW and the switching frequency is chosen to be 100 kHz. The parameters of the dc/dc boost converter are presented in Table IV. The switch is made of parallel-connected CMF20120 Silicon Carbide Power MOSFETs from Cree 1200 V/33 A ratings and a SPD30S120 SiC Schottky Barrier Diode with ratings 1200 V/30 A from Semisouth. The MOSFETs are controlled by the same driver which was used to perform the DPT. The inductor is designed with a PM 74/59 core with Litz wire and has been made in order to minimize the resistive and magnetic power losses [51]. The final prototype of the boost converter is shown in Fig. 3.4.
## 3.3 Static Characteristics

The resistance of a SiC MOSFET is divided in three parts: (a) the channel resistance $R_{CH}$, the JFET region resistance $R_{JFET}$, and the drift layer resistance $R_{drift}$ [50]. While $R_{JFET}$ and $R_{drift}$ have a positive temperature coefficient, $R_{CH}$ has a negative temperature coefficient. At temperatures below 50 °C, the change of $R_{CH}$ is dominant compared to the other two resistance components. As a result, the total ON-state resistance of the SiC MOSFET decreases with increasing temperature up to 50 °C. Above 50 °C, $R_{JFET}$ and $R_{drift}$ are dominant which leads to a positive temperature coefficient of the ON-state resistance.

The results obtained for 10 A and 25 A are plotted in Fig. 3.5 and Fig. 3.6, respectively. The evolution of the temperatures ($T_1$ and $T_2$), $V_{DS}$, and the two drain currents ($I_1$ and $I_2$) have also been plotted. $V_{DS}$ as a function of the temperature has also been plotted and is used to calculate the temperature coefficient. Extended results can be found in *Publication I*.

In all three cases, the higher current flows through $M_1$, resulting in a slightly higher case temperature, which is confirmed by the measurements. With time, the temperature in both devices increases until it reaches equilibrium. The stabilization
3.4 DYNAMIC CHARACTERISTICS

ensures that no thermal runaway is to be expected from the current unbalance, the latter being reasonable. The thermal image in Fig. 3.2 confirms the good sharing among the devices.

3.4 Dynamic Characteristics

The switching losses of SiC MOSFETs are affected by the temperature. The threshold voltage of the SiC MOSFET has a negative temperature coefficient which result in a lower $V_{th}$ at higher temperatures. This has an impact on the switching transients. The SiC MOSFET exhibits a better turn-ON when driven fast and hot [52,53]. This is due to the positive coefficient of the $dI_{dt}/dt$ at turn-ON. Due to the same mechanism, the switching loss increase for the turn-OFF. At the turn-OFF, the $dI_{dt}/dt$ decreases with increased temperature. However, the sum of the switching energies remain constant [47].

The dynamic characteristics are investigated in four different cases. All cases can be found in Publication I. The first set of measurement focuses on device with the same threshold voltage and the same ON-state resistance. The complete switching pulse is shown in Fig. 3.7. The two devices are turned-ON and turned-OFF in approximately 20 ns. The device with lower ON-state resistance takes a higher current. The unbalance in current sharing is stable and within 10 %. Very low oscillations in the switching transients have been observed even at high switching speeds.
CHAPTER 3. PARALLEL CONNECTION OF SiC MOSFET DISCRETE DEVICES

Figure 3.5: Static test results for $I_{\text{shared}} = 10$ A.

Figure 3.7: Double-pulse test of case 1.

The second case consists of devices with different ON-state resistances. This case has the worse current sharing at the beginning of the double-pulse test. However, due to the positive temperature coefficient of the on-state voltage drop, the
3.5. BOOST CONVERTER WITH PARALLEL-CONNECTED MOSFETS

3.5.1 Static Test Results

Figure 3.6: Static test results for $I_{\text{shared}} = 25$ A.

Sharing is improved towards the end of the pulse. The latter supports that the sharing is improved once the devices are "heated". This is in accordance with the fact that the ON-state resistance has a positive temperature coefficient at higher temperatures as presented in Section 3.3. The third case investigates devices with different threshold voltages. It was found that the threshold voltage difference does not substantially influence the steady-state current sharing. Finally, the fourth case focuses on devices with both different on-state resistance and threshold voltage. Even though the device characteristics are very different, the sharing is acceptable. For all cases, the turn-ON and turn-OFF times are in the range of 20 ns. As expected, a mismatch in the device characteristics result in different switching losses among the two devices. The ON-state sharing is also deteriorated. However, since the ON-state voltage drop has a positive temperature coefficient at higher temperatures, the system is trying to balance the power sharing among the two parallel-connected devices.

3.5 Boost Converter with parallel-connected MOSFETs

The dc/dc converter presented in Section 3.2 has been tested experimentally at rated input current with a resistive load. The recorded electrical quantities are the gate-source voltage $V_{gs}$, the MOSFETs currents $I_{m7}$ and $I_{m8}$ and the drain-source voltage of the parallel-connected devices $V_{ds}$. The currents are measured...
at the source leg of the SiC MOSFET. The electrical measurements are performed using CWT ultra-mini Rogowski coils for the switch currents, Tektronix P5100 high-voltage probe for $V_{ds}$ and a standard low voltage probe for $V_{gs}$. These quantities are shown in Fig. 3.8. The reached output voltage is 560 V and the output power is 870 W. Thus, the semiconductor power losses are 30 W. The input of current is shared between M7 and M8. The sharing is within 20 % as $I_{m7} = 10$ A and $I_{m8} = 8$ A. The 'poor' current sharing is due to the negative temperature coefficient of the channel resistance. The unbalance is clearly shown by Fig. 3.9, where the MOSFET situated on the left side, is much hotter than the one on the right side of the heat sink.

Figure 3.8: Boost-converter waveforms. Gate-source voltage (green 50 V/Div), drain-source voltage (purple 200 V/Div), $I_d$ MOSFET 7 (yellow (5 A/Div), $I_d$ MOSFET 8 (pink (5 A/Div), timebase 2 $\mu$s/Div

Figure 3.9: Temperature distribution Between the parallel connected devices in the boost converter
3.6 Conclusion

From experiments on two parallel-connected SiC MOSFETs, it was found that the relative unbalance in static current sharing was approximately 5%. At elevated temperatures this mismatch was even reduced. From double-pulse tests it was found that the sharing is better when the devices share similar characteristics. However, the devices still have good sharing when they have similar on-resistances even if the threshold voltages are different. Too different values of ON-state resistances are to be avoided. The loss values are, however, very low. The turn-ON waveforms in the present paper have low oscillations even if the turn-ON time was only approximately 20 ns which demonstrates that a simple driver is good enough to drive SiC MOSFETs in parallel. A dc/dc boost converter with parallel-connected MOSFETs was built to verify the steady state operation of parallel-connected devices. It was found that at low temperatures there is a risk of unbalance between the two devices in parallel due to the negative temperature coefficient of the channel resistance below 50 °C.
4.1 Introduction

One solution to achieve high power densities using Silicon Carbide (SiC) is to build power modules populated with SiC dies. Custom modules from various manufacturers have been made for SiC JFETs previously. For SiC MOSFETs, a first version has been made by Cree (now Wolfspeed) with the first generation of SiC MOSFET dies. A second version, based on a standard package already used for Si IGBTs has been released by the same manufacturer with the desire to accelerate the exploitation of SiC power devices in industry applications previously designed using Si IGBTs. Doing so, the SiC technology can be employed with very minor changes which come down mainly to the driver circuits. In fact, since the modules packages are identical, no change in the converter geometry is required although considerable efficiency improvements can be made.

However, the advantages of SiC transistors at the chip level are compromised when using such packages developed for Si technology. The design and packaging issues for such modules are presented in [54]. It was found that the difference in the placement of the switching devices results in a difference in the parasitic inductances for each of the switching devices in the power module. As shown in the previous chapter for discrete and in [55] multi-module based converters, an imbalance in parasitic inductances can lead to imperfections in current sharing during switching transients and steady-state operation. However, for the time being the 'plug-and-play' replacement of Si IGBT modules by SiC MOSFET modules does not necessary require high-temperature operations. Another advantage of SiC is the higher switching speeds which lead to the possibility of operating the converters at higher switching frequencies. Higher switching speeds and lower ringing can reduce the switching losses, which are related to the major components of the overall losses of power converters operating at high switching frequencies [56].
This chapter assesses the impact of the parasitic inductances in the gate loop of the SiC MOSFETs inside a commercially available power module housing, and the impact of these parasitic inductances on reliability. The reason one focuses on the gate loop is that the gate oxide has a greater impact on the lifetime in comparison to the main current path [57].

4.2 Methodology

The investigation was performed in three parts. First an extraction of the the internal parasitic elements of the module was realized using the software ANSYS Q3D. The reconstructed module is shown in Fig. 4.2. The extracted parasitic elements where then used to implement an electrical simulation model. To validate the model, experimental measurements were performed first at the module terminals and then inside the module directly on a chip. Doing so, a detailed verification of the accuracy of the model is obtained. The validated model is finally used to investigate and discuss the impact of the gate-loop inductance on the reliability of the SiC MOSFET in the selected power module.

4.3 Modeling and Equivalent Circuit

The investigated module is the commercially available 1.2 kV/300 A power module from Wolfspeed (CAS200M12BM2). It is a half-bridge SiC power MOSFET module using a standard 62-mm package. Fig. 4.1 shows the Q3D model of the CAS200M12BM2 and Fig. 4.2 shows the top view of the same model. The parasitic elements are then extracted from the module reconstruction by ANSYS Q3D. The module with the extracted parasitic elements is then simulated in LTSPICE. Fig. 4.3 gives a simplified example of how the module looks like in the electrical simulation model. The chip model (C2M0025120D) used for the simulation in LTSPICE was provided by the device manufacturer. The chips 1-6 as well as the Schottky diodes 1-6 are situated in the lower switch position of the half bridge. Similarly, chips 7-12 and Schottky diodes 7-12 are situated in the upper switch position of the module. From Fig 4.2 it is clearly visible that the distances from the chips to the gate of the module are very different for the upper and lower switch positions. As a result, the gate-loop inductance is approximately 3-4 times higher for the chips situated in the lower switch position compared to the ones situated in the upper switch position. This issue has already been observed in [58].

4.4 Experimental Verification of the Model

Two tests are performed to verify the electrical simulation model (c.f Figure 4.3). The first one is a standard double-pulse test (DPT) and the second is a single-pulse test. In both cases the measured switch position is the lower one. In the DPT, the drain and gate voltages $V_{ds}$ and $V_{gs}$ are measured at the corresponding
module terminals whereas in the single-pulse test, the same voltages are measured directly on the chip as in Fig. 4.2.

In both the simulations, the stray inductance $L_{g,\text{stray}}$ corresponds to the parasitic inductance of the leads between the gate-driver output and the gate and source terminals of the module. The stray inductance of the dc bus bars has been estimated such that the frequency of the oscillations in the simulation matches the frequency of the oscillations in the experiments. Doing so, it was found that the amplitudes (current and voltage) of the oscillations in the simulation match those obtained from the experiments. The dc-bus inductance influences the frequency and the amplitude of the oscillations in such a way that a higher inductance results in
higher voltage amplitude and lower oscillation frequency. Similarly, a lower dc-bus inductance results in lower voltage amplitude and higher oscillation frequency.

A. Double-Pulse Test: Measurements on the Terminals

The first test is a DPT with the measurement performed at the module terminals. In the simulation, the measurement points are identical to those in the experiment. The DPT measurements are shown in Figs. 4.4 and 4.5 for the turn-ON and turn-OFF, respectively. The simulation results for the same conditions are shown in Figs. 4.6 and 4.7. In this case, the experimental results confirm the simulation. It can be noted that the frequency and amplitude of the oscillations in the simulation are similar to those recorded during the experiment.

B. Single-Pulse Test: Measurements on the Chip

The second test is a single-pulse test with the measurement performed on the module chip as in Fig. 4.2. In the simulation model, the measurement points are identical to those in the experiment except the gate-source voltage measurement which is not realized exactly on the gate pad. The SPT measurements and simulation results are shown in Figs. 4.8 and 4.9 for the drain source voltage and the gate-source voltage, respectively. A complete discussion can be found in Publication II.

4.5 Reliability Aspects

By comparing the results from the simulations and experiments, it is found that the agreement is good. The model will now be used to investigate reliability...
4.5. RELIABILITY ASPECTS

Figure 4.4: Double-pulse test turn-ON transients, lower switch position. Measurements at the module terminals. Gate-source voltage on the Kelvin source (yellow, 20 V/div), drain-source (purple 200 V/div), drain current (pink, 100 A/div). Time base (50 ns/div).

Figure 4.5: Double-pulse test turn-OFF transients of the SiC MOSFET module, lower switch position. Measurements at the module terminals. Gate-source voltage on the Kelvin source (yellow, 20 V/div), drain-source (purple 200 V/div), drain current (pink, 100 A/div). Time base (50 ns/div).

issues of the gate oxide which may arise if the gate resistor is reduced or if the gate-loop inductance is increased. In real applications where high efficiency is targeted, a fast switching performance is needed in order to reduce the switching losses. However, if this is done, oscillations are observed at the gate-source terminals. The simulation results show that the overshoot and the oscillations observed at the gate-source terminal are not present directly on the chip (see Fig. 4.10 and Fig. 4.11). In this work, three cases are simulated in order to observe the effect
Figure 4.6: Simulation results of the SiC MOSFET Module. Drain-source voltage (blue, 200/div), drain current (red, 100A/div). Time base 50 ns. Turn-ON transients measured at the module terminals.

Figure 4.7: Simulation results of the SiC MOSFET Module. Drain-source voltage (blue, 200/div), drain-source current (red, 100A/div). Time base 50 ns. Turn-OFF transients measured at the module terminals.

of a gate resistor reduction or an increase of the inductance in the gate-loop since they both are known to increase the oscillations and the cross-talk effect [59,60]. A small gate resistor is often used when considering fast switching speeds. A high gate-loop inductance can occur when the gate driver is connected far away from the gate terminal of the module. The three cases (including the reference case) are stated in Table 4.1. Note that the value of 2.5Ω for the gate resistor is the recommended value taken from the datasheet of the module under test. As a result from these simulations, it was observed that a lower gate resistance results in an increased voltage overshoot on the low-switch position at turn-ON (26.6 V). This value exceeds the maximum absolute voltage rating specified by the datasheet (25 V). The overshoot at turn-ON of the high switch position is of 22.3 V peak which is "acceptable" though still exceeding the recommended value of 20 V. For the
4.5. RELIABILITY ASPECTS

Figure 4.8: Single-Pulse test - Turn-off transients of the drain-to-source voltage Vds and the drain current Id (a) simulation (b) "on-chip" measurements. Drain-source voltage (blue, 100 V/div), drain-current (green, 100 A/div). Time base 100 ns.

Figure 4.9: Single-Pulse test - Turn-off transients of the gate-to-source voltage Vgs6 (a) simulation, measured as in Fig. 4.2 and at the gate-source terminals (b) experimental "on-chip" measurements (see Fig. 4.2) and at the gate-source terminals.

higher gate-loop inductance case, an increase in the cross-talk between the switch positions is observed. The gate-source voltage of the high switch position is not kept firmly to -5 V at the turn-on of the low switch position. It goes up to -1.8 V for one of the observed devices and -2.4 V for the other one. At the turn-off of the low-switch, the gate-voltages are -10.3 V and -9.4 V respectively instead of -5 V. Thus, the maximum rated gate voltage of -10 V is exceeded. As presented in [61], a higher voltage on the gate may reduce the lifetime of the device. Although no publication refers to lifetime reduction in case the maximum absolute negative voltage is exceeded, the authors believe that this case represents a reliability issue.

From the observation done in the present section and detailed in Publica-
Figure 4.10: Switching transients on the gate of the lower switch position under nominal conditions - lower switch position.

Figure 4.11: Cross-talk of the upper-switch position at turn-on and turn-off of the lower switch position - nominal conditions.

Table 4.1: Simulation Parameters

<table>
<thead>
<tr>
<th>Simulation case</th>
<th>$V_{ds}$ [V]</th>
<th>$V_{gs}$ [V]</th>
<th>$R_g$ [Ω]</th>
<th>$L_{g,stray}$ [nH]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Nominal Case</td>
<td>540</td>
<td>-5 / 20</td>
<td>5</td>
<td>20</td>
</tr>
<tr>
<td>2. Low Gate Resistance</td>
<td>540</td>
<td>-5 / 20</td>
<td>2.5</td>
<td>20</td>
</tr>
<tr>
<td>3. High Gate Driver Inductance</td>
<td>540</td>
<td>-5 / 20</td>
<td>5</td>
<td>100</td>
</tr>
</tbody>
</table>

Indeed, it can be concluded that the design of SiC MOSFET modules based on existing packages previously designed for Si-IGBT devices may not be optimal to fully utilize the high switching speeds offered by the SiC technology. In fact, in order to remain in a safe operation area and limit the cross-talk between the lower and upper switch positions, one has to limit the switching speed and connect the driver as close as possible to the module to avoid further parasitic inductance. The
author believes that there is a need to develop low-inductive packages adapted to the high-switching speeds of the new SiC technology. A reduction of the gate-loop inductance is desired to increase the reliability, decrease the cross-talk, but also to increase the switching speeds and thus decrease the switching losses. This is in accordance to what has been observed by Lemmon and al. in [60].

4.6 Conclusion

A SiC MOSFET power module available on the market has been modeled using ANSYS Q3D. The developed electrical model has been validated experimentally. The validity of the model has been confirmed by on-chip measurements. An analysis of the impact of parasitic elements on the gate-source voltages inside the module has been conducted, revealing a difference between the measured voltage at the gate terminal and the gate voltage on the chip. The oscillations observed at the gate-source terminal are not present at the chip level. The high over-shoot on the lower switch position gates observed at the terminal during turn-on is not present on the chip. However, when increasing the switching speeds, it was found that the gate-oxide was exposed to voltages exceeding the recommended operation values. This could lead to reliability issues, particularly when high-switching speeds are targeted. The investigation also supports the minimization of the parasitic inductance in the gate-drive connection in order to minimize the parasitic inductance in the gate loop since it can also be harmful for the device lifetime. The author believes that the short term over- and under- voltages on the gate do not influence the lifetime of the power module significantly. Similarly, it is not likely that a significant threshold voltage shift would result from the short-time over-voltages or under-voltages observed on the gate. However, this remains to be proven experimentally. For these reasons, the gate-drive design may have to compromise on the switching speeds while the distance between the gate driver output and the gate and source terminals of the 62 mm module has to be minimized. There is thus a need to develop low-inductive packages adapted to the fast switching SiC technology. Eventually, an integrated driver could minimize the gate-loop inductance accordingly.
Chapter 5

Long Term Testing of SiC MOSFETs

The information presented in this chapter is based on Publication III.

5.1 Introduction

In Chapter 2, the gate-oxide reliability and the body-diode reliability of SiC MOSFETs have been pointed out as possible reliability issues for the commercialization of SiC MOSFETs. If SiC power devices are foreseen to replace state-of-the-art Si devices, it is important to show that this technology is at least as robust as Si. This interest motivates research efforts towards application reliability such that their commercialization reaches its full potential [62–65]. The reliability assessment of SiC power devices is using methods previously used for Si power devices. This may result in ambiguous test results [66]. With the higher capability of SiC power devices in terms of temperature, the accelerated stress test methods might become obsolete [66] at least with respect to the device itself (in contrast to packaging).

The first generation of SiC power MOSFETs suffered from gate oxide reliability problems, especially at elevated temperatures [30]. Moreover, the gate threshold voltage of the SiC MOSFET has been found to be unstable when the gate is biased for a long time with a positive or negative gate voltage [66–70]. Another issue reported is the reliability of the intrinsic body-diode of the SiC power MOSFET [33, 34]. In industrial applications, it is not uncommon that the devices are powered OFF for long durations of time. A drift of the threshold voltage towards 0 V would compromise the reliability of the system in case the SiC MOSFET loses the normally-OFF property. Another concern, when a diode-less operation is targeted, an augmentation of the ON-state resistance due to bipolar degradation in the body-diode is not acceptable.

Therefore, in this work, experimental investigations on the threshold voltage stability and body-diode reliability of commercially available SiC MOSFETs from
the second generation are performed. The body-diode conduction test is performed with a current density of 50 A/cm$^2$ in order to determine if the body diode of the MOSFETs is free from bipolar degradation. This density value is higher than the data-sheet specification. The second test is stressing the gate oxide. A negative bias is applied on the gate oxide in order to detect and quantify potential drifts. Firstly, a device characterization is made on 80 devices from two manufacturers. The high number of tested devices is motivated by the desire to have sufficient data for further reliability assessments [71]. The aim is to compare the characteristics prior to the stress and after stressing the devices for a total of 1000 hours. Then, the devices are split randomly into two groups. The first group consisting of 20 devices from each manufacturer is exposed to a body diode reliability test. The remaining 40 devices are biased negatively at room temperature. The focus in this paper is the detection of a possible drift of the threshold during normal operating conditions. Therefore, unlike [64,67,68][15], [28], and [72], no accelerating factors, such as temperature or increased gate bias, are applied on the devices. Another particularity is that the setups are automated and constantly performing one measurement every hour. Thus, a fast measurement can be performed, while limiting the disturbance caused by the measurement. This is especially valid for the threshold-voltage stability stress test [68].

5.2 Methodology

In this work, two reliability issues have been investigated. The first one is the body-diode degradation that early generations of SiC MOSFETs were suffering from. The second one is the threshold voltage stability against an applied negative gate bias. The reason to investigate negative gate bias is that, since the gate threshold voltage of SiC MOSFETs is close to zero, a potential reduction of this value when a negative gate bias is applied could possibly lead to a normally-ON device. Moreover, the probability in a real application to have a negative bias applied for a prolonged time (for example a powered-OFF converter) is greater than the probability that a positive bias is applied. On the contrary to other studies realized on threshold stability [67,72], the devices have been tested at room temperature. The reason is that, if the converter is powered OFF, it is unlikely that the device dissipates energy. The two failure causes under study are not related to each other, however, it has been decided to use new devices in a desire to avoid testing "damaged" devices. Moreover, in a desire to test a statistically relevant amount of devices, 20 devices per type and per test have been tested. Sections 5.3 and 5.4 are detailing the test setups for the body-diode stress and threshold voltage stability test, respectively.
5.3 Body Diode Degradation

To evaluate the body diode reliability a direct forward current is continuously applied. To ensure that the channel is not conducting, the gate and source terminals of the device are short-circuited. Four circuits consisting of 10 devices in series are mounted on heat sinks, which are fan-cooled. The schematic diagram of the test circuit and a photograph of the final implementation are shown in Figs. 5.1a and 5.1b. The heat sinks are maintained below 95 °C to avoid recovery of the Shockley stacking faults by thermal annealing [73]. The results for the 20 devices from Cree (C2M0025120D) and from Rohm (SCT280KE) are shown in Fig. 5.2 and Fig. 5.3, respectively.

![Figure 5.1: Body-Diode Conduction Test: (a) Schematic diagram (b) Photograph of the Set-up](image)

5.4 Threshold Voltage Stability

The negative gate bias test is stressing electrically the gate oxide at the maximum rated negative direct bias voltage, which is -10 V for the Cree devices and -6 V for the Rohm devices. The purpose of this test is to detect a potential drift caused by random defects in the oxide as well as ionic contamination in the oxide. The test, which consists of measuring the gate threshold voltage once per hour, is automated in order to have a regular and precise measurement for a large amount of devices. A schematic diagram of the setup is shown in Fig. 5.4a. The threshold voltage is measured using the constant current method [74,75]. A photograph of the physical implementation of the test circuit is shown in Fig. 5.5 for four devices. The total test setup consists of five circuit boards. Thus, 20 devices can be tested simultaneously under equal conditions. The measurement procedure is shown in Fig. 5.4b. The gate and drain terminals are short-circuited, while a fixed current is fed through the drain-source channel. The measured voltage across the gate and source terminals is the threshold voltage defined for this particular current. Since the threshold voltage
CHAPTER 5. LONG TERM TESTING OF SIC MOSFETS

Figure 5.2: Body-Diode forward voltages monitored during 780 hours for the Cree devices.

is highly dependent on the temperature, the temperature is measured simultane-
ously. Thus, the measured data can be temperature-compensated and normalized
for 25 °C. The measurements are performed every hour for a total of 1000 hours.

Figure 5.4: Schematic diagrams of (a) stress test of the SiC MOSFETs (2 devices shown) and of the (b) constant current measurement technique.
5.4. **THRESHOLD VOLTAGE STABILITY**

![Figure 5.3: Body-Diode forward voltages monitored during 1800 hours for the Rohm devices.](image)

![Figure 5.5: Test set-up for the threshold voltage stability measurement.](image)

The threshold voltage drift test results are shown in Figs. 5.6 and 5.7. The results are a shift of 15 mV to 30 mV for the Cree devices and 50 mV to 100 mV for the Rohm devices. The drift occurs at the first hours of the stress test and the values tend to stabilize after 30 hours for Cree and 200 hours for Rohm.
CHAPTER 5. LONG TERM TESTING OF SiC MOSFETS

Figure 5.6: Evolution of the threshold voltages for 5 of the Cree devices for $I_{dss} = 300 \, \mu A$ at room temperature during 1000 hours.

![Figure 5.6: Evolution of the threshold voltages for 5 of the Cree devices for $I_{dss} = 300 \, \mu A$ at room temperature during 1000 hours.](image)

Figure 5.7: Evolution of the threshold voltages for 5 of the Rohm devices for $I_{dss} = 2 \, mA$ at room temperature during 1000 hours.

![Figure 5.7: Evolution of the threshold voltages for 5 of the Rohm devices for $I_{dss} = 2 \, mA$ at room temperature during 1000 hours.](image)

5.5 Conclusion

In this work, two different reliability issues of commercially available SiC MOSFETs have been investigated for a total of 80 devices for the gate threshold
voltage stability test and the body diode degradation test. Two different automated test setups have been built, allowing simultaneous measurement on each device once per hour. The body-diodes of a total of 40 MOSFETs from 2 different manufacturers were stressed with forward current for a total of 1000 hours. One device is currently possibly in the ON-state. The 39 remaining devices have shown no sign of bipolar degradation so far. A threshold voltage test has also been performed on 40 MOSFETs at room temperature. While stressed during 1000 h with a negative voltage of -10 V, the Cree devices (C2M0025120D) revealed a threshold voltage reduction of approximately 15-30 mV. The Rohm devices (SCT280KE) revealed a threshold voltage reduction of approximately 50-100 mV. The contribution of this work is the investigation of the body-diode stress for larger currents than what is done during the fabrication process and the non temperature-accelerated voltage stress on the gate oxide.
Chapter 6

SiC MOSFET Modules in Humid Environment

The information presented in this chapter is based on Publication IV and Publication V.

6.1 Introduction

The effect of humidity on SiC Power MOSFET modules is investigated in a real application. In many applications, for instance traction and industrial implementations, it is common that power electronic converters (PE) are placed outdoor where the air humidity is not controlled. Moreover, applications placed outdoor are unprotected from toxic gases, daily temperature variations and dust. In traction applications, the converters are placed on the vehicle roof or under the chassis for space reasons. In industrial facilities, PE units may be exposed to uncontrolled harsh environment and climate conditions when placed outside. The integrity of the converters and modules inside the enclosures see their integrity compromised by moisture, gases, salt and dust among others [76].

Typically, the converter units are not sealed hermetically. Thus, moisture builds up in the enclosures in which the converters are placed. A simulation model describing the moisture inside the converters and power modules is presented in [77]. The moisture inside the converter cabinets can exceed the ambient conditions significantly. Moreover, if condensation occurs in the un-sealed module and above the chips, corrosion can lead to failure of the power semiconductor module [20]. The latter is one of the reasons in this work to not use the standard tests based on Si technology. The humidity is often tested in the so-called temperature humidity bias (THB) 85/85 test with an 80 V bias [12]. As the condensation in humid environments occurs at low temperatures and the fact that higher voltage levels accelerate the moisture diffusion considerably for Si IGBTs [18], this work focuses on a real application case. In fact, in most cases, the temperature in the converter
enclosure is lower than 85 °C and may even go down to the moisture dew point when the temperature outside is low (winter for instance) and the converter is turned off. An accelerated THB test on IGBT modules at high bias levels is presented in [19]. Similar work has been presented in [78] where pressure as a failure factor is included.

The present work targets specifically the reliability of SiC MOSFETs with regards to humidity and aims to exclude other failure mechanisms which could potentially result from highly accelerated tests. This work is a follow up of what was presented in [79]. The evolution of the blocking voltages after another 6000 h of test is presented. The total time of the test will eventually be 8000 h. As for SiC diodes [16], the edge termination of the SiC MOSFET chips are of concern, partly due to the higher electric field applied on SiC technology while the chips are thinner than corresponding silicon chips.

In this work, four modules are operated outdoor and four modules are operated indoor in identical setups, while their breakdown voltages are monitored regularly. The evolution of the leakage current, indicating humidity-induced degradation is observed.

6.2 Application

The application considered in this work is a full-bridge LCC resonant converter as shown in Fig. 6.1. It is part of a power supply for Electrostatic Precipitators (ESP) presented in [80]. The converter units may be placed outdoor for space reasons. In that case, humidity and gases can penetrate the enclosure of the converter since this is not sealed hermetically. The commercially available version of these converters is based on a design using Si IGBTs. In that case, the humidity has not been a problem. For this work, four converter have been taken where the Si IGBT modules have been replaced by SiC MOSFET modules. The second modification was the gate drivers, as the voltage levels required to drive SiC MOSFETs are slightly different than those for Si IGBTs. Apart from these two modifications, the converters are run under exactly the same conditions as the Si version.

Figure 6.1: Simplified schematic diagram for one converter
6.3 Methodology and Test Setup

The monitoring of the degradation during the humidity testing consists of measuring the leakage current of the blocking devices. According to the datasheet of the device under test (DUT), the blocking voltage is defined by the blocking voltage when the leakage current is of 1 mA. This paper, as previously presented in [79], focuses on a non-accelerated degradation of humidity-exposed SiC MOSFET 62 mm modules previously used for IGBT technology. In order to do so, the devices will be operated in a converter at rated current and voltage for an extended period of time while their blocking voltages are measured periodically. The reason to extend the test time to a few thousands of hours is that since the test is not accelerated, the degradation mechanisms may take longer to develop and be visible. The periodical measurement of breakdown voltages permits to monitor the evolution of the blocking voltages and to collect data for further analysis. Figs. 6.2a and 6.2b show the blocking voltages of the low-side and high-side switch position of the modules, respectively.

The modules are placed by pairs in four different converters. Of the four converters, two are placed indoors and two outdoors as in the schematic diagram of Fig. 6.3a. The cooling system has been organized so that the two indoor converters share the same cooling system and the two outdoor converters share the same cooling system. The outdoor implementation is pictured in Fig. 6.3b.

Figure 6.2: Pre-test breakdown voltage of the 8 modules (a) low-side switch position (b) high-side switch position
CHAPTER 6. SIC MOSFET MODULES IN HUMID ENVIRONMENT

Figure 6.3: (a) Converter setup (b) Experimental setup located outdoors. The two converters are placed on top of each other. The cooling system is on the far right. The box on the left is sealed (IP66) and contains the control and the power supply for the drivers of the MOSFET modules.

6.4 Experimental Results

The modules have been characterized after 280 h, 630 h, 1700 h, 4460 h, and 5924 h. The test results are shown in Fig. 6.4 for one module placed indoors and one module placed outdoors. For the lowest switch position of the module placed outdoors, a noticeable difference in the leakage current between 4460 h and 5924 h is observed. The device only blocks 1090 V which is below the datasheet specifications. On the contrary, the module placed indoor presents almost
no variation both for the upper switch position and the lower switch position. The evolution over time of the blocking voltage (for 1 mA of leakage current) for all the DUTs is shown in Fig. 6.5. It can be seen that the device 122, also placed outdoor, also presents noticeable variations between the pre-test and the first post-test measurement.

Figure 6.4: Evolution of the breakdown voltage of (left) a module situated indoor (right) a module situated outdoor
In this work, the impact of humidity on SiC MOSFET modules has been investigated. Four power modules have been operated in an environment exposed to humidity and four power modules have been operated indoors. Several parameters have been monitored while the blocking voltages of the modules were measured regularly. Even though the test has not been accelerated, one module situated outdoor shows signs of degradation and is no longer blocking according to the datasheet specifications after 5924 h which is equivalent to approximately 8 months. This shows that it may be required to use better packages for SiC MOSFET modules when the converters are operated outdoor or in harsh environments. The tests are still ongoing and will be terminated after one year (approx. 8000 h).

Figure 6.5: Evolution of the blocking voltage over time - indoor operated modules (upper figure) and outdoor operated modules (lower figure)
Chapter 7

Short-Circuit Behaviour of SiC Power Devices, Thermal Analysis and Protection Circuits

The information presented in this chapter is based on Publication VI and Publication VII.

7.1 Introduction

The introduction of SiC devices has brought new possibilities for the design engineers. Higher power densities are involved as well as the possibility to operate at higher temperatures. However, the higher power densities enabled bring the issue of how long a short-circuit fault can be sustained by a SiC power device. Regardless of the short-circuit robustness, the short-circuit fault must be turned OFF as soon as detected to preserve the device from degradation. The present chapter focuses on establishing how fast a short-circuit fault can be detected and how fast it can be turned OFF. To complement the behaviour analysis, an electrothermal simulation based on the SiC device physics is given.

Transient robustness of SiC transistors under short-circuit conditions has already been investigated. In [36–38], the conclusions are that the SiC MOSFET can withstand short-circuit conditions for 13-80 µs depending on its gate-to-source voltage and on the dc-bus voltage. This time is however, reduced if the case temperature is increased [81]. Similar work has been done on SiC JFETs and SiC BJTs [26,35,43,44,82,82–84]

There are four types of short-circuit faults. Among those, a fault occurring during the transistor turn-ON transient is referred to as hard switching fault (HSF), and a fault occurring during ON-state conditions is referred to as fault under load (FUL). A complete analysis of these two types of faults has been given in [85]. During both types of short-circuits, the current rises rapidly and the device de-
CHAPTER 7. SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES, THERMAL ANALYSIS AND PROTECTION CIRCUITS

saturates. For SiC MOSFETs, both fault types have been investigated in [86], and it was found out that in both cases, the short-circuit event can be detected by means of the de-saturation technique. However, the detection delay times are longer for HSF than for FUL. Consequently, only the HSF will be studied in this paper to limit the scope of investigation.

7.2 Methodology

In this work the short-circuit behavior of SiC power devices is observed in Section 7.3. The observed behavior will permit to identify the variables which can be measured on the device and in the circuit in order to detect a short circuit as fast as required. The short-circuit protection is presented in Section 7.4. Finally, the devices have been decapsulated and reconstructed as simulation models. The models have been verified by experiments and an electro-thermal simulation of the temperature rise in the die is performed. This is done in order to confirm the requirement to turn OFF a short-circuit fast but also in order to compare the different topologies in terms of short-circuit behaviour. This is discussed in Section 7.3. Finally, in Section 7.5 for the SiC MOSFET, the impact of circuit parameters on the temperature rise in the die during a short-circuit event is investigated through simulations.

7.3 Short-Circuit Behaviour of SiC Power Devices

Prior to designing a short-circuit protection (SCP) for SiC power devices, the behavior of SiC power transistors during the early stage of a short-circuit fault is investigated. Besides extracting information on how a short-circuit fault can be detected and how fast it can be detected, the aim of the experiment is to analyze the turn-OFF transients to define an appropriate turn-OFF procedure in case of a short circuit. The high switching speeds of SiC power transistors may cause excessive over-voltage when turning OFF a short-circuit current. This is especially true for designs utilizing the fast-switching properties of SiC power devices. Moreover, once a short-circuit condition has been detected, any additional delay before turning the short-circuit current OFF may reduce the lifetime of the device due to excessive localized heating. A short duration of the short-circuit condition is, therefore, preferable for reliability reasons.

The test circuit for the experiment is shown in Fig. 7.1. The dc-link voltage is \( V_{dc} = 600 \, \text{V} \). The circuit stray inductance \( L_s \) (excluding the capacitor and the device) has been determined experimentally to 32 nH. Assuming that the internal stray inductance \( L_{ss} \) of the TO-247 package is 10 nH, the total circuit stray inductance is approximately 42 nH.
Short-Circuit Behaviour of SiC Power MOSFETs

Two different SiC MOSFETs from different manufacturers are investigated. Their characteristics can be found in Table 7.1. The main difference between the two MOSFETs is the chip size and the chip thickness. The driver output stage is powered by a positive voltage source of +24 V and a negative power source of -5 V. The external gate resistance is 20 \( \Omega \) for both turn-ON and turn-OFF to facilitate low oscillations during switching transients and switching times below 40 ns. The duration of the predefined short-circuit pulse is 500 ns. The short-circuit behavior of the SiC MOSFETs are shown in Figs. 7.2 and 7.3. The voltage across the SiC MOSFET does not drop significantly during the short-circuit pulse. However, the current starts rising fast and then the slope decreases with time. The device structure for the SiC MOSFET from Rohm is shown in Figure 7.4. The device has been reconstructed in the simulation software Taurus Medici and the simulated curves are shown in Figure 7.5. For all the simulated structures the reconstruction procedure has been the same. First, the structure dimensions (lateral and vertical) has been obtained from SEM analysis after decapsulation. Secondly, the doping levels of n-type and p-type regions have been adjusted by comparing simulated conduction, transfer, and blocking characteristics to measurements and datasheet values. Finally, thermal boundary conditions were defined by fitting the transient impedance data in data sheets for pulse times shorter than 500 \( \mu s \) with a single value of \( C_{th} \) and \( R_{th} \) for each device. A very good fit is obtained for short pulses. The device reconstruction and simulation were performed for all the devices in

<table>
<thead>
<tr>
<th>SiC DUTs</th>
<th>( I ) [A]</th>
<th>( R_{ds, on} ) [m( \Omega )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M0025120D</td>
<td>90</td>
<td>25</td>
</tr>
<tr>
<td>SCT2080KE</td>
<td>40</td>
<td>80</td>
</tr>
</tbody>
</table>
CHAPTER 7. SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES, THERMAL ANALYSIS AND PROTECTION CIRCUITS

Figure 7.2: Short-circuited Cree MOSFET, $R_G = 20 \ \Omega$. Measured gate-to-source voltage (yellow line, 50 V/DIV), drain-to-source voltage (purple line 200 V/DIV) and drain current (pink line, 200 A/DIV). Time base 200 ns/DIV.

Figure 7.3: Short-circuited Rohm MOSFET, $R_G = 20 \ \Omega$. Measured gate-to-source voltage (yellow line, 50 V/DIV), drain-to-source voltage (purple line 200 V/DIV) and drain current (pink line, 200 A/DIV). Time base 200 ns/DIV.

this chapter by Mietek Bakowski and Jang-Kwon Lim at Acreo. The evolution of the temperature in the chip during a 1 $\mu$s short-circuit event is shown in Fig. 7.6 for a device with a stray inductance $L_{ss} = 10 \ \text{nH}$. A variation in source stray inductance results in higher temperature rise for lower stray inductance values and lower temperature rise for higher stray inductance values, respectively. The temperature distribution in the chip after 500 ns of short-circuit event is shown in Fig. 7.7. It can be seen that the hottest point is situated 2 $\mu$s below the gate oxide, which is just below the surface where the top metallization and passivation layers are located.
7.3. SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES

Figure 7.4: Device structures of the SiC MOSFET (Rohm) using scanning electron microscopy.

Figure 7.5: Simulated electrical short-circuit behaviour of the SiC MOSFET.

Short-Circuit Behaviour of SiC Power JFETs

The latest normally-ON JFET from United SiC (USCi) has also been tested. Its characteristics are stated in Table 7.2. The driver output stage is powered by a negative power source of -15 V and 0 V is used for the on-state. The external driver structure is a so-called "DRC" network as presented in [42]. The predefined short-circuit pulse is of 500 ns. The short-circuit behavior of the SiC JFET is shown in Fig. 7.8. As for the SiC MOSFET, the voltage across the SiC JFET does not drop significantly during the short-circuit pulse. The current starts rising slower than for the SiC MOSFET and the peak current is lower than for the SiC MOSFET. The peak current is of 120 A while the over-voltage at turn-OFF is of 200 V. The

<table>
<thead>
<tr>
<th>SiC DUTs</th>
<th>I [A]</th>
<th>$R_{ds.on}$ [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>UJN1205K</td>
<td>38</td>
<td>45</td>
</tr>
</tbody>
</table>

Table 7.2: 1.2 kV SiC JFET under Test
CHAPTER 7. SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES, THERMAL ANALYSIS AND PROTECTION CIRCUITS

Figure 7.6: Evolution of the hottest temperature point the chip during a 1 µs short-circuit pulse.

Figure 7.7: Temperature distribution in the chip after 500 ns $T_{max} = 273^\circ C$

turn-OFF time after the fault is of 40 ns. The device structure for the SiC JFET is shown in Fig. 7.9. The device is reconstructed in Taurus Medici and the simulated curves under similar short-circuit conditions as in the experimental setup are shown in Fig. 7.10. The simulated curves are in accordance with the experimental curves shown in Fig. 7.8. The temperature evolution of the hottest point in the die is shown in Fig. 7.11a. The maximum temperature is of 500 °K, which is slightly lower than for the SiC MOSFET. Also, the peak temperature occurs slightly after 1µs, since the device is still producing heat as long as the short-circuit has not been turned OFF completely. The distribution of the temperature in the die after 500 ns is shown in Fig. 7.11b, revealing that the hot spot is situated the deepest in the structure and farthest away from the top surface compared to the SiC MOSFET. The distance from the hot spot to the surface is of 6 µs and the distance to the trench bottom is of 2.5 µs.
7.3. **SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES**

![Image 1](image1.png)

Figure 7.8: Short-circuited normally-on JFET, $R_G = 10 \, \Omega$. Measured gate-to-source voltage (yellow line, 50 V/DIV), gate current (green line 5 A/DIV), drain-to-source voltage (purple line 500 V/DIV) and drain current (pink line, 100 A/DIV). Time base 50 ns/DIV.

![Image 2](image2.png)

Figure 7.9: Device structure of the SiC JFET using scanning electron microscopy.

**Short-Circuit Behaviour of SiC Power BJTs**

Two different SiC BJTs have been tested. The first device tested is the FSICBH017A120 from Fairchild which has been tested with two different base currents. In fact, since the BJT is a current controlled device, it is possible to limit the short-circuit peak current since the maximum collector current is dependent on the base current. The second device is the newly released super-junction transistor (SJT) from Genesic. The driver in this experiment is the driver presented in [87] and the short-circuit duration is of $1 \mu$s. The short-circuit curves for the Fairchild device are shown in Fig. 7.12a for 1 A base current and in Fig. 7.12b for 0.5 A base current. The short-circuit curves for the Genesic device are shown in Fig. 7.12c for a base current of 0.75 A. As can be seen, the BJT is the device having the lowest peak short-circuit current. Moreover, due to bipolar nature of the device
and the transient dynamics, but also the fairly small current to turn-off, the over voltage at turn off is of 25 V. This is considerably smaller than for the SiC unipolar devices. The device structure for the SiC SJT from Genesic is shown in Fig. 7.13.

Table 7.3: 1.2 kV SiC JFET under Test

<table>
<thead>
<tr>
<th>SiC DUTs</th>
<th>$I$ [A]</th>
<th>$R_{ds,on}$ [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>UJN1205K</td>
<td>38</td>
<td>45</td>
</tr>
</tbody>
</table>

The reason for the device choice is that Fairchild is no longer producing SiC BJTs,
7.4. SHORT-CIRCUIT DETECTION DESIGN

Figure 7.12: (a) Short circuited SiC BJT, $I_b = 1$ A (b) Short circuited SiC BJT, $I_b = 0.5$ A (c) Short-circuited SiC SJT, $I_b = 0.75$ A. Measured base-to-emitter voltage (yellow line, 10 V/DIV), base current (green line (a) 1 A/DIV (b)-(c) 2 A/DIV), collector-emitter voltage (purple line (a)-(b) 200 V/DIV (c) 500 V/DIV) and collector current (pink line, (a) 20 A/DIV (b) 50 A/DIV). Time base 200 ns/DIV.

and the devices from Genesic are available on the market. Therefore, it is more relevant to study this particular device. The device has been reconstructed in the simulation software and the simulation results for the electrical curves are shown in Fig. 7.14. In the SiC BJT, the hottest area is located in the collector region close to the base-collector junction and under the edge of the emitter. In that case, the distance to the surface is of 4 µs and 1.5 µs to the base-collector junction.

7.4 Short-Circuit Detection Design

Since the ON-state voltage drop of the device during a short-circuit fault is much higher than during normal operation, the short-circuit condition can easily
be detected by comparing the control input with the drain-to-source voltage (or
the collector-emitter voltage). This detection method is known as the de-saturation
method [88–90]. As emphasized above, a fast detection not only reduces the current
level at which the device has to be shut-down, but it limits the self-heating of the
device as well and further risks for the device immunity. Additionally, the voltage
overshoot at turn-OFF is limited. The proposed implementation has the following
targets:

- Fast detection
- Fast reaction in order to limit over-heating
- Limited turn-OFF speed for the SiC MOSFET and JFET
- Easy implementation in any driver design
- High noise immunity
Besides these targets, the driver has to be placed as close as possible to the gate and source pins of the device in order to avoid undesired parasitic elements.

The speed of detection is limited by the turn-ON and turn-OFF times of the protected device. In addition, margins have to be considered to avoid false triggering or the SCP. In the present implementation, the fault detection delays are defined by RC filters. Fast detection delays are also limiting the overshoot at turn-OFF. A limited turn-OFF speed is also easily achieved by using different gate resistors for turn-ON and turn-OFF. A drawback of this solution is that the switching losses at turn-OFF are increased. However, if very high switching speeds (and low switching losses) are targeted a solution using an alternative gate resistance in case of a fault could be a solution. The proposed solution provides an easy implementation enhancing the driver reliability without affecting the driver characteristics during normal operation.

The structure of the short-circuit detection is shown in Fig. 7.16 for the case of a SiC BJT. The concept of the detection circuit is the same for the SiC JFET and MOSFET. The logic circuits used in this realization are from the TTL series, with a 5 V supply voltage for the SiC BJT and from the CD4000B series, with modifications, for the SiC MOSFET and JFET (12 V and 15 V respectively). A detailed description of the operation of the short-circuit protection can be found in Publication VI. The presented short-circuit detection can be directly integrated into a conventional SiC power semiconductor driver. This integration allows a fast turn-off of the device at the inception of a short-circuit, because the fault handling is performed locally without involvement of external control circuits. Being fully independent from the driver, it can easily be combined with almost any kind of
CHAPTER 7. SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES, THERMAL ANALYSIS AND PROTECTION CIRCUITS

Figure 7.16: Schematic diagram of the short-circuit detection.

Table 7.4: Truth table of the short-circuit detection method

<table>
<thead>
<tr>
<th>Control Signal</th>
<th>$V_{ds}$</th>
<th>AND</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Circuit OFF</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>OFF-state</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ON-state</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Short-circuit or Fault</td>
</tr>
</tbody>
</table>

driver without adding much complexity. Three different SCP drivers have been designed. The performance of the SCP drivers is investigated by performing a short-circuit test and a double-pulse test. These tests are performed in order to verify that there are no erroneous short-circuit detections. The drivers - though without SCP - used in this work, have already been tested successfully in [55, 91], and [92], for the SiC BJT, MOSFET and JFET, respectively. Moreover, the robustness of the presented SiC MOSFET driver against noise was tested in a converter in [55] where it is implemented in a 20 kHz 3-phase 312 kVA inverter for an electrical vehicle with a total of 30 SiC MOSFET modules and 60 SCP drivers.

Short-Circuit Protection of SiC Power BJTs

As seen in Section 7.3, the peak fault current during a short-circuit condition is inherently limited for SiC BJTs. For a similar short-circuit duration, the SiC BJT will dissipate less energy than the SiC JFET and MOSFET. Nevertheless, there is no need to wait more than a few times the duration of a normal turn-ON in order to turn-OFF the short circuit. The RC filters are calibrated in order to achieve a short-circuit detection within 380 ns. The SiC BJT driver is the one used in Section 7.3 without modifications combined with the short-circuit detection [87].

The schematic diagram of the SCP driver for SiC BJTs is shown in Fig. 7.17 and its physical implementation is shown in Fig. 7.19(a). Additional components required for the detection circuit are also shown in the figure. The SCP driver performance during a short-circuit event is illustrated in Fig. 7.18 for both SiC BJTs and SJTs. The time delay between detection and protection $T_d$, the peak
short-circuit current $I_{peak}$ as well as the short-circuit duration $T_{sc}$ are summarized in Table 7.5. The under-shoot of the enable signal is due to noise induced by the turn-OFF transients. The noise immunity of the system is sufficiently high such that the short-circuit fault is turned OFF safely within less than 100 ns after its detection. The operation of the SCP driver during normal operation is validated by Fig. 7.19(b).

Table 7.5: Short-circuit protection driver performance with SiC BJTs

<table>
<thead>
<tr>
<th>SiC DUTs</th>
<th>$T_d$</th>
<th>$I_{peak}$</th>
<th>$T_{sc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSICBH017A120</td>
<td>380 ns</td>
<td>120 A</td>
<td>450 ns</td>
</tr>
<tr>
<td>GA50JT12-247</td>
<td>380 ns</td>
<td>80 A</td>
<td>500 ns</td>
</tr>
</tbody>
</table>
CHAPTER 7. SHORT-CIRCUIT BEHAVIOUR OF SiC POWER DEVICES, THERMAL ANALYSIS AND PROTECTION CIRCUITS

Figure 7.19: (a) Hardware realization of the SCP driver for SiC BJTs. (b) Double pulse test of the SiC BJT from Fairchild using the SCP driver. Measured collector-emitter voltage (purple line, 200 V/DIV) and collector current (pink line 10 A/DIV). Time base 50 ns/DIV.

Short-Circuit Protection of SiC Power JFETs

The short-circuit protection of SiC JFETs is very similar to the one of SiC MOSFETs. The chosen power stage of the SiC JFET driver is the DRC network [42] with a -30 V power supply. Even though this driver topology speeds up the turn-ON and turn-OFF transients, the over-voltage of 200 V is judged to be within the reliability margin since the peak over-voltage is 800 V. Moreover, the DRC network provides a stiff negative voltage to the gate at turn-OFF. The hardware realization of the SiC JFET SCP driver is presented in Fig. 7.20(a). Fig. 7.20(b) shows the operation of the SCP driver with the normally-on JFET UJN1205K from
7.5 SIC MOSFET - ANALYSIS OF THE CIRCUIT PARAMETER IMPACT ON THE TEMPERATURE RISE IN THE DIE

USCi. The short circuit is turned-OFF within 610 ns after the turn-ON which is a reasonable value since the JFET is known to be the most robust SiC device in terms of short circuit durability (> 20 µs).

7.5 SiC MOSFET - analysis of the circuit parameter impact on the temperature rise in the die

The SiC MOSFET is nowadays the device of choice when it comes to replacement of Si IGBT by SiC technology. For that reason, a deeper analysis of the temperature distribution in the die during a short circuit is performed for MOSFETs. Five cases are analyzed and compared to a reference case. The reference case is a short circuit of 1 µs duration with a 10 nH source stray inductance with a direct voltage of 600 V. The gate-to-source voltage is always 20 V in the ON-state and -5 V in the OFF-state and the gate resistance is 20 Ω. As previously mentioned, the maximum temperature occurs 2 µm below the oxide and semiconductor interface and approximately 2.25 µm below the surface. Recently, for 10 kV MOSFETs, visual degradation were observed on the surface metalization through SEM after repetitive short-circuit events have been observed [93]. This also supports the need to avoid localized hot spots which can be done by fast the detection and clearance of a short-circuit fault.

First, the effect of different switching speeds is analyzed. The gate driver resistance is varied in order to speed-up and slow-down the switching transients. Secondly, the variation of the stray inductance in the circuit is investigated. Thirdly, the impact of the dc-link voltage on the temperature rise is considered. Then, different length of short-circuit detection times are studied in order to observe clearly the importance of fast detection whenever possible to protect the device
and avoid further degradations in case of a fault. The turn-OFF time has to be taken into account since the temperature will rise during the total stress time $t_{sc,tot} = t_{detection} + t_{reaction} + t_{turn,off}$. Finally, the impact of the gate-source voltage is also analyzed.

A complete analysis where the impact of various circuit characteristics on the temperature rise in the die and a comprehensive description of each case is being investigated. The temperature rise in the die is higher for the case of low stray inductance compared with the case of high stray inductance. The gate-source voltage variation also impacts the maximum temperature considerably. A higher inductance affects the switching losses. Similarly, a lower gate-source voltage affects the ON-state loss.

The outcome of this study results in design guidelines for design engineers who have to integrate a short-circuit protection to their system accordingly. As the SiC technologies suggest low inductive designs to operate at high switching frequencies and low on-state losses (thus higher gate voltages), the faster the detection, the better the devices will be protected. If there are no possibilities to detect the short-circuit within the first few hundreds of nanoseconds, it is of course possible to modify the design and include higher inductance or a lower gate-source voltage. However, as mentioned earlier, doing so, the overall loss in normal operation will increase. This goes against the trend of developing converters utilizing the full advantages brought by the newly introduced SiC technology. The possibilities of faster switching and low volume and weight is then compromised.

In conclusion, the main difference between short-circuit protection for Si devices and SiC devices is that the design considerations when using SiC devices are not allowing long short-circuit durations as it was the case with Si devices. Higher power densities, higher voltages, higher current densities, together with the desire to reach high switching speeds, low losses and small cooling system volumes require to implement fast short-circuit detections and protection. Moreover, since the junction depth and device dimensions are smaller, the distance between the hot spot in the die and the surface is smaller in SiC than for Si. This supports the need to turn-off the short-circuit fault as soon possible, including sufficient margins for the turn-ON and turn-OFF transients. In fact, during the switching transients, faulty detection can occur for instance if the voltage across the switch is still high while the control signal is "ON". Delays are introduced in the detection procedure in order to avoid these situations and ensure that no erroneous fault detection occurs. This has been realized in Publication VI by means of RC circuits and ultra-fast diodes. Nevertheless, the authors believe that the Integrated Circuits (ICs) are sufficiently fast to detect faults in less than 200 ns. Thus, fast detection of short-circuit faults are not an issue.
7.6 Conclusion

In this paper the short-circuit behavior of SiC MOSFETs, SiC JFETs, and SiC BJTs is presented together with their respective transient thermal device simulation. A short-circuit protection concept has been presented based on the de-saturation technique coupled with state-of-the-art SiC device drivers. The performance of the proposed drivers has been verified. The detection speeds are below 200 ns. Through thermal device simulations, the location of the hottest point in the die and its temperature evolution is investigated. A detailed analysis of the influence of the circuit design on the short-circuit behavior of SiC MOSFETs is presented. The analysis supports a fast detection of short-circuits for designs utilizing the benefits of SiC technology.
Chapter 8

Investigation of the Surge Current Capability of the Body Diode of SiC MOSFETs

The information presented in this chapter is based on Publication VIII.

8.1 Introduction

A possible application for SiC devices is high-voltage direct current (HVDC) transmission where SiC technology can offer higher efficiencies due to lower on-state resistance and faster switching capability [5]. State of the art HVDC converters are often built with Si IGBT technology combined with a high-power antiparallel diode since the IGBTs cannot conduct current in the reverse direction. SiC MOSFETs are foreseen to replace IGBTs in the next generations of power electronic converters, and, as they have an intrinsic diode, diode-less operation is an attractive option to reduce the overall system cost. However, as mentioned in Chapter 2, the body diode of SiC MOSFETs has, in the past, suffered from Shockley Stacking Faults (SSFs), growing from Basal Plane Dislocations (BPDs) or Threading Dislocations (TDs) [33]. Even though this failure mode has been suppressed (c.f Chapter 5), in HVDC converters, one of the antiparallel diode is exposed to very high transient currents during a short-circuit event on the dc side [94], as seen in Fig. 8.1 for a two-level voltage source converter (VSC) and in Fig. 8.2 for a modular multilevel converter (MMC). The peak surge current may be as high as 10 times the rated current of the device. If SiC MOSFETs are considered in HVDC applications, the reliability and ruggedness of the SiC MOSFET body diode with regards to surge currents has to be investigated, in particular because a thick drift layer has a large impact on the MOSFET degradation during forward current stress [95]. Furthermore, the possibility to turn the SiC MOSFET channel ON during a surge-current event [96] is investigated.
CHAPTER 8. INVESTIGATION OF THE SURGE CURRENT CAPABILITY
OF THE BODY DIODE OF SiC MOSFETS

Figure 8.1: Schematic of a two-level VSC dc-side short-circuit. The antiparallel diodes conduct the ac-side current.

Figure 8.2: Schematic of a half-bridge MMC after a pole-to-pole dc fault. The antiparallel diodes conduct the ac-side current.

8.2 Methodology

The standard datasheet test for surge currents through the body diode of SiC MOSFETs typically uses a half sine wave with a duration of 10 $\mu$s. However, the diode in a two-level VSC or MMC for HVDC transmission may have to withstand longer surge current durations. During a surge current, the temperature rise in the die depends on the pulse current amplitude and its duration, the initial die temperature and the diode forward voltage. The thermal impedance of the device and the initial case temperature also have an impact on longer pulse durations [97].

Preliminary tests were performed on the devices C1 and C2. The devices were tested with a 10 $\mu$s pulse having a peak value of 280 A with 0 V across their gate-source terminals. Moreover, the devices were heated from room temperature (25 $^\circ$C) to 150 $^\circ$C to study the effect of temperature on the surge current of the body-diode [98]. The results are presented in Section 8.3.

The schematic diagram of the setup built for this work is shown in Fig. 8.3a and a picture of the laboratory experiment is shown in Fig 8.3b. The DUTs, which are the latest 900 V, 1.2 kV, and 1.7 kV discrete devices and modules available on
8.2. METHODOLOGY

the market are placed in such a way, so that, when the auxiliary switch closes, a surge current flows through their body diode. The device characteristics are stated in Table 8.1. The gate-source voltage of the DUTs is set to -5 V in order to keep the devices firmly in the OFF state. In this way, one guarantees that the current surges flows only in the body diode and not in the channel of the discrete devices. Three out of the four modules (M2, M3, and M4) are populated with parallel Schottky diode dies. Since the Schottky diode knee voltage is lower than the knee voltage of the SiC MOSFET body-diode, at low forward voltages ($V_f$), only the SiC Schottky dies are conducting. However, at $V_f$ higher than the cut-off voltage of the body diode, both diodes are sharing the surge current. Consequently, at higher current levels, the current will flow both in the Schottky die and the MOSFET die via the body diode. In a second step the surge current capability of the devices in the reverse direction with a conducting channel is also investigated. The surge current magnitude depends on the impedance of the setup circuit and on the magnitude of the direct voltage applied. The duration of the half-sine current wave and the peak surge current can be adjusted by a proper selection of the dc capacitance $C_{dc}$ and the inductance $L$. The duration of the pulse is chosen through the angular resonant frequency

$$\omega_o = \frac{1}{\sqrt{LC_{dc}}},$$

and the peak value of the surge current is chosen through

$$\hat{i} = \frac{V_{dc}(0)}{Z_o},$$

where

$$Z_o = \sqrt{\frac{L}{C}}.$$
Chapter 8. Investigation of the Surge Current Capability of the Body Diode of SiC MOSFETS

8.3 Experimental Results: preliminary tests at 10 \( \mu \text{s} \)

Preliminary tests were performed on the devices C1 and C2. It was found that the temperature has no significant influence on the body-diode characteristics at high currents. However, as can be observed in Figs. 8.5 and 8.6, at low current, an increase in case temperature has an impact on the body-diode characteristics.

8.4 Experimental Results: longer duration tests and destructive tests

In this part, the DUTs have been tested with surge current durations up to 2 ms. The discrete devices and modules were characterized prior to test. The modules
8.4. EXPERIMENTAL RESULTS: LONGER DURATION TESTS AND DESTRUCTIVE TESTS

Figure 8.4: Half-sine wave pulse (10 $\mu$s) with varying current for the DUT C2.

Figure 8.5: C2 - Half-sine wave (10 $\mu$s, 10 A peak)

were tested after the 680 $\mu$s surge current test and 1.8 ms surge current test revealing a reduction in blocking capability for some devices. The DUTs were tested until failure or until 10 times the rated current. The post-destructive characterization revealed a broken diode and a broken junction for C1, C2, R1, and R2. In all cases, the gate-source junction was shorted after failure and the diode was no longer blocking. Some MOSFETs had a channel conducting with a high resistance and others were completely short-circuited. A discussion about the observed failure modes is given in Section 8.5 below. The hypothesis of the authors is that the failure mechanism of the SiC MOSFETs is the activation of the parasitic npn-transistor, leading to a bipolar second breakdown as described in [99, 100]. Tables summarizing the maximum tested surge current without failure for different lengths of surge currents except for section 2 can be found in Publication VIII. After all these tests, the devices were still operating and the diode still blocking. The pulse could be repeated without breaking the device. Not all devices have been tested for all cases due to the limited amount of devices available. The failure modes observed in those experiments are explained in Section 8.5.
CHAPTER 8. INVESTIGATION OF THE SURGE CURRENT CAPABILITY OF THE BODY DIODE OF SiC MOSFETS

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Figure 8.6: C2 - Body-Diode characteristics at 25 °C and 150 °C.

In this work, the following cases have been investigated:

- Surge current at room temperature - discrete devices (280 µs, 870 µs, and 1.8-2 ms) surge current

- Surge current of C1 at different temperatures

- Surge current while opening the SiC MOSFET channel during a 2 ms surge current

- Multiple surge current (20 times) - discrete devices (C1 and R1)

- Surge current at room temperature - SiC MOSFETs modules

8.5 Failure Modes

Two failure modes have been observed for the discrete SiC MOSFETs. A degradation of the blocking capabilities and a dynamic failure mode leading to the short between gate and source. The failure pulses can be observed in Fig. 8.7, 8.8, 8.9 and, 8.10 for C1, R1, R2, and C2, respectively. At first there is a reduction in blocking capabilities and finally leakage through the gate-eventually, the gate-source junction is shorted. While analyzing the discrete devices after the destructive test, it was found that the body diode was broken as well.
8.5. FAILURE MODES

Figure 8.7: Source-Drain Current $I_{SD}$, Source-Drain Voltage $V_{SD}$ in C1 during failure.

Figure 8.8: Source-Drain Current $I_{SD}$, Source-Drain Voltage $V_{SD}$ in C2 during failure.
CHAPTER 8. INVESTIGATION OF THE SURGE CURRENT CAPABILITY OF THE BODY DIODE OF SIC MOSFETS

Figure 8.9: Source-Drain Current $I_{SD}$, Source-Drain Voltage $V_{SD}$ in R1 during failure.

Figure 8.10: Source-Drain Current $I_{SD}$, Source-Drain Voltage $V_{SD}$ in R2 during failure.
8.5. FAILURE MODES

Fig. 8.11 shows a cross-sectional drawing of the SiC MOSFET where the critical point (A), right below the edge of the oxide, can be observed. It is at the corner of the source junction. The lateral voltage drop over the p-base - under the source junction - exceeds the building voltage of the source junction. The source junction is locally forward biased which activates the NPN parasitic transistor. Eventually, there will be a current filament formed at this location all the way to the drain side. When this happens, this will lead to excessive heat generation and destruction of the device. It is important to understand here that the failure mode is the activation of the NPN parasitic transistor which leads to filamentation leading to excessive heat generation. The short-circuited gate can be explained by the excessive heat produced at point A which is right below the edge of the oxide. This is a weak point of the oxide since excessive heat at this point could cause interlayer dielectric erosion leading to a gate-source short-circuit as observed in [30]. This phenomenon can already occur when the device is stored at 500 °C for 2 h. Considering the amount of current flowing through the device when the failure occurs (above 9 x rated current), the authors believe that the temperature reached at the oxide edge during a failure exceeds 500 °C. Additionally, it is the authors’ hypothesis that due to the excessive heating, solder layers and metallization may have been destroyed.

![Figure 8.11: Reverse recovery current path in the body diode within the SiC power MOSFET DMOS structure](image)

An example of the gate-source voltage and source-drain voltage of the device during a failure is shown in Fig. 8.12 for the device R2. The gate slowly fails into a short-circuit over a few ms. Similar observations have been made in [101] for SiC MOSFETs under short-circuit operation where the gate failed due to the dissipated energy 11 µs after turning off the short-circuit event. This observation supports the hypothesis of high temperature stress on the gate-oxide which leads to high leakage current in the gate. Similar observations, but during short-circuit tests of Rohm devices versus Cree 2nd generation devices, were presented in [101, 102].
8.6 Conclusion

In this work, the surge current capability of SiC MOSFET discrete devices and modules is investigated. The failure mode of SiC MOSFETs when a surge occurs in reverse direction is observed. It is the author’s hypothesis that the cause of failure of the DUTs is the latch-up of the parasitic npn-transistor in the SiC MOSFET. All the devices failed when the voltage across their body-diode exceeded a critical value, regardless of the duration of the surge current. The modules containing Schottky diodes show an identical behavior. As long as the current flowing in the reverse direction does not exceed this critical voltage, the devices could withstand repetitive surge events far above their rated current. An increase of leakage current at 1.2 kV was observed. At this stage, the presence of stacking faults in the body-diode has not been observed.
Chapter 9

Introduction of SiC MOSFETs in converters based on Si IGBTs: a reliability and efficiency analysis

The information presented in this chapter is based on Publication IX.

9.1 Introduction

Silicon carbide (SiC) offers three main benefits compared to the currently used silicon (Si) [99,103]. These benefits are higher efficiency, higher switching frequency and higher permissible junction temperature capability [104]. Over the past few years, there has been a special emphasis on SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [103]. The benefits of using SiC MOSFETs compared to Si IGBTs have been identified in many applications such as aeronautics [38], automotive applications [55], wind turbines [105], and soft-switching converters [106], [107]. The SiC MOSFET is currently under mass production, mainly due to the fact that it is comparably uncomplicated to replace Si IGBTs with SiC MOSFETs. In existing designs, one of the main reasons for this is that the gate-drive unit of a Si IGBT can easily be modified for use with SiC MOSFETs. Finally, the replacement of Si-IGBT technology with SiC MOSFET technology in the 900 V to 1.7 kV range is beneficial in terms of efficiency. However, if the efficiency is not the main target, a combination of higher switching frequency and higher temperature operation results in smaller passive components and cooling systems, respectively. This may result in a higher power density as well as significant cost reduction.

The SiC technology is fairly new and studies on the reliability of SiC MOSFETs have pointed out issues arising from imperfections in oxide quality, threshold stability, and body diode ruggedness (among others) [67,68,108,109]. With the recently introduced 3rd generation of SiC MOSFETs from Cree, the oxide layer
stability and body-diode ruggedness seem to have improved significantly [58]. Manufacturers are also considering new package designs in order to decrease the stray inductances in the package so as to fulfill high-switching-speed requirements and, therefore, taking full advantage of the SiC properties [25, 110–112]. New package concepts are also considered for high-temperature operation. A promising reliability analysis on SiC MOSFET power modules considering parallel connection as well as gate-voltage dependency has recently been presented in [57]. This study aims at comparing the reliability and the efficiency of a resonant converter topology using SiC instead of Si devices with the reference case using Si IGBTs. From a risk management point of view, it is important when introducing a new technology, to verify that the system robustness is equivalent of higher than the one of the previous technology. Additional maintenance is costly. Moreover, in most PE systems, the unavailability of the system has to be minimized in order to avoid additional costs. Consequently, an identical converter with SiC MOSFETs has also been evaluated. The comparison of these two identical converters will permit to identify how the benefits in efficiency impact the reliability. Furthermore, an analysis on how much the switching frequency can be increased while maintaining the efficiency and the reliability is also presented. Finally, introducing redundancy in the overall system is investigated. The three different topologies (Si IGBTs based, SiC MOSFETs based, and SiC MOSFET with redundancy) are finally compared through a Life Cycle Cost Analysis (LCCA) based on 20 years of lifetime.

9.2 Resonant Converter Configuration

The converter topology investigated in this paper is a full bridge LCC series load (SLR) resonant converter as shown in Fig. 9.1. LCC stands for one inductor and two capacitor connected in series in the resonant tank. The second capacitor is the winding capacitor of the transformer as shown in Fig. 9.1. It is part of a power supply for Electrostatic Precipitators (ESP) presented in [80]. A simplified schematic diagram of the system with one converter unit is shown in Fig. 9.2. The

![Figure 9.1: Full bridge resonant converter.](image)

electrical parameters of the resonant converter and the devices under investigation are stated in Table 9.1. The devices chosen are both rated 1.2 kV and 300 A
and are built with a 62 mm package based on Si technology. The calculations are made based on a case where the load is constant. The reliability study focuses on the lifetime of the semiconductors as well as the capacitors (dc and resonant). The failure rates (FIT) of the transformer and the inductors are not considered in this study since they are much lower than the other two components and do not determine the reliability of the system. The resonant tank capacitor lifetime will be unchanged for the Si and the SiC variants provided that the power rating at the load is similar. However, higher losses in the semiconductors for the Si IGBT reference case compared to the SiC MOSFET case results in higher current in the input dc capacitor, thus higher operation temperatures. Therefore, a slight increase of the FIT rate is expected for the capacitors in the reference case.

<table>
<thead>
<tr>
<th>Table 9.1: Converter Electrical Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Rating</td>
</tr>
<tr>
<td>Input Voltage</td>
</tr>
<tr>
<td>Output Current</td>
</tr>
<tr>
<td>Switching Frequency</td>
</tr>
<tr>
<td>Dc Capacitance 1</td>
</tr>
<tr>
<td>Dc Capacitance 2</td>
</tr>
<tr>
<td>Resonant tank Capacitance</td>
</tr>
<tr>
<td>Blanking Time</td>
</tr>
<tr>
<td>Si IGBT module</td>
</tr>
<tr>
<td>SiC MOSFET module</td>
</tr>
</tbody>
</table>

9.3 SiC MOSFET Module - FiT rate calculation

The SiC MOSFET power module investigated in this study is configured as a half bridge. This power module is built with parallel connection of six SiC
MOSFET chips and six anti-parallel SiC Schottky diodes per switch position, as shown in Fig. 9.3.

The mean time to failure (MTTF), defined as the inverse of the FIT rate for the SiC MOSFETs and SiC Schottky diodes are given by the manufacturer for a single chip. The FIT are shown in Table 9.2. For the Si IGBT, the module FIT rate is provided by the manufacturer and is stated in Table III. Therefore, for the SiC MOSFET, a reliability calculation in order to derive the FIT rate of the power module must be performed. In that case it will be assumed that when one of the chips fails, the module fails entirely. Thus, the calculation consists of a series connection of all the single chips contained in the module. Accordingly, the FIT rate of the module is calculated using \( \lambda_{\text{Module}} = \sum \lambda_{\text{MOSFET}} + \sum \lambda_{\text{Schottky}} \), where \( \lambda_{\text{MOSFET}} \) and \( \lambda_{\text{Schottky}} \) are the FIT rates of a single MOSFET chip and a single Schottky diode chip, respectively. Additionally, \( n \) is the number of chips which is equal to 12 for the SiC power module. The representative diagram of the SiC MOSFET module is shown in Fig. 9.3. Table 9.3 shows the calculated FIT rate for the SiC MOSFET module and the FIT rate for the Si IGBT as given by the manufacturer. It can be observed that the FIT rate of the SiC MOSFET power module is almost half that of the Si IGBT power module.

<table>
<thead>
<tr>
<th>Device (chip) Failure rate</th>
<th>[( \lambda )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET</td>
<td>3.03</td>
</tr>
<tr>
<td>SiC Schottky Diode</td>
<td>0.10</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device (chip) FIT</th>
<th>[( \lambda )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET module</td>
<td>37.56</td>
</tr>
<tr>
<td>Si IGBT module</td>
<td>75</td>
</tr>
</tbody>
</table>

### 9.4 Reliability of the Resonant Converter

From the reliability data derived in the previous section, one can estimate the reliability of the resonant converter. In order to limit the scope of the study to the power module comparison, the investigated components are the semiconductor devices in the half-bridge, the dc capacitors \( C_r \) in the dc-link, and the resonant capacitor \( C_s \) (c.f Fig. 9.2). The dc-link capacitors are composed of the parallel connection of three AVX FFVE6B0666K and two AVX FFL6B0687KJ. The system is seen as a series connection of all the components from a reliability perspective. In this study, the FIT rate of the total converter is calculated as \( \lambda_{\text{Converter}} = \sum \lambda_{\text{Module}} + \sum \lambda_{\text{Cap1}} + \sum \lambda_{\text{Cap2}} + \sum \lambda_{\text{Res, cap}} \). Thus, if one single component stops
9.5 REDUNDANT SYSTEMS

In a second step, redundant systems are considered in order to observe the impact of introducing redundancy on the system reliability. An example of how
CHAPTER 9. INTRODUCTION OF SIC MOSFETS IN CONVERTERS BASED ON SI IGBTS: A RELIABILITY AND EFFICIENCY ANALYSIS

redundancy can be achieved in this application is presented in Fig. 9.4. In fact, since each single converter is rated at 60 kW, it is possible to connect two or three units in parallel in order to increase the power rating and/or increase the possibility to fulfill the load requirement in case one converter fails. The higher efficiency and higher reliability of the SiC-based converter can allow cutting down costs (lower losses, and longer interval in between maintenance). Moreover, if the load is split among two or more converters, the total loss will go down as \( \frac{1}{n} \) for \( n \) converters connected in parallel. The reliability of such a system can be calculated using the parallel connection representation. The MTTF of parallel systems with two (2) identical components can be calculated as \( MTTF_S = \frac{n}{2\lambda} \) [113]. The FIT rate and the MTTF are stated in Table 9.4. Considering the low failure rate of the systems and the efficiency improvements, only the case of 2 converters connected in parallel is considered here.

\[
MTTF_S = \frac{n}{2\lambda}
\]

Figure 9.4: Example of parallel connection of two low voltage units

9.6 Life Cycle Cost Analysis

In order to determine the most cost-effective option among the different proposed alternatives, a LCCA is performed. The main factors affecting the LCCA are the purchase price, the operation costs, the maintenance costs and eventually the disposal costs. In addition to the initial cost, the LCCA takes into account all the user costs. All the costs are discounted and summed to a present-day value. This value is called net present value (NPV). Considering the high MTTF values, the outage cost per year is disregarded in the analysis. The maintenance is however estimated at 5000 SEK per occurrence and scheduled every 5 years for the Si based units and every 10 years for the SiC based units due to increased reliability.

In this work, three cases are analysed. The main difference between the converters is the switching semiconductor devices. The first alternative, which is taken
here as reference case, is the Si IGBT converter which is currently commercialized. The second case is the SiC MOSFET based converter and, the third is a parallel connection of two SiC-based low voltage units. The investment prices are given in Swedish Crowns (SEK) and stated in Table 9.5. The SiC power devices are, presently, about eight times more expensive than the Si power devices. Each SiC MOSFET module costs 5300 SEK and two SiC MOSFET modules are required per converter. Additionally, one SiC MOSFET driver has to be taken into account. Therefore, the additional costs when using SiC technology compared to Si are estimated at around 15000 SEK. Finally, the cost of the redundant system is two times the cost of the single system.

As it can be seen, the reliability for the SiC converter with redundancy is 1.6 times higher than for the reference case. Moreover, the redundancy results in a power loss reduction of 10 MWh per year which leads to savings of 4000 SEK per year based on an electricity rate of 0.4 SEK per kWh [114]. Finally, the NPV for the SiC MOSFET (single) is 32.5 % lower than for the Si IGBT case. The case with redundancy has an almost identical NPV. This is mainly due to the large investment cost and the relatively short duration (20 years) of the economic lifetime of this product. However, considering the noticeable reliability improvements, increasing the economic lifetime of the product would be the natural step forward.
Table 9.4: Comparison of the three different converters: losses, efficiency, FIT, and MTTF

<table>
<thead>
<tr>
<th>Technology</th>
<th>Losses [W]</th>
<th>Efficiency</th>
<th>FIT</th>
<th>MTTF (years)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si IGBT Converter (ref. case)</td>
<td>1200</td>
<td>98</td>
<td>128.74</td>
<td>572.78</td>
</tr>
<tr>
<td>SiC MOSFETs Converter</td>
<td>350</td>
<td>99.48</td>
<td>199.3</td>
<td>917.45</td>
</tr>
<tr>
<td>SiC MOSFETs Redundant</td>
<td>175</td>
<td>99.71</td>
<td>-</td>
<td>82.95</td>
</tr>
</tbody>
</table>

Table 9.5: Life Cycle Costs Analysis - Converters

<table>
<thead>
<tr>
<th>Converter</th>
<th>Si-IGBT</th>
<th>SiC MOSET</th>
<th>Redundant (SiC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Investment Costs</td>
<td>30 000 SEK</td>
<td>45 000 SEK</td>
<td>90 000</td>
</tr>
<tr>
<td>Failure Rate</td>
<td>128.74</td>
<td>199.3</td>
<td>82.95</td>
</tr>
<tr>
<td>Loss/Year</td>
<td>12 MW</td>
<td>4 MW</td>
<td>2 MW</td>
</tr>
<tr>
<td>Electricity Costs</td>
<td>4800 SEK</td>
<td>1600 SEK</td>
<td>800 SEK</td>
</tr>
<tr>
<td>Outage Costs / Year</td>
<td>negligible</td>
<td>negligible</td>
<td>negligible</td>
</tr>
<tr>
<td>Preventive Maintenance</td>
<td>5 years</td>
<td>10 years</td>
<td>10 years</td>
</tr>
<tr>
<td>Costs / Maintenance</td>
<td>5000 SEK</td>
<td>5000 SEK</td>
<td>5000 SEK</td>
</tr>
<tr>
<td>Interest rate</td>
<td>5 %</td>
<td>5 %</td>
<td>5 %</td>
</tr>
<tr>
<td>Economic Lifetime</td>
<td>20 years</td>
<td>20 years</td>
<td>20 years</td>
</tr>
<tr>
<td>Net Present Sum</td>
<td>105 895 SEK</td>
<td>71 494 SEK</td>
<td>105 725 SEK</td>
</tr>
</tbody>
</table>
9.7 Conclusion

In this application, the redundancy is attractive in terms of power loss. Both single and redundant converters result in a lower NPV calculated over 20 years. The case without redundancy is economically more attractive due to the consequent savings brought by this solution. The next step towards the integration of SiC devices into converter designs made previously with Si is the reduction of the system passive by increasing the switching frequency. The power density can be further increased by allowing a higher temperature of operation. In this way, the benefits of SiC can be fully used and SiC will become even more economically interesting. From a risk management point-of-view the SiC MOSFET based system has an improved reliability while being less costly. Furthermore, the improved reliability permits to reduce the planned and unplanned maintenance costs as well as minimize the converter unavailability. Introducing redundancy will only be interesting if the converter expected lifetime is increased. This can clearly be considered in accordance to the improvement of the reliability.
Chapter 10

Conclusions and Future Work

10.1 Conclusions

In this thesis, various reliability aspects of SiC semiconductor devices have been discussed. The work has followed the evolution of the SiC devices, in particular the SiC MOSFET from the early generations to the latest generation as of today. To introduce the thematic, this work introduce notions of reliability engineering as well as the relevant tests that are performed in order to evaluate the device robustness. A summary of potential remaining issues for the different SiC devices is provided.

For the SiC MOSFET, an evaluation of the robustness towards relevant stress was performed. First, the challenges regarding parallel connection of SiC MOSFET discrete devices is investigated. The parallel connection of SiC devices is required in order to compensate for the smaller chip size in comparison with similar Si devices. The parallel connection can also be used in order to reduce the ON-state resistance of a switch position and therefore reduce the conduction losses. The conclusions were that the parallel connection of SiC discrete MOSFET is not a problem also when the devices have slightly different characteristics.

In the same context, the impact of the imbalance in stray inductances in the gate-loop of a standard 62 mm SiC MOSFET module populated with parallel connected SiC MOSFET chips (and SiC Schottky diodes) was performed. The 62 mm module has half-bridge configuration and a housing designed previously for Si IGBT chips and Si diode. From this point of view, Si IGBT modules can easily be replaced by SiC MOSFET modules wile minimizing modifications in the system layout. It was found that the gate-loop inductances are not identical for the higher and lower switch position. While this has not been problematic for Si technology switching at lower speeds, it was found to be not adequate for the higher switching frequency made possible with SiC. When switching at higher speeds, voltage overshoot across the gate oxide and cross talk can occur. It was also found that, when using this housing, the design has to minimize the stray inductance
between the gate driver and the gate pins of the 62 mm module. Moreover, the external gate resistance should not be too small. Finally, when targeting higher switching speeds, the housing should be improved.

Long term tests on the gate-threshold voltage stability and body diode conduction have been performed for the SiC MOSFET. Very little voltage drift has been noticed when connecting the gate-source pins to the most negative allowable voltage for 1000 h. No traces of stacking faults were found. This reveals an improvement from first to second (and third for Wolspeed) generations of SiC MOSFET discrete devices. The long-term tests on humidity revealed that some modules situated outdoors had already started to degrade after 6000 hours of operation.

The short-circuit behavior of the SiC MOSFET has been evaluated in non-destructive tests in order to determine how fast it is possible to detect a short-circuit event. An adequate driver circuit with an integrated short-circuit protection has been developed and validated experimentally. To support the need of fast detection, a simulation model has been developed by Mietek Bakowski and several cases of short-circuit event with varying circuit parameters have been investigated. The analysis support the need to detect and turn OFF the short-circuit fault as soon as possible in order to limit local heating and further propagation of the heat towards the chip top surface.

The ruggedness of the SiC MOSFET body diode was further investigated in order to verify the possibility of designing diode-less power electronics converters when using SiC. Surge currents where applied to SiC MOSFET discrete devices and modules. The device failure has not been related to stacking faults but to the triggering of the npn parasitic bipolar transistor which is present in the device structure. Multiple surges have shown no degradation in the device below the critical voltage triggering the npn parasitic transistor. Further investigations have to be performed in order to exclude the presence of stacking faults in the device before failure.

Finally, a life-cycle cost analysis has been performed in order to investigate the economical impact of introducing SiC devices in already existing power electronic converter designs using Si IGBTs. From a risk management point-of-view it was shown that the introduction of SiC MOSFETs in place of Si IGBTs improves the reliability of the converter considerably.

For the SiC BJT and SiC JFET, the short-circuit behaviour has been investigated and analyzed in detail. Also for these devices drivers with protection against short-circuit for both have been realized and verified. Simulation models have also been developed by Mietek Bakowski. The analysis of the thermal distribution within the chip during a fault reveals that there is also a need to turn OFF the SiC BJT and JFET quickly, but the temperature rise is not as rapid as for the SiC MOSFET.

In conclusion, this work has investigated various reliability aspects of SiC MOSFETs, but also has covered some reliability aspects of SiC JFETs and SiC BJTs.
10.2 Suggested Future Work

The parallel connection of SiC MOSFETs has been implemented with discrete devices and modules in converter designs in [10,55]. However, in both designs, one driver per device (or module) has been used. This is costly and is consuming space. The possibility to drive a whole switch position consisting of several parallel connected discrete SiC MOSFETs or modules still has to be investigated. The performance of such a structure would have to be evaluated.

The short-circuit behavior of SiC switches has been widely covered. However, the dynamics of the thermal problems have not been investigated sufficiently. Also, other types of short-circuits (type III, and IV) are still to be investigated.

For the SiC MOSFET, the parasitic BJT turn-ON when surge current flows through the body diode should be studied in more details. The phenomena has been observed but not thoroughly verified by simulations and decapsulation of the device.

For ultra-fast switching applications, new module designs are necessary. These concepts must be studied from several points-of-view such as thermal robustness, dielectric aspects, and humidity among others.

Further investigations on humidity are necessary and must be done with different types of tests, preferably with cycles to get condensation. A solution would be to develop special packages for demanding applications. Passivation and filling materials for harsh environments have to be further investigated. Possibly, the JTE should be revised, especially for high-voltage devices.
Appended Publications

Publication I


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Experimental investigations of static and transient current sharing of parallel-connected Silicon Carbide MOSFETs

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Keywords
«Silicon Carbide (SiC)», «MOSFET», «Parallel operation», «MOS device», «Switching losses»

Abstract
An Experimental performance analysis of a parallel connection of two 1200/80 mΩ silicon carbide SiC MOSFETs is presented. Static parallel connection was found to be unproblematic. The switching performance of several pairs of parallel-connected MOSFETs is shown employing a common simple totem-pole driver. Good transient current sharing and high-speed switching waveforms with small oscillations are presented. To conclude this analysis, a dc/dc boost converter using parallel-connected SiC MOSFETs is designed for stepping up a voltage from 50 V to 560 V. It has been found that at high frequencies, a mismatch in switching losses results in thermal unbalance between the devices.

Introduction
In recent years a dramatic improvement of both material properties and fabrication processes for silicon carbide (SiC) power semiconductor components has been observed. Currently, several types of power transistors in SiC are available on the market. Common to all these components is that the chip sizes are still small compared to their silicon counterparts. This means that in order to achieve high current ratings, several chips have to be connected in parallel, either as separate components or in a multi-chip module. Several attempts to achieve this have already been presented [1], [2]. However, many details regarding these issues are still uncertain, especially issues regarding transient mismatches. For SiC junction field effect transistors (JFETs) detailed investigations regarding parallel connection have been presented in [3], [4] and [5]. For parallel-connected metal-oxide semiconductor field-effect transistors (MOSFETs) in SiC, however, only little has been presented so far. One particular point of interest is the fact that the threshold voltage of the SiC MOSFETs available on the market has a negative temperature coefficient. The question is if this property could have adverse effects on static and transient currents sharing. In [6] switching transients of SiC MOSFETs have been presented, and in [7] parallel-connection issues have been treated. The turn-ON transients of parallel-connected SiC MOSFETs reported in [7] are, however, quite oscillative. It is the opinion of the authors of the present paper that these waveforms could be improved without losing switching speed. Such waveforms will be presented in the present paper using a double-pulse test setup. Additionally, in [7] it is stated that small imbalances in the stray inductances may introduce severe mismatches in the individual currents of parallel-connected SiC MOSFETs. The authors of the present paper agree that this may occur. However, if the circuit is reasonably symmetrical, very good transient current sharing and low switching energy losses may be obtained, even if the parallel-connected SiC MOSFETs have different characteristics, and even if a very simple gate driver is used. This will also be shown in the present paper along with measurements of static current sharing of parallel-connected
devices. To conclude this analysis, a dc/dc boost converter has been built with parallel-connected SiC MOSFETs as main switch.

**Components and Circuit**

The performance of the parallel connection of two SiC MOSFETs, has been investigated. At first, static performance is measured and then a double-pulse test is executed to analyze the switching performance of the parallel-connected MOSFETs. The main parameters of the Cree CMF20120 SiC MOSFET used are listed in Table I.

<table>
<thead>
<tr>
<th>Table I: CMF20120 – SiC MOSFET parameters (Cree)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS} )</td>
</tr>
<tr>
<td>1200 V</td>
</tr>
</tbody>
</table>

**Static Characteristics**

A static test is performed in order to investigate the current sharing of the two parallel MOSFETs. They are mounted on a common heat sink and current is fed through them using a current source. The gate signal is common to both MOSFETs and is supplied by a current-limited voltage source as shown in Fig. 1. At regular intervals of 3 minutes \( I_1 \) and \( I_2 \), i.e. the currents flowing through \( M_1 \) and \( M_2 \), are measured as well as their common drain-source voltage, \( V_{DS} \). The case temperatures of \( M_1 \) and \( M_2 \) are also measured using an infrared thermal camera as shown in Fig. 1. The average case temperatures \( (T_1 \) and \( T_2) \) are then derived from the image by using software provided by the manufacturer of the infrared thermal camera. The test is performed with three values of shared current \( (I_{shared} = I_1 + I_2): 10\, \text{A}, 20\, \text{A}, \) and \( 25\, \text{A}. \) Higher currents give rise to steady-state case temperatures higher than \( 100^\circ \text{C}, \) which is not desirable.

![Fig. 1 : Static test set-up and thermal image of the set-up (MOSFETs and heat-sink)](image)

The measurements results with a shared current of 20 A are plotted in Fig. 2. The results obtained for 10 A and 25 A are plotted in Fig. 3 and 5 respectively. The evolution of the temperatures \( (T_1 \) and \( T_2), V_{DS}, \) and the two drain currents \( (I_1 \) and \( I_2) \) have also been plotted. \( V_{DS} \) as a function of the temperature has also been plotted and is used to calculate the temperature coefficient.
From the plots, it can be seen that the average difference between the individual drain currents is approximately 0.6 A at 10 A, 0.4 A at 20 A, and 0.7 A at 25 A. In all three cases, the higher current flows through M1, resulting in a slightly higher case temperature, which is confirmed by the measurements. With time, the temperature in both devices increases until it reaches equilibrium.

The results obtained are very promising since the sharing is constant for all three cases. The stabilization ensures that no thermal runaway is to be expected from the current unbalance, the latter being reasonable. From Figs 3 and 4, it can be seen that the current in the hotter MOSFET M1 slightly decreases as its temperature increases. In fact, the on-state resistance of the SiC MOSFET has a positive temperature coefficient. Thus, the drain-source voltage $V_{DS}$ increases almost linearly as the temperature increases as well as its on-state resistance, $R_{DS(on)}$. This is very well observed in Fig. 2 and a positive temperature coefficient of $18 \cdot 10^{-4} \frac{\Omega}{^\circ C}$ could be identified.
Double-Pulse Test

Apart from the investigation of the static current sharing at different temperatures, it is also important to study the switching performance of the devices when they are parallel connected. For this purpose, several devices have been sorted with regards to their on-state resistance $R_{ds(on)}$ and their threshold voltage $V_{th}$. Then they have been tested in 4 different pairs to investigate if the current sharing is still acceptable with most different device characteristics. The device characteristics, which have been measured with the curve tracer 370 A from Tektronix are listed in Table II. The on-state resistance for a given gate voltage (24 V here) is derived by taking the slope of the i-v characteristics for this gate voltage.

<table>
<thead>
<tr>
<th>Device</th>
<th>$R_{ds(on)}$ [mΩ]</th>
<th>$V_{th}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>85.3</td>
<td>3.22</td>
</tr>
<tr>
<td>$M_2$</td>
<td>85.5</td>
<td>3.140</td>
</tr>
<tr>
<td>$M_3$</td>
<td>112.2</td>
<td>2.88</td>
</tr>
<tr>
<td>$M_4$</td>
<td>70.0</td>
<td>2.86</td>
</tr>
<tr>
<td>$M_5$</td>
<td>75.4</td>
<td>2.65</td>
</tr>
<tr>
<td>$M_6$</td>
<td>75.7</td>
<td>3.26</td>
</tr>
</tbody>
</table>

A schematic diagram of the circuit used for the double-pulse test (DPT) and its layout are shown in Fig. 5 and 7. The circuit consists of a voltage supply $V_{DC}$, a capacitor in parallel with the voltage source $C$, an inductor $L$, and two SiC Schottky diodes $D$. The two MOSFETs and the two SiC Schottky diodes are mounted on the same heat sink. The driver used is a simple resistive totem-pole with an additional gate resistor $R_G = 0.56 \, \Omega$. With the transistor’s internal gate resistor of 5 Ω, the total gate resistance is 5.56 Ω. The parameters of the experimental setup are stated in Table III.

The resulting experimental waveforms are shown in the following sections for different devices pairs. The currents shown in Fig. 7 were measured with CWT ultra-mini Rogowski coils without measuring voltages in order to keep the parasitical stray inductance and stray capacitance low. Then the test was repeated while measuring both currents and voltages. The voltages are measured with Tektronix P5100 high-voltage probes. The delays of the voltage and current probes were adjusted as well in order to compute the switching losses correctly. Regarding the static current sharing during the double-pulse test, no significant differences compared to the static test could be observed.

![Fig. 5 : Double-pulse test schematic](image1)

![Fig. 6 : Double-Pulse Test Layout](image2)

| Table III : Parameters of the Experimental Setup |
|-----------------|---------------|
| Dc supply voltage, $V_{DC}$ | 600 V         |
| Inductor $L$    | 200 µH        |
| $R_G$           | 0.56 Ω        |
| Gate Driver Supply | -5V / 24 V   |
| SiC Schottky diode $D$ | SDP30S120 |

![Table II: CMF20120 – SiC Power MOSFETs Characteristics (Cree)](image3)
Devices with the same threshold voltage and the same on-state resistance

The first set of measurements deals with devices having similar characteristics, $M_1$ and $M_2$. One complete switching pulse is shown in Fig. 7 and the turn-on and turn-off transients are shown in Fig. 8. As shown in Fig. 8, the two devices are turned on in approximately 20 ns. $M_1$ turns on faster and takes a higher current than $M_2$ as it has a slightly lower on-state resistance. The two devices are turned off in the same time in 20 ns as well. The unbalance in current sharing is stable and within 10%. With a simple driver, very low oscillations in the switching transients have been observed even at high switching speeds.

The turn-on losses are 123 $\mu$J and 133 $\mu$J for $M_1$ and $M_2$ respectively. The turn-off losses are 30 $\mu$J and 56 $\mu$J. Thus, the total switching losses are 156 $\mu$J and 186 $\mu$J.

![Fig. 7: Drain currents of the parallel-connected MOSFETs during a complete pulse of the DPT.](image1)

![Fig. 8: Turn-on and turn-off transients of the parallel-connected MOSFETs with similar characteristics.](image2)

Devices with different on-state resistances

For the second set of measurements two devices, $M_3$ and $M_4$, which differ by their on-state resistance have been selected. $M_3$ and $M_4$ have an on-state resistance of 112.2 $\Omega$ and 70.0 $\Omega$ respectively. This represents a variation of 37.5 %. However, as shown in Fig. 9, the sharing is within 20 % at the beginning of the switching pulse and 10 % at the end of it. The positive temperature coefficient of the
SiC MOSFET helps balancing the current sharing. The devices turn on at the same time in approximately 20 ns. $M_4$ is taking longer time to switch off. In this case, the switching losses are 200 µJ and 234 µJ for $M_3$ and $M_4$ respectively. Those are 21 % higher than for the previous case with similar devices.

For the third set of measurements, two devices which differ in threshold voltage by 0.61 V, $M_5$ and $M_6$, have been selected. Their respective threshold voltages are 2.65 V and 3.26 V. The on-state resistances are 75.4 Ω and 75.7 Ω for $M_5$ and $M_6$ respectively.

The threshold voltage does not substantially influence the steady-state current sharing. From Fig. 10, it can be clearly seen that $M_5$ takes slightly higher current than $M_6$. Since the voltage across the parallel-connected MOSFET is the same, $M_5$ has more switching losses. Its on-state resistance increases slightly and the current sharing is quite good right after turn-on. The sharing stays within 10-12 % during the whole switching pulse. For both turn-on and turn-off, the switching transients occur simultaneously and within approximately 20 ns. The switching losses in this case are 224 µJ and 200 µJ for $M_5$ and $M_6$ respectively.
Devices with different threshold voltage and different on-state resistance

For the last set of experiments, two completely different devices have been chosen. The first device, M₃, has a threshold voltage of 2.88 V and an on-state resistance of 112.2 Ω. The second device, M₅, has a threshold voltage of 2.65 V and an on-state resistance of 75.4 Ω. The resulting waveforms are shown in Fig. 11. The sharing is very good after the switching transients and is within 8% at the end of the switching pulse. The turn-on and turn-off transients are approximately 20 ns. The two devices turn on and turn off simultaneously. At turn-on, the devices have an almost perfect current sharing. A possible explanation to this is that the unbalances in threshold voltage and in on-resistance compensate each other. In this case, the total switching losses are 256 µJ and 235 µJ for M₃ and M₅ respectively. The difference in switching losses is due to extra losses at turn-on for M₃.

![Fig. 11: Turn-on and turn-off transients of the parallel-connected MOSFETs with different R_ds(on) and different V_th](image)

**Discussion**

For all cases, the turn-on and turn-off times are in the range of 20 ns. Since the on-state voltage drop has a positive temperature coefficient, the system is trying to balance the power sharing among the two parallel-connected devices. As expected, a mismatch in the device characteristics results in different switching losses among the two devices. The on-state sharing is also deteriorated. These mismatches could have an effect on the power loss sharing among the devices in a converter steady-state operation. Therefore, a boost converter was designed and built in order to verify if the mismatch in power losses is within acceptable bounds.

**Boost Converter with parallel-connected MOSFETs**

In order to validate the safe realization of the parallel connection in steady-state operation, a dc/dc boost converter is built. The converter has a nominal input power of 6 kW and the switching frequency is chosen to be 100 kHz. In order to have full input current and full output voltage without dissipating 6 kW, the converter was tested at lower power (900 W). The parameters of the dc/dc boost converter are presented in Table IV.

The schematic of the SiC boost converter is depicted in Fig. 14. The switch is made of parallel-connected CMF20120 – Silicon Carbide Power MOSFETs from Cree 1200 V /33 A ratings and a SPD30S120 SiC Schottky Barrier Diode with ratings 1200 V / 30 A from Semisouth. The MOSFETs are controlled by the same driver which was used to perform the DPT but with a higher gate resistance in order to limit the high di/dt. The inductor is designed with a PM 74/59 core with Litz wire and has been made in order to minimize the resistive and magnetic power losses [8].
The SiC devices are characterized by very low voltage drop at room temperature (approximately 0.61 V). The on-state losses per switch are then 7 W per transistor. The on-state losses of the SiC Schottky diode are 5 W. The other main contribution to the power losses are the switching losses. From the switching losses measured in the double-pulse test, the switching losses are approximated to 10 W per switch. The total semiconductor losses are approximately 29 W.

### Experimental Results

The dc/dc converter has been tested experimentally at rated input current with a resistive load. The recorded electrical quantities are the gate-source voltage $V_{gs}$, the MOSFETs currents $I_{m7}$ and $I_{m8}$ and the drain-source voltage of the parallel-connected devices $V_{ds}$. The currents are measured at the source leg of the SiC MOSFET. The electrical measurements are done using CWT ultra-mini Rogoswki coils for the switch currents, Tektronix P5100 high-voltage probe for $V_{ds}$ and a standard low voltage probe for $V_{gs}$. These quantities are shown in Fig. 14. The reached output voltage is 560 V and the output power is 870 W. Thus, the semiconductor power losses are 30 W.

The input of current $I_m = 18$ A is shared between $M_7$ and $M_8$. The sharing is within 20% as $I_{m7} = 10$ A and $I_{m8} = 8$ A.

### Table IV : Switch parameters

<table>
<thead>
<tr>
<th>Device</th>
<th>$R_{ds(on)}$ [mΩ]</th>
<th>$V_{th}$ [V]</th>
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<tr>
<td>$M_7$</td>
<td>61</td>
<td>3.3</td>
</tr>
<tr>
<td>$M_8$</td>
<td>64.7</td>
<td>3.22</td>
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</table>

### Table V : Parameters of the converter

<table>
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<th></th>
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<tr>
<td>Input Voltage/Current</td>
<td>50 V / 18 A</td>
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<tr>
<td>Output Voltage/Current</td>
<td>560 V / 1.6 A</td>
</tr>
<tr>
<td>Duty cycle, $D$</td>
<td>0.91</td>
</tr>
<tr>
<td>Frequency, $f_{sw}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td>SiC Schottky diode D</td>
<td>SDP30S120</td>
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<tr>
<td>Load</td>
<td>360 Ω</td>
</tr>
<tr>
<td>Inductor L</td>
<td>150 μH / 25 A</td>
</tr>
<tr>
<td>Output Capacitor C</td>
<td>40 μF</td>
</tr>
<tr>
<td>$R_G$</td>
<td>10 Ω</td>
</tr>
<tr>
<td>Gate Driver Supply</td>
<td>-5V / 24 V</td>
</tr>
</tbody>
</table>
Switching Transients

In order to be able to compare the switching transients with the double-pulse test, the input voltage of the boost converter is increased to 54 V in order to have 600 V across the parallel-connected MOSFETs and at the output. The switching transients are shown in Fig. 15. Both MOSFETs turn on in less than 25 ns, which is slightly slower than the speed obtained in the double-pulse test due to the larger total gate resistor (15 Ω). $M_8$ has more turn-on losses and thus, heats up more than $M_7$. The calculated losses are 121 µJ and 102 µJ for $M_8$ and $M_7$ respectively. As a result, its on-state resistance will increase. The total switching losses are 10.24 W for $M_7$ and 12.1 W for $M_8$. A possible explanation to the higher turn-on losses for switch $M_8$ is an unbalanced parasitic inductance in the experimental layout due to the placement.
The temperature sharing is shown in Fig. 16 and it is clear that \( M_8 \), on the left, is suffering from significant heating as a result of higher switching losses than \( M_7 \). This is an issue at high frequencies, as it can be seen on Fig. 16. The MOSFET on the left, \( M_7 \), is heating much more than the one on the right, \( M_7 \). The system doesn’t have time to balance itself and tends to thermal runaway. One reason for this unbalance might be the converter layout. In fact, an unbalance in parasitic inductances can increase the unbalance in switching losses among the devices.

**Conclusion**

From experiments on two parallel-connected SiC MOSFETs, it was found that the relative unbalance in static current sharing was approximately 5%. At elevated temperatures this mismatch was even reduced. From double-pulse tests it was found that the sharing is better when the devices share similar characteristics. However, the devices still have good sharing when they have similar on-resistances even if the threshold voltages are different. Extreme values of on-resistances are to be avoided. The loss values are, however, very low. Compared to previously presented results, the turn-ON waveforms in the present paper are less oscillative even if the turn-ON time was only approximately 20 ns. A dc/dc boost converter with parallel-connected MOSFETs was built to verify the steady state operation of parallel-connected devices. It was found that unbalance in switching losses can lead to thermal runaway at high frequency operation.

**References**


Publication II


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Analysis of Parasitic Elements of SiC Power Modules With Special Emphasis on Reliability Issues

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Abstract—Commercially available silicon carbide (SiC) MOSFET power modules often have a design based on existing packages previously used for silicon insulated-gate bipolar transistors. However, these packages are not optimized to take advantage of the SiC benefits, such as high switching speeds and high-temperature operation. The package of a half-bridge SiC MOSFET module has been modeled and the parasitic elements have been extracted. The model is validated through experiments. An analysis of the impact of these parasitic elements on the gate-source voltage on the chip has been performed for both low switching speeds and high switching speeds. These results reveal potential reliability issues for the gate oxide if higher switching speeds are targeted.

Index Terms—Multichip modules, packaging, power MOSFETs, reliability, silicon carbide (SiC).

I. INTRODUCTION

Silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) have undergone great development over the past few years [1]–[3]. With the emerging third generation of SiC MOSFETs, the oxide-layer stability seems to have improved significantly [4], [5]. Although the wide-bandgap technologies are improving rapidly, there are still challenges to overcome in order to fully utilize their advantages while ensuring a high reliability [3], which is an important and nonnegligible aspect [6]. The main advantages of SiC MOSFETs are the higher maximum switching frequency, lower ON-state voltage, and higher maximum operating temperature capability compared with silicon (Si) insulated-gate bipolar transistors (IGBTs) [7].

In spite of the tremendous advantages of SiC transistors at the chip level, the expected high switching speeds may be compromised due to the impact of parasitic elements of the electrical circuit, and the interaction of these with parasitic capacitances of the SiC transistors [2], [4], [5], [8]. The design of commercially available SiC modules is often based on existing packages previously designed for Si-IGBTs [9]. The design and packaging issues for such a module are presented in [10]. It was found that the difference in the placement of the switching devices results in a difference in the parasitic inductances for each of the switching devices in the power module. Higher switching speeds and lower ringing can reduce the switching losses, which are a major component of the overall losses of power converters operating at high frequencies [11]. As recently presented in [12], it is possible to build ultralow inductance power modules by means of an antiparallel placement of the switching cells inside the module. More recently, it was shown that switching losses can be reduced by improving the peak-current sourcing capability of the gate-drive circuit [13]. Similarly, an active gate driver suppressing parasitic-induced cross-talk of SiC devices in a phase-leg configuration has been presented in [14] and [15]. Efforts have been put into modeling packages that will permit a better utilization of the advantages of SiC devices regarding high temperature and high switching speeds. In [16], the status and trends for the packaging of SiC power semiconductors are discussed. It is also mentioned that new packages are essential in order to improve the reliability as well as the thermal and electrical properties of SiC power modules. According to these new trends, in [17]–[20], recent advances in all-SiC power modules technology are presented. High-temperature modules are presented in [18]–[21]. A low-inductance package solution is also presented in [19] which addresses both the high-temperature and the parasitic issues. Modules targeting high switching frequency operation are presented in [20] and [22].

This paper assesses the impact of parasitic inductances in the gate loop of the SiC MOSFETs inside a commercially available power module housing, and the impact of these parasitic inductances on reliability. In fact, it is possible to measure the external values of the gate-source voltage and current as well as the drain–source voltage and current from the terminals of the power modules. However, very little has yet been investigated on what occurs inside, more specifically in the gate loop. Recently, an extraction procedure for SiC power modules has been presented in [23]. In contrast to
This paper presents on-chip measurements that validate the parasitic extraction method. The objective of this paper is to determine whether there are higher transients inside the housing of the power module compared with what is observable from the outside. Based on this information, it may then be possible to predict whether the internal gate-loop inductance has an impact on the reliability of SiC power MOSFETs. Higher voltages on the gate can strongly influence the lifetime of the gate oxide of SiC Power MOSFETs [4].

First, in Section II, an extraction of the internal parasitic elements of a commercially available SiC MOSFETs power module has been realized using the software ANSYS Q3D. The extracted parasitic elements are then used to develop an electrical simulation model. Experimental measurements are performed in order to verify the accuracy of the developed model (Section III). The measurements are first performed directly on a chip inside the module in order to obtain a detailed verification of the accuracy of the model. Moreover, in Section IV, the impact of the gate-loop inductance on the reliability of SiC Power MOSFETs is discussed based on the simulation model. Finally, Section V concludes this paper.

II. MODELING AND EQUIVALENT CIRCUIT

The investigated module in this paper is the commercially available CAS300M12BM2 1.2 kV/300 A from Cree (now Wolfspeed). It is a half-bridge SiC power MOSFET module encapsulated in a standard 62-mm package. This package is an existing package used for Si-IGBT-based modules. Fig. 1 shows a side view of the module reconstruction in ANSYS Q3D. This software has previously been used for estimating the stray inductance of Si-IGBTs [24]–[26] and for the design of an ultralow inductance SiC MOSFET module [10], [12]. The parasitic elements used in the simulation model are extracted from the module reconstruction by ANSYS Q3D. The parasitic elements of the module are extracted from the geometry and material properties of the actual module and the results are the capacitance, inductance, and resistance matrices at a given frequency. The module is then simulated with LTSpice using the extracted parasitic elements. The device model (C2M0025120D) used for the simulation in LTSpice was provided by the device manufacturer Cree (Wolfspeed). Fig. 2(a) shows a top view of the module where $V_{ds}$ and $V_{gs}$ indicate the location where the on-chip measurements were performed. The chips 1–6 correspond to the chips situated in the lower switch position of the half-bridge. Similarly, chips 7–12 are situated in the upper switch position. The reader can appreciate the difference in chip placement within the power module. Fig. 2(b) shows a schematic of the parasitic inductances and resistances in the module. In addition to these, there are parasitic capacitances between all the nets and the module base plate and in between the different metal parts. For clarity, these have been omitted in the schematic, but they are present in the simulation. The extracted parameters reveal that the main inductance in the gate loop is 3–4 times higher for the chips situated in the lower switch position compared with those situated in the upper switch position. This issue has been previously mentioned in [5] and can be understood by looking at Fig. 2(a), where the lower switch position is situated on the right half of the module. The gate signal has thus to cross the whole module to reach the chip gate pad situated at the far right of the module. The simulation model is verified with two tests. The following section presents these tests in detail. Fig. 2(a) also highlights that the chip placement in the upper switch is different from the chip placement in the lower switch. A schematic of the circuit including the parasitic elements of the module and the
parasitic elements involved when connecting the module to the dc bus and driver circuits is shown in Fig. 2(b). The gate resistors $R_g$ are also included since they influence the switching transients in the gate loop. The stray inductance $L_g$ represents the addition of the inductance of the lead connecting the driver to the module gate terminals as well as the inductance resulting from the gate-driver output tracks. The dc-bus connection stray inductance and stray resistance are also represented here since they are included in the simulation model.

### III. Experimental Verifications of the Model

In order to verify the model, two tests have been performed. The first is a standard double-pulse test (DPT) where the drain–source voltage and gate-source voltage of the lower SiC MOSFET position are measured at the corresponding module terminals. The second is a single-pulse test where the same voltages are measured directly on the chip as shown in Fig. 2.

In both the simulations, the stray inductance $L_{g\_stray}$ corresponds to the parasitic inductance of the leads between the gate-driver output and the gate and source terminals of the module. The stray inductance of the dc bus bars has been estimated such that the frequency of the oscillations in the simulation matches the frequency of the oscillations in the experiments. Doing so, it was found that the amplitudes (current and voltage) of the oscillations in the simulation match those obtained from the experiments. The dc-bus inductance influences the frequency and the amplitude of the oscillations in such a way that a higher inductance results in higher voltage amplitude and lower oscillation frequency. Similarly, a lower dc-bus inductance results in lower voltage amplitude and higher oscillation frequency.

#### A. Double-Pulse Test: Measurements on the Terminals

The first test is a DPT with the measurement done at the module terminals. In the simulation model, the measurement points are identical to those in the experiment. The parameters of the DPT circuits are given in Table I. The DPT measurements are shown in Fig. 3(a) and (b) for the turn-ON and turn-OFF, respectively. The simulation results for the same conditions are shown in Fig. 4(a) and (b). In this case, the experimental results confirm the simulation. It can be noted that the frequency and amplitude of the oscillations in the simulation are similar to those recorded during the experiment.

#### B. Single-Pulse Test: Measurements on the Chip

To obtain a detailed verification of the model, a single-pulse test was performed on-chip. To measure transients directly on the chip a special setup has been realized. The module has been opened and the voltage probes are inserted through the silicone gel at the locations indicated in Fig. 2. The measured chip is the sixth chip in the model, which is the furthest away from the gate-source terminals of the power module. The drain current is measured at the phase terminal. The setup parameters are stated in Table II, where the parasitic inductance of the bus bars has been estimated. For safety reasons, the transients are measured at 200 $V_{ds}/100$ A for $V_{ds}$ and $I_d$. Similarly, the on-chip $V_{gs}$ measurements are done at 100 $V_{ds}/50$ A. The simulation is done according to the parameters stated in Table II.

The results of the single-pulse tests are shown in Figs. 5 and 6, with the simulation (top) and the measurement (bottom). Fig. 5 shows the drain–source voltage $V_{ds}$ on the chip and the drain current $I_d$. The measurement in Fig. 6(b) is the gate-to-source voltage $V_{gs}$ measured as shown in Fig. 2. The measurement of $V_{gs}$ has not been realized exactly on the gate pad, which probably explains the additional oscillations observed in Fig. 6(b).
IV. DISCUSSION AND RELIABILITY CONCERN

Comparing the results from the simulations and experiments, it is found that the agreement is good. The model will now be used to investigate the reliability issues of the gate oxide, which may arise if the gate resistor is reduced or if the gate-loop inductance is increased. In real applications where high efficiency is targeted, a fast switching performance is needed in order to reduce the switching losses. However, if this is done, oscillations are observed at the gate-source terminals as shown in Fig. 7. The simulation results show that the overshoot and the oscillations observed at the gate-source terminal are not present directly on the chip (see Figs. 8 and 9). These results are explained in detail in the following.

To observe the effect of a gate-resistor reduction or an increase of the inductance in the gate loop, three different simulations are performed. First, a nominal case matching the characteristics of the driver used to validate the simulation model in the previous section is investigated. Second, a simulation with a reduced gate resistance (recommended in the device data sheet) and unchanged gate-driver parasitic inductance is studied. Finally, the gate-driver parasitic inductance was increased to investigate the case where the driver is not situated...
close to the device. The two latter cases are regarded as worst case scenarios. In fact, a higher voltage overshoot and possibly higher ringing are expected. The simulation parameters for these three cases are given in Table III.

In all the cases, cross-talk is observed on the upper switch position when turning ON and OFF the lower switch position. Cross-talk in wide-bandgap half-bridge modules has been explained in detail in [27] and [28]. The negative spike in the gate voltage of the high-side switch observed at the turn-OFF of the low-side switch is a typical phenomenon caused by the Miller effect. This can be seen in Figs. 9, 11, and 13. There is also a positive spike on the high-side switch observed at the turn-ON of the low-side switch due to cross-talk. Eventually, if these oscillations are not damped by a proper driver design or a snubber, self-sustained oscillations will result in a short-circuit in the dc bus through the device. The risk of self-sustained oscillations is governed by the Miller capacitance, the total gate-loop inductance and the transconductance of the SiC MOSFET. Additionally, oscillations are observed at the terminals of the module in the very first phase when turning-ON the SiC MOSFET. These oscillations and their frequency are governed by the total gate-loop inductance and the input capacitance of the SiC MOSFET. The damping of these oscillations depends on the total gate-loop resistance. All the oscillations described above may also be affected by coupling effects between other subcircuits within the module.

### TABLE III

**Simulation Parameters**

<table>
<thead>
<tr>
<th>Simulation parameters</th>
<th>( V_{gs} )</th>
<th>( V_{gs} )</th>
<th>( R_g )</th>
<th>( L_{g_stray} )</th>
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</thead>
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<td>1. Nominal case</td>
<td>540 V</td>
<td>-5/-20 V</td>
<td>5 ( \Omega )</td>
<td>20 mH</td>
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<td>Worst cases</td>
<td></td>
<td></td>
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<tr>
<td>2. low gate resistance</td>
<td>540 V</td>
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<td>2.5 ( \Omega )</td>
<td>20 mH</td>
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<td>3. high gate driver inductance</td>
<td>540 V</td>
<td>-5/-20 V</td>
<td>5 ( \Omega )</td>
<td>100 mH</td>
</tr>
</tbody>
</table>

![Fig. 9. Cross-talk on the upper switch position (chips 9 and 12) at turn-ON and turn-OFF of the lower switch position—nominal conditions.](image)

Fig. 9. Cross-talk on the upper switch position (chips 9 and 12) at turn-ON and turn-OFF of the lower switch position—nominal conditions.

at the pin oscillates and has an overshoot of 21 V peak. No undershoot is observed at turn-OFF. Taking into consideration the results of the simulation, the gate voltage on the chip does not suffer from this kind of oscillation. Experimental results from the gate-source voltage (yellow) and the inverted waveform of the gate-source current (green) at turn-ON and turn-OFF are shown in Fig. 7. It corresponds to what is observed in the simulations. The cross-talk in the upper switch position resulting from the switching transients of the lower switch position is shown in Fig. 9. During the turn-ON transient of the lower switch position, the gate voltages of the upper switches \( V_{g9} \) and \( V_{g12} \) reach -1.3 and -1.6 V respectively. As for the lower switch, the gate-loop voltage measured at the pin oscillates with an envelope reaching values exceeding the device ratings. During the turn-OFF transient of the lower switch position, \( V_{g9} \) and \( V_{g12} \) have an undershoot of -9.81 and -9.05 V, respectively. This is below the recommended values (-5/+20 V) but still within the maximum ratings (-10 V/+25 V). At this point, it can be observed that there is an unbalance between the gate voltages of the individual chips in the module. This unbalance may result in a reduced lifetime of the chips exposed to higher voltages in the same module.

### B. Second Case: Low External Gate Resistance

The gate-loop switching transients of the module when the switching speed is increased are shown in Fig. 10. The voltage seen at the gate-source terminal outside the module reveals an overshoot of 26.6 V, exceeding the voltage rating of the gate oxide. However, the voltages on the chips of the position switch of the module \( (V_{g9} \) and \( V_{g6} \) in the figure) remain within the recommended values (-5 V/+20 V). Fig. 11 shows the effect of reduced external gate resistance on the cross-talk from the lower switch position on the upper switch position. The gate voltages of the upper switches \( V_{g9} \) and \( V_{g12} \) reach -2.49 and -2.51 V, respectively during the turn-ON transient. During the turn-OFF transient of the lower switch position, \( V_{g9} \) and \( V_{g12} \) have an undershoot of -9.37 and -8.65 V, respectively. These values are lower than for the nominal case. The cross-talk is slightly reduced. Fig. 11 also reveals that an increase in the switching speed results in an overshoot at the turn-ON of the upper switch. The peak values of \( V_{g9} \) and \( V_{g12} \) are 22.32 and 22.24 V, respectively. These values exceed the recommended values without exceeding the maximum tolerated values of the gate-source voltage. Exceeding the gate-source voltage recommended values may
lead to a lifetime reduction. According to [13], a dc stress of this magnitude would mean a lifetime reduction by a factor of 10 approximately. However, it is very likely that the lifetime reduction is very much lower than this prediction since the transients are very short in time. A discussion of the reliability considerations is given in Section IV-D.

C. Third Case: High Inductance Between Gate Drive and Module

The gate-loop switching transients of the module when the inductance between the gate driver and the gate terminal is increased are shown in Figs. 12 and 13. In this case, a lower overshoot at the gate-source terminal of the module is observed. The peak value is 25 V. Similarly, no overshoot is observed on the on-chip gate-source voltages. The gate voltages of the upper switches $V_{gs9}$ and $V_{gs12}$ reach $-1.8$ V and $-2.4$ V respectively during the turn-ON transient. During the turn-OFF transient of the lower switch position, $V_{gs9}$ and $V_{gs12}$ have an undershoot of $-10.28$ V and $-9.4$ V, respectively. Thus, $V_{gs9}$ exceeds the maximum ratings allowed in the data sheet. Although no publication refers to lifetime reduction in the case the absolute maximum negative voltage is exceeded, the authors believe that this case also presents a reliability issue.

D. Discussion

From the observations in this section, it can be concluded that the design of SiC MOSFET modules based on existing packages previously designed for Si-IGBTs devices may not be optimal to fully utilize the high switching speeds offered by the SiC technology. In fact, in order to remain in a safe-operation area and limit the cross-talk between the lower and upper switch positions, one has to limit the switching speed and connect the driver as close as possible to the module to avoid additional parasitic inductance. However, it is not clear yet how the overvoltage transients and the undervoltage transients across the gate oxide of the SiC MOSFET affect the lifetime. For Si IGBTs the maximum transient gate-emitter voltage and the pulse duration (or the maximum duty ratio) is in many cases stated in the data sheet as mentioned in [29]. For Si-IGBTs, the voltage across the dielectric between the gate and the emitter can cause tunneling of carriers in case the leakage limit is exceeded. This is particularly true where traps (imperfections) exist. Due to this process, which is cumulative, significant damage occurs in the gate oxide. Therefore, it is recommended in [29] that overvoltage and undervoltage transients across the gate oxide of Si-IGBTs should be limited. For SiC MOSFETs, the oxide has been proved to have a lifetime of 100 years at high temperature and $E < 2.9$ MV. This reduces to 10 years if the electric field increases to $E < 3.6$ MV [30]. In [31], the gate-oxide degradation under switching conditions is investigated when the gate voltage is switched between $-5$ and $+20$ V at 250 °C, which is lower voltages but higher temperature than what is investigated in this paper. The authors believe that a few volts’ overvoltage compared with the absolute maximum value of gate bias stated in the data sheet of the SiC MOSFET does not have a significant impact on the lifetime of the device. However, the values used for cases 2 and 3 presented in Sections IV-B and IV-C are fairly conservative. A further decrease in the gate resistance (to increase switching speeds) would result in a higher overvoltage peak on the gate oxide resulting in a higher peak electric field. Similarly, an increased stray inductance coming from the driver leads and tracks will result in a lower undervoltage. It is not clear from the literature how much these stresses impact the lifetime of the MOSFET modules. Nevertheless, it is wise to limit the cross-talk. Doing so, a higher gate resistance will damp the cross-talk and avoid overvoltages on the oxide. Similarly, appropriate connections between the drivers and the module upper and lower switch positions will limit $L_{g, stray}$ and the undershoot over the gate oxide will be limited. The authors believe that there is a need to develop low-inductive packages adapted to the high switching speeds of the new SiC technology as previously mentioned in [3]. A reduction of the gate-loop inductance is desired to increase the reliability, decrease the cross-talk, but also to increase the switching speeds and thus decrease the switching losses.

V. Conclusion

A SiC MOSFET power module available on the market has been modeled with ANSYS Q3D and validated experimentally. The validity of the model has been confirmed by
on-chip measurements. An analysis of the impact of parasitic elements on the gate-source voltages inside the module has been conducted, revealing a difference between the measured voltage at the gate terminal and the gate voltage on the chip. The oscillations observed at the gate-source terminal are not present at the chip level. The high overshoot on the lower switching speeds, it was found that the gate oxide was exposed to voltages exceeding the recommended operation values. This could lead to reliability issues, particularly when high switching speeds are targeted. Moreover, a poorly designed gate-drive design may have to compromise on the switching speeds but also minimize the distance between the gate driver output and the gate and source terminals of the 62-mm module. There is thus a need to develop low-inductive packages adapted to the fast switching SiC technology.

REFERENCES


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Publication III


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Investigation of Long-term Parameter Variations of SiC Power MOSFETs

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Keywords


Abstract

Experimental investigations on the gate-oxide and body-diode reliability of commercially available Silicon Carbide (SiC) MOSFETs from the second generation are performed. The body-diode conduction test is performed with a current density of 50 A/cm\textsuperscript{2} in order to determine if the body-diode of the MOSFETs is free from bipolar degradation. The second test is stressing the gate-oxide. A negative bias is applied on the gate oxide in order to detect and quantify potential drifts.

Introduction

Silicon carbide (SiC) transistors have undergone a great development over the past few years. SiC power devices show several advantageous characteristics that make them more attractive than their silicon (Si) counterparts \cite{1}. SiC power devices are foreseen, at least partly, to replace the actual Si technologies in several power electronics applications such as railway traction and automotive applications. The main advantages of SiC are the higher operating temperature capability, lower on-state resistance, and higher maximum switching frequency. This interest motivated research efforts toward application reliability. However, since these investigations identified several potential reliability problems for SiC power devices, their commercialization has not yet reached its full potential \cite{2}-\cite{5}. Moreover, the reliability assessment of SiC power devices is using methods previously used for Si power devices. This may result in ambiguous test results \cite{6}. With the higher capability of SiC power devices in terms of temperature, the accelerated stress test methods might become obsolete \cite{6} at least with respect to the device itself (in contrast to packaging).

The first generation of SiC power MOSFETs suffered from gate dielectric reliability problems, especially at elevated temperatures \cite{7}. Moreover, the gate threshold voltage of the SiC MOSFET has been found to be unstable when its gate is biased for a long time with a positive or negative gate voltage \cite{6} and \cite{8}-\cite{11}. Another issue reported is the reliability of the intrinsic body-diode of the SiC power MOSFET \cite{12} and \cite{13}.

In industrial applications, it is not uncommon that the devices are powered off for long durations of time. A drift of the threshold voltage towards 0 V would compromise the reliability of the system in case the SiC MOSFET loses the normally-off property. Moreover, when a diode-less operation is targeted, an augmentation of the on-state resistance due to bipolar is not acceptable.
The present paper is organized in three parts. Firstly, a device characterization is made on 80 devices from two manufacturers. The high number of tested devices is motivated by the desire to have sufficient data for further reliability assessments [14]. The aim is to compare the characteristics prior to the stress and after stressing the devices for a total of 1000 hours. Then, the devices are split randomly into two groups. The first group consisting of 20 devices from each manufacturer is exposed to a body-diode reliability test. The remaining 40 devices are biased negatively at room temperature. The focus in this paper is the detection of a possible drift of the threshold during normal operating conditions. Therefore, unlike [4], [10], [15], [16], and [17] no accelerating factors, such as temperature or increased gate bias, are applied on the devices. Another particularity is that the setups are automated and constantly performing one measurement every hour. Thus, a fast measurement can be performed, while limiting the disturbance caused by the measurement. This is especially valid for the threshold-voltage stress test [11].

**Characterization of the Devices Under Test (DUTs)**

The devices investigated here are the latest released devices from Cree and Rohm. Their characteristics are presented in Table 1. According to [18] a device is considered as failed when its threshold voltage has changed by 20 %. For the body-diode test, a positive variation of the forward voltage of 10 % is considered as failure. The characteristics of the devices can differ from the datasheet and also within a batch. Therefore, they have to be characterized prior to reliability testing in order to identify the overall drift caused by the applied stress. As can be seen in Fig. 1 and Fig. 2, a spread in characteristics is present.

<table>
<thead>
<tr>
<th>DUT</th>
<th>$V_{ds}$</th>
<th>$I_d$ at 25°C</th>
<th>$I_d$ at 100°C</th>
<th>$V_{gs}$</th>
<th>$R_{ds(on)}$ (typ)</th>
<th>Integrated SiC SBD</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M0025120D</td>
<td>1200 V</td>
<td>90 A</td>
<td>60 A</td>
<td>-10 V / +25 V</td>
<td>25 mΩ</td>
<td>No</td>
</tr>
<tr>
<td>SCT2080KE</td>
<td>1200 V</td>
<td>40 A</td>
<td>28 A</td>
<td>-6 V / +22 V</td>
<td>80 mΩ</td>
<td>No</td>
</tr>
</tbody>
</table>

**Table 1: main characteristics of the devices under test (DUT)**

In Fig. 1, the body-diode characteristics of the SiC MOSFETs from Cree are fairly similar. However, the SiC MOSFETs from Rohm have two devices presenting higher forward voltage already for fairly low forward source-drain current ($I_{sd}$). This will be observed in the body-diode stress test in the following section. The slope which corresponds to the differential conductance in Fig. 1b is approximately three times lower for the outliers. This indicates that the differential resistance in that case is three times higher. The authors have no explanation to this, because the $R_{(on)}$ in forward conduction for these two devices is not significantly different compared to the other devices. Nevertheless, the spread is within with the datasheet specifications.

On the other hand, when observing the threshold voltages presented in Fig. 2a, and Fig. 2b, the Rohm devices have a slightly higher threshold voltage at room temperature than the Cree devices. The spread in characteristics is also present.
Fig. 1: Body-Diode characteristics of the SiC MOSFETs from (a) Cree and (b)-(c) Rohm

Fig. 2: Threshold voltage characteristics for the SiC MOSFETs from (a) Cree and (b) Rohm
Body-diode Degradation Test

The reliability of the SiC MOSFET is known to be affected by a potential degradation caused by the conduction of its body-diode. If forward current is continuously applied to the body-diode, a crystal defect called stacking fault will grow due to the hole-electron recombination energy. These faults are progressively blocking the current path which results in an increased on-state resistance as well as an increased forward voltage of the body-diode. An increase of the leakage current in blocking mode is also observed in [12] and [13]. The increased forward losses and blocking losses affect the thermal design of a system. For these reasons, for circuit topologies where the body-diode conducts a significant current, it is important to use a device free from stacking faults.

To evaluate the body-diode reliability of the SiC MOSFET a direct forward current is continuously applied through its body-diode. To ensure that the channel is not conducting, the gate and source terminals of the device are short-circuited. The applied direct current for each device type is stated in Table 2. The current density is calculated using the total chip area. The experimental set-up is shown in Fig. 3.

<table>
<thead>
<tr>
<th>Device</th>
<th>Current rating at 25°C [A]</th>
<th>Die size [mm²]</th>
<th>Current at 50 A/cm² [A]</th>
<th>Forward Voltage drop [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M0025120D</td>
<td>60 A</td>
<td>26.0176</td>
<td>15 A</td>
<td>3.3 for 25 A</td>
</tr>
<tr>
<td>SCT2080KE</td>
<td>35 A</td>
<td>17.3451</td>
<td>10 A</td>
<td>4.6 for 10 A</td>
</tr>
</tbody>
</table>

Table 2: Current densities of the devices under test

Prior to the testing, the devices are characterized by means of their on-state resistance $R_{ds(on)}$, their blocking voltage $V_{ds(max)}$ and the body-diode I-V curve. These characterizations are to be repeated after the test completion.

As a pre-study, only 2 devices from Cree (M1 and M2) are being investigated and manually monitored. The setup is similar to that shown in Fig. 3(a), but for two devices. The monitored parameters are the forward voltages $V_{f1}$ and $V_{f2}$, the ambient temperature, and the case temperature. After 6000 h of stress with 10 A (38.4 A/cm²) no significant differences in threshold voltage were found. The results of this preliminary test are shown in Fig. 4. For clarity, only the first 1000 h are shown here. The first voltage drop occurs in the first 30 minutes of the test. The body-diode voltage is decreasing with the temperature increase of the heat-sink, due to self-heating of the devices. As expected, the body-diode forward voltage of both devices drops in the first hours due to an increase of the case temperature from ambient to 80 °C. After four hours, the forward voltages stabilized at approximately 2.36 V. The small fluctuations are believed to be related to fluctuations of the ambient temperature.

For the final setup, four circuits consisting of 10 devices in series are mounted on heat sinks, which are fan-cooled. The schematic of the test circuit and the final implementation are shown in Fig. 3. The heat sinks are maintained below 95 °C to avoid recovery of the Shockley stacking faults by thermal annealing [19]. The results for the 20 devices from Cree (C2M0025120D) and from Rohm (SCT280KE) are shown in Fig. 5 and Fig. 6, respectively. The tests are ongoing to this date. The total stress times are thus 300 hours and 227 hours, respectively.
The forward voltage of the device C22 from Cree dropped from 2.7 V to 0.37 V after approximately 1 hour of stress. It is the hypothesis of the authors that the failure mode of the device consists of being in the on state. This is mainly due to the voltage drop of the device which fits the Eq. (1), meaning that the device could be in the on-state, considering an on-state resistance of 25 mΩ.

\[ 15.0 \text{A} \cdot 25 \text{mΩ} = 0.375 V \approx 0.37 V \quad (1) \]

However, it will be necessary to investigate the failure mode after the completion of the test. As the device is connected in series with 9 other devices, it cannot be removed without stopping the stress. The remaining 19 devices were operated in reverse-bias mode for over 300 hours and no sign of bipolar degradation is observed so far.

For the Rohm devices, all body-diodes are showing stable operation after 227 hours of stress. Their forward voltage drop has been stable over the whole test duration and no indication of bipolar degradation is observed. As foreseen in the device characterization (c.f. Fig. 1b), two devices have higher forward voltages compared to the rest of the batch.
Fig. 5 : Body-Diode forward voltages monitored during 150 hours for the Cree devices

Fig. 6 : Body-Diode forward voltages monitored during 227 hours for the Rohm devices

Fig. 5 : Body-Diode forward voltages monitored during 150 hours for the Cree devices

Fig. 6 : Body-Diode forward voltages monitored during 227 hours for the Rohm devices
Negative Gate Bias Test

The negative gate bias test, performed here at room temperature, is stressing electrically the gate oxide at the maximum rated negative direct bias voltage (c.f. Table 1). The outcome of this test is to detect a potential drift caused by random defects in the oxide as well as ionic contamination in the oxide. The test is automated in order to have a regular and precise measurement for a large amount of devices and simultaneously. The measurement duration is of 1 second. The monitored parameter is the gate threshold voltage. A schematic diagram of the setup is shown in Fig. 7a. The threshold voltage is measured using the constant current method [20]-[22]. The physical implementation of the test circuit is shown in Fig. 8 for four devices. The total test setup consists of five circuit boards. Thus, 20 devices can be tested simultaneously under identical conditions. The measurement procedure is shown in Fig. 7b. The gate and drain terminals are short-circuited, while a fixed current is fed through the drain-source channel. The measured voltage across the gate and source terminals is the threshold voltage defined for this particular current. Since the threshold voltage is highly dependent on the temperature, the temperature is measured simultaneously. Thus, the measured data can be temperature-compensated and normalized for 25 °C. The measurements are performed every hour for a total of 1000 hours.

Fig. 7 : Schematic diagrams of (a) stress test of the SiC MOSFETs (2 devices shown) and of the (b) constant current measurement technique.

Fig. 8 : Test set-up for the threshold voltage measurement

Twenty devices from Cree have been tested for 1000 hours. The negative gate bias is set to –10 V, which is the datasheet negative limit. The evolution of the threshold voltages for 300 μA is presented in Fig. 9. For clarity reasons, only five devices are shown here. The variation of threshold voltage is a
decrease of approximately of 15–30 mV. This decrease occurs mainly during the first 45 hours of the stress.

The tests for the twenty devices from Rohm are ongoing upon the date of submission of the present paper. The final test time is to be 1000 hours. The negative gate bias is set correspondingly to – 6 V. The evolution of the threshold voltages for 2 mA is presented in Fig. 10. A higher current is chosen in order to be in the steep slope of threshold voltage characteristic. Again, a drop of threshold voltage is observed. The decrease of threshold voltage is approximately 50–100 mV. It is yet too early to determine if the threshold voltage stabilizes after a certain number of hours under stress.

Fig. 9: Evolution of the threshold voltages for 5 of the Cree devices for Idss = 300 μA at room temperature during 1000 hours.

Fig. 10: Evolution of the threshold voltages for 5 of the Rohm devices for Idss = 2 mA at room temperature during 92 hours.
Conclusion
In this paper, two different reliability issues of commercially available SiC MOSFETs have been investigated for a total of 80 devices. Two different automated test setups have been built, allowing simultaneous measurement on each device once per hour. The body-diodes of a total of 40 MOSFETs from 2 different manufacturers were stressed with forward current for a total of 300 hours and 227 hours respectively. One device is currently possibly in the on-state. The 39 remaining devices have shown no sign of bipolar degradation so far. A threshold voltage test has also been performed on 40 MOSFETs at room temperature. While stressed during 1000 h with a negative voltage of –10 V, the Cree devices (C2M0025120D) revealed a voltage drop of approximately 15–30 mV. The Rohm devices (SCT280KE) are currently under test with –6V stress. So far, and after 92 hours, a voltage drop of approximately 50–100 mV is observed.

References


Publication IV


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Humidity Testing of SiC Power MOSFETs

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Abstract—Humidity and outdoor application are a challenge for Silicon (Si) and Silicon Carbide (SiC) applications. This paper investigates the effect of humidity on SiC power MOSFET modules in a real application where no acceleration factors such as pressure or high temperature are applied. Since SiC devices can operate at higher temperature than Si, the high-temperature acceleration factor may be obsolete. Moreover, the humidity might be more critical when the temperature inside the converter enclosure and modules housing is varying with daily temperature variations and weather constraints in harsh environments. The breakdown voltages of the humidity-exposed modules are monitored regularly over a extended period of time in order to detect any increase of leakage current which indicates humidity-induced degradation. After 630 hours, the modules operated outdoor presented an increased leakage current at 1.2 kV and over the whole range of applied voltage.

Keywords – Power MOSFETs, Silicon Carbide (SiC), multichip packaging, reliability, corrosion, humidity, failure analysis.

I. INTRODUCTION

Silicon Carbide (SiC) MOSFETs have in the latest years become of interest in power electronics and are foreseen to replace Si IGBT modules for instance in industrial and traction applications [1]–[4]. The advantages of SiC MOSFETs is the possibility to operate at higher temperatures, higher frequencies and with a lower on-state resistance. These advantages allow a reduction of volume and weight which is favorable for traction applications. For industrial applications, the advantage of SiC MOSFETs lies also in the lower on-state resistance and fast switching speeds which, with proper main-circuit design, result in considerably higher efficiencies compared to Si technology.

Nowadays, power electronic (PE) applications are often placed outdoor where the air humidity is not controlled. In traction applications, for instance, the converters are often, for space reasons, placed on the vehicle roof or under the chassis. In industrial facilities, PE converters may also lay outside. In these cases, the PE units are exposed to uncontrolled harsh environment and climate conditions. Not only moisture, but also gases, salt and dust compromise the integrity of the converter and the modules inside the converter enclosures [5]. Typically, the converter units are not sealed hermetically and moisture builds up in the enclosure in which the converter is placed. In [6], a model to simulate the moisture inside the converters and power modules is presented. It was found that the moisture inside the converter cabinets can exceed significantly the ambient conditions. If condensation occurs in the un-sealed module and over the chips, corrosion can lead to failure of the power semiconductor module [7].

Although after manufacturing, every power semiconductor device has to be tested with regards to reliability standards [8]. These standards are based on Si technology and sometimes even low-voltage technology. With regards to humidity and temperature the devices are often tested in the so-called temperature humidity bias (THB) 85/85 test with an 80 V bias [8]. In [9], it was shown that higher voltages levels accelerate the moisture diffusion considerably for Si IGBTs. An accelerated THB test on IGBT modules at high bias levels is presented in [10]. Similar work has been presented in [11] where pressure as a failure factor is included. All the work presented above is focused on reliability of Si IGBTs specifically. The present publication targets specifically the reliability of SiC MOSFETs with regards to humidity. This investigation, which has not been performed previously in the literature, is necessary to fulfill the rough requirement of outdoor industrial applications. This generally, as for SiC diodes [12], concerns the edge termination of the SiC MOSFET chips. The present paper investigates modules in order to stress an increased number of chips at once, but also because modules are the device of choice to replace IGBTs for high-power applications.

To this day, the most mature SiC power device is the SiC Schottky diode which counts billions of operation hours [12]. Recently, the reliability of the SiC MOSFET, in particular with regards to its body-diode and threshold-voltage [13]–[16] has been improved. The body-diode of early generation of SiC MOSFETs was suffering from Shockley stacking faults resulting from basal plane dislocation in the SiC substrate [17], [18]. The threshold voltage shift, observed in [19] seems to no longer be an issue [14], [20]. High temperature operation of SiC MOSFETs still needs improvement with regards to packaging. However, reliability of SiC power devices with regards to humidity needs to be further investigated [21]. The topic is of great importance since a growing number of PE units for outdoor and harsh environment are designed.

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accelerated tests are performed in the present investigation in order to exclude other failure mechanisms resulting from highly accelerated tests at high temperature.

In this paper, the humidity induced failures observed in power semiconductor devices are first briefly discussed. Then the test setup and test procedure of the non-accelerated humidity test of SiC MOSFET power modules is presented. The early results reveal that there is a difference between the modules operated outdoor and those who are not with regards to blocking voltage evolution.

II. HUMIDITY TESTING - BACKGROUND

Temperature humidity bias (THB) test is the standard for Si and SiC devices. The devices are exposed to 85 % relative humidity (R.H) and 85 °C for 1000 h under a bias of max. 80 V [8]. Due to this comparably low voltage, for Si IGBTs, it was shown in [9] that this test might be obsolete for higher voltage devices, as high bias levels accelerate the moisture-induced degradation significantly. For power semiconductors, the corrosion mechanisms induced by an exposition to humidity are the electromechanical migration and the aluminum corrosion [10].

In multi-chip power modules, moisture is able to enter the non-sealed housing. The moisture reaches the chips through the molding-compound or silicone gel. The most critical region for power semiconductors is the junction terminations. A detailed explanation can be found in [7] for Si IGBTs.

A. Reliability of SiC Power MOSFETs with regards to humidity

Humidity can deteriorate the ohmic contacts of the SiC semiconductors due to chemical reactions with the passivation when exposed to high temperature and oxygen-rich environments. Very little work has been presented so far on SiC power transistors. However, in [22], 4H-SiC MOSFETs with a stable protecting coating for harsh environment application is presented. The presented solution consists of a stacked ONO gate dielectric and Ti/TiN/Pt/Ti interconnect together with Ti ohmic contacts in combination with a-SiOx/a-SiC coating. This demonstrates that solutions toward a higher reliability against humidity and moisture are possible and are being investigated.

Infineon and Cree have made reliability investigations on the impact of humidity on SiC schottky diodes [12], [23]. The junction terminations are – for all SiC devices types – exposed to higher electric fields compared to Si devices. Moreover, since the substrate is thinner in SiC, the junction termination are stressed even more.

Even though the impact of humidity on SiC MOSFETs may be similar to the impact observed on SiC schottky diodes, there is a need to investigate this specifically. Likewise, even though the oxide layer of SiC MOSFETs has been considerably improved the deterioration of the oxide layer due to humidity cannot be excluded at this stage.

III. NON ACCELERATED HUMIDITY TEST OF SiC POWER MOSFET MODULES

Degradation monitoring during THB testing consists of measuring the leakage current of the blocking devices. On the contrary, this paper focuses on a non-accelerated degradation monitoring of humidity exposed SiC MOSFET power modules. Therefore, the modules will be operated in a converter at rated current and voltage for an extended period of time while their blocking voltage is measured after 280 h and 630 h the first time and then after every 1000 h. The drawback of such a test is that in order to have a statistical result of the failure mode, we would need a high number of converters exposed to humidity for a long time, which is costly. However, as the devices are characterized during the testing period, parameter drifts can be detected before the devices have failed. Similarly, if a unit fails for other reasons than humidity, this trend can still be observed and the data can be collected for further analysis.

A. Test procedure

In order to test the effect of humidity in SiC MOSFET power modules, 8 commercially available MOSFET modules in a 62 mm standard package (previously used for IGBT technology) are divided in 2 groups. 4 modules will be tested in 2 PE units placed outdoor and 4 modules will be tested in 2 PE units placed indoor. The breakdown voltage of each of the 8 modules is tested before the test is started. Fig. 1 shows the breakdown voltages of all the modules prior to exposition to the testing measured at room temperature, where the breakdown voltage is defined as a leakage current equals to 1 mA. Fig. 1a shows the high-side switch position of the modules and the low-side switch position is shown in Fig. 1b. Every 1000 h (i.e. approximately 40 days) the modules will be removed from the PE units and tested in the same conditions as for the preliminary tests. The drift of the breakdown voltage will be the main observed phenomenon. Any increase in leakage current indicates a degradation of the junction termination [7]. A drastic increase in leakage current leads to a failure of the power module. Since half of the power modules are placed indoor and half outdoor, the evolutions of the breakdown voltages can be compared.

Additionally, a humidity and temperature sensor is placed in the converter enclosure, close to the devices. This will permit to monitor the variation of temperature and humidity locally inside the converter enclosure which are different from the temperature and humidity observed outside the enclosure. The heat sink temperature is also constantly monitored.
Pre-Test Breakdown Voltage High Side

![Graph](image)

(b)

Pre-Test Breakdown Voltage Low Side

![Graph](image)

(b)

Fig. 1: Pre-test breakdown voltage of the 8 modules (a) high side switch position (b) low side switch position

**B. Test setup**

The 4 converters are connected in parallel as presented in Fig. 2. A fuse is connected in the current path to disconnect the converter in case of fault without affecting the other converters. The converter is a full-bridge with a resonant load as shown in Fig. 3. The devices under test are the CAS300M12BM2 from Cree rated at 300 A and 1.2 kV. There are 2 half-bridge SiC MOSFET modules per converter. The dc source feeds the losses of the 4 converters. The converter characteristics are: \( V_{dc} = 540 \text{ V}, f_{sw} = 25 \text{ kHz}, I_{rms} = 150 \text{ A} \) and the resonant inductor needed is thus

\[
L = \frac{V \cdot \Delta T}{\Delta I} = \frac{540 \cdot 20 \cdot 10^{-6}}{2 \cdot 150 \sqrt{3}} = 20.8 \mu \text{H} \rightarrow 21 \mu \text{H}
\]

A capacitor is connected in series with the inductor.

The setup located outdoor (i.e converters 3 and 4) is shown in Fig. 4. The outdoor setup is protected from rain dropping on the converters and water penetration but not from humidity and moisture, neither daily temperature variations. The converters are exposed to humidity since the enclosures in which they are built are not hermetically sealed.

The setup located indoor is identical to the outdoor version, but protected from the outdoor humidity. The 4 converters are operated with an identical procedure. Additionally, the heat-sink temperature is monitored and a system of thermal switches located on the heat sink and resonant tank guarantees that the converters are safely operated so that failures from over temperatures can be avoided. The humidity inside the converter box is also monitored.

**TABLE I. MODULE REPARTITION IN THE CONVERTERS**

<table>
<thead>
<tr>
<th>Indoor</th>
<th>Outdoor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modules</td>
<td>225 102 122 88</td>
</tr>
<tr>
<td></td>
<td>275 59 89 33</td>
</tr>
</tbody>
</table>

Converters 1 and 2 are placed indoor and converters 3 and 4 are placed outdoor, just outside the lab facilities. The converters are water-cooled with converters 1 and 2 (respectively 3 and 4) sharing the same cooling system. The part numbers of the modules in the different converters are given in TABLE I.
IV. TEST RESULTS

Unlike other reliability tests, the present investigation is a long-term test which is planned to run for one year (8000 hours). Since it is not accelerated, it was decided that the breakdown voltage of the 8 modules under test will be regularly measured in order to follow the evolution of the breakdown voltage for all modules whether they are exposed to humidity or not. The modules are tested every time using the same curve tracer, with identical settings and procedure. One first has to disconnect all the modules from the setups, measure them, place them back into the converters, and restart the converters.

The modules have been, in a first stage, characterized after 280 h of operation and then after 630 h. The results can be seen in Figs. 6 and 7, where the leakage current is given as a function of the voltage applied to the MOSFET module when the voltage applied to his gate its 0 V. The current at breakdown voltage – as specified in the module datasheet – is of 1 mA.

Already after 280 h of operation, there is a noticeable difference between the modules located outdoor (122 and 33) and those located indoor (225 and 275). In Fig. 6, it can be seen that the modules located outdoors have a larger variation of leakage current over the whole range of applied voltage compared with those situated indoors. The leakage current at 1.2 kV has increased from 0.3 mA to 0.6 mA for the low switch position of Module 122. This is an increase of 50 %. Consequently, the voltage corresponding to 1 mA of leakage current for the low switch position of module 122 has been reduced by 90 V. For the upper switch position of module 122, the increase in leakage current at 1.2 kV is of 0.22 mA. For module 33, the increase in leakage current is less significant with an increase of 0.14 mA for the high switch position and 0.10 mA for the low switch position.. For modules 88 and 89, the evolution is similar to what is observed for module 33. For the sake of brevity, the plots are not repeated here. No noticeable further changes were observed after 630 h.

The modules 225 and 275 situated indoor present a negligible variation of leakage current of + 0.02 mA, as shown in Fig. 7. The variation in blocking voltage is also negligible. Similarly, the leakage current did not change much between 280 h and 630 h.

However, these are very early test results. The evolution of the leakage current and blocking voltage for all 8 modules will be analyzed during the whole test period. Moreover, as the test time increases, it is expected that the humidity will penetrate even more deeply into the modules and the silicon gel.
V. CONCLUSION AND FUTURE WORK

The present paper investigates the impact of humidity on the breakdown voltage of the SiC MOSFET. A total of four modules have been exposed to humidity in a non-accelerated test setup and compared with four reference modules. The test is ongoing. However, after approximately 280 hours of operation in a full-bridge converter operating at 540 V and 150 A rms current, the breakdown voltage was found to be reduced by 6.5% in the worst case for the modules exposed to humidity. An increase in leakage current is also observed over the entire range of blocking voltage applied for the outdoor modules. In the worst case an increase of 50% was observed at 1.2 kV. On the contrary, for the modules located in a similar setup indoors, the leakage current variations at 1.2 kV where found to be negligible. The breakdown voltage was also unchanged. After 630 h no further changes were observed. In the accelerated test presented in [10], after 200 h, most device had lost approx. 10% of their blocking voltage capability. Further reduction in blocking voltage capabilities might be observed after more than 1000 h. The test is planned be continued for a whole year (8000 h) provided that none of the devices fails.

VI. REFERENCES


10.2. SUGGESTED FUTURE WORK

Publication V


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Humidity Testing of SiC Power MOSFETs – An Update

Topics: 1b: New materials and active devices & 1e: Reliability (U)

Abstract

The effect of humidity on SiC Power MOSFET modules is investigated in a real application. Four modules are operated outdoor and four modules are operated indoor in identical setups, while their breakdown voltages are monitored regularly. The evolution of the leakage current, indicating humidity-induced degradation is observed.

Introduction

Silicon Carbide (SiC) MOSFETs are foreseen to replace Silicon (Si) IGBT modules for some industrial and traction applications. The advantages of SiC technology is the higher maximum allowable temperature, higher maximum switching frequency and lower on-state resistance. As a result, reductions of volume and weight are achievable which is favorable for traction applications as well as automotive. Moreover, a reduction of volume and weight often brings a reduction in costs as well. For industrial applications, the advantage of SiC MOSFETs lies primarily in the lower on-state resistance and fast switching speeds. In fact, with a proper main circuit design, these advantages will result in considerably higher efficiencies compared with Si technology. In many applications, it is common that power electronic converters (PE) are placed outdoor where the air humidity is not controlled. Moreover, applications placed outdoor are unprotected from toxic gases, daily temperature variations and dust. In traction applications, the converters are placed on the vehicle roof or under the chassis for space reasons. In industrial facilities, PE units may be exposed to uncontrolled harsh environment and climate conditions when placed outside. The integrity of the converters and modules inside the enclosures see their integrity compromised by moisture, gases, salt and dust among others [1]. Typically, the converter units are not sealed hermetically. Thus, moisture builds up in the enclosures in which the converters are placed. A simulation model describing the moisture inside the converters and power modules is presented in [2]. The moisture inside the converter cabinets can exceed the ambient conditions significantly. Moreover, if condensation occurs in the un-sealed module and above the chips, corrosion can lead to failure of the power semiconductor module [3]. The latter is one of the reasons in this work to not use the standard tests based on Si technology. The humidity is often tested in the so-called temperature humidity bias (THB) 85 / 85 test with an 80 V bias [4]. As the condensation in humid environments occurs at low temperatures and the fact that higher voltage levels accelerate the moisture diffusion considerably for Si IGBTs [5], this work focuses on a real application case. In fact, in most cases, the temperature in the converter enclosure is lower than 85°C and may even go down to the moisture dew point when the temperature outside is low (winter for instance) and the converter is turned-off. An accelerated THB test on IGBT modules at high bias levels is presented in [6]. Similar work has been presented in [7] where pressure as a failure factor is included. In contrast to the work presented above, which focuses on the reliability of Si IGBTs, the present publication targets specifically the reliability of SiC MOSFETs with regards to humidity and aims to exclude other failure mechanisms resulting from highly accelerated tests. This work is a follow up of what was presented in [8]. The evolution of the blocking voltages after another 4200 h of test is presented. The final paper will include the final results of the test after 8000 h. As for SiC diodes [9], the edge termination of the SiC MOSFET chips are of concern, partly due to the higher electric field applied on SiC technology while the chips are thinner.

Humidity Testing – Background

Temperature humidity bias (THB) test is the standard for Si and SiC devices. The devices are exposed to 85 % relative humidity (RH) and 85 °C for a total of 1000 h under a bias of max 80 V [4]. This is a comparably low voltage for high power applications. For Si IGBTs it was shown that it was obsolete [5] for high voltage devices as high bias accelerates the humidity-induced degradation significantly.
The humidity-induced corrosion mechanisms for power semiconductors are the electromechanical migration and the aluminum corrosion [6].

In multichip power modules, moisture is able to enter the non-sealed housing. The moisture reaches the chip and its passivation layer through the silicone gel. From this point of view, the most critical region for power semiconductors is the junction termination (see [3] for Si IGBTs). The humidity can also deteriorate the ohmic contacts of the SiC semiconductors. This is due to chemical reactions with the passivation when exposed to high temperature and oxygen-rich environments. Efforts toward protecting coatings have been made for harsh environment applications [10]. In SiC compared with Si, the junction terminations (for all device types) are exposed to higher electrical fields while the substrate is thinner. This results in a higher stress. Infineon and Cree have investigated the impact of humidity on SiC Schottky diodes [9], [11]. The impact of humidity on SiC MOSFETs may be similar to the impact observed on SiC schottky diodes but the authors believe that there is still a need to investigate this specifically. Moreover, the deterioration of the oxide layer due to humidity cannot be excluded at this stage. However, this will not be investigated in this work.

**Non-Accelerated Humidity Test of SiC Power MOSFET Modules**

The monitoring of the degradation during THB testing consists of measuring the leakage current of the blocking devices. According to the device under test (DUT) datasheet, the blocking voltage is defined by the blocking voltage when the leakage current is of 1 mA. This paper, as previously presented in [8], focuses on a non-accelerated degradation of humidity-exposed SiC MOSFET 62 mm modules previously used for IGBT technology. In order to do so, the devices will be operated in a converter at rated current and voltage for an extended period of time while their blocking voltages are measured periodically. The reason to extend the test time to a few thousands of hours is that since the test is not accelerated, the degradation mechanisms may take longer to develop and be visible. The drawback of such a test, is that in order to have a statistical result of the failure mode, we would need a high number of modules (i.e. converters) exposed to humidity for a long time, which is costly. This is the main reason in favor of characterizing the devices during the testing period. Doing so, the parameter drifts can be detected before the devices have failed. Similarly, if a unit fails for other reasons than humidity, this trend can still be observed and data can be collected for further analysis.

**Test setup and test procedure**

In order to test the effect of humidity in SiC MOSFET power modules, height commercially available MOSFET modules with a 62 mm standard package are divided into two groups. The device under test is the CAS300M12BM2 from Wolfspeed (Infineon). Four modules are tested in two PE units placed outdoor and four are tested in two PE units placed indoor. More details on the setup can be found in [8]. The breakdown voltages are measured prior to testing and regularly during the year of testing, at room temperature. The breakdown voltage pre-stress is shown in Fig. 1. It can be seen that all devices have a breakdown voltage above 1.2 kV. Any increase in leakage current during the test indicates a degradation of the junction terminations [3]. If there is degradation, the avalanche will occur earlier in the blocking voltage span and what is observed is a reduced blocking voltage capability for 1 mA leakage current. A humidity and temperature sensor is placed in the converter enclosure close to the devices in order to monitor the variation of temperature and humidity locally inside the converter. The heat sink temperature is also constantly monitored.

The four converters are connected in parallel as presented in Fig. 2a. A fuse is connected in the current path to be able to disconnect immediately a converter in case of fault without affecting the other converters. The test setup placed outdoor is shown in Fig. 2b. The outdoor setup is protected from rain pouring on the converters and water penetration but neither from humidity and moisture, nor from daily temperature variations. The converters are exposed to humidity since the enclosures in which they are built are not hermetically sealed. The converter is a full-bridge with a resonant load as shown in Fig. 3. Thus, there are two half-bridge SiC MOSFET modules per converter. Converters 1 and 2 are placed indoor and converters 3 and 4 are placed outdoor, just outside the lab facilities. The converters
are water-scooled with converters 1 and 2 (respectively 3 and 4) sharing the same cooling system. Nevertheless, the 4 converters are operated with identical procedure. The part numbers of the modules in the different converters are given in Table I.

![Graph](image1.png)

**Fig. 1:** Pre-test breakdown voltage of the 8 modules (a) high side switch position (b) low side switch position

![Graph](image2.png)

**Fig. 2:** (a) Setup schematic diagram (b) test setup of the converter placed outdoor

![Diagram](image3.png)

**Fig. 3:** Schematic diagram for one converter

| Table I: Modules repartition in the converter |
|----------------|---|---|---|---|
| Converter #1    | #2 | #3 | #4 |
| Modules         | 225| 102| 122| 88 |
| Outdoor Modules | 275| 59 | 89 | 33 |

**Test results**

The modules have been characterized after 280 h, 630 h, 1700 h, 4460 h, and 5924 h. The test results are shown in Fig. 4 for one module placed indoor and one module placed outdoor. For the lowest switch position of the module placed outdoor, a noticeable difference in the leakage current between 4460 h and 5924 h is observed. The device only blocks 1090 V which is below the data-sheet specifications. On the contrary, the module placed indoor presents almost no variation both for the upper switch position and the lower switch position. The evolution over time of the blocking voltage...
(for 1 mA of leakage current) for all the DUTs is shown in Fig. 5. It can be seen that the device 122, also placed outdoor, also presents noticeable variations between the pre-test and the first post-test measurement.

All the modules are put back in the converters and the tests are ongoing. Even though module 33 has failed according to the device ratings, it is placed back into the outdoor located converter as well. The blocking voltage is still sufficiently above the 540 V dc-bus voltage. The reason to do so, is the test aims to observe degradation and potentially run the device until complete failure.

Conclusions and future work

In this work, four power modules have been operated in an environment exposed to humidity and fours power modules have been operated indoors. Several parameters have been monitored while the blocking voltages of the modules were measured regularly. Even though the test has not been accelerated, one module situated outdoor shows signs of degradation and is no longer blocking according to the datasheet specifications after 5924 h which is equivalent to approximately 8 months.
This shows that it may be required to use better packages for SiC MOSFET modules when the converters are operated outdoor or in harsh environments. The tests are still ongoing and the final results after 1 year (8000 h) will be presented in the final paper.

References


Publication VI

Abstract—An experimental analysis of the behavior under short-circuit conditions of three different silicon-carbide (SiC) 1200-V power devices is presented. It is found that all devices take up a substantial voltage, which is favorable for detection of short circuits. A transient thermal device simulation was performed to determine the temperature stress on the die during a short-circuit event, for the SiC MOSFET. It was found that, for reliability reasons, the short-circuit time should be limited to values well below Si IGBT turn-off times. Guidelines toward a rugged design for short-circuit protection (SCP) are presented with an emphasis on improving the reliability and availability of the overall system. A SiC device driver with an integrated SCP is presented for each device-type, respectively, where a short-circuit detection is added to a conventional driver design in a simple way. The SCP driver was experimentally evaluated with a detection time of 180 ns. For all devices, short-circuit times well below 1 µs were achieved.

Index Terms—Bipolar junction transistor (BJT), driver circuits, failure analysis, fault detection, fault protection, junction field-effect transistor (JFET), power MOSFET, semiconductor device reliability, short-circuit current, silicon carbide (SiC), wide-bandgap semiconductors.

I. INTRODUCTION

Silicon-carbide (SiC) transistors have undergone a great development over the past few years, and their level of maturity is now sufficient for product development of converters for various applications [1] ranging from motor drives for different kinds of vehicles [2] to various industrial applications [3], high-temperature operation [4]–[7], high-frequency applications [8], and renewable energy generation [9]. This interest motivates research efforts toward application reliability. The currently existing SiC power devices are junction field-effect transistors (JFETs) and metal-oxide semiconductor field-effect transistors (MOSFETs), which are unipolar and voltage-controlled, and the bipolar junction transistor (BJT), which is bipolar and current-controlled. However, it behaves as a unipolar device both with respect to conduction and switching properties [10].

Transient robustness of SiC transistors under short-circuit conditions has already been investigated. In [11]–[13], the conclusions are that the SiC MOSFET can withstand short-circuit conditions for 13–80 µs depending on its gate-to-source voltage and the dc-bus voltage. The short-circuit withstand time and critical energy of SiC MOSFETs are, however, reduced with the increase of case temperature [14]. In [15]–[20], the SiC JFET is also investigated and is found to be more rugged than the SiC MOSFET. It can handle short-circuit times of more than 1.4 ms with a 400-V dc-bus voltage [16]. The SiC BJT has been reported to withstand short-circuit conditions with durations of 15–20 µs [17], [21], and [22]. The good ruggedness indicates that a second breakdown is not likely with the SiC BJT, as it was with the power BJT in silicon [23].

For unipolar devices, it is observed in [16] that the saturation current density during a short-circuit event decreases significantly faster for the SiC JFET than for the SiC MOSFET leading to a faster temperature rise for the SiC MOSFET. The slower saturation process of the SiC MOSFET results in a higher current density than for the SiC JFET. Since the SiC BJT has the benefit of an intrinsic current limitation directly related to its amplification factor β, the SiC MOSFET is the device that will experience the highest short-circuit current with regard to the chip size. For this reason, it is likely that the MOSFET will experience the highest overvoltages when turning off the short-circuit current.

The failure analysis of the different SiC devices under short-circuit condition is in favor of an early short-circuit fault detection and extinction. Not only this strategy is limiting self-heating of the device, but also it is limiting the current that the device has to turn off. The oxide layer of SiC MOSFETs may be sensitive to high-temperature stress [24], [25], and gate failure can occur even after short-circuit has been turned off due to the heat spread from the drift region to the oxide [12], [26]. In [26], the gate oxide of SiC MOSFETs is shown to be less reliable than that of Si MOSFETs. The increased temperature during short-circuit conditions results in an increase of the gate leakage current [26], [27]. Even though it is likely that these issues will be alleviated in new generations of SiC MOSFETs [28], a limitation of the short-circuit time is probably still beneficial in terms of reliability.

The present paper investigates the possibility of detection and protection of a short-circuit event in the early stage of a fault as
II. SHORT-CIRCUIT BEHAVIOR OF SiC POWER DEVICES

There are two types of short-circuit faults. A fault occurring during the transistor turn-ON transient is referred to as hard switching fault (HSF), and a fault occurring during ON-state conditions is referred to as fault under load (FUL). A complete analysis of these two types of faults has been given in [34]. During both short-circuit types, the current rises rapidly and the device saturates. As previously investigated in [30], for SiC MOSFETs, both fault-types can be detected by means of the desaturation technique. However, the detection delay times are higher for HSF than for FUL. Consequently, only the HSF will be studied in this paper to limit the scope of investigation.

Prior to designing a SCP for SiC Power devices, the behavior of SiC power transistors during the early stage of a short-circuit fault is investigated. In Section III, the maximal short-circuit time acceptable with regards to reliability considerations will be discussed. The experiments aim for extracting the information on how a short-circuit fault can be detected and on how fast it can be detected. Moreover, the turn-OFF transients are analyzed to define an appropriate turn-OFF procedure in case of a short circuit. In fact, if the high switching speeds of SiC power transistors are fully utilized, this may cause excessive overvoltages when turning OFF a short-circuit current. Moreover, once a short-circuit condition has been detected, any additional delay before turning the short-circuit current OFF may reduce the lifetime of the device due to excessive localized heating. A short duration of the short-circuit condition is, therefore, preferable for reliability reasons. The test circuit is shown in Fig. 1. The dc-link voltage is $V_{dc} = 600$ V. The circuit stray inductance $L_s$ (excluding the capacitor and the device) has been determined experimentally to 32 nH. Assuming that the internal stray inductance $L_{ss}$ of the TO-247 package is 10 nH, the total circuit stray inductance is approximately 42 nH.

The currently available SiC power semiconductors are the MOSFET, the JFET, and the BJT. The SiC MOSFET and the SiC JFET are voltage-controlled, and the BJT is current-controlled. As these two device “types” perform differently with regards to overcurrent, they will be analyzed separately in the following sections.

A. Short-Circuit Behavior of Voltage-Controlled SiC Power Semiconductors

First, two different SiC MOSFETs (C2M0025120D from Cree and SCT2080KE from Rohm) and one SiC normally-ON JFET (UJN1205K from USCI) are investigated. The short-circuit pulse is of 500 ns for the MOSFETs and 250 ns for the JFET. The main difference between the two MOSFETs is the chip size and the chip thickness. The driver output stage is powered by a positive voltage source of +24 V and a negative power source of −5 V. The external gate resistance is 20 Ω for both turn-ON and turn-OFF. This value guarantees low oscillations at turn-ON and turn-OFF, while the switching times remain below 40 ns. In the case of the normally-ON SiC JFET, the driver was powered by a negative voltage source of −30 V, and the gate resistor was replaced by a DRC network as in [35] and [36].

The short-circuit behavior of the SiC MOSFETs from Cree and Rohm is shown in Figs. 2 and 3, respectively. The voltage across the SiC MOSFET does not drop significantly during the short-circuit pulse. As soon as the switch is turned ON, the current starts rising fast. Then, the rising slope decreases with time. Fig. 4 shows the short-circuit behavior of the SiC JFET under test. This device has the smallest chip area/volume of all the investigated devices. Since the SiC JFET saturation current density has a negative temperature coefficient [16], this device saturates faster than the previously investigated devices, and the current rises at a slower pace. The short-circuit peak current
Fig. 2. Short-circuited Cree MOSFET, \( R_G = 20 \Omega \). Measured gate-to-source voltage (yellow line: 50 V/div), drain-to-source voltage (purple line: 200 V/div), and drain current (pink line: 200 A/div). Time base: 200 ns/div.

Fig. 3. Short-circuited Rohm MOSFET, \( R_G = 20 \Omega \). Measured gate-to-source voltage (yellow line: 50 V/div), drain-to-source voltage (purple line: 200 V/div), and drain current (pink line: 200 A/div). Time base: 200 ns/div.

Fig. 4. Short-circuited normally ON JFET, \( R_G = 10 \Omega \). Measured gate-to-source voltage (yellow line: 50 V/div), gate current (green line: 5 A/div), drain-to-source voltage (purple line: 500 V/div), and drain current (pink line: 100 A/div). Time base: 50 ns/div.

Fig. 5. (a) Short-circuited SiC BJT, \( I_b = 1 \) A. (b) Short-circuited SiC BJT, \( I_b = 0.5 \) A. (c) Short-circuited SiC SJT, \( I_b = 0.75 \) A. Measured base-to-emitter voltage (yellow line: 10 V/div); base current (green line: (a) 1 A/div, (b) and (c) 2 A/div); collector–emitter voltage (purple line: (a) and (b) 200 V/div (c) 500 V/div); and collector current (pink line: (a) 20 A/div and (b) 50 A/div). Time base: 200 ns/div.

**TABLE I**

<table>
<thead>
<tr>
<th>SiC DUTs</th>
<th>( I_{\text{peak}} ) (A)</th>
<th>Overvoltage (V)</th>
<th>Turn-off time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M0025120D</td>
<td>500</td>
<td>200</td>
<td>320</td>
</tr>
<tr>
<td>SCT2080KE</td>
<td>300</td>
<td>150</td>
<td>140</td>
</tr>
<tr>
<td>UJN1205K</td>
<td>120</td>
<td>200</td>
<td>40</td>
</tr>
</tbody>
</table>

\( I_{\text{peak}} \), the overvoltage, and the short-circuit turn-off time for the voltage-controlled devices are summarized in Table I.

**B. Short-Circuit Behavior of Current-Controlled SiC Power Semiconductors**

In this section, two devices rated at 1200 V/50 A from two different suppliers are analyzed. Those are the SiC BJT from Fairchild (FSICBH017A120) and the super-junction transistor (SJT) from GeneSiC (GA50JT12-247). SJTs are super-high current gain SiC BJTs. For simplicity, this device will be regarded as a BJT in this paper. The SiC BJTs are driven by a so-called dual-source driver using a high voltage for fast switching and a low voltage for the continuous base current [37].

Even though the SiC BJT has similar conduction and switching properties as the voltage-controlled devices, it is current-controlled with regards to the maximum collector current. This feature, which can be seen as a limitation when it comes to driver designs, turns into an advantage when a reliable short-circuit protection is targeted. As the current is intrinsically limited, the turn-off voltage overshoot is expected to be limited. To emphasize the intrinsic current limitation of the SiC BJT, which depends on the base current \( I_b \), the two tests are performed with a base current of 1 A and 0.5 A, respectively, for the device from Fairchild. The short-circuit pulse is of 1 \( \mu \)s. This can be seen in Fig. 5(a) and (b). The results are also stated in Table II. The collector peak currents are, as expected, considerably lower than the maximum currents observed for the unipolar devices. This results in a considerably low overvoltage at turn-off. A similar behavior is shown in Fig. 5(c) for the GeneSiC device although this device saturates quicker.

![Diagrams](image1.png)

For all the tested devices, the voltage across the device during a short-circuit fault is approximately 300 times higher than during normal operation. Thus, the devices never leave the active region. As \( V_{ds} \) does not drop below 80% of the dc-bus voltage, an early detection is possible by measuring the
drain-to-source voltage of the device. This method, called “desaturation” technique, has already been used for Si devices [38]–[40]. SiC devices have a higher power density than their Si counterparts. Thus, it is important to clear the fault as soon as it has been detected to avoid unnecessary power dissipation and associated excessive heating. From a reliability point-of-view, a fast protection can prevent the device from early degradation. The short-circuit protection of SiC unipolar devices requires additional attention regarding the high-voltage overshoot at turn-off. On the contrary, the short-circuit protection of SiC BJTs does not require special considerations to handle the turn-off transients following a fault clearance. In fact, the limited short-circuit current reduces the overvoltages at turn-off. Moreover, the limited current limits the losses produced in the chip during fault events, which is certainly beneficial for reliability considerations. The authors believe that a proper protection strategy should improve the overall robustness of the converter.

III. TEMPERATURE DISTRIBUTION IN THE DIE DURING A SHORT CIRCUIT

This section discusses the time evolution of the temperature distribution in the chip during a short-circuit event. The device investigated here is the SiC MOSFET as its oxide layer may be sensitive to heat dissipation in the die [41], [42]. The gate oxide of SiC MOSFETs is thinner than the one of Si MOSFETs [26]. It is thus exposed to a higher electric field for a given gate bias. The high electric field and current density to which the oxide layer is exposed to during short-circuit conditions may increase the tunneling effect known as the main degradation mechanism of the oxide layer of SiC power MOSFETs [41]. The failure modes of SiC MOSFETs when subjected to longer short-circuits have been investigated in [43]. The presence of a gate leakage current after a few microseconds of short circuit is observed, which is not the case for Si devices. SiC MOSFETs showed low robustness to cumulative short circuits for longer short-circuit durations. The failure mode translates in a short circuit between gate and source for some devices, and other devices additionally have shorted drain and source.

A transient simulation is performed on the SiC MOSFET from Rohm (SCH2080KE). The device was decapsulated and analyzed by optical microscopy and scanning electron microscopy, and reconstructed by the numerical simulation program Synopsis Medici [44]. The boundary conditions were implemented according to the datasheet values for the packaged DUT, considering the specific construction of the package. The results from this simulation agree with the measured results in Section II. The thermal resistance and capacitance used in the simulation are \( R_\theta = 0.0918 \, \text{K/W} \) and \( C_\theta = 5 \times 10^{-3} \, \text{Ws/K} \).

In Fig. 6, the temperature distribution in the chip of the DUT after 500 ns of short circuit is shown. The maximum temperature is 267 °C, and any prolongation of the short-circuit duration will increase this value. The hotspot appears in the JFET region of the MOSFET (where the current concentrates) situated 2 \( \mu \text{m} \) below the gate oxide. This is not surprising, because this is the typical heat profile in any D-MOS device even during normal operation. Therefore, for any D-MOS SiC MOSFET, regardless of doping levels, the highest temperature will be situated just below the gate oxide. This supports the idea to clear the short circuit as fast as possible to prevent localized overheating of the gate oxide (for reliability reasons). The leakage current increase accelerates the oxide degradation during repetitive tests. An increase of the drain-to-source leakage current has also been reported in [12].

The SiC JFET has a recessed gate (or surface gate). In this case, the highest temperature is also situated close to the gate, and thus, the surface. Even though there is no oxide layer, repeated exposure to high temperature in time can be harmful for the passivation and metallization layers. The ageing of the SiC JFET due to multiple short-circuit events is characterized by an increase of the ON-state resistance [18], [45]. In [46], it is emphasized that, for the SiC JFET, a short duration of short circuit allows the device to sustain a considerably higher number of short-circuit events. Finally, for the BJT, the base region and collector region are about one order of magnitude narrower for SiC than for Si.

As the power density is higher for SiC compared to Si and since everything is thinner in SiC compared to Si, it is recommended, for reliability reasons, to consider short short-circuit times. The highest temperature occurs close to the top surface, which has much poorer cooling in wire-bonded encapsulated devices compared to the bottom surface. The reliability of SiC devices may be improved by means of an intelligent gate/base driver.

The source stray inductance also has an effect on the short-circuit behavior of SiC devices as shown in Fig. 7. Low-inductive circuits thus require a faster reaction to preserve the chip and package immunity. At times when even more circuits are desired to be low-inductive, the need of turning OFF the fault quickly becomes very relevant.

IV. SHORT-CIRCUIT PROTECTION

With the knowledge of the behavior of various SiC devices under short-circuit conditions acquired in Section II, several
Fig. 7. Effect of the source stray inductance $L_{ss}$ on the temperature rise.

design rules toward a rugged short-circuit detection can be derived. A driver with an integrated SCP can be designed based on those rules. While most driver manufacturers are targeting SiC MOSFETs, the proposed solution can also be applied to other SiC types. The main objective of this work is to implement a simple yet robust short-circuit detection that can be directly applied to a conventional driver design. Besides turning-off the short-circuit as quickly as possible, the SCP driver has to turn-off the fault in a safe manner. A fast detection combined with a slower turn-off is advisable for unipolar SiC devices, whereas for the BJT, only fast detection is beneficial due to the low-voltage overshoot at turn-off. Solutions for a gate driver providing a slower turn-off have been presented in [47]. In this paper, the slower turn-off is achieved, for the SiC MOSFET with asymmetrical gate resistors for turn-on and turn-off, as shown in Fig. 1.

A solution for SiC MOSFETs has recently been presented in [30], where rapid short-circuit detection is achieved. However, the turn-off times are relatively long. A solution for SiC JFETs has also been presented in [31]. While these two concepts involve the use of a comparator for the detection of de-saturation, the proposed design proposes a novel solution to increase the noise immunity in fast-switching environments. Logic gates with integrated Schmitt triggers are used here for voltage comparison. This solution is motivated by the fact that the voltage during a fault is of the order of hundreds of volts as shown in Section II.

Gate drivers for IGBTs and SiC MOSFETs with desaturation protection are already available. Prodrive in association with Cree offers a driver with overcurrent protection. The turn-off time is stated to be of maximum 1 µs. Cree has another dual-channel driver for SiC MOSFET modules with SCP (CGD15H62P). CISSOID also offers a driver (CHT-HADES2S) with SCP for high-temperature applications. This driver offers soft turn-off within 300 ns. The voltage comparison uses a comparator. The detection times are not clearly specified. Depending on the temperature of operation, 300 ns may be too long considering the change in short-circuit capabilities of SiC devices at higher temperatures [14].

SCALE-2 IGBT gate driver planar core from power integration is also offering an SCP. Its minimum response time is 1.2 µs. Even though time may have been improved in a newer version of the driver, the maximum output voltage (15–16 V) is below the required voltage to drive SiC MOSFETs in an efficient way. Similarly, Texas Instruments also have an IGBT and MOSFET driver with an integrated desaturation circuit having a reaction time of 2.7 µs.

Commercially available IGBT drivers using the desaturation detection technique could be used to detect a short circuit for SiC devices. Most drivers are also compatible with SiC MOSFETs and can offer a soft shutdown of the device in case of a short circuit. However, the offered reaction times are often too slow to provide a reliable protection of the device under fault. Nevertheless, from all the drivers specified above, the driver from CISSOID (CHT-HADES2S) is the most suitable driver for the short-circuit protection of SiC MOSFETs. The authors would like to stress the importance of dedicated desaturation circuits for SiC power devices.

The parameters that have to be taken into account when designing a SCP for SiC devices are briefly summarized in Section IV-A, where a clear description of the design challenges is provided.

A. Short-Circuit Detection Design

Since the on-state voltage drop of the device during a short-circuit fault is much higher than during the normal operation, the short-circuit condition can easily be detected by comparing the control input with the drain-to-source voltage (or the collector–emitter voltage). This detection method is known as the desaturation method [38]–[40]. As emphasized earlier, a fast detection not only reduces the current level at which the device has to be shutdown but also it limits the self-heating of the device as well. Additionally, the voltage overshoot at turn-off is limited. The proposed implementation has the following targets:

1) fast detection;
2) fast reaction to limit overheating;
3) limited turn-off speed for the SiC MOSFET and JFET;
4) easy implementation in any driver design;
5) high noise immunity.

Besides these targets, the driver has to be placed as close as possible to the gate and source pins of the device to avoid undesired parasitic elements.

The speed of detection is limited by the turn-on and turn-off times of the protected device. In addition, margins have to be considered to avoid false triggering or the SCP. In the present implementation, the fault detection delays are defined by RC filters. Fast detection delays are also limiting the overshoot at turn-off. A limited turn-off speed is also easily achieved by using different gate resistors for turn-on and turn-off. A drawback of this solution is that the switching losses at turn-off are increased. However, if very high switching speeds (and low switching losses) are targeted, a solution using an alternative gate resistance in case of a fault could be a solution. The proposed solution provides an easy implementation enhancing the driver reliability without affecting the driver characteristics during normal operation.

The structure of the short-circuit detection is shown in Fig. 8 for the case of a SiC BJT. The concept of the detection circuit is the same for the SiC JFET and MOSFET. The logic circuits used in this realization are from the TTL series, with a 5-V supply voltage for the SiC BJT and from the CD4000B series,
with modifications, for the SiC MOSFET and JFET (12 V and 15 V, respectively).

The collector–emitter voltage is sensed through $D_1$. The diode $D_2$ clamps the sensed voltage to protect the logic circuits. A Schmitt trigger AND $M_1$ is chosen for its high noise immunity. Above a certain voltage sensed by $D_1$, $M_1$ will sense a high voltage at its input $a$. This voltage can be adjusted by means of the voltage divider formed by $R_3$ and $R_4$. Its output will toggle to high if, and only if, the voltage sensed by its input $b$, sensing the control signal, is high at the same time. Thus, the AND gate acts as a comparator. For a better understanding, the truth table for the detection circuit is given in Table III. A D-type flip-flop $M_2$ is used in a later stage to hold the detected short-circuit signal when the control signal returns to zero. At the rising edge of the clock signal, the D-latch transfers its D input to its Q and $\bar{Q}$ outputs. The Q and $\bar{Q}$ outputs are the error signal (err) and the enable signal (en), respectively. Depending on the application, the err signal can be used to alert the main control system that a failure has occurred while the en signal is used to force the driver input to the OFF state. Q remains low until the whole system is shut down. The RC filters $\tau_1$ and $\tau_2$ are added before $M_1$, as shown in Fig. 9. The detection delays corresponding to $\tau_1$ and $\tau_2$ are then calibrated depending on the chosen device and the final application.

The presented short-circuit detection can be directly integrated into a conventional SiC power semiconductor driver. This integration allows a fast turn-OFF of the device at the inception of a short circuit, because the fault handling is performed locally without involvement of external control circuits. Being fully independent from the driver, it can easily be combined with almost any kind of driver without adding much complexity. Three different SCP drivers have been designed.

The SCP drivers for SiC power BJTs, SiC power MOSFETs, and SiC power JFETs are presented in Sections IV-B, IV-C, and IV-D, respectively. The performance of the SCP drivers is investigated by performing a short-circuit test and a double-pulse test. These tests are performed to verify that there are no erroneous short-circuit detections. The drivers—though without SCP—used in this paper have already been tested successfully in [48]–[50] for the SiC BJT, MOSFET, and JFET, respectively. The switching times during normal operation without SCP can be observed in these publications. Moreover, the robustness of the driver against noise was tested in an industrial converter in [49], where it is implemented in a 20-kHz three-phase 312-kVA inverter for an electrical vehicle with a total of 30 SiC MOSFET modules and 60 SCP drivers.

### B. Short-Circuit Protection of SiC Power BJTs

As seen in Section II, the peak fault current during a short-circuit condition is inherently limited for SiC BJTs. For a similar short-circuit duration, the SiC BJT will dissipate less energy than the SiC JFET and MOSFET. Nevertheless, there is no need to wait more than a few times the duration of a normal turn-ON to turn-OFF the short circuit. The RC filters are calibrated to achieve a short-circuit detection within 380 ns. The SiC BJT driver is the one used in Section II without modifications combined with the short-circuit detection [37].

The schematic diagram of the SCP driver for SiC BJTs is shown in Fig. 9, and its physical implementation is shown in Fig. 11(a). Additional components required for the detection circuit are also shown in the figure. In Fig. 9, $M_1$ and $M_2$ are two out of the four AND gates of a quadruple AND-gate circuit with Schmitt-trigger inputs SN74HC7001. The Schmitt trigger buffers are the single Schmitt-trigger buffer 741G17, and the flip-flop $M_2$ is a quad positive-edge triggered D-type flip-flop with reset 74HCT175.

The SCP driver performance during a short-circuit event is shown in Fig. 10 for both SiC BJTs and SJTs. The time delay between detection and protection $T_{d}$, the peak short-circuit current $I_{\text{peak}}$, as well as the short-circuit duration $T_{\text{sc}}$, are summarized in Table IV. The undershoot of the enable signal is due to noise induced by the turn-OFF transients. The noise immunity

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**TABLE III**

<table>
<thead>
<tr>
<th>Control signal</th>
<th>$V_{DS}$</th>
<th>AND</th>
<th>Meaning</th>
</tr>
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<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Circuit off</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Off-state</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>On-state</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Short-circuit or fault</td>
</tr>
</tbody>
</table>
of the system is sufficiently high, such that the short-circuit fault is turned off safely within less than 100 ns after its detection. The operation of the SCP driver during normal operation is validated by Fig. 11(b).

C. Short-Circuit Protection of SiC Power MOSFETs

The SCP driver for SiC MOSFETs should be designed carefully for the reasons mentioned in Sections II and III. Thus, the short-circuit detection times are reduced to the minimum value allowing a small margin to avoid false triggering. The turn-off is slowed down by means of asymmetrical gate resistors. As for the SiC BJT, a high noise immunity is also a requirement. This is achieved by the use of a Schmitt-trigger buffer instead of a comparator. In the scope of this paper, the chosen gate resistance values are 20 \(\Omega\) for turn-on and 20 \(\Omega\) for turn-off. These values can be tuned with regard to the final application.

The SCP driver for SiC MOSFETs is shown in Fig. 12. The schematic diagram of this realization is very close to the BJT implementation (see Fig. 9) with minor modifications. This driver has been tested in [49] in a real application for SiC MOSFET modules that have higher parasitic inductances than discrete devices. So far, no erroneous triggering of the SCP protection has been reported. In this realization, there is no real difference between driving a SiC discrete power device and a SiC power module.

The SCP driver is tested using the Cree (C2M0025120D) and Rohm (SCT2080KE) discrete devices as shown in Fig. 13. The short circuit is detected within 180 ns. The SCP driver with modified delays is also tested on a SiC MOSFET module (CAS100H12AM1 from Cree rated at 1.2 kV/100 A). The performance of the SCP driver during short-circuit conditions for the discrete devices and the module is stated in Table V.

Comparing these values with the values obtained in Section II for a discrete SiC MOSFET (see Table I), the voltage overshoot has been reduced by 25% while the peak current was reduced by 40% for the Cree device. The overshoot voltage reduction is explained by the lower current to be turned off. The lower current peak is explained by the shorter short-circuit duration. The SCP driver turns off the fault within 450 ns for both Cree and Rohm devices. The SCP driver was also tested during normal operation. For the sake of brevity, the double-pulse test is not shown here.

D. Short-Circuit Protection of SiC Power JFETs

The short-circuit protection of SiC JFETs is very similar to one of the SiC MOSFETs. The chosen power stage of the SiC JFET driver is the DRC network [35] with a \(-30\) V power supply. Even though this driver topology speeds up the turn-on and turn-off, the overvoltage of 200 V is judged to be within the reliability margin, since the peak overvoltage is 800 V. Moreover, the DRC network provides a stiff negative voltage to the gate at turn-off. The hardware realization of the SiC JFET SCP driver is presented in Fig. 14(a).

Fig. 14(b) shows the operation of the SCP driver with the normally on JFET UJN1205K from USCi. The short circuit is turned-off within 610 ns after the turn-on, which is a reasonable value since the JFET is known to be the most robust SiC device in terms of short-circuit durability (> 20 \(\mu s\)).

V. Discussion

In Section II, it was found that all three SiC transistors had a \(V_{ds}\) that remained high during the short-circuit event. However,
the different devices had different behaviors with respect to the current and overvoltage during the turn-OFF of a short circuit. From this point of view, the BJT was superior to the other devices, and the MOSFET was found to exhibit the highest current peaks and overvoltages among the devices. In the MOSFET case, it may be advantageous to have a separate slow-switching turn-OFF procedure in case of short circuit to prevent excessive overvoltages during turn-OFF. For all cases, a fast detection is possible since the short circuit can be clearly differentiated from the normal operation. As discussed in Section III, short-circuit events should be turned off as soon as possible to avoid unnecessary heating which may compromise the device integrity. The latter is particularly important regarding the SiC MOSFET whose oxide layer may be sensitive to overheating. Consequently, if the protection integrated in the driver is able to limit the fault duration, a larger number of short-circuit events can be endured by the SiC transistor before an impact on its characteristics can be detected.

In the previous section, designed rules toward an SCP driver improving the system reliability and availability have been presented. According to these rules, three different SCP drivers were designed and evaluated for different kinds of SiC devices. A selective and fast detection was implemented using the desaturation method and Schmitt-trigger gates for noise immunity. It was shown to be reliable, even in a fast-switching environment. The detection speed is of 180 ns. The protections have successfully been tested under short-circuit conditions as well as in a double-pulse test. For the SiC Rohm MOSFET, the short circuit was turned-off in 360 ns and for the SiC Cree MOSFET in 420 ns.

In state-of-the-art SiC converters, it is not uncommon that discrete devices or modules are placed in parallel [36], [48]–[51]. In such cases, each device could have a separate driver if fast-switching transients are targeted. If every driver is equipped with a short-circuit detection, the protection will probably be faster than if only one detection circuit for the whole switch position is used. The reason for this is that the current is likely to be unevenly shared among the parallel-connected devices. Since both the enable and error signals are available on the driver, a fault can be reported to the main control circuitry.

An important aspect on how to tune the delays of the detection circuit is to match those to the waveform of the turn-ON transient of the specific application. Special care has to be taken on this aspect if the load exhibits significant capacitive currents at turn-ON, as, for instance, a motor winding [52], [53]. If the detection delay is too short, even normal transients may erroneously be detected as short circuits.

VI. CONCLUSION

In this paper, the short-circuit behaviors of SiC MOSFETs, SiC JFETs, and SiC BJTs have been presented. A transient thermal device simulation was performed for the SiC MOSFET revealing that the hottest temperature is located 2 µm below the oxide layer. After 500 ns, this point reaches a temperature of 267 °C. The analysis of the behavior led to guidelines toward the design of a selective and fast short-circuit detection and protection. The fastest detection speed was 180 ns. This value includes the delays considered to avoid erroneous triggering of the short-circuit protection. One driver for each device-type is presented and tested. The experimental results show that the drivers have the capability to clear a short-circuit fault within less than 600 ns for all three devices investigated (360 and 420 ns for MOSFETs, 500 ns for BJTs, 600 ns for JFET). For all SiC device-types, the proposed short-circuit protection can easily be integrated in custom driver designs.

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Publication VII


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Comparison of Thermal Stress during Short-Circuit in Different Types of 1.2 kV SiC Transistors Based on Experiments and Simulations

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Keywords: Bipolar junction transistor (BJT), junction field-effect transistor (JFET), power MOSFET, semiconductor device reliability, failure analysis, short-circuit current, silicon carbide (SiC), wide-bandgap semiconductors

Abstract. The temperature evolution during a short-circuit in the die of three different Silicon Carbide 1200-V power devices is presented. A transient thermal simulation was performed based on the reconstructed structure of commercially available devices. The location of the hottest point in the device is compared. Finally, the analysis supports the necessity to turn-off short-circuit events rapidly in order to protect the device immunity after a fault.

Introduction

The short-circuit (SC) behaviour of three Silicon Carbide (SiC) devices available on the market was investigated in [1]. The present paper compares the evolution in time of the temperature distribution in the chip of 3 different types of 1.2 kV SiC transistors during a short-circuit event. In [2] the maximum junction temperature evolution in time for a SiC MOSFET and a SiC BJT (SJT) has been computed by means of a Cauer model. In contrast, in this work, devices have been de-capsulated in order to reconstruct their structures in Taurus MEDICI [3]. Similar work for the SiC JFET has already been performed in [4]. The temperature distribution in the chip of each device is then simulated based on the experimental short-circuit tests. Moreover, results for a SiC JFET are presented.

Experimental Setup

The measured and simulated structures were SiC MOSFET, SiC BJT and SiC JFET, rated at 1.2 kV. The test circuit is illustrated in Fig. 1, where \( V_{dc} = 600 \) V, \( C_{in} = 160 \) \( \mu \)F and \( L_{stray} = 10 \) nH. The drivers used to turn the devices on are adapted to the device type. More informations on the drivers used in this work can be found in [1]. The short circuits experimental results for the SiC MOSFET, SiC BJT and SiC JFET are illustrated in Fig. 2, where the devices are turned into a short-circuit (short-circuit type I) under \( V_{ds} = 600 \) V. The devices under test and their short-circuit peak current \( I_{sc,peak} \) and the over-voltage at turn-off are stated in Table 1.

<table>
<thead>
<tr>
<th>SiC DUTs</th>
<th>( I_{peak}[A] )</th>
<th>Overvoltage [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCT2080KE</td>
<td>300</td>
<td>150</td>
</tr>
<tr>
<td>UJN1205K</td>
<td>120</td>
<td>200</td>
</tr>
<tr>
<td>GA50JT12-247</td>
<td>80</td>
<td>25</td>
</tr>
</tbody>
</table>

Device Structure

To obtain precise information on the device structure, the devices were decapsulated as in [5]. Dimensions of the device structures for simulation were investigated and obtained by scanning electron...
Fig. 1: Schematic diagram of the short-circuit test for a discrete device

Fig. 2: Short-circuit behaviour of SiC devices (a) SiC MOSFET, (b) SiC JFET and, (c) SiC BJT

microscopy (SEM) [4]. The structures were further calibrated by comparison of simulated static electrical characteristics – output, gate transfer and blocking characteristics – with the datasheet values. SEM pictures are given in 3, for the SiC MOSFET, SiC JFET and, SiC BJT (SJT). The driving conditions are as in the experiment and the source stray inductance has been measured and is set to 10 nH for the best fit to the measured currents and voltages during the SC tests, see Fig. 3a for the SiC MOSFET, Fig. 3b for the SiC JFET and, Fig. 3c for the SiC BJT respectively. The simulated curves are shown in Fig. 4. It can be seen that they are corresponding to the experimental curves shown in Fig. 2.

Fig. 3: Device structures of the (a) SiC MOSFET, (b) SiC JFET and, (c) SiC BJT

Electro-thermal simulations of SiC MOSFETs, BJTs and normally-On JFETs

The temperature distributions in the SiC JFET, SiC BJT and SiC MOSFET after 500 ns can be observed in Fig. 6a, Fig. 6b, and Fig. 6c, respectively. In the SiC JFET device the hottest area is located in the drift region and also deepest in the structure and farthest away from the top surface compared to the
SiC BJT and SiC MOSFET. The distance to the surface is 6 µm and the distance to the trench bottom is 2.5 µm. In the SiC BJT the hottest area is located in the collector region close to the base-collector junction and under the edge of the emitter. The distance to the surface is 4 µm and 1.5 µm to the base-collector junction. Finally, in the SiC MOSFET the hottest area is located under the gate and just below the JFET region of the DMOSFET structure. The distance between the hottest area and the surface (and gate-oxide) is 2 µm. This is significantly smaller than for the two other device types. After 500 ns, the maximum temperature values from the simulations are 273 °C, 108 °C and 136 °C for SiC MOSFET, SiC JFET and SiC BJT, respectively. After 1 µs of SC stress the maximum temperatures are 402 °C, 227 °C and 187 °C . The temperature evolution for a short-circuit event of 1 µs is shown in Fig. 5. It can be observed that for the SiC MOSFET, the temperature in the die rises significantly higher than for the other devices. This may be critical considering the narrow distance between the hottest point and the surface and gate-oxide. The active device area is 0.071, 0.141 and 0.096 cm² for the SiC JFET, SiC BJT and SiC MOSFET, respectively. Thermal boundary conditions were obtained from the fit to the thermal impedance data for pulse width less than 0.001 sec for each device. The differences between the localization of the hottest region and the simulated maximum temperature values are clearly related to the physics of operation and unit cell design of the different devices. Although for the SiC MOSFET, the oxide layer can withstand higher temperatures than 273 °C, this high temperature can be critical for the encapsulating material or lead to increased gate leakage current due to charge transport over the potential barrier. The latter observations show that it is important to turn-off a short-circuit fault quickly when using SiC MOSFETs since the temperature rise is quicker. The turn-off time can be longer for SiC JFETs and SiC BJTs. The two latter devices are therefore more robust against short-circuit faults.
Fig. 6: Temperature distribution in the device die after a 500 ns short-circuit event a) SiC MOSFET $T_{\text{max}} = 273 \, ^\circ\text{C}$, (b) SiC JFET $T_{\text{max}} = 108 \, ^\circ\text{C}$, (c) SiC BJT $T_{\text{max}} = 136 \, ^\circ\text{C}$

Summary

The present paper investigated the temperature distribution in the chip of three different SiC devices after 1 $\mu$s of short-circuit fault. The results of the simulations revealed that the SiC MOSFET was the device that requires the fastest turn-off response time in case of a short-circuit since it has both the highest temperature rise after 1 $\mu$s as well as the shortest distance between the hottest point in the die and the surface. Moreover, considering that the oxide-layer may be more sensitive to higher temperature than the surface, limitation of the short-circuit duration is desirable in order to preserve the device immunity. Secondly, although the SiC JFET has a wider distance between the hottest point and the surface than the SiC BJT, the temperature rise in the SiC JFET is approx. 8 % higher after a short-circuit of 1 $\mu$s compared to the SiC BJT. This value increases to 33 % for the SiC MOSFET.

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Publication VIII


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Investigation of the Surge Current Capability of the Body Diode of SiC MOSFETs for HVDC Applications

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Abstract

<<Silicon Carbide (SiC)>>, <<MOSFET>>, <<Diode>>, <<Reliability>>, <<Faults>>, <<Voltage Source Converter (VSC)>>

Abstract

The surge current capability of the body-diode of SiC MOSFETs is experimentally analyzed in order to investigate the possibility of using SiC MOSFETs for HVDC applications. SiC MOSFET discrete devices and modules have been tested with surge currents up to 10 times the rated current and for durations up to 2 ms. Although the presence of stacking faults cannot be excluded, the experiments reveal that the failure may occur due to the latch-up of the parasitic n-p-n transistor located in the SiC MOSFET.

Introduction

Over the past few years, silicon carbide (SiC) power transistors, especially SiC MOSFETs, have been developed extensively. They present several advantageous characteristics that make them attractive for power electronic applications such as railway traction and automotive applications [1] where they are foreseen to replace Si technology. Another possible application is high-voltage direct current (HVDC) transmission where SiC technology can offer higher efficiencies due to lower on-state resistance and faster switching capability [2]. Nowadays, HVDC converters are often built with Si IGBT technology combined with a high-power antiparallel diode since the IGBTs cannot conduct current in the reverse direction. SiC MOSFETs are foreseen to replace IGBTs in the next generations of power electronic converters, and, as they have an intrinsic diode, diode-less operation is an attractive option to lower the overall system cost.

However, the body diode of SiC MOSFETs has, in the past, suffered from Shockley Stacking Faults (SSFs), growing from Basal Plane Dislocations (BPDs) or Threading Dislocations (TDs) [3]. These structural defects, which grow when current is conducted in the body-diode forward direction, translate in an increase of the forward voltage drop of the body-diode as well as an increase of the on-state resistance. The latest generations of SiC MOSFETs with optimized epitaxial layers have been reported to suffer less from this issue [4]–[7] than previous generations. In [5], the body-diode of 3.3 kV MOSFETs have been successfully tested with a current density of 100 A/cm² during 1000 h. In [6] and [7], 1.2 kV discrete MOSFETs have been successfully tested during 1000 h (50 A/cm²).

Nevertheless, in HVDC converters, one of the antiparallel diode is exposed to very high transient currents during a short circuit event on the dc grid [8], as seen in Fig. 1. The peak surge current may be as high as 10 times the rated current of the device. If SiC MOSFETs are considered in HVDC applications, the reliability and ruggedness of the SiC MOSFET body-diode with regards to surge currents has to be
investigated, in particular because a thick drift layer has a large impact on the MOSFET degradation during forward current stress [1]. So far, no study has been found on the topic. Finally, the possibility to open the SiC MOSFET channel during a surge-current event [9] will be investigated and discussed.

**Surge Current Requirements for HVDC converters**

The dc grid and its components must in particular be protected against short-circuits, which represent the most harmful event in a dc network [11]. This situation arises whenever a fault on the dc line occurs which is particularly common with dc overhead lines and is usually caused by a lightning strike. However, the worst case fault for voltage source converters (VSCs) is a fault at the local dc bus [12]. During the dc fault the current flows from the ac grid to the dc fault. Shortly after the dc fault instance, the IGBTs have to be tripped by the feedback overcurrent protection [13]. Once the IGBTs are blocked, the VSC behaves as an uncontrolled diode bridge where the diodes experience the full fault current until circuit breakers (CB), either on the ac side or, if available, on the dc-side terminal of the converter, open and isolate the faulty line. This is the most critical phase for the system because the diode currents jump to a dangerously high value which might be beyond their surge current rating [14]. The current through the diodes is determined by the fault level of the local ac grid limited by the transformer impedance and the phase reactor impedance. The worst case peak diode current can therefore be calculated as,

\[ I_{sc} = 2\sqrt{2} \frac{V_{ac}}{Z_{sc} + Z_{ac}} \]  

where \( Z_{sc} \) is the short-circuit impedance of the grid and \( Z_{ac} \) represents the overall ac-side impedance of the converter. The peak short-circuit current given by (1) is generally much higher than the normal operating current, see Fig. 2. The fault response of a two-level VSC, (Fig. 1a) is similar to that of an MMC (Fig. 1b). However, only the two-level VSC will have uncontrolled dc capacitor discharge, whereas an MMC will not discharge the cell capacitors into the fault. Therefore, the initial transient of direct current is lower with an MMC compared to a two-level VSC [13].

Fig. 2: One of the ac-side currents during a stiff dc-side short-circuit fault in a half-bridge MMC.
Table I shows high-power IGBT data relevant for fault tolerance. The IGBTs should be tripped before the fault current exceeds the peak current $I_{CM}$ which is normally twice the direct current rating. The surge current capability $I_{FSM}$ provides information on the capability of the diode to withstand a dc fault for 10 ms half-cycle. As can be seen from Table I, for an HVDC system the surge peak current in the diode may be as high as 7-10 times the direct current rating. If only ac CBs are used which have clearing times around 50 ms [13], the diode surge current will have to be well below the given 10 ms $I_{FSM}$ values. However, dc CBs feature a much shorter overall fault clearing time of about 2 ms [14]. Thus, using dc CB would be favorable with regards to the maximum surge current that has to be endured by the diodes.

<table>
<thead>
<tr>
<th>IGBT</th>
<th>Rated Voltage $V_{CBS}$ (V)</th>
<th>Rated Current $I_C$ (A)</th>
<th>Peak Current $I_{CM}$ (A)</th>
<th>Diode Surge Current $I_{FSM}$ (A) (10ms, half sine)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABB 5SNA 0750G650300</td>
<td>6500</td>
<td>750</td>
<td>1500</td>
<td>8000</td>
</tr>
<tr>
<td>ABB 5SNA 1200G450300</td>
<td>4500</td>
<td>1200</td>
<td>2400</td>
<td>9000</td>
</tr>
<tr>
<td>ABB 5SNA 1500E330300</td>
<td>3300</td>
<td>1500</td>
<td>3000</td>
<td>14000</td>
</tr>
</tbody>
</table>

The arm inductor $L_{arm}$ has a direct impact on the diode current and can be designed, according to Equation (2), to limit the peak current to $i_{D,max}$ for known values of the dc-bus voltage $V_{dc}$, direct current $I_d$ and IGBT turn-on time $t_f$ [14].

$$L_{arm} > \frac{V_{dc}}{2} \left( \frac{t_1 - t_0}{i_{D,max}} - \frac{i_{dc}}{3} \right)$$

(2)

**Test Setup**

The standard datasheet tests for SiC MOSFETs typically use a half sine wave with duration of 10 µs. However, as mentioned in the previous paragraph, the diode in a HVDC configuration may have to withstand longer surge current durations. During a surge current, the temperature rise in the die will depend on the pulse current amplitude and its duration, the initial die temperature and the diode forward voltage. The thermal impedance of the device and the initial case temperature also have an impact on longer pulse durations [15].

In order to investigate the behavior of the body-diode of the SiC MOSFET during surge current, a surge current setup was built as shown in Fig.3. The devices under test (DUTs) are placed in the circuit in such a way, so that, when the auxiliary switch closes, a surge current flows through their body-diode. The DUTs are the latest 900 V, 1.2 kV and 1.7 kV SiC discrete MOSFET devices and SiC MOSFET modules available on the market and their characteristics are stated in Table II. The gate-source voltage of the DUTs is set to -5 V in order to keep the device firmly in the off-state. In this way, the surge current flows only in the body-diode and not in the channel for the discrete devices. Three out of the four modules (M2, M3 and M4) are populated with parallel Schottky diode chips. Therefore, at low forward voltages ($V_f$) only the SiC Schottky will be conducting and the MOSFET chip is not conducting current. However, at a $V_f$ higher than the cut-off voltage of the body-diode, the SiC Schottky diode and the body-diode are sharing the surge current. Consequently, at higher current levels, the current will flow both in the Schottky and the MOSFET via the body-diode. In a second step the surge current capability of the devices in the reverse direction while turning-on the channel is also investigated. The surge current magnitude depends on the impedance of the setup circuit and on the magnitude of the direct voltage applied. The duration of the half-sine current wave and the peak surge current can be adjusted by a proper selection of the dc capacitor $C_{dc}$ and of the inductor $L$ according to Equations (3.1)-(3.3).

Table II: High-power IGBT data [12]
\[ Z_0 = \sqrt{\frac{L}{C}} \quad (3.1) \]
\[ \omega_0 = \frac{1}{\sqrt{L}C} \quad (3.2) \]
\[ \hat{i} = \frac{V_{dc}(0)}{Z_0} \quad (3.3) \]

Table II: Main characteristics of the devices under test (DUTs)

| SiC DUTs | Part number | \( V_{DS} \) [V] | \( I_D \) [A] | \( R_{DS(on)} \) [mΩ] | \( V_{GS} \) [V] | Schottky diode
|---------|-------------|-----------------|---------------|---------------------|--------------|---------------------------
| R1      | SCT2080KE   | 1200            | 40            | 80                  | -6 / 22      | NO                        |
| R2      | SCT3040KL   | 1200            | 55            | 40                  | -10 / 22     | NO                        |
| C1      | C2M0025120D | 1200            | 60            | 65                  | -5 / 20      | NO                        |
| C2      | C3M0065090D | 900             | 23            | 25                  | -5 / 15      | NO                        |
| M1      | BSM180D12P2C101 | 1200          | 180           | TBD                 | -6 / 22      | NO                        |
| M2      | BSM120D12PC005 | 1200          | 120           | TBD                 | -6 / 22      | YES                       |
| M3      | APTMCT70AM07CD3AG | 1700          | 240           | TBD                 | -10 / 25     | YES                       |
| M4      | CAS300M17BM2 | 1700            | 225           | 10                  | -5 / 20      | YES                       |

**Experimental Results – preliminary tests at 10 μs**

Preliminary tests were performed on the devices C1 and C2. The devices were tested with a 10 μs pulse at 280 A with 0 V across their gate-source junction. Moreover, the devices were heated from room temperature (25 °C) to 150 °C to study the effect of temperature on the surge current of the body-diode [16]. As can be seen in Fig. 5(a) and Fig. 5(b), the temperature has no significant influence on the body-diode characteristics at high currents. However, as can be observed in Fig. 6, at low current, an increase in case temperature has an impact on the body-diode characteristics.
Experimental Results – longer duration tests and destructive tests

In this part, the DUTs have been tested with surge current durations up to 2 ms. The discrete devices and modules were characterized prior to test. The modules were tested after the 680 µs surge current test and 1.8 ms surge current test revealing a reduction in blocking capabilities for some devices. The DUTs were tested until failure or until 10 times the rated current. The post-destructive characterization revealed a broken diode and a broken junction for C1, C2, R1, and R2. In all cases, the gate-source junction was shorted after failure and the diode was no longer blocking. Some MOSFETs had a channel conducting with a high resistance and others were completely short-circuited. A discussion about the observed failure modes is given in the section “Failure Modes” below. The hypothesis of the authors is that the failure mechanism of the SiC MOSFETs is the activation of the parasitic npn-transistor, leading to a bipolar second breakdown as described in [17], [18]. The following tables summarize the maximum tested surge current without failure for different lengths of surge currents except for section 2. After all these tests, the devices were still operating and the diode still blocking. The pulse could be repeated without breaking the device. Not all devices have been tested for all cases due to the limited amount of devices available.

1. Surge current at room temperature – discrete devices -  
   a. 280 µs surge currents at 1-10 times rated current (R1, C1)

<table>
<thead>
<tr>
<th>DUT</th>
<th>I_{sd,max} [A]</th>
<th>V_{sd,max} [V]</th>
<th># of samples tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>469</td>
<td>9.5</td>
<td>1</td>
</tr>
<tr>
<td>R1</td>
<td>401</td>
<td>13.0</td>
<td>1</td>
</tr>
</tbody>
</table>

Fig. 5: Body-Diode Characteristics of (a) C1 and (b) C2 for a 10 µs pulse (280 A peak) at 25 ºC and 150ºC

Fig. 6: C2 - (a) Half-sine wave (10 µs, 10 A peak) (b) Body-Diode characteristics at 25 ºC and 150ºC
b. 870 µs surge currents at 1-10 times rated current (R1, R2, C1, C2)

Table IV: 870 µs surge currents

<table>
<thead>
<tr>
<th>DUT</th>
<th>Isd,max [A]</th>
<th>Vsd,max [V]</th>
<th># of samples tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>388</td>
<td>9.8</td>
<td>1</td>
</tr>
<tr>
<td>C2</td>
<td>205</td>
<td>12.7</td>
<td>2</td>
</tr>
<tr>
<td>R1</td>
<td>270</td>
<td>12.7</td>
<td>6</td>
</tr>
<tr>
<td>R2</td>
<td>177</td>
<td>13.0</td>
<td>1</td>
</tr>
</tbody>
</table>

For the device R1, the surge current test with length of 870 µs was repeated identically on a total of 6 devices. The observation is that all devices fail when the forward voltage of the body-diode exceeds approximately 13 V. This result is similar to what has been observed on R1 in section 1a. for 280 µs. Similar observations concern device C1 which fails when $V_{SD}$ exceeds 9.5 V. Note that the body-diode forward voltage may vary for similar devices in the same batch [7]. Thus, the values observed here may vary.

c. 1.8 – 2 ms surge currents at 1 – 10 times rated current (C1, C2, R1)

Table V: 1.8 – 2 ms surge currents

<table>
<thead>
<tr>
<th>DUT</th>
<th>Surge length</th>
<th>Isd,max [A]</th>
<th>Vsd,max [V]</th>
<th># of tested devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1.8 ms</td>
<td>590</td>
<td>8.6</td>
<td>4</td>
</tr>
<tr>
<td>C2</td>
<td>2.0 ms</td>
<td>95.6</td>
<td>9.5</td>
<td>2</td>
</tr>
<tr>
<td>R1</td>
<td>2.0 ms</td>
<td>275</td>
<td>12.5</td>
<td>2</td>
</tr>
</tbody>
</table>

2. Surge current of C1 at different temperatures

The device C1 has been tested until failure at temperatures from 25 °C to 100 °C with steps of 25 °C. The DUTs are placed for 30 min in a temperature chamber at the desired temperature and then tested while being in the chamber. The results are summarized in Table 6 below where the current at failure and the diode forward voltage are given. The maximum surge current is decreasing as the temperature increases and the voltage over the diode is decreasing as well. One possible explanation is that the temperature affects the threshold voltage of the parasitic npn-transistor in such a way that less current is required to provoke its turn-on at higher chip temperatures [19]. This supports the hypothesis that the failure is triggered by the latch-up of the parasitic npn-transistor in the SiC Power MOSFET rather than by stacking faults.

Table VI: Surge currents at different temperatures

<table>
<thead>
<tr>
<th>DUT</th>
<th>Temperature [°C]</th>
<th>Isd,max [A]</th>
<th>Vsd,max [V]</th>
<th># of tested devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>25</td>
<td>617</td>
<td>10.0</td>
<td>4</td>
</tr>
<tr>
<td>C1</td>
<td>50</td>
<td>550</td>
<td>8.9</td>
<td>1</td>
</tr>
<tr>
<td>C1</td>
<td>75</td>
<td>544</td>
<td>9.7</td>
<td>2</td>
</tr>
<tr>
<td>C1</td>
<td>100</td>
<td>512</td>
<td>8.5</td>
<td>2</td>
</tr>
</tbody>
</table>

3. Surge current while opening the SiC MOSFET channel during a 2 ms surge current

Surge current while opening the SiC MOSFET channel has also been tested on discrete devices. However, the SiC MOSFET did not survive for as high currents as the ones supported by the body-diode conduction. The probable reason is that the channel area is narrower than the body-diode conduction region. Therefore, there will be a higher current concentration flowing into the open channel during a surge event. As presented in [20], the hottest point in the SiC MOSFET during a short-circuit event is located in the JFET region, just below the gate-oxide. This can cause irreversible damage to the gate-oxide but also the heat dissipated on the top surface of the SiC MOSFET will be concentrated in a smaller area than when the body-diode is conducting. For these reasons, and since no signs of stacking faults have been observed in the commercialized devices, the authors believe that – while the current levels remain below the critical current causing the npn-parasitic transistor to turn on – conduction through the body diode is appropriate for discrete devices.
4. Multiple surge current (20 times) – discrete devices (C1 and R1)
The robustness of the body-diode SiC MOSFETs against multiple 2 ms surge events at currents up to 9 times the rated current has been tested for the discrete devices C1 at 450 A (2 DUTs) and R1 at 250 A (3 DUTs). The maximum surge current was chosen such that \( V_{SD} \) remains below the value potentially latching up the npn parasitic transistor. The devices have been characterized before stress and after 20 surge current pulses. The characterization post-test revealed an increase of leakage current at 1.2 kV of 30 – 40 %. However, the body-diode characteristics remained identical after stress.

5. Surge current at room temperature – SiC MOSFETs modules
The surge current in the reverse direction of SiC MOSFET modules has also been tested. The modules under test are stated in Table II. Three out of the four modules in this test contain Schottky diode chips in parallel with the SiC MOSFET chips. Therefore – since the body-diode knee voltage is somewhat higher than the Schottky diode knee voltage – at low current levels, only the Schottky chips will be conducting. However, as higher current flows between the source and the drain, the voltage drop across the source-drain terminals becomes sufficiently high to turn the body-diode on. At this point, the current \( I_{SD} \) will be shared between the body diodes and the Schottky diodes.

The modules have been tested from 1 to approximately 10 times the rated current. The summary of the tests is presented in Table VII. The modules M1 and M2 are populated with the same SiC MOSFET chips which correspond to the chip contained in the discrete device R1. Although one of the modules (M2) contains parallel Schottky chips, it also fails at 10 times rated current when \( V_{SD} \) is almost 15 V. As observed in the previous sections, the maximum voltage across the body-diode prior to failure was 13 V. Since both devices M1 and M2 (with and without parallel connection of Schottky and body diode) failed at voltages above 13 V, it is the hypothesis of the authors that the cause of failure is also the latch-up of the parasitic npn-transistor in the SiC MOSFET chips. The fault is thus dependent on the voltage across the body-diode. Note that the devices M3 and M4 are 1.7 kV devices. Their chips have not been tested in discrete devices. However, M3 and M4 experienced lower voltage drops during a surge in the reverse direction at 10 times the rated current than M1 and M2.

<table>
<thead>
<tr>
<th>DUT</th>
<th>Pulse length [ms]</th>
<th>( I_{sd,max} ) [A]</th>
<th>( V_{sd,max} ) [V]</th>
<th>Schottky</th>
<th>Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>1.25</td>
<td>1850</td>
<td>15.8</td>
<td>No</td>
<td>Yes – shorted (gate + channel)</td>
</tr>
<tr>
<td>M2</td>
<td>1.75</td>
<td>1190</td>
<td>14.9</td>
<td>Yes</td>
<td>Yes – shorted (gate + channel)</td>
</tr>
<tr>
<td>M3</td>
<td>1.75</td>
<td>2310</td>
<td>8.7</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>M4</td>
<td>1.75</td>
<td>2220</td>
<td>8.0</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Failure Modes
There are two observed failure modes for the discrete SiC MOSFETs. The failure pulses can be observed in Fig. 7 and Fig. 8 for C1, R1, R2, and C2, respectively. At first there is a reduction in blocking capabilities and finally leakage through the gate – eventually, the gate-source junction is shorted. While analyzing the discrete devices after the destructive test, it was found that the body diode was broken as well.

Fig. 9 shows a cross-sectional drawing of the SiC MOSFET where the critical point (A), right below the edge of the oxide, can be observed. Eventually, there will be a current filament formed at this location all the way to the drain side and destruction will occur due to excessive heat. The short-circuited gate can be explained by the excessive heat produced at point A which is right below the edge of the oxide. This is a weak point of the oxide since excessive heat at this point could cause interlayer dielectric erosion leading to a gate-source short-circuit as observed in [21]. This phenomenon can already occur when the device is stored at 500 °C for 2 h. Considering the amount of current flowing through the device when the failure
occurs (above 9 x rated current), the authors believe that the temperature reached at the oxide edge during a failure exceeds 500 °C. However, this has to be verified by thermo-electrical device-level simulations which will be performed in the near future. Additionally, it is the authors’ hypothesis that due to the excessive heating, solder layers and metallization may have been destroyed. None of these hypotheses have been confirmed, but a close future post-fault examination of these devices will be performed.

Fig. 7: Source-Drain Current $I_{SD}$ and Source-Drain Voltage $V_{SD}$ in C1 during failure.

For some of the R1, the observed failure is a gate-source high leakage current (or short-circuit) and an open channel. The diode is in every case broken. Thus, the device no longer blocks voltage. The authors believe that the failure mode may be due to a fusion of the metallization on the top side of the SiC MOSFET chip. For C2, the observed failure is also a gate-source high leakage current.

Fig. 8: Source-Drain Current $I_{SD}$ and Source-Drain Voltage $V_{SD}$ of (a) R1, (b) R2, (c) C2 during failure.
Fig. 9: Reverse recovery current path in the body diode within the SiC power MOSFET DMOS structure

An example of the gate-source voltage and source-drain voltage of the device during a failure are shown in Fig. 10 for the device R2. The gate slowly fails into a short-circuit over a few ms. Similar observations have been made in [22] for SiC MOSFETs under short-circuit operation where the gate failed due to the dissipated energy 11 µs after turning off the short-circuit event. This observation supports the hypothesis of high temperature stress on the gate-oxide which leads to high leakage current in the gate. Similar observations, but during short-circuit tests of Rohm devices versus Cree 2nd generation devices, were presented in [22], [23].

![Gate voltage during fault - R2](image)

Fig. 10: Gate-Source Voltage during a failure pulse where the voltage slowly rises from -5 V to 0 V

**Conclusions and Future Work**

In this paper, the surge current capability of SiC MOSFET discrete devices and modules is investigated. The hypothesis of the authors is that the cause of failure of the DUTs is the latch-up of the parasitic npn-transistor of the SiC MOSFET. All the devices failed when the voltage across their body-diode exceeded a critical value, regardless of the duration of the surge current. An identical behavior was observed for the modules containing Schottky diode chips. However, as long as the current flowing in the reverse direction does not induce this critical voltage, the devices could withstand repetitive surge events far above rated current. An increase of leakage current at 1.2 kV was observed. At this stage, the presence of stacking faults in the body-diode has not been observed. In future work, the devices will be opened in order to confirm the failure mechanism observed and eventually exclude the presence of stacking faults in commercially available devices.

**References**


10.2. SUGGESTED FUTURE WORK

Publication IX


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Introduction of SiC MOSFETs in Converters
based on Si IGBTs
A Reliability and Efficiency Analysis

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Abstract—Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) have the potential to increase the power density in power electronics converters compared to the currently used silicon (Si). Their benefits are higher efficiency, higher switching speeds, and higher operating temperatures. Moreover, SiC MOSFETs, which are normally-off, offer the possibility to directly replace Si Isolated-Gate-Bipolar-Transistors (IGBTs) in already existing converter designs with minimal circuit changes. Nevertheless, as an emerging technology, the reliability performance remains to be investigated. A reliability analysis has been performed based on a full-bridge resonant converter rated at 60 kW for modern Electrostatic Precipitator (ESP) power supplies. This analysis shows that introducing SiC devices will increase the lifetime of the converter while reducing the losses. The investment costs of replacing the Si IGBTs with SiC MOSFETs can thus be covered with the reduction of the losses over the economical operational lifetime. Furthermore, a theoretical analysis on how introducing SiC MOSFETs could increase the power density of the converter while maintaining the efficiency and the reliability. Finally, an analysis on introducing redundancy as a way to improve the reliability of the system has been performed.

Keywords—Silicon Carbide (SiC), Reliability, MOSFETs, IGBTs, Multichip Module, Reliability Engineering.

I. INTRODUCTION

Silicon Carbide (SiC) offers three main potential benefits compared to the currently used silicon (Si) [1], [2]. These benefits are higher efficiency, higher switching frequency and higher temperature of operation [3]. Over the past few years, there has been a special emphasis on SiC Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) [1]. The benefits of using SiC MOSFETs compared with Silicon (Si) Isolated-Gate-Bipolar-Transistors (IGBTs) has been identified in many applications such as aeronautics [4], automotive [5], wind turbine [6] and, soft switching converters [7], [8]. The SiC MOSFET is currently under mass production, mainly due to the fact that it is comparably uncomplicated to replace Si IGBTs with SiC MOSFETs. One of the main reasons for this is that the gate-driver unit of a Si IGBT can easily be modified for use with SiC MOSFETs. Finally, the replacement of Si-IGBT technology with SiC MOSFET technology in the 900 V – 1.7 kV range is beneficial in terms of efficiency. However, if the efficiency is not the main target, a combination of higher switching frequency and higher temperature operation results in smaller passive components and cooling system, respectively. This may result in a higher power density as well as a considerable costs reduction.

However, the SiC technology is fairly new and numerus studies on the reliability of SiC MOSFETs have pointed out several issues arising from imperfections in oxide quality, threshold stability, and body-diode ruggedness (among others) [9]–[12]. With the recently introduced 3rd generation of SiC MOSFETs from Wolspeed, which is the leader on the market, the oxide layer stability and body-diode ruggedness seem to have improved [13]. Manufacturers are also considering new package designs in order to decrease the stray inductances in the package so as to fulfill high switching speed requirements and, therefore, taking full advantage of the SiC properties [14]–[17]. New package concepts are also considered for high-temperature operation. A promising reliability analysis on SiC MOSFET power modules considering parallel
connection as well as gate-voltage dependency has recently been presented in [18].

This study aims at comparing the reliability and the efficiency of a resonant converter topology using SiC instead of Si devices with the reference case using Si IGBTs. Consequently, an identical converter with SiC MOSFETs has also been evaluated. The comparison of these two identical converters will permit to identify how the benefits in efficiency impact the reliability. Furthermore, an analysis on how much the switching frequency can be increased while maintaining the efficiency and the reliability is also presented. Finally, introducing redundancy in the overall system is investigated. The three different topologies are finally compared through a Life Cycle Cost Analysis based on 20 years of lifetime.

II. THE RESONANT CONVERTER

The converter topology investigated in this paper is a full bridge LCC resonant converter as shown in Fig. 1. It is part of an industrial power supply. An illustration of the whole system with one converter unit is shown in Fig. 2.

The electrical parameters of the resonant converter and the devices under investigation are stated in Table I. The devices chosen are both rated 1.2 kV and 300 A and are built with a 62 mm package based on Si technology. The calculations are made based on a case where the load is constant.

<table>
<thead>
<tr>
<th>TABLE I. CONVERTER ELECTRICAL CHARACTERISTICS</th>
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<tr>
<td><strong>Resonant Converter</strong></td>
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<tr>
<td>Power Rating</td>
</tr>
<tr>
<td>Input Voltage</td>
</tr>
<tr>
<td>Output Current</td>
</tr>
<tr>
<td>Switching Frequency</td>
</tr>
<tr>
<td>DC Capacitance 1</td>
</tr>
<tr>
<td>DC Capacitance 2</td>
</tr>
<tr>
<td>Resonant tank Capacitance</td>
</tr>
<tr>
<td>Blanking Time</td>
</tr>
<tr>
<td><strong>Power Semiconductor Devices (1.2 kV, 300 A)</strong></td>
</tr>
<tr>
<td>Si IGBT module</td>
</tr>
<tr>
<td>SiC MOSFET module</td>
</tr>
</tbody>
</table>

The reliability study focuses on the lifetime of the semiconductors as well as the capacitors (dc and resonant). The failure (FIT) rates of the transformer and the inductors are not considered in this study since they are much lower than the other two components and will have negligible impact on the reliability of the system. The resonant tank capacitor lifetime will be unchanged for the Si and the SiC variants providing that the power rating at the load is similar. However, increased losses in the semiconductors for the Si IGBT reference case compared to the SiC MOSFETs case results in higher current in the input dc capacitors, thus higher operation temperatures. Therefore, a slight increase of the FIT rate for the dc capacitors is expected for the Si IGBT case.

Fig. 1: Full bridge converter with resonant tank

Fig. 2: Modern ESP power supplies based on LCC resonant converter
III. SIC MOSFET Module – Fit Rate Calculation

The SiC MOSFET power module investigated in this study is configured as a half bridge. This power module is built with parallel connection of 6 SiC MOSFET chips and, 6 anti-parallel SiC Schottky diodes per switch position, as shown in Fig. 3.

Under the assumption of an exponential distribution, the mean time to failure (MTTF), defined as the inverse of the FIT rate for the SiC MOSFETs and SiC Schottky diodes are given by the manufacturer for a single chip. The failure rates are shown in Table II. For the Si IGBT, the module FIT rate is provided by the manufacturer and is stated in Table III.

Therefore, for the SiC MOSFET, a reliability calculation in order to derive the FIT rate of the power module must be performed. In that case it will be assumed that when one of the chips fails, the module fails entirely. Thus, the calculation consists of a series connection of all the single chips contained in the module. Accordingly, the FIT rate of the module is calculated using

\[
\lambda_{\text{Module}} = \sum_{i=1}^{n} \lambda_{\text{MOSFET}} + \sum_{i=1}^{n} \lambda_{\text{Schottky}} \quad (1)
\]

where \( \lambda_{\text{MOSFET}} \) and \( \lambda_{\text{Schottky}} \) are the FIT rates of a single MOSFET chip and a single Schottky diode chip, respectively. Additionally, \( n \) is the number of chips which is equal to 12 for the SiC power module. The representative diagram of the SiC MOSFET module is shown in Fig. 4. The figure shows the series connection from a reliability perspective, which implies that if one chip fails, the complete power module fails. Table III shows the calculated FIT rate for the SiC MOSFET module and the FIT rate for the Si IGBT as given by the manufacturer. It can be observed that the FIT rate of the SiC MOSFET power module is almost half that of the Si IGBT power module.

IV. Reliability of the Resonant Converter

From the reliability data derived in the previous section, one can estimate the reliability of the resonant converter. In order to limit the scope of the study to the power module comparison, the investigated components are the semiconductor devices in the half-bridge, the dc capacitors \( C_r \) in the dc-link, and the resonant capacitor \( C_s \) (c.f Fig. 2). The dc-link capacitors are composed of the parallel connection of three AVX FFVE6B0666K and two AVX FFLI6B0687KJ. In this study, the FIT rate of the total converter is calculated using (2), as a series connection of all the components from a reliability perspective. Thus, if one single component stops working, the complete system fails. Table IV shows the efficiency and the FIT rates of the full bridge resonant for the reference case and the SiC MOSFETs case. Note that the efficiencies are only considering the semiconductor devices at this stage. Capacitor losses will be added in the final study.

![Fig. 3: SiC MOSFET module – internal configuration](image)

![Fig. 4: Reliability block diagram for the SiC MOSFET module](image)

**TABLE II. FIT RATE OF THE SiC MOSFET CHIP AND THE SiC SCHOTTKY DIODE.**

<table>
<thead>
<tr>
<th>Device (chip)</th>
<th>Failure rate, ( \lambda ) (valid field fail per billion device hour)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET</td>
<td>3.03</td>
</tr>
<tr>
<td>SiC Schottky</td>
<td>0.10</td>
</tr>
</tbody>
</table>

**TABLE III. FIT RATE OF THE SiC MOSFET MODULE (CALCULATED) AND Si IGBT**

<table>
<thead>
<tr>
<th>Device</th>
<th>Failure rate, ( \lambda ) (valid field fail per billion device hour)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFET module</td>
<td>37.56</td>
</tr>
<tr>
<td>Si IGBT module</td>
<td>75</td>
</tr>
</tbody>
</table>
\[ \lambda_{\text{LCC}} = \sum_{p=1}^{n_{\text{module}}} \lambda_{\text{module}} + \sum_{p=1}^{n_{\text{device}}} \lambda_{\text{device, } p} + \sum_{p=1}^{n_{\text{cap}}} \lambda_{\text{cap, } p} + \sum_{p=1}^{n_{\text{res}}} \lambda_{\text{res, } p} \]  

Furthermore, since the SiC MOSFET based converter has lower losses, the heat sink temperature will be reduced. A reduction of system costs can be obtained by either reducing the heat sink size or increasing the switching frequency and therefore, reducing the size of the passive components. If the heat sink size is maintained, the switching frequency can be increased up to 3.3 times (82.5 kHz) in order to have the same efficiency as the reference case. This will enable a considerable reduction in the size of the passive components in the resonant tank and the dc-link. A size reduction of the passive components results in a reduction of the total cost of the converter. Furthermore, in a second step, the overall converter design can be modified in order to reduce its volume. Thus, the space taken by the converter on site will be reduced.

\[ MTTF_S = \frac{3}{2\lambda} \]  

VI. LIFE COST ANALYSIS

In the life cost analysis of this study, three cases are considered. The focus of the comparison concerns only the low-voltage unit of the resonant converter as the main difference between the converters is the switching semiconductor devices. The first one, taken as reference case is the Si IGBT converter currently commercialized. The second case is the SiC MOSFET based converter and, the third a parallel connection of two SiC-based low voltage units. The costs are given in Swedish crowns and stated in Table V. As it can be seen, the reliability for the SiC converter with redundancy is 2.5 times higher than for the reference case. Therefore, the outage costs per year are further reduced for this case. Moreover, the redundancy results in a power loss reduction of 50 % compared with the SiC MOSFET based converter without redundancy which leads to a total savings of a further 4000 SEK per year based on an electricity rate of 0.4 SEK/kWh (Average 2016) [20].

As it can be seen in Table V, the net present sum is lower for both SiC MOSFET based converter. I.e. that the additional investment costs are covered by the energy savings mostly, but also, by the fact that...
the outage costs per year are lower, and the preventive maintenance is done less frequently. The net present value (NPV) for the SiC MOSFET single converter is 32.5 % lower than for the Si IGBT case. The case with redundancy has an almost identical NPV. This is mainly due to the large investment cost and the relatively short duration of the economic lifetime of this product. However, considering the noticeable reliability improvements, increasing the economic lifetime of the product would be the natural step forward.

<table>
<thead>
<tr>
<th>Converter</th>
<th>Si IGBT</th>
<th>SiC MOSFET</th>
<th>SiC MOSFET redundancy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Investment Costs</td>
<td>30 000 SEK</td>
<td>45 000 SEK</td>
<td>2 x 45 000 SEK</td>
</tr>
<tr>
<td>Loss / year</td>
<td>12 MW</td>
<td>4 MW</td>
<td>2 MW</td>
</tr>
<tr>
<td>Electricity Costs – due to losses</td>
<td>4800 SEK</td>
<td>1600 SEK</td>
<td>800 SEK</td>
</tr>
<tr>
<td>Outage Costs / year</td>
<td>Negligible</td>
<td>Negligible</td>
<td>Negligible</td>
</tr>
<tr>
<td>Preventive Maintenance</td>
<td>5 years</td>
<td>10 years</td>
<td>10 years</td>
</tr>
<tr>
<td>Costs / maintenance (estimation)</td>
<td>5000 SEK</td>
<td>5000 SEK</td>
<td>5000 SEK</td>
</tr>
<tr>
<td>Interest Rate</td>
<td>5 %</td>
<td>5 %</td>
<td>5 %</td>
</tr>
<tr>
<td>Economic Lifetime</td>
<td>20 years</td>
<td>20 years</td>
<td>20 years</td>
</tr>
<tr>
<td>Net Present Sum</td>
<td>105 895 SEK</td>
<td>71 494 SEK</td>
<td>105 725 SEK</td>
</tr>
</tbody>
</table>

In this application, the redundancy is attractive in terms of power loss. Both single and redundant converters result in a lower net present sum calculated over 20 years. However, the case without redundancy is economically more attractive due to the consequent savings brought by this solution. Finally, the next step towards the integration of SiC devices into converter designs made previously with Si is the reduction of the system passives by increasing the switching frequency. The power density can be further increased by allowing a higher temperature of operation. In this way, the benefits of SiC can be fully used and SiC will become even more economically interesting.

VII. CONCLUSION

In this paper, a reliability and efficiency analysis has been presented when introducing SiC MOSFETs in order to replace the Si IGBTs. The reliability of an identical single system was improved by 1.6 times and the efficiency by a factor of 3. Moreover, including redundancy in the system can further improve the reliability and lower the losses. The reliability is 2.5 times better than the reference case and the losses are 6 times lower. Furthermore, a life cycle cost analysis is performed, revealing that replacing Si IGBTs by SiC is economically interesting since the investment costs can be fully covered by the reduction of losses over the economic lifetime of the product. Finally, introducing redundancy will only be interesting if the converter expected lifetime is increased. This can clearly be considered in accordance to the improvement of the reliability.

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