Transient Behaviour of VSC-HVDC Links with DC Breakers Under Faults

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Keywords

≪HVDC≫, ≪Power transmission≫, ≪Multilevel converters≫, ≪Voltage Source Converter (VSC)≫, ≪Fault handling strategy≫

Abstract

In future high-voltage direct current (HVDC) systems, a large number of HVDC breakers will be required. In this paper, the influence of HVDC breakers on the transient performance of point-to-point HVDC links in both asymmetrical and symmetrical monopolar configuration with half-bridge modular multilevel converters is studied with simulations in PSCAD. As HVDC breakers, the active resonant breaker and ABB's hybrid breaker are considered. The analyzed scenarios include DC line faults, DC bus faults, and AC faults between the converter and the transformer. The highest DC breaking capability is required during DC line faults in the asymmetric and symmetric monopole. The converter stress is highest for DC bus faults and unbalanced converter AC faults in the asymmetric monopole and for DC bus pole-to-pole faults in the symmetric monopole. During DC pole-to-ground faults in the symmetric monopole, the HVDC breaker combined with DC side arrestors yields the lowest overvoltage stress on the cable of the healthy pole. The fault current shapes depend strongly on the interaction of the converter and the travelling waves on the lines, and differ from the fault current shapes in typical HVDC breaker test circuits. Furthermore, the active resonant breaker and the ABB hybrid breaker perform similarly in the used benchmarks due to the very fast DC line fault detection.

Introduction

Many high-voltage direct current (HVDC) links have been commissioned around the world. Due to the demand for renewable energy resources more HVDC links and HVDC grids will be built in the future. Most of the HVDC systems today are point-to-point links. Tapped HVDC links with line commutated converters (LCC) have also been realized. In the link between Sardinia to Italy's mainland, only a small tap is needed to supply Corsica [1]. The Quebec-New England link was the first multiterminal project with large power involved and initially five terminals in operation (two have been shut down). The North-East Agra project in India is under construction and will run at 800 kV. Two rectifier stations 432 km apart from each other operate in parallel and transmit power to two inverters in parallel in the Agra region [2]. Voltage source converters (VSC) offer advantages over LCCs such as flexible reactive power support for AC grids, connection to weak AC grids and black start capability. An example for this is the Caprivi link with overhead lines and DC circuit breakers (DCCB) [3]. As the number of HVDC

links increases it will become economical to form grids. It is expected that most of these grids will use VSCs [4]. Two radial VSC-HVDC grids already exist in China with the three-terminal 160 kV Nan'Ao grid and the five-terminal 200 kV Zhoushan grid [2]. Before meshed grids are formed, many studies have to be carried out, since the system protection is more demanding for DC than for AC. DCCBs are required if non-fault-blocking converters are used and selective protection is required. Furthermore, HVDC grid stability issues are not known from operation. Thus, intense research is carried out at the time of writing, especially on the European supergrid.

In conventional VSC-HVDC point-to-point links with non-fault-blocking converters, DC faults are handled by blocking the converters and opening the AC circuit breakers. However, opening the AC circuit breakers takes three to four AC cycles [5], which puts tremendous stress on the converters. Moreover, the converters cannot provide reactive power support to the AC grid during and after the fault. In meshed HVDC grids, this strategy is inappropriate, because the whole grid would have to be shut down. In overhead line systems, temporary faults may occur frequently and operating the AC circuit breakers each time would lead to unacceptable system downtimes. If non-fault-blocking converters are used in such systems, it is expected that a DCCB will be placed at each line end. Even if cables are used in point-to-point links, DCCBs may be advantageous, because after fast separation of DC line faults, the converters can provide reactive power to the AC grids again. In case of DC bus or converter AC faults, operating the DCCBs would limit the infeed from the other converter. Thus, DCCBs will have a significant influence on the transient performance of future HVDC systems.

The demands on DCCBs are much higher compared to the AC counterparts and they are expected to be opened a few ms after tripping. Several DCCB concepts for HVDC have been proposed [6–11]. These can be grouped into mechanical switches with current injection and hybrid breakers. Mechanical switches with current injection use pre-charged capacitors or a small converter in an LC circuit to inject a current into the arcing mechanical switch to create a zero crossing. Hybrid breakers combine disconnectors and power electronics to interrupt the current. A current limiting inductor may be connected in series with the DCCB to limit the rate of rise of the fault current.

The stability of HVDC grids was studied in detail in [12]. The influence of the current limiting inductor of the DCCB on grid stability was studied in [13]. Both papers conclude that small-signal instability could occur. Apart from this, DCCBs will not influence normal operation. Thus, the analysis of DCCBs needs to focus on transient scenarios: system start, faults, and switching operation.

In this paper, the transient performance of a point-to-point VSC-HVDC link in both asymmetric and symmetric monopolar configuration with a DCCB at each line end under faults is analyzed. The following scenarios are considered: DC line faults, DC bus faults, and converter AC faults. The paper is structured as follows: In the section *Modelling and Simulation Setup*, the benchmark systems are introduced, the transient behaviour of the converters and DCCBs is described, and the protection system is explained. In the section *Results & Discussion*, simulation results are shown and explained. All findings are summarized in the *Conclusion* section.

Modelling and Simulation Setup

The asymmetric monopole is shown in Fig. 1. The converters are connected with a 500 km overhead line and a ground return. The rated DC pole-to-ground voltage equals the rated converter DC pole-to-pole voltage U_{DC}. The symmetric monopole is shown in Fig. 2. The converters are connected with 200 km cables between the respective converter poles. The rated DC pole-to-ground voltage is $\pm U_{\mathrm{DC}}/2$. The cables and overhead lines are modelled with PSCAD components, which consider the actual line geometry and the line's distributed parameters. The AC grids are modelled as three-phase voltage source u_{AC} with the RMS voltage U_{AC} each in series with the grid inductance L_{AC} and the grid resistance R_{AC}. The transformer turns ratio is set to one. Furthermore, arrestors rated for 1,40625 times the respective DC pole-to-ground voltage are placed between the poles and ground to protect the system against overvoltages. All parameters are summarized in Tab. I.

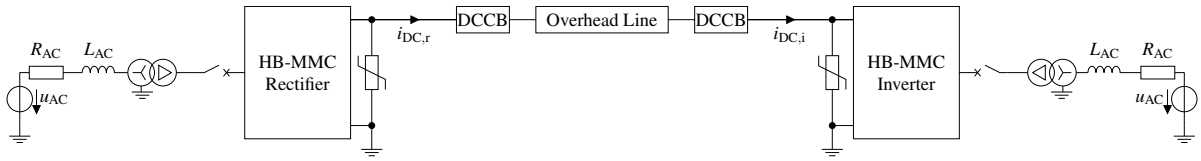


Fig. 1: Asymmetric monopole HVDC link with overhead lines, HB-MMCs, and DCCBs

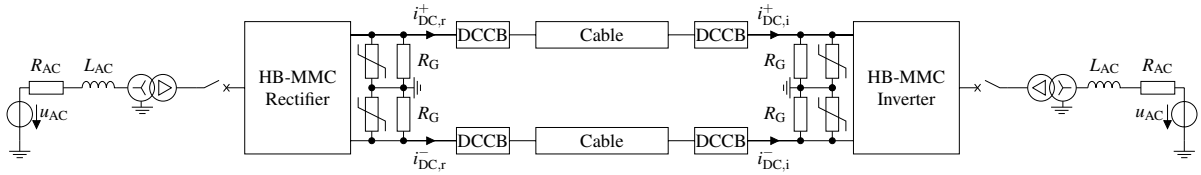


Fig. 2: Symmetric monopole HVDC link with cable connections, HB-MMCs, and DCCBs

Faults

The analyzed faults include DC line faults, DC bus faults, and converter AC faults. In the asymmetric monopole, the DC faults are pole-to-ground faults, whereas for symmetric monopoles pole-to-pole faults are possible as well, and are considered more severe, although their probability is very low in cable systems. DC line faults are considered to be faults on the line at the fault distance l. DC line terminal faults are considered to be faults at a line end. DC bus faults are considered to be faults on the connection between the converter and the DCCB. All possible internal AC faults in the HVDC station between the converter and the transformer have been simulated (single-phase-to-ground, phase-to-phase, three-phase faults and the last two with ground connections). These are referred to as converter AC faults and only critical cases are commented on in this paper.

To identify the worst-cases, each fault is simulated and the fault inception is varied within an AC period. Faults in the AC networks are not considered, because VSCs can ride through faults. Studies on the impact of the fault resistance have also been performed, but are not shown here. Generally, fault currents decrease with increasing fault resistance which eases interruption, but makes fault detection more challenging. In this paper, i_{DC} denotes the DC line current, and i_{arm} the arm current of the converter with the highest absolute peak value. An additional subscript r stands for rectifier, and i for inverter. For the symmetric monopole, the superscript $+$ stands for positive DC pole, and $-$ for negative DC pole.

HB-MMC

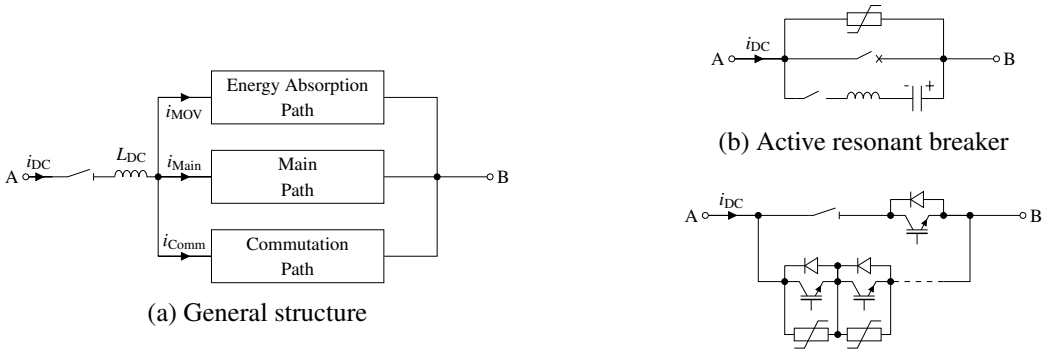
As converters, modular multilevel converters (MMC) with half-bridge (HB) submodules are used and modelled using the continuous model from [14], characterized by the arm inductance L_{arm}, the equivalent arm capacitance C_{arm}, and the arm resistance R_{arm}. The rectifier controls the transmitted power to 700 MW and the inverter is in DC voltage droop control. A bypass thyristor or an anti-parallel diode with high surge current capability is placed in parallel to the lower IGBT in an HB submodule to protect the submodule if the converter is blocked.

The fault behaviour of the HB-MMC depends on the fault type. For DC pole-to-ground faults in an asymmetric monopole and DC pole-to-pole faults in a symmetric monopole, the behaviour is similar. First, the submodule capacitors of the inserted submodules discharge into the fault until the converter is blocked. Then, the HB-MMC is in uncontrolled rectifier mode and the AC grid feeds the fault. The DC line current increases steeply until it stays at relatively high current values. For DC pole-to-ground faults in a symmetric monopole, the voltage of the faulty pole collapses and the voltage of the healthy pole increases, because the HB-MMC keeps the DC pole-to-pole voltage essentially constant. The DC arrestor at the healthy pole limits the voltage increase. The DC line current of the faulty pole decreases again after this phase. During a converter AC fault, the submodules in the faulty phases contribute to the fault current as long as the HB-MMC is not blocked. In case of an unsymmetrical converter AC fault, the voltages of the healthy phases rise, leading to uncontrolled rectifier mode of the lower arm submodules in

an asymmetric monopole and of all submodules in a symmetric monopole when the converter is blocked.

DCCB

All DCCBs for HVDC may be represented by the general circuit shown in Fig. 3a. The current limiting inductor L_{DC} limits the $\mathrm{d}i/\mathrm{d}t$ of the DC line current in a fault case and is considered to be part of the DCCB. Under normal operating conditions, only the main path is conducting. When the DCCB is tripped, the current is commutated into the commutation path. How this commutation process is realized, depends on the DCCB concept. It shall also be mentioned that many hybrid breaker concepts are able to trip *proactively*. This means that the current is commutated to the commutation path before the DCCB is tripped by the protection system due to an internal DCCB protection mechanism. Proactive tripping can speed up the interruption, because it can compensate for fault detection and communication delays. After some time, the current is commutated into the energy absorption path. Here, the system energy is dissipated. Most concepts use a metal-oxide varistor (MOV) in this path. When the MOV starts to conduct, it inserts a voltage which increases beyond the system voltage and drives the fault current very close to zero. The line disconnector is necessary to interrupt the residual current which flows, but opens as slowly as the AC breakers. From a system perspective, the internal functioning of a DCCB is of minor importance [15]. For the system, mainly the timing of the commutation processes and the characteristics of the inserted components matter. The most influential ones are the current limiting inductor, the MOV and LC circuits if used. Active resonant breakers with a pre-charged capacitor (see Fig. 3b) and ABB's hybrid breaker (see Fig. 3c) are used in the simulations. The DCCBs are modelled as described in [15]. For the active resonant breaker, the MOV voltage is set to 1.5 times the respective DC pole-to-ground voltage. For the ABB hybrid breaker, this voltage is kept at 120 kV per stack, but the number of stacks is set to four for the symmetric and eight for the asymmetric monopole.



(a) General structure

(b) Active resonant breaker

(c) ABB hybrid breaker

Fig. 3: Examples for DCCBs for HVDC

Protection Method

The method for DC line fault detection in this study is a simplified version of the one proposed in [16]: The instantaneous local current is compared to a moving average over the local current using 20 samples at 2 kHz. If the absolute difference between instantaneous local current and its moving average exceeds a threshold, a DC line fault is detected. Additionally, an under- and overvoltage criterion is implemented for DC line fault detection. Once a DC line fault is detected on a pole, the local DCCB is tripped.

The method for DC bus fault detection for the symmetric monopole uses the sum of all DC bus currents and compares its absolute value to a threshold. If the threshold is exceeded, the adjacent DCCBs and the AC breakers of the adjacent HB-MMC are tripped.

The method for detection of the converter AC faults with ground connection uses the sum of the converter AC currents and compares its absolute value to a small threshold. This is possible because the sum of currents should always be zero in abscence of faults due to the delta connection of the transformer. To detect phase-to-phase faults without ground connection, the d-component of the converter's AC currents

is compared to its setpoint. Large deviations are interpreted as fault. Once a converter AC fault is detected, the AC breakers are tripped and the converter is blocked.

The converters are blocked if an arm current exceeds a blocking threshold or if a converter AC fault is detected. The converters are deblocked if the arm current falls below a deblocking threshold after a time delay to avoid premature deblocking. In a symmetric monopole, tripping of a DCCB also initiates tripping of the DCCB on the other pole. If a DC line fault is separated, the HB-MMCs are deblocked once the arm current falls below its deblocking threshold and their active power references are set to zero. For the inverter, the DC voltage droop is disabled as well. If a DC bus fault or a converter AC fault is detected, the same actions are executed as previously mentioned. All these measures ensure that a deblocked HB-MMC provides reactive power to the AC grid again.

Table I: System parameters (for L_{DC}, first value for asymmetric and second for symmetric monopole)

$U_{\mathrm{AC}}/\mathrm{kV}$	$U_{\mathrm{DC}}/\mathrm{kV}$	$L_{\mathrm{AC}}/\mathrm{mH}$	R_{AC}/Ω	R_{arm}/Ω	$L_{\mathrm{arm}}/\mathrm{mH}$	$C_{\mathrm{arm}}/\mu\mathrm{F}$	$R_{\mathrm{G}}/\mathrm{M}\Omega$	$L_{\mathrm{DC}}/\mathrm{mH}$
380	640	28.25	0.885	0.885	84.8	29.3	10	5/2.5

Results & Discussion

Asymmetric Monopole

The simulation results for the asymmetric monopole HVDC link are shown in Fig. 4. First, a DC line terminal fault towards the rectifier is considered. In Fig. 4a, the rectifier DC line current is depicted during the fault. The simulation was carried out with the ABB breaker, the active resonant breaker, and without DCCB. The DC line current rises steeply until the converter is blocked and reaches a plateau. After some delay, the DC line current rises again due to the AC grid infeed until the MOV is inserted. As visible, the curves for both DCCBs are similar and the interruption time is almost the same. This seems surprising since the ABB breaker features proactive tripping. However, the used DC line protection is very fast and trips the DCCB before the ABB breaker trips proactively. The DC line current rises slightly higher for the active resonant breaker, because after current injection the capacitor is charged from the line until the MOV starts to conduct. This time increases with capacitor size and can only be minimized by dimensioning the LC circuit as small as possible while respecting the $\mathrm{d}i/\mathrm{d}t$ limitation of the mechanical switch. Due to the higher peak current, the MOV inserts a higher voltage if the MOVs have the same rating for both DCCBs. This drives the DC line current faster to zero for the active resonant breaker yielding similar interruption time. Note that the current injection frequency of a few kHz for the active resonant breaker requires a relatively small simulation time step. Therefore, the ABB breaker has been used in the remaining simulations. Without DCCB, the DC line current is not decreased by the system, stays at relatively high current values, and changes in an oscillatory fashion. In Fig. 4b, the corresponding results for the rectifier arm current with the highest peak current are shown. Without DCCB, the converter is heavily stressed by the fault current. The bypass thyristors or anti-parallel diodes in the blocked converter are thus stressed until the AC breakers have opened. If a DCCB is used, the peak arm current can be limited to a fraction of the corresponding value without DCCB. Furthermore, the conduction time of the bypass thyristors or anti-parallel diodes can be reduced to a few ms.

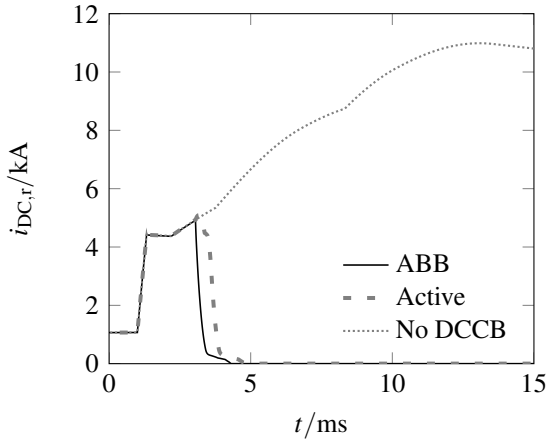
Fig. 4c illustrates the dependence of the peak rectifier arm current and DC line current on the fault distance, which has been varied across the whole line length. Both currents decrease with increasing fault distance, because the inductance of the overhead line increases with fault distance and limits the fault current. However, the peak rectifier DC line current does not increase monotonously. The reason for this is the interaction of travelling waves and the converter which depends on the fault distance. In contrast to the peak DC line current, the peak arm current depends strongly on the time of fault inception within an AC cycle. The worst-case corresponds to the time when one of the arm currents is at its positive peak. From $l = 250\,\mathrm{km}$, the peak currents become much smaller and the rapid change in the curve shape appears strange at first, but this is unrelated to the fact that this is at the middle of the line. The rectifier DC

line current is independent of the line segment towards the inverter during a solid ground fault and thus this phenomenon would occur for every line longer than 250 km at the same fault distance. To explain this phenomenon, the rectifier DC line current is shown as a function of time for selected fault distances in Fig. 4d. With increasing fault distance the DC line current increases later because the travelling wave coming from the fault point first has to reach the line terminal. For $l = 50$ km, the travelling waves cause the triangular-like current ripple. When the converter is blocked, the DC line current peaks and oscillates until the MOV is inserted. For $l = 250$ km, the DC line current reaches a plateau which is also visible as initial peak for $l = 50$ km at a similar current level. The travelling wave has to travel from the converter to the fault and back to the converter before the current increases again. For $l = 250$ km, this process takes approx. 1.7 ms which is almost the opening time of the disconnector in the main path. Hence, the MOV is inserted before the second plateau is reached, which is in total the reason for the step visible in Fig. 4c. If the opening time of the disconnector is varied, the step occurs at a different fault distance. Another reason for the different curve shape is that with increasing fault distance the converter is not blocked. Due to this, the submodule capacitors contribute to the fault current although the MOV is already conducting which leads to comparably long interruption times and considerable stress for the MOV. By blocking the converter temporarily the interruption times could be reduced. However, whether this is allowed depends on the grid code and the rules on reactive power support. In any case, long stressing of the MOV has to be considered in HVDC breaker testing as well.

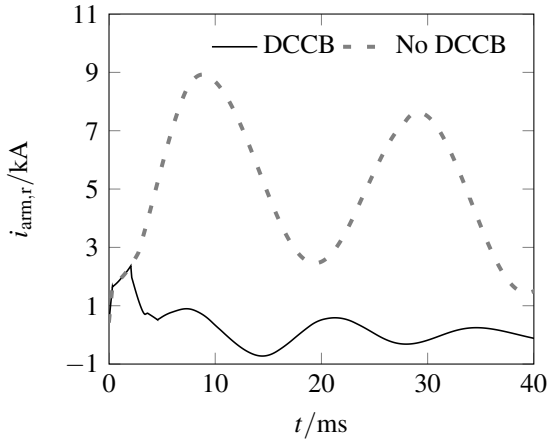
To obtain the peak current stresses, simulations have been run for all cases described in the *Faults* section. It has been observed that phase-to-phase and three-phase faults without ground connection led to less severe stress than with ground connection and thus only the latter are considered in the results presentation. The findings are summarized in Table II. If two values are given, the first value corresponds to a fault at the rectifier and the second to a fault at the inverter. DC line terminal faults at the rectifier led to the largest DC line current. In general, DC faults adjacent to the rectifier are more severe, because the DC line current has to reverse on the inverter side. DC bus faults and unbalanced converter AC faults are the most severe faults for the HB-MMC and DCCBs cannot limit the converter stress in these fault cases. For the DCCBs, DC bus faults and converter AC faults are no challenge as the DC line current decreases directly which is why the peak values are almost identical. The maximum arm currents are in the same order of magnitude for these faults. In a DC bus fault case, very large AC fault current infeed through the bypass thyristor or anti-parallel diodes of the lower IGBT stresses the converter and only the arm inductances and the transformer limit the current. Interestingly, the peak DC line current during a DC bus fault at the inverter is larger at the DCCB adjacent to the rectifier and vice versa. This is caused by the travelling wave which travels across the whole line and causes the converter to react to the fault. Phase-to-phase converter AC faults with ground connection can be understood as follows. After the fault, the voltage on the healthy phase increases. When the submodules are blocked, no current can flow between the AC and DC side through the upper arm submodules, because the total arm voltage approximately equals the DC pole-to-ground voltage. Due to the ungrounded converter side of the transformer, the fault current infeed from the AC grid into the faulty phases equals the phase current of the healthy phase. Since this current cannot pass through the upper arm submodules, it has to come through the lower arm submodules bypass thyristors from ground. The mechanism is similar for single-phase faults, only that the fault current is divided between the lower arms of the two healthy phases. From a design perspective, the only possibility is to minimize the propability of such faults.

Table II: Maximum DC line current and converter arm current during faults for asymmetric monopole (in case two values are given, first for rectifier and second for inverter side fault)

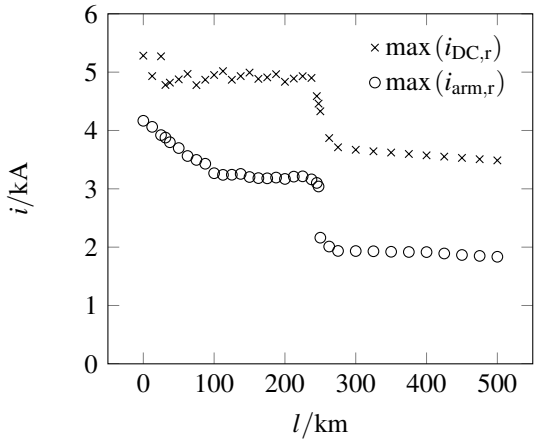
Fault Type	DC Line	DC Bus	AC 1-Phase GND	AC 2-Phase GND	AC 3-Phase GND
$i_{\mathrm{DC}}/\mathrm{kA}$	5.283	1.336/3.403	1.073/1.391	1.073/1.491	1.073/1.505
$i_{\mathrm{arm}}/\mathrm{kA}$	4.166	9.054/9.23	9.94/9.94	9.786/9.73	1.149/1.378



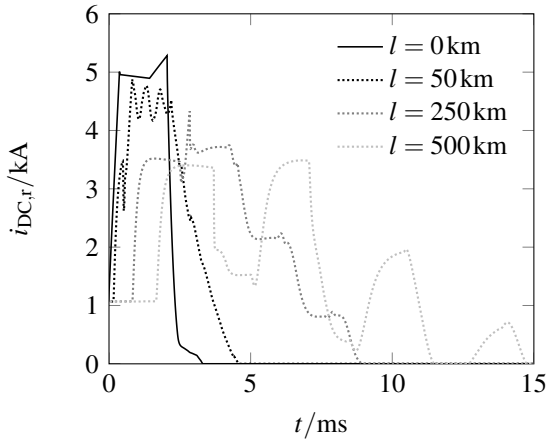
(a) Rectifier DC line current during DC line terminal fault



(b) Rectifier arm current during DC line terminal fault



(c) Maximum rectifier DC line and arm current during DC line fault as function of fault distance



(d) Rectifier DC line current during DC line fault as function of time for different fault distances

Fig. 4: Results for asymmetric monopole HVDC link with overhead line, HB-MMCs and DCCBs

Symmetric Monopole

The simulation results for the symmetric monopole HVDC link are shown in Fig. 5. In Fig. 5a, the peak rectifier DC line current of the positive pole is depicted for DC line pole-to-ground and DC line pole-to-pole faults as function of the fault distance. In contrast to the asymmetrical monopole with overhead lines, the curves depend weakly on distance. This is mainly due to the slower wave propagation on cables and the small inductance of cables. The results also show that the highest peak DC line current during a DC line pole-to-pole fault flows for a fault on the cable and not for a terminal fault as already discussed in [17]. As expected, DC line pole-to-pole faults lead to larger peak currents than DC line pole-to-ground faults. For the worst-case DC line pole-to-pole faults, the rectifier was blocked on average for 4.5 ms for all fault distances and the rectifier was blocked for every fault distance.

In Fig. 5b, the DC pole-to-ground voltage $u^{-}_{\mathrm{cable,r}}$ at the cable terminal of the negative pole towards the rectifier is depicted during a DC line pole-to-ground fault at $l = 0\,\mathrm{km}$ on the positive pole. Three cases are considered: no protection at all, DC side arrestors from pole-to-ground, and DC side arrestors from pole-to-ground with DCCBs. Both protection measures reduce the overvoltage on the cable significantly and the system with DCCBs yields the lowest overvoltages.

In Fig, 5c, the positive rectifier pole DC pole-to-ground voltage $u^{+}_{\mathrm{DC,r}}$ at the converter terminal and the

DC line current are shown during a DC line pole-to-pole fault at $l = 62.5\,\mathrm{km}$, which corresponds to the worst-case in Fig. 5a. After the voltage wave coming from the fault reaches the converter terminal, the DC line voltage drops to a negative value and the converter starts feeding the fault. The DC line current increases steeply until the converter is blocked and enters the uncontrolled rectifier mode. The DC line voltage and the DC line current are formed by an interaction of the converter and the voltage wave which reflects at the fault and travels back. Each time the voltage wave reaches the converter terminal, the DC line voltage decreases again. Current is fed from the AC side through the submodules depending on the instantaneous AC voltages at the AC terminals of the converter and the DC line voltage. This happens even when the MOV of the DCCB is already conducting and can be seen at $t = 2.6\,\mathrm{ms}$.

In Fig, 5d, an arm current of the rectifier and of the inverter during a DC bus pole-to-pole fault at the rectifier are depicted. The arm current of the rectifier oscillates around a large, slowly decaying DC offset, which puts tremendous stress on the submodules until the AC breakers are opened. Note that the rectifier arm current is similar in an asymmetric monopole during a DC bus fault at the rectifier. Due to the opening of the DCCBs, the inverter does not feed the fault and the arm currents are limited. In the simulations, the maximum peak arm current of the inverter would have been 151.2 % larger for operation without DCCBs compared to operation with DCCBs. This figure would be even worse for a DC bus pole-to-pole fault at the inverter for the rectifier submodules, because the rectifier DC line current would not reverse.

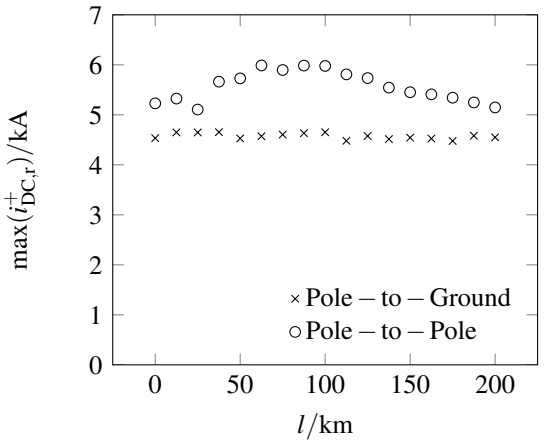
As for the asymmetric monopole, the values for the peak current stress for the symmetric monopole are given in Tab. III. The worst-case DC line pole-to-ground faults correspond to the peak in Fig. 5a. This peak lies below the values for DC line pole-to-pole faults, and is therefore not repeated. DC bus pole-to-pole faults do not require high DCCB current breaking capability, but yield high stress because the cable discharges through the DCCB into the fault. For the symmetric monopole, DC bus pole-to-pole faults are the worst-case fault as seen in Fig. 5d. The converter AC faults are not a serious stress for the symmetric monopole. As for the asymmetric monopole, converter AC faults with ground connection yielded higher fault currents than without ground connection. In contrast to the asymmetric monopole, the unbalanced converter AC faults are not dangerous for the submodules either. As the voltage on the healthy AC lines rises, it exceeds the DC pole-to-ground voltage at the converter terminals depending on the time in the AC cycle. The converter is blocked, and thus current flows through the submodules in uncontrolled rectifier mode. Due to the DC arrestors, the DC pole-to-ground voltages will not increase significantly and the current infeed from the AC system is limited. For the single-phase converter AC fault, the corresponding values are higher than for the phase-to-phase converter AC fault with ground connection, because the voltage on the healthy lines increases more if only one AC phase is grounded.

Table III: Maximum DC line current and converter arm current during faults for symmetric monopole (in case two values are given, first for rectifier and second for inverter side fault)

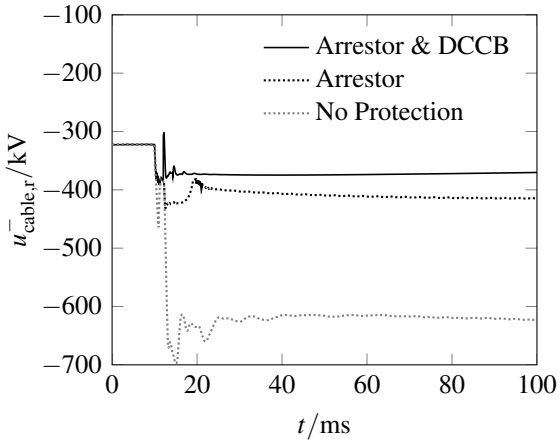
Fault Type	DC Line	DC Bus	AC 1-Phase GND	AC 2-Phase GND	AC 3-Phase GND
$i_{\mathrm{DC}}/\mathrm{kA}$	5.987	7.265/9.334	2.105/1.309	1.962/1.286	1.085/1.241
$i_{\mathrm{arm}}/\mathrm{kA}$	4.287	9.043/8.603	2.343/1.304	2.101/1.297	1.129/1.385

Conclusion

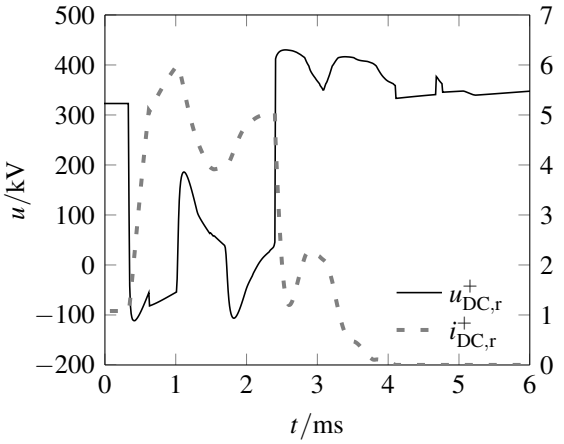
The transient behaviour of HVDC links with HB-MMCs and DCCBs in asymmetrical and symmetrical monopolar configuration under faults was analyzed in this paper. DCCBs reduce the stress on the converter during a DC line fault tremendously. The worst-case faults in terms of converter stress for the asymmetrical monopole were found to be DC bus faults and unsymmetrical converter AC faults. The worst-case faults in terms of converter stress for the symmetrical monopole were found to be DC pole-to-pole bus faults. DC side arrestors combined with DCCBs provide the best DC overvoltage protection during DC pole-to-ground faults in the symmetrical monopole. Travelling waves and the interaction with the converter have a major influence on the fault currents. This has to be analyzed thoroughly for every



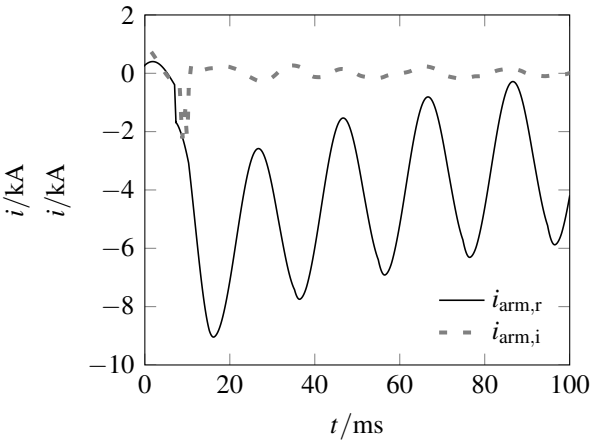
(a) Maximum rectifier DC line current during DC line faults as function of fault distance



(b) Cable voltage of negative pole during a DC line pole-to-ground fault on the positive pole cable terminal towards inverter



(c) Positive rectifier pole DC voltage and DC line current during DC line pole-to-pole fault at $l = 62.5\,\mathrm{km}$



(d) Rectifier and inverter arm current during DC bus pole-to-pole fault

Fig. 5: Simulation results for symmetrical monopole HVDC link with cables, HB-MMCs and DCCBs

HVDC project considering the actual geometry of the used overhead lines or cables, and the converter control in the design phase to get optimal system performance.

The simulated DC line fault current shapes differ from the conventional triangular shape which has been used in most published DCCB tests. These tests may be representative for HVDC grids, but for point-to-point links with small DC inductors and without large DC pole capacitors the relations are completely different. Furthermore, travelling waves and possibly unblocked converters lead to relatively long conducton times of the MOV. Thus, appropriate test circuits are needed which consider all of these findings.

Another finding is that the performance of the active resonant breaker and ABB's breaker are similar in the analyzed benchmarks. This is due to the very fast DC line fault detection used in this work, which detects the DC line fault before the proactive tripping mode in the ABB breaker is activated. Proactive tripping will be advantageous in the above-mentioned benchmarks, if the DC line fault detection is slower or if the communication delay is increased. In future work, different DC line fault detection methods should be compared with simulations and their robustness should be tested in other transient scenarios such as reference power steps. Furthermore, it has to be evaluated whether proactive tripping may be needed in HVDC grids to allow for selectivity or in HVDC point-to-point links with ratings different from the ones used in this work.

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