Electrical Performance of Directly Attached SiC Power MOSFET Bare Dies in a Half-Bridge Configuration

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Abstract—The demand for high-efficiency power converters is increasing continuously. The switching losses are typically significant in power converters. During the switching time, the component is exposed to a considerable voltage and current causing power loss. The switching time is limited by parasitic inductance produced by traces and interconnections inside and outside the package of a device. Moreover, the parasitic inductances at the input-terminal together with the Miller capacitance generate oscillations causing instability and additional losses. In order to eliminate the package parasitic inductance, four 1.2kV SiC-MOSFET bare dies, two in parallel in each position, were directly attached to a PCB sandwich designed as a half bridge. The obtained structure forms a planar power module. From ANSYS Q3D simulations it was found that the parasitic inductance between drain and source for each transistor in the proposed planar module could be reduced 92 % compared to a TO247 package. The planar module was also tested as a dc-dc converter. Switching waveforms from these experiments are also presented.

Keywords—SiC MOSTEF, bare die, low inductive circuit, fast switching, parasitic inductance, converter, planar Module.

I. INTRODUCTION

The most critical instant in all types of converters is the switching time when the instantaneous power developed in the switches reaches its highest level. Decreasing the switching time has always been preferred when designing power electronics. Fast switching decreases the switching losses and makes it possible to increase the switching frequency. This enables the use of smaller passive components, which results in high-density circuits and lower losses [1]. However, forcing the switching time to the limits leads to undesirable behaviors like oscillations in current, overshoots, EMI, and oscillations in control voltage, which may turn the device on and off during parts of the time. This will consequently increase the losses even more and degrades the component, and decreases its life time due to increased temperatures [2][3]. The parasitic inductances and capacitances produced by the device itself, the device package, and the external circuit, as seen in Fig. 1, are the reasons for the finite switching time and the oscillations. In general, different methods have been developed to reduce the package inductance in electronic devices. As examples, Chip-on-Board, System-in-Chip, FlipChip, DirectFET and press-

pack technology particularly for higher power applications can be mentioned. However, the most fast switching technologies are developed for data transition systems or low-power converters and the switches used in high power applications are still much slower than for many other applications.

Generally, wide band gap (WBG) devices are employed in high-power converters. The packaging is one of the main hurdles that WBG power devices have to overcome in order to gain wide acceptance in the power electronics industry. The problems with conventional packages are: large parasitic inductance, mediocre thermal properties, need for thermal grease to mount them on heatsinks, and the limited reliability of soldering/sintering joints in the package.

Fig. 1: Model of power MOSFET including the parasitic elements.

Considering Silicon carbide (SiC) MOSFETs, the interconnections and leads in a package of the device may create inductance up to 10 nH at each terminal (Gate-Drain-Source) which together with the loop inductance of the circuit board results in a considerable inductance limiting the rise- and fall times more than necessary. The impact of the different parasitic

inductances for MOSFETs was derived earlier in [4] and the inductance of wire bonds and leads was studied in [1]. By creating a planar power module using SiC-MOSFET bare dies, and excluding the conventional package, it was assumed that the parasitic inductances could be reduced significantly. Simply, by attaching the bare dies directly to a PCB configured as a half-bridge the inductance of the package could be eliminated. It was found that by this technique, not only the package inductance can be eliminated but also due to the smaller die pads, the loop inductance can be reduced compared to a regular design. Moreover, the direct attached planar module offers possibility for double-sided cooling and/or press-mounting, which will significantly improve the thermal performance and reliability of the module. The present work should be regarded as a first attempt to realize such a planar half-bridge module. In this first attempt several issues regarding thermal and dielectric issues have been disregarded for the sake of a simple demonstration of the idea. Some design problems remain unsolved. These problems include material choices for the thermal paths and associated thermo-mechanical design issues, choices of assembly technology, choices regarding electric passivations, and sealing against moisture. The paper is organized as follows. In Section II the design of the planar module is described along with numerical calculations of its parasitic inductances. In Section III and IV simulation and experimental results from a first generation prototype of the planar module are presented, and in Section V conclusions are drawn.

II. DESIGN

A half-bridge design with two MOSFETs in parallel in both the high and low positions was proposed as seen in Fig. 2. The MOSFETs used were Cree's 1200 V, 98 A, 25 m Ω with a die size shown in Fig. 3.

Fig. 2: The Half-bridge configuration with two SiC MOSFETs in parallel in each position.

The dies were placed between two PCBs to create connections between the two sides of the dies as shown in Fig. 5 and the layout of the upper PCB is shown in Fig. 4. As it can be seen in this figure, the distance between source and gate traces are dictated by the distance of the pads which in this case is about 80 μm resulting in extremely small loop inductance. The parasitic elements of the structure were analyzed using ANSYS Q3D. The results from this analysis confirm that the

parasitic inductances of the structure are very low compared to a circuit using packaged devices.

Fig. 3: The layout of the bare die (right) and the planar module (left).

Fig. 4: Layout of the upper PCB(2).

Fig. 5: Sketch of the cross section of the planar module.

Due to the encouraging results from the analysis of parasitic elements it was decided to build a first generation of the planar half-bridge module following the design outlined in Fig. 5. The bare dies were connected to the PCBs through a soldering process. The choice of using standard PCBs for the structure was made to simplify manufacturing and to save time. For the final design it is likely that ceramic substrates are used instead. The PCBs forming the planar module were attached to a larger PCB for the main circuit of a step-down converter. The gate drivers were also placed on this PCB as close as possible to the planar module in order to minimize the gate-loop inductance.

The source inductances are less than 700 pH, which should enable fast switching. This will be verified by simulations and

experiments and discussed in the coming sections. Also the other parasitic inductances are significantly reduced compared to conventional designs, see Table I where the inductance and resistance of traces are shown. Diagonal components in the table show the inductances of each trace connected to the pads of the transistors and the other components are the mutual inductances which are negligible.

TABLE I: Results of parasitic inductance in [nH] and resistances in [$\mu\Omega$] of PCB traces from ANSYS Q3D. The diagonal components in the table shows the main inductance of each traced connected to the pads and the remaining are the mutual inductances between traces.

Inductance Matrix													
	FET_1_G	FET_2_G	FET_3_G	FET_4_G	FET_3_S	FET_4_S	FET_1_S	FET_2_S	FET_3_D	FET_4_D	FET_1_D	FET_2_D	
FET_1_G	7.2094	3.924	-0.155	-0.411	0.042	-0.041	0.196	-0.201	0.039	-0.0236	0.121	-0.114	
FET_2_G	3.9244	3.471	-0.068	-0.182	0.0179	-0.018	0.0723	-0.0719	0.0178	-0.0096	0.039	-0.03	
FET_3_G	-0.155	-0.068	2.373	2.75	-0.035	0.0395	-0.0147	0.0194	-0.019	0.039	-0.008	0.008	
FET_4_G	-0.412	-0.182	2.75	5.961	-0.139	0.147	-0.0406	0.0503	-0.13	0.141	-0.021	0.0214	
FET_3_S	0.042	0.0179	-0.035	-0.138	2.249	0.152	-0.0411	-0.0478	-0.0342	-0.0765	0.021	0.0143	
FET_4_S	-0.041	-0.0177	0.0395	0.142	0.152	2.2535	-0.0542	-0.0429	-0.0785	-0.035	0.0207	0.0214	
FET_1_S	0.196	0.0723	-0.015	-0.041	-0.041	-0.054	0.632	0.50536	0.089	0.0892	-0.021	-0.064	
FET_2_S	-0.201	-0.0719	0.0195	0.0507	-0.048	-0.043	0.505	0.6375	0.0734	0.0863	-0.064	-0.02	
FET_3_D	0.039	0.0178	-0.016	-0.13	-0.035	-0.079	0.089	0.0734	0.3465	0.301	-0.018	-0.021	
FET_4_D	-0.023	-0.0096	0.033	0.141	-0.077	-0.035	0.0894	0.0863	0.301	0.3455	-0.022	-0.018	
FET_1_D	0.128	0.039	-0.008	-0.021	0.021	0.0207	-0.021	-0.0639	-0.0181	-0.022	0.0861	0.0538	
FET_2_D	-0.114	-0.0297	0.008	0.0214	0.0143	0.0214	-0.064	-0.02	-0.0206	-0.0181	0.0538	0.0876	
Resistance Matrix													
	FET_1_G	FET_2_G	FET_3_G	FET_4_G	FET_3_S	FET_4_S	FET_1_S	FET_2_S	FET_3_D	FET_4_D	FET_1_D	FET_2_D	
FET_1_G	8534.4	4322.7	0	0	0	0	0	0	0	0	0	0	
FET_2_G	4322.7	4322.7	0	0	0	0	0	0	0	0	0	0	
FET_3_G	0	0	3130.7	3130.7	0	0	0	0	0	0	0	0	
FET_4_G	0	0	3130.7	7344.1	0	0	0	0	0	0	0	0	
FET_3_S	0	0	0	0	122.41	61.972	0	0	0	0	0	0	
FET_4_S	0	0	0	0	61.972	122.42	0	0	0	0	0	0	
FET_1_S	0	0	0	0	0	0	216.52	147.95	0.0331	0.04281	0	0	
FET_2_S	0	0	0	0	0	0	147.95	217.13	0.0232	0.03009	0	0	
FET_3_D	0	0	0	0	0	0	0.0331	0.02324	132.29	102.14	0	0	
FET_4_D	0	0	0	0	0	0	0.0428	0.03009	102.14	132.61	0	0	
FET_1_D	0	0	0	0	0	0	0	0	0	0	58.512	32.994	
FET_2_D	0	0	0	0	0	0	0	0	0	0	32.994	59.144	

From the Q3D calculations on the planar module it was found that the sum of the drain and source inductances was between 0.6 nH and 0.7 nH for the four transistors in the module. This could be compared to the corresponding inductances of a TO247 package. Using Eq. (9) in [5] the inductance of a rectangular loop can be found. Inserting the geometrical dimensions of a TO247 package and multiplying the obtained value from the mentioned equation with 0.75 it is found that the TO247 package has approximately 8.7 nH parasitic inductance between the drain and source terminals. This means that using the proposed planar module concept, it is possible to reduce the parasitic inductance by approximately 92 %.

III. SIMULATION RESULTS

The obtained values from Table I together with the model of the SiC-transistor, provided by the manufacturer, were used to study the behavior of the the module in simulation environment. For this purpose, LTspice with a maximum time-step of 5 ns was used. The complete schematic of the simulated circuit can be seen in Fig. 6. Simulation results show an extremely fast switching and comparably low oscillations. Figure 7 and 8 show part of simulation results where the upper graph shows the inductor current, the middle graph shows VDS and the lower part show the VGS of the upper and lower switches.

Fig. 6: Complete schematic of the step-down converter including all parasitic components.

Fig. 7: Simulation results showing the inductor current, VDS and VGS. Switching frequency is set to 27 kHz and duty ratio is 40 %.

Fig. 8: Simulation results showing the inductor current, VDS and VGS.

IV. EXPERIMENTAL RESULTS

The bare dies were connected to the PCBs through a soldering process and the connections were tested by applying a direct voltage to the gate and a constant VDS. Later on, in order to verify proper switching, the system was configured as a synchronous step-down converter with an operating frequency of 27 kHz and tested with an obtained efficiency of 97.7 % at V_{in} 100 V and input power of 50 W. The signals were studied on an oscilloscope and the input and output powers were observed on a high-accuracy power meter (0.02 % accuracy). It should be mentioned that these values were earned from the system without any tuning, only to verify the technique and correct operation. The complete board, the components as well as the experimental set up can be seen in Fig. 9. An isolated gate driver was employed to drive the gate with the voltages at -3 and +15 V.

Fig. 9: The planar module (left) and the experimental setup (right).

Fig. 10: Shows VDS of upper (green) and lower (yellow) transistors as well as the inductor current of the buck converter. The duty ratio was 40 % in this test.

Fig. 11: Shows VGS of upper (yellow) and lower (green) transistors as well as the inductor current of the buck converter.

Proper switching could be verified by measuring the drain-source voltage of the transistor (VDS) as well as the current of the inductor of the step-down converter, see Fig. 10. The rise- and fall times of VDS are approximately 20 ns. Figure 11 shows the gate signals (VGS) of the upper and lower transistors. Almost no oscillations and fast switching time can be observed from this figure.

V. CONCLUSIONS

To improve the switching properties of SiC Power MOSFETs, a half-bridge was designed using SiC bare dies which were directly connected to the PCB, successfully forming a planar module. In the layout, all chips at the upper and lower switch positions are laid with their drains on the bottom substrate, which is normally sintered on the copper base-plate that is mounted on a heatsink. The reason for using bare dies was to eliminate the inductance of the package of the MOSFETs which for a TO247 package corresponds to approximately 8.7 nH between the drain and source terminals. Due to the smaller die pads compared to lead pads of a package, the PCB could be designed with lower loop inductance which reduces the total inductance even more. From Q3D calculations on the proposed planar module concept it was found that the parasitic inductances of the transistors were between 0.6 and 0.7 nH between drain and source. This corresponds to a reduction of 92 %. The proposed planar module was also tested in dc-dc converter operation. Switching waveforms from these experiments are also presented.

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