Design Optimization and Realization of 4H-SiC Bipolar Junction Transistors

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To My Parents
“When yesterday is vanished in the past,
And morrow lingers in the future vast,
To neither give a thought but prize the hour;
For that is all you have and Time flies fast.”

Omar Khayyám
Abstract

4H-SiC-based bipolar junction transistors (BJTs) are attractive devices for high-voltage and high-temperature operations due to their high current capability, low specific on-resistance, and process simplicity. To extend the potential of SiC BJTs to power electronic industrial applications, it is essential to realize high-efficient devices with high-current and low-loss by a reliable and wafer-scale fabrication process. In this thesis, we focus on the improvement of the 4H-SiC BJT performance, including the device optimization and process development.

To optimize the 4H-SiC BJT design, a comprehensive study in terms of cell geometries, device scaling, and device layout is performed. The hexagon-cell geometry shows 42% higher current density and 21% lower specific on-resistance at a given maximum current gain compared to the interdigitated finger design. Also, a layout design, called intertwined, is used for 100% usage of the conducting area. A higher current is achieved by saving the inactive portion of the conducting area. Different multi-step etched edge termination techniques with an efficiency of >92% are realized.

Regarding the process development, an improved surface passivation is used to reduce the surface recombination and improve the maximum current gain of 4H-SiC BJTs. Moreover, wafer-scale lift-off-free processes for the n- and p-Ohmic contact technologies to 4H-SiC are successfully developed. Both Ohmic metal technologies are based on a self-aligned Ni-silicide (Ni-SALICIDE) process.

Regarding the device characterization, a maximum current gain of 40, a specific on-resistance of 20 mΩ·cm², and a maximum breakdown voltage of 5.85 kV for the 4H-SiC BJTs are measured. By employing the enhanced surface passivation, a maximum current gain of 139 and a specific on-resistance of 579 mΩ·cm² at the current density of 89 A/cm² for the 15-kV class BJTs are obtained. Moreover, low-voltage 4H-SiC lateral BJTs and Darlington pair with output current of 1–15 A for high-temperature operations up to 500 °C were fabricated.

This thesis focuses on the improvement of the 4H-SiC BJT performance in terms of the device optimization and process development for high-voltage and high-temperature applications. The epilayer design and the device structure and topology are optimized to realize high-efficient BJTs. Also, wafer-scale fabrication process steps are developed to enable realization of high-current devices for the real applications.

Keywords: 4H-SiC, BJT, high-voltage and ultra-high-voltage, high-temperature, self-aligned Ni-silicide (Ni-SALICIDE), lift-off-free, wafer-scale, current gain, Darlington.
Sammanfattning

Bipolärtransistorer (BJT) baserade på 4H-SiC är lovande komponenter för högspännings- och högtemperatur-tillämpningar tack vare hög strömdrivningförmåga, låg specifik resistans i framspänning och enkel tillverkningsprocess. För att utnyttja potentialen hos 4H-SiC bipolärtransistorer i kraftelektronikttillämpningar är det viktigt att demonstrera mycket effektiva komponenter med låga förluster med en pålitlig tillverkningsprocess som kan användas på hela skivor. I den här avhandlingen fokuserar vi på hur man kan förbättra prestandan hos bipolärtransistorer genom att optimera komponenten och dess tillverkningsprocess.

För att optimera komponentdesignen gjordes en omfattande undersökning av cellgeometri, komponentskalning och komponentlayout. En hexagonal geometri resulterade i 42 % högre strömtäthet och 21 % lägre specifik resistans i framspänning för en given strömförstärkning jämfört med ett fall där cellgeometrin var uppdelad i fingrar. Layouten var gjord på ett sammanflätat vis så att 100 % av den ledande ytan kunde utnyttjas. Därför kunde högre ström uppnås genom att undvika inaktiva delar av ytan. Olika etsade termineringstekniker med en effektivitet upp till 92 % visades.


Komponentprestanda som uppnåddes var en maximal strömförstärkning på 40 gånger, specific resistans i framspänning på 20 mΩ·cm² och en maximal genombrotts-spänning på 5.85 kV. Med den förbättrade ytpassiveringen blev förstärkningen 139 gånger, och den specifika resistansen 579 mΩ·cm² vid en strömtäthet på 89 A/cm² för bipolärtransistorer i 15 kV klass. Dessutom kunde lågspänning laterala BJT:er och Darlington par demonstreras med en ström mellan 1 och 15 A för högtemperatur-tillämpningar upp till 500 °C.

Sammanfattningsvis så fokuserar denna avhandling på att förbättra komponentprestanda för bipolärtransistorer i SiC genom att optimera komponenterna och att utveckla tillverkningsprocessen för högspännings- och högtemperatur-tillämpningar. Epitaxiella lager och komponentstruktur och topologi har optimerats för att demonstrera mycket effektiva bipolärtransistorer. En tillverkningsprocess på skivnivå har utvecklats för att uppnå högströmskomponenter som svarar mot behoven i verkliga tillämpningar.
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Most of all, I wish to express my deepest gratitude to my dear sister, brothers, sister-in-laws, brother-in-law, and my lovely nieces and nephew in Iran for their kind support, care, and true love. Finally, and most importantly, I sincerely dedicate this PhD thesis to my parents, whom remind me that kindness is the most beautiful thing of all. None of these would have been possible without your endless love and incredible support. Success is in my stride, because I have you by my side. I love you all.

Hossein

August 2017, Kista
List of appended papers*

I. 15 kV-Class implantation-Free 4H-SiC BJTs with Record High Current Gain

II. Modification of Etched Junction Termination Extension for the High Voltage 4H-SiC Power Devices

III. Area- and Efficiency-Optimized Junction Termination for a 5.6 kV SiC BJT Process with Low ON-Resistance

IV. 5.8-kV Implantation-Free 4H-SiC BJT with Multiple-Shallow-Trench Junction Termination Extension

V. A Comprehensive Study on the Geometrical Effects in High Power 4H-SiC BJTs

VI. Optimal Emitter Cell Geometry in High Power 4H-SiC BJTs

VII. Intertwined Design: A Novel Lithographic Method to Realize Area Efficient High Voltage SiC BJTs and Darlington Transistors

VIII. A Wafer-Scale Self-Aligned Ni-Silicide (SALICIDE) Low-Ohmic Contact

* Dr. Arash Salemi and I started our PhD almost together to realize high-voltage and ultra-high-voltage 4H-SiC bipolar devices, including the BJTs and PiN rectifiers. During the work, we separately performed the device simulation and the layout design whereas we did most of the fabrication process and characterization together. Besides, I focused more on the device optimization, layout design, and wafer-scale process development with special attention to the improvement of the device efficiency in terms of reducing the device total area and increasing the current density.
Technology on n-type 4H-SiC


IX. 500 °C High Current 4H-SiC Lateral BJTs for High-Temperature Integrated Circuits

Related publications not included in the thesis

1. Conductivity Modulated Ultra-High-Voltage Implantation-Free 4H-SiC PiN Diodes
   Arash Salemi, Hossein Elahipanah, Carl-Mikael Zetterling, and Mikael Östling, to be presented at ICSCRM 2017.

2. Electrical Characterization of Integrated 2-input TTL NAND Gate at Elevated Temperature, Fabricated in KTH Bipolar SiC-Technology

3. Low temperature Ni-Al ohmic contacts to P-type 4H-SiC using semi-SALICIDE processing

4. Gated Base Structure for Improved Current Gain in SiC Bipolar Technology
   Bengt Gunnar Malm, Hossein Elahipanah, Arash Salemi, and Mikael Östling, to be presented at ESSDERC 2017.

5. High-temperature passive components for extreme environments

6. 10+ kV Implantation-Free 4H-SiC PiN Diodes

7. 4.5-kV 20-mΩ·cm² Implantation-Free 4H-SiC BJT with Trench Structures on the Junction Termination Extension

8. Conductivity Modulated On-axis 4H-SiC 10+ kV PiN Diodes


10. Area-Optimized JTE for 4.5 kV Non Ion-Implanted 4H-SiC BJT
11. Investigation of the Breakdown Voltage in High Voltage 4H-SiC BJT with Respect to Oxide and Interface Charges

12. Geometrical Effect Dependency on the On-State Characteristics in 5.6 kV 4H-SiC BJTs

13. State of the art power switching devices in SiC and their applications
Summary of appended papers

Paper I. 15 kV-Class Implantation-Free 4H-SiC BJTs with Record Current Gain of 139

Implantation-free mesa-etched ultra-high-voltage 4H-SiC bipolar junction transistors (BJTs) with the record maximum current gain of 139 are fabricated and studied. A high current gain is achieved by optimized surface passivation and optimal cell geometries. An area-optimized multi-step etched junction termination extension (O-JTE) is employed to obtain a high breakdown voltage. Also, different cell geometries (single finger, square, and hexagon cell geometries) are compared with each other.

The author contributed in the simulation and layout design, 30% of the data analysis, and the manuscript writing.

Paper II. Modification of Etched Junction Termination Extension for the High Voltage 4H-SiC Power Devices

High voltage 4H-SiC bipolar junction transistors (BJTs) with modified etched junction termination extension (JTE) are fabricated and optimized in terms of the length and remaining dose of JTEs. It is found that the JTE1 is the most effective one in spreading the electric field. Hence, for a given total termination length, a decremental JTE length from the innermost edge to the outermost mesa edge of the device results in better modification of the electric field. A breakdown voltage of 4.95 kV is measured for the modified device, which shows ~20% improvement of the termination efficiency for no extra cost or extra process step. Equal-size BJTs by interdigitated-emitter with different number of fingers and cell pitches are fabricated. It is presented that the maximum current gain decreases by having more fingers while the maximum current gain is achieved at higher current density.

The author performed 100% of the layout design, 80% of the fabrication process, 100% of the characterization and data analysis, and 90% of the manuscript writing.

Paper III. Area- and Efficiency-Optimized Junction Termination for a 5.6 kV SiC BJT Process with Low ON-Resistance

In this paper, an efficient area-optimized JTE with triple-step etching is designed and demonstrated to realize high-voltage 4H-SiC BJTs. A breakdown voltage of 5.65 kV with a high termination efficiency of 92% is achieved. A maximum current gain of 44 at a current density of 472 A/cm² and a specific on-resistance of 18.8 mΩ·cm² is obtained.
The author contributed in the layout design, performed 50% of the fabrication process, 40% of the data analysis, and contributed in the manuscript writing.

**Paper IV. 5.8-kV Implantation-Free 4H-SiC BJT with Multiple-Shallow-Trench Junction Termination Extension**

In this paper, an implantation-free 4H-SiC bipolar junction transistors with multiple-shallow-trench junction termination extension is demonstrated. A maximum open-base breakdown voltage of 5.85 kV is obtained, which is 93% of the theoretical value. The maximum current gain of 40 at a current density of 370 A/cm² is measured. A specific on-resistance of 28 mΩ·cm² is obtained.

The author performed 100% of the layout design, 80% of the fabrication process, 100% of the characterization and data analysis, and 90% of the manuscript writing.

**Paper V. A Comprehensive Study on the Geometrical Effects in High Power 4H-SiC BJTs**

In this paper, the scaling and geometrical effect on the forward characteristics of high power BJTs is comprehensively studied. The effect of varying the emitter-base geometry, i.e., the emitter width, the base width, emitter contact–emitter edge distance, and base contact–emitter edge on the on-state characteristics for different emitter cell geometries are studied. The emitter and base size show significant influence on the maximum current gain.

The author contributed in the layout design, performed 50% of the fabrication process, 30% of the data analysis, and contributed in the manuscript writing.

**Paper VI. Optimal Emitter Cell Geometry in High Power 4H-SiC BJTs**

In this paper, three 4H-SiC BJT designs including the linear interdigitated fingers, square cell geometry, and hexagon cell geometry are fabricated. The device characteristics are analyzed in terms of design, maximum current gain, on-resistance, current density, and temperature performance. Moreover, the emitter size effect and surface recombination are investigated for all designs. The linear interdigitated fingers indicate the highest maximum current gain whereas the hexagon- and square-cell geometries show a higher current density and a lower on-resistance at a given current gain with respect to their emitter widths.

The author contributed in the layout design, performed 50% of the fabrication process, 40% of the data analysis, and contributed in the manuscript writing.
Paper VII. Intertwined Design: A Novel Lithographic Method to Realize Area Efficient High Voltage SiC BJT s and Darlington Transistors

In this paper, a novel lithographic method called intertwined design for high power SiC devices is demonstrated. This improves the area usage and current capability with more uniform current distribution along the device. The higher current drive is achieved by employing the inactive area underneath the base metal contact pads; the more uniform current distribution is obtained by the center-base design; whereas the hexagon and square cell geometries results in >15 % higher current density at lower on-resistance compared with the conventional finger design. Also, we have experimentally shown the intertwined design to combine these advantages and realize a high efficient SiC power device. Center-base high voltage 4H-SiC BJT s and Darlington pairs with different square and hexagon cell geometries are fabricated and compared with conventional designs to prove the ability of the intertwined design. The method can widely be used for large-area high voltage BJT s as well as for integrated devices.

The author performed 100% of the layout design, 80% of the fabrication process, 100% of the characterization and data analysis, and 90% of the manuscript writing.

Paper VIII. A Wafer-Scale Self-Aligned Ni-Silicide (SALICIDE) Low-Ohmic Contact Technology on n-type 4H-SiC

A self-aligned nickel (Ni) silicide process for n-type Ohmic contacts on 4H-SiC is demonstrated and electrically verified in a wafer-scale device process. The key point is to anneal the contacts in two steps. The process is successfully employed on wafer-level and a contact resistivity below \(5 \times 10^{-6} \, \Omega \cdot \text{cm}^2\) is achieved. The influence of the proposed process on the oxide quality is investigated and no significant effect is observed. The proposed self-aligned technology eliminates the undesirable effects of the lift-off process. Moreover, it is simple, fast, and manufacturable at wafer-scale, which saves time and cost.

The author performed 90% of the process development and experimental design, 70% of the characterization and data analysis, and 75% of the manuscript writing.

Paper IX. 500 °C High Current 4H-SiC Lateral BJT s for High-Temperature Integrated Circuits

High-current 4H-SiC lateral BJT s for high-temperature monolithic integrated circuits are fabricated. The BJT s have three different sizes and the designs are optimized in terms of emitter finger width, emitter finger length, and the device layout in order to reach higher current density, lower on-resistance, and more uniform current distribution. A maximum current gain of >53 at significantly higher current densities is
achieved for both large- and small-area BJTs compared to the conventional design. The BJTs are measured from room temperature to 500 °C. A breakdown voltage of >50 V is measured for the devices.

The author performed 100% of the layout design, 100% of the fabrication process, 100% of the characterization and data analysis, and 90% of the manuscript writing.
### List of acronyms and Symbols

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Abbreviation and Description</th>
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<tbody>
<tr>
<td>AFM</td>
<td>Atomic-force microscopy</td>
</tr>
<tr>
<td>Al</td>
<td>Aluminum</td>
</tr>
<tr>
<td>AlN</td>
<td>Aluminum nitride</td>
</tr>
<tr>
<td>Ar</td>
<td>Argon</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar junction transistor</td>
</tr>
<tr>
<td>C</td>
<td>Carbon</td>
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<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>FET</td>
<td>Field effect transistor</td>
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<tr>
<td>FSA</td>
<td>First step annealing</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium nitride</td>
</tr>
<tr>
<td>GTO</td>
<td>Gate turn-off thyristor</td>
</tr>
<tr>
<td>H</td>
<td>Hydrogen</td>
</tr>
<tr>
<td>HF</td>
<td>Hydrofluoric acid</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>ICP</td>
<td>Inductively-coupled plasma</td>
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<tr>
<td>IGBT</td>
<td>Insulated-gate bipolar transistor</td>
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<tr>
<td>JBS</td>
<td>Junction barrier Schottky</td>
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<tr>
<td>Jc</td>
<td>Current density</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction field effect transistor</td>
</tr>
<tr>
<td>JTE</td>
<td>Junction termination extension</td>
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<tr>
<td>MESFET</td>
<td>Metal semiconductor field effect transistor</td>
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<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>MPS</td>
<td>Merged PiN Schottky</td>
</tr>
<tr>
<td>N</td>
<td>Nitrogen</td>
</tr>
<tr>
<td>Ni</td>
<td>Nickel</td>
</tr>
<tr>
<td>NO</td>
<td>Nitric oxide</td>
</tr>
<tr>
<td>N2O</td>
<td>Nitrous oxide</td>
</tr>
<tr>
<td>NPT</td>
<td>Non-punch-through</td>
</tr>
<tr>
<td>O-JTE</td>
<td>Area-optimized junction termination extension</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma-enhanced chemical vapor deposition</td>
</tr>
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</table>
PT  \text{Punch-through} \\
\textit{R}_\text{ON} \text{ Specific on-resistance} \\
\text{RIE} \text{ Reactive ion etching} \\
\text{RTA} \text{ Rapid thermal annealing} \\
\text{SALICIDE} \text{ Self-aligned silicide} \\
\text{SBD} \text{ Schottky barrier diode} \\
\text{SCR} \text{ Space charge region} \\
\text{SEM} \text{ Scanning electron microscopy} \\
\text{Si} \text{ Silicon} \\
\text{SiC} \text{ Silicon carbide} \\
\text{SiO}_2 \text{ Silicon dioxide} \\
\text{SOI} \text{ Silicon on insulator} \\
\text{SSA} \text{ Second step annealing} \\
\text{ST-JTE} \text{ Multiple-shallow-trench junction termination extension} \\
\text{TCAD} \text{ Technology computer aided design} \\
\text{Ti} \text{ Titanium} \\
\text{TiW} \text{ Titanium tungsten} \\
\text{TLM} \text{ Transmission line model} \\
\text{V}_\text{BR} \text{ Breakdown voltage} \\
\text{WBG} \text{ Wide bandgap} \\
\text{XRD} \text{ X-ray diffraction} \\
\alpha \text{ Current transfer ratio} \\
\beta \text{ Common-emitter maximum current gain} \\
\rho_c \text{ Contact resistivity}
Chapter 1. Introduction

Perhaps electrical energy is the most important phenomenon that the modern society is affected by. Today’s information-oriented world is connected through the networks, which are all based and supplied by electrical power. Nowadays, by the enormous growth of the information technology, the electrical energy consumption is vastly increasing. Supplying, transferring, and using this huge amount of energy consequently raises the power loss, which is mostly in form of heat dissipation and causes carbon dioxide (CO₂) emission. This becomes more and more critical for the global warming and climate changes [1].

To use the electrical energy more efficiently with lower power loss, it is inevitable to generate, store, transport, and convert it to higher or lower voltages and currents in different AC and DC forms. This forces us to replace the current technology with a new generation of reliable technology with more efficient energy utilization and lower loss. The power electronic systems employ power semiconductor devices like power rectifiers and switches to convert DC and AC electrical energies. Fig. 1.1 schematically presents the main applications of such high-power devices. Most of available power semiconductors are fabricated on silicon (Si) technology. Thanks to the maturity of the Si process, which is mostly due to the development of the nanoscale Si integrated circuits (ICs), advanced Si-based power devices are developed in large-area wafer-size, extending the performance of the power devices beyond the Si unipolar limits.

Figure 1.1. Different examples of the electric power conversion.
However, a further development of the high-voltage Si devices is limited by the Si material properties. Therefore, there is a demand to replace the Si with an alternative semiconductor for power electronics.

1.1 Silicon Carbide

Nowadays, very high-current (> 1 kA) and high-voltage (~6 kV) wafer-size Si power devices and modules are commercially available [2]–[7]. The high-power modules are made of these packaged devices in series, which can handle thousands of kilowatts of power on a system level. Even though the power efficiency of these systems are relatively high (> 90 %), their power loss leads to an enormous amount of dissipated heat in a massive system with such output power. Therefore, it is inevitable to use cooling components to increase the system durability and maintain the efficiency and functionality. Moreover, such structures are large in volume and weight. High-voltage devices fabricated by wide bandgap (WBG) semiconductors have been proposed and investigated to overcome these problems. These materials can sustain higher blocking voltage with a lower leakage current, and offers lower on-resistance ($R_{ON}$). Wide-bandgap semiconductors like silicon carbide (SiC) and gallium nitride

![Figure 1.2. (a) Schematic atomic structure of SiC (b) 4-inch and 6-inch 4H-SiC wafers that are currently available on the market [8].](image)

<table>
<thead>
<tr>
<th>Material Property</th>
<th>Symbol</th>
<th>Si</th>
<th>4H-SiC</th>
<th>GaN</th>
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<tbody>
<tr>
<td>Bandgap (eV at 300 K)</td>
<td>$E_g$</td>
<td>1.12</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Critical electric field (MV/cm)</td>
<td>$E_C$</td>
<td>0.25</td>
<td>2.2</td>
<td>3</td>
</tr>
<tr>
<td>Electron mobility (cm$^2$/V·cm)</td>
<td>$\mu_n$</td>
<td>1350</td>
<td>1020</td>
<td>400</td>
</tr>
<tr>
<td>Hole mobility (cm$^2$/V·cm)</td>
<td>$\mu_p$</td>
<td>480</td>
<td>120</td>
<td>30</td>
</tr>
<tr>
<td>Saturation electric velocity (cm/s)</td>
<td>$V_{sat}$</td>
<td>1</td>
<td>2</td>
<td>2.5</td>
</tr>
<tr>
<td>Thermal conductivity at 300 K (W/cm·K)</td>
<td>$\lambda$</td>
<td>1.5</td>
<td>4.5</td>
<td>1.3</td>
</tr>
<tr>
<td>Relative permittivity</td>
<td>$\varepsilon_r$</td>
<td>11.9</td>
<td>10</td>
<td>9.5</td>
</tr>
</tbody>
</table>
(GaN) are of great interest as potential alternatives for Si in high-power and high-temperature applications. Table 1.1 compares the material properties of SiC and GaN with Si. Currently, SiC is more desirable for high-voltage (>1200 V) devices compared to GaN. This is mainly due to the lower cost and better quality of the material, which gives the possibility of making vertical devices with a high yield. In addition, it has a higher thermal conductivity that is beneficial for higher power densities. Fig. 1.2a presents the atomic structure of a SiC crystal. Thanks to the recent development of SiC growth technology, 6-in SiC wafers are currently available in the market (see Fig. 1.2b). Among different SiC polytypes, 4H-SiC is more attractive due to the higher career mobility, wider bandgap, and high quality of the bulk and epitaxial grown material [9]. Currently, high-voltage SiC devices up to 1.7 kV are commercially available [7], [8], [10]–[13]. There is a high demand for higher voltage and current rates for the next generation power electronics [14]. For instance, if a high power module including 3.3-kV Si devices is replaced by a high-current 15-kV (or 30-kV) SiC device, one can significantly reduce the voltage drop ($V_f$) and power loss on the chip level. On a larger scale, changing a high-power (> 1 MW) system with a SiC-based package or modules the weight, volume, power loss and the total cost of the system can be reduced. The isolation of such high-voltage devices, testing and measurement, and finally the packaging are some of the current challenges, which appear after the device design and fabrication. Fig. 1.3 represents the roadmap for SiC devices for targeted applications in power electronics.

Other than high-power applications, semiconductor devices are employed for high-temperature electronics and harsh environment applications (see Fig. 1.4). Beside the interesting high-voltage properties originating from the wide bandgap of the SiC, this

Figure 1.3. The targeted application of SiC and GaN power devices in power electric systems [14].
Figure 1.4. The application of semiconductor devices for high-temperature electronics. SiC-based devices and integrated circuits paved the way for > 300 °C operations.

material is also capable of operating at much higher temperature than Si, which is mainly due to the wide bandgap and low intrinsic carrier concentration of the SiC. This along with its high thermal conductivity provides a superb capability for SiC for extreme-temperature electronics. These SiC devices can be used for direct sensing and operation in reactors, engines, turbines, traction, aviation etc. in which the temperature can rise up to 600 °C. The current silicon on insulator (SOI) technology is barely operational up to 300 °C. It is worth noting that the device packaging for such extreme temperatures is a challenging issue. Nowadays, most of the high-temperature SiC devices and ICs are in use on a bare die or implemented on ceramic or aluminium nitride (AlN) substrate without package.

Among various power semiconductor devices, 4H-SiC bipolar junction transistors (BJTs) are attractive candidates for high-voltage applications due to their high current capability, low specific on-resistance, and simple fabrication process. Moreover, the absence of a gate oxide and their negative bias temperature dependency behavior make them suitable for high-temperature operations. In order to industrialize the developed 4H-SiC BJTs, it is necessary to reduce the die size and total cost. Therefore, one has to improve the device design and the fabrication process of 4H-SiC BJTs. This becomes more important for higher voltage rates, which have a higher ratio of the edge termination area to the total die size. Therefore, the device design and performance should be optimized to minimize the area usage for each die. It is exactly the device optimization and process development of 4H-SiC BJTs that this thesis focuses on.

1.2 Thesis Objective

The objective of this thesis is to improve the 4H-SiC BJT performance, including the device optimization and process development in order to realize high-current 4H-SiC BJTs for different applications. To achieve this, different device parameters,
1.2. Thesis Objective

including the epilayers design, device dimension, area-usage, the layout design, and the fabrication process are optimized and enhanced. An established 4H-SiC BJT technology reported in [15]–[17] show the attractive potential of these devices for high-voltage and high-temperature applications. Large-area vertical ultra-high-voltage and lateral high-temperature SiC BJTs with sophisticated performance can be designed and realized by a comprehensive investigation on design consideration and an enhanced fabrication process of 4H-SiC BJTs.

In order to reach this objective, a device modeling is required as the starting point. To implement an accurate model, we employed the properties of SiC material and the details of our simulation and modeling parameters for high-voltage and high-temperature applications from [17] and [18]. The same SiC parameters are used in this thesis to implement the designs in the TCAD simulation [19]. The device simulation is a powerful tool to design new devices, track the device behavior, virtually observe the changes inside the device, and study the trends. The feedback from the measurements of previous batches can be used as an input to calibrate the TCAD simulation and modeling.

The methodology of this thesis, defined as device development loop, including the design, fabrication, measurement, and optimization is shown in Fig. 1.5. Accurate SiC parameters are required for a meaningful simulation study, particularly for high-temperature modeling. We upgraded the simulation parameters over the years with the new extracted parameters from experimental studies to find a good agreement between simulation and experimental results. We performed a great deal of device simulation to provide an optimum design for the 4H-SiC BJTs in terms of the epilayer design, maximum current gain ($\beta$), on-resistance, current density ($J_C$), breakdown voltage ($V_{BR}$) etc. Afterward, we drew the layout designs with different cell geometries, area-efficient designs, various sizes etc. Once the device and layout design were accomplished, the first batch including the high-voltage (4.5-kV class) 4H-SiC BJTs is fabricated with the established process [16]. The characterization of BJTs in the first batch demonstrated a blocking behavior as expected from the simulation results. However, the current gain is lower than the simulated value and dramatically lower than the ideal value. This showed that a higher current gain is achievable by improvement of the fabrication process. As presented in the device development flow, it is very important to have feedback from post-process measurements, or even during the processing in order to optimize the device design and development. Therefore, we investigated the effect of fabrication process on the performance of the previous fabricated batches, iterated the characterization and simulation loop, and extracted the investigated parameters. The surface recombination is the main factor, which degrades
Figure 1.5. The SiC device development loop including the device simulation, fabrication, and characterization.

the current gain. In the next batch for ultra-high-voltage (15-kV) BJTs, a significantly higher current gain was achieved by using an enhanced surface passivation.

At the same time in another development batch, we tried to eliminate the lift-off process from our fabrication process steps. Even though this might not directly affect the device performance, however it is inevitable to remove the lift-off process for industrialization of a developed device. The self-aligned silicide process is very well-known from Si technology. However, a much higher temperature (950 °C) is required in SiC to form an Ohmic contact. The high temperature annealing of the metal/oxide layer can affect the quality of oxide and degrade the device performance. We developed a wafer-scale nickel (Ni) self-aligned nickel silicide (Ni-SALICIDE) process for the n-Ohmic contact by performing separate low-temperature and high-temperature annealing steps. Also, a lift-off-free process for the p-Ohmic contact technology to 4H-SiC is developed. The process consists of a low-temperature (600 °C) Ni-SALICIDE and removal of unreacted Ni as of for the n-contact, deposition and patterning of a Ti/Al stack, and a final high temperature annealing (>900 °C) to transform the Ni-silicide/Ti/Al for the p-Ohmic contact.
1.3 Thesis Structure

In this thesis, the main goal is to design and realize 4H-SiC devices for high-voltage and high-temperature applications with the focus on the npn BJT technology. Efficient termination techniques are designed and implemented to realize high-voltage (4.5-kV) and ultra-high-voltage (15-kV) devices. The effect of device geometry and scaling are investigated and optimized to achieve a high current gain and current density. Furthermore, high current BJTs and Darlington pairs are designed and fabricated for the high-temperature low-voltage operations as well as the high-voltage application. Additionally, the device topology is optimized to have more efficient usage of the area. The main purpose is to find an optimum design for the devices to minimize the area and total cost as well as to improve the device performance. Process dependent parameters are also studied and enhanced to minimize the effect of fabrication related parameters. Besides, some process steps are improved for a wafer-scale fabrication, which is important for industrialization of the devices.

In Chapter 2, the current SiC technology and the advanced power SiC devices are explained. The performance of the state-of-the-art SiC power rectifiers and power switches is summarized. Also, a brief overview on the best reported GaN power devices is given and the performance of the SiC and GaN power devices is compared.

A comprehensive investigation on the device design, including the epilayer design, scaling and geometries, edge termination techniques, and efficient layout designs is performed and described in Chapter 3. Compared to the interdigitated finger design, the hexagon- and square-cell geometries show 42% higher current density and 21% lower specific on-resistance at a given maximum current gain. Moreover, a layout design called intertwined design is used to save the inactive portion of the conducting area. More than 14% higher current is achieved by 100% usage of the conducting area. To achieve a high breakdown voltage, various edge termination designs based on multi-step etched junction termination extension (JTE) are implemented. A termination efficiency of 92% and 93% is achieved for the area-optimized-JTE (O-JTE) and multiple-shallow-trench-JTE (ST-JTE), respectively, compared to the 75% for the conventional double-JTE.

Chapter 4 summarizes the fabrication process technology used for different batches described in this thesis. The overall process steps for the high-voltage and high-temperature batches are presented and briefly explained. An enhanced surface passivation technique to diminish the effect of surface recombination and improve the maximum current gain of the 4H-SiC BJTs is developed. Furthermore, special attention is dedicated to eliminate the lift-off process from the n- and p-Ohmic contact technology to 4H-SiC. A wafer-scale Ni-SALICIDE process for n-Ohmic
contact technology to 4H-SiC is successfully developed. The process is based on a low-temperature annealing (600 °C), removal of unreacted Ni, and a final high-temperature annealing (950 °C) to form a low-resistive n-Ohmic contact. Besides, a lift-off-free p-Ohmic contact technology to 4H-SiC by assist of Ni-SALICIDE is developed. A low-temperature (600 °C) Ni-SALICIDE is formed both on the n- and p-epilayers. Afterward, a Ti/Al stack is deposited and exclusively patterned on the p-type opening. A final high temperature annealing (>900 °C) transforms both the Ni-silicide and Ni-silicide/Ti/Al to the n- and p-Ohmic contacts. A contact resistivity of $5 \times 10^{-6} \ \Omega \cdot \text{cm}^2$ and $7 \times 10^{-4} \ \Omega \cdot \text{cm}^2$ for the n- and p-Ohmic contacts are achieved, respectively.

In Chapter 5, the characterization results of the 4H-SiC BJTs are presented and discussed. A maximum current gain and a specific on-resistance of 40 and 20 mΩ·cm$^2$ at the current density of 330 A/cm$^2$ for the high-voltage (4.5-kV class) is achieved, respectively. Also, a breakdown voltage of 5.65 kV and 5.85 kV for the 4H-SiC BJTs with O-JTE and ST-JTE edge terminations is measured. By employing the improved surface passivation, a $\beta$ and $R_{ON}$ of 139 and 579 mΩ·cm$^2$ at the current density of 89 A/cm$^2$ for the 15-kV class BJT is obtained, respectively. Moreover, 4H-SiC lateral BJTs with different sizes and output current of 1–11 A for high-temperature operations up to 500 °C are fabricated. Although the output current of the 4H-SiC BJTs decreases to 30% of the maximum value by increasing the temperature from 27 to 500 °C, the BJTs are fully operational. Additionally, Darlington pairs are designed and fabricated for high-current drive applications. A maximum current gain of 3300 at 15 A is measured.

Finally, Chapter 6 summarizes the achievements and main results of this thesis. The results pave the way to develop more efficient 4H-SiC BJT devices which are manufacturable in large- and wafer-scale process. Finally, the design considerations for the further development of the presented technology in future research is proposed.
Chapter 2. Current Technology and Prospective of SiC Power Devices

Chapter 1 briefly introduced SiC devices and their applications in power electronics and high-temperature electronics. In this chapter, we give an overview on the state-of-the-art SiC power devices, the challenges, and the prospective developments of such devices. Also, the most recent reports on GaN power devices are summarized and briefly discussed.

Semiconductor devices can be split into two different groups, based on the operation and functionality of different devices: (1) rectifiers and (2) switches. The former controls the current in one direction and blocks the current in the opposite way, whereas the latter is a triggerable switch, which can control the duration of the current flow. Each device has an input and output power. The ideal device should have identical input and output power with no power dissipation. The actual devices require a certain voltage or current to function. This introduces a power loss on the device apart from the type of device. This power loss appears as heat, which cause issues to save the energy and to cool down the circuits and systems. There has always been great challenges and progress to reduce the voltage drop, on-resistance, and the leakage current in the devices in order to reduce the total power loss. Fig. 2.1 presents the characteristics of ideal and actual rectifiers and switches. As is apparent from the figures, the performance of the actual devices is limited by:

- Non-zero voltage drop in conduction (on-resistance)
- Non-zero leakage current ($I_{Leakage}$)
- Limited blocking capability (breakdown voltage)
- Non-zero switching time between on- and off-states
- Limited variation of voltage and current in a short time

As a result, a real device exhibits power loss in the conduction, blocking, and switching modes. The improvement of these factors is the main directions for device designers and manufacturer to approach the ideal characteristics.
Figure 2.1. The $I$-$V$ characteristics of an (a) ideal power rectifier, (b) actual power rectifier, (c) ideal power switch, and (d) actual power switch.

All SiC devices can be divided into unipolar and bipolar devices depending on the flow of the majority and minority carriers [9]. For unipolar devices, such as Schottky barrier diode (SBD), junction barrier Schottky diodes (JBS), and field effect devices (JFET, MESFET, and MOSFETs), the current flow is due to majority carriers. Unlike the unipolar devices, the current flow consists of both majority and minority carriers in bipolar and hybrid devices e.g. the PiN diode and merged PiN Schottky diode (MPS), bipolar junction transistor (BJT), thyristor and gate turn-off thyristor (GTO), and insulated-gate bipolar transistor (IGBT). Solely unipolar and bipolar devices have their advantages and disadvantages in operation which will be discussed in the Chapter 3. Among these devices, nowadays, those with capability of working in both modes are of great interest for the next generation of power electronics [9]. The unipolar SiC devices are suitable for the mid-range voltage class (up to 3.3 kV) where the on-resistance of the drift layer is reasonable in forward conduction. A thicker and lower-doped drift layer for high-voltage and ultra-high-voltage ranges is required, which makes the drift layer very resistive. Therefore, one has to use bipolar SiC devices for the high-voltage range, particularly for ultra-high-voltage classes (> 10 kV) in which both p- and n-layers inject carriers into the drift layer. The amount of injection increases at higher current density and the holes and electrons flood the drift region. Hence, the carrier concentration in the drift region exceeds the doping concentration in this layer leading in dramatic reduction of the drift resistance, which is called as conductivity modulation. This is the main advantage of bipolar devices that enables them to handle high current density with surge current capability. A high carrier lifetime in
the drift layer can improve the conductivity modulation and significantly reduce the on-resistance [9]. To obtain a low on-resistance and benefit from the conductivity modulation of the bipolar devices, the minimum carrier lifetime of ~2, 5, and 10 µs for the 10-, 15-, and 20-kV devices are required, respectively [20]. There have been progress to improve the carrier lifetime by introduction of carbon atoms to occupy the carbon vacancies at certain levels [21]–[27]. Currently, three different methods are known to improve the SiC carrier lifetime: (1) carbon implantation following by high-temperature annealing [25]; (2) thermal sacrificial oxidation to introduce atomic layers of carbon at SiC surface [26]; (3) filling up the vacancies by re-crystallizing the SiC with controlled annealing and cooling down the SiC in thermodynamic equilibrium [27]. The SiC bipolar technology mainly suffers from the bipolar degradation effect originating from basal plane dislocations [28], high enough carrier lifetime, and the robustness of edge termination to achieve avalanche capability. The two former are related to the epitaxial and fabrication process whereas the latter one is more design dependent. It should be noted that the drift layer of the high-voltage devices mainly sustains the blocking voltage. Therefore, the drift epilayer is thicker than the other layers. Therefore, n-type epilayer is typical for the drift layer of the high-voltage devices due to higher mobility of the n-type and the limitations of the growth process of lowly-doped p-epilayers. In the following sections, an overview of the state-of-the-art SiC power devices together with a brief report on the recent reported GaN devices is given.

### 2.1 SiC Power Rectifiers

SiC rectifiers are of great interest for high power electronic applications, mostly used as freewheeling diodes. A favorable device should exhibit high blocking voltage, low leakage current, and low forward voltage drop. Also, a low switching loss is needed for high power circuits in which the device continuously switches between on- and off-states. In this section, the structure and properties of the main SiC rectifiers are shortly described. In addition, the advantages, drawbacks, and challenges of each technology are discussed and some most advanced devices are highlighted.

#### 2.1.1 SiC PiN Diodes

The PiN rectifier is one of the fundamental structures that is developed for power electronics (see Fig. 2.2). The device is basically made of a p-epilayer to inject holes and a thick n-drift layer to sustain the blocking voltage. The drift layer consists of a lowly-doped n-layer, which is close to intrinsic level (i), and a highly-doped n-layer underneath to inject electrons. The lowly-doped layer is sandwiched between the highly-doped p- and n-layers. Both highly-doped p- and n-layers inject carriers into the intrinsic layer until the conductivity modulation occurs. The knee voltage of the PiN
rectifiers is ~2.5 V due to the wide bandgap of SiC. A low on-resistance in the conduction mode can compensate this issue to obtain a reasonably low forward voltage drop at required current density.

PiN rectifiers have some drawbacks in switching applications. During the on-state, a high overshoot occurs which is harmful for the power circuits. This is mainly due to the high resistance of the drift layer. On the other hand, once the device is switched off, the stored charges must be discharged from the drift layer. This requires longer time for the higher concentration of the charges leading to higher power loss, which is not desirable for the power system. Therefore, there is a trade-off between on- and off-states, switching frequency, and the forward voltage drop and conduction performance of the PiN rectifier. This should be considered during the design of the devices and circuits for specific applications. Besides, compared to Si, SiC PiN rectifiers show better high-temperature performance. However, it is worth noting that the current drive of the PiN rectifiers dramatically increases by rising the temperature, which makes them unstable at high temperature operations.

2.1.2 SiC Schottky Barrier Diodes (SBDs)

Schottky rectifiers are known as the principal semiconductor device in which the semiconductor-metal introduces the rectifying behavior (Fig. 2.3). SBDs are unipolar devices in which the current flow is due solely to majority carriers. Hence, the switching speed of SBDs is very fast and the reverse recovery time and loss is almost equal to zero. The difference between SiC bandgap and Schottky metal work function determines the SiC SBD forward voltage drop which is approximately 1 V. Finding a metal to make a proper Schottky without barrier inhomogeneity and a good uniformity, achieving low leakage current, and fabrication process to treat the SiC-metal interface are the main challenges for SiC SBD devices. Although a low-voltage drop is in favor of forward characteristic, the low Schottky barrier height results in a leaky device, which is not desirable in blocking mode. Therefore, one has to increase
the barrier and decrease the doping concentration of the drift layer to compensate the poor blocking behavior of these devices that sacrifices the on-resistance. It should be noted that raising the temperature lowers the current in forward mode whereas it dramatically increases the leakage current in reverse mode. This is due to the behavior of the Schottky metal-semiconductor junction [9].

2.1.3 SiC JBS and MPS rectifiers

As mentioned above, the PiN and SBD rectifiers have advantages and drawbacks in switching and DC operations. To benefit from both advantages and diminish the disadvantages, JBS and MPS designs with different technologies have been realized. As presented in Fig. 2.4, JBS and MPS structures are quite similar in which the p⁺ grids are introduced under the Schottky contacts to protect the Schottky contact from the high electric field of the drift layer. This slightly decreases the forward current while it significantly reduces the leakage current level. The main difference between the MPS and JBS rectifiers is the additional Ohmic contact to the p⁺ grids for the MPS rectifiers. This improves the surge current capability in high-current densities for the MPS rectifiers. The ratio of the Schottky contact area to the PiN area determines the conducting behavior of the device. Nowadays, these devices are of great interest for power electronic applications due to their low-voltage drop, fast switching speed,
surge current capability, low leakage current, and low reverse recovery loss. There is an increasing demand on JBS and MPS diodes for applications like automotive and traction due to the hybrid unipolar and bipolar operation of these devices [29]. This encourages providers to aim for higher voltage classes and improved on-state performance of their latest device generations. Different techniques have been developed and realized to optimize the JBS and MPS device characteristics. Currently, high-voltage JBS and MPS devices are commercially available [7], [8], [10]–[13]. Table 2.1 summarizes the most advanced SiC JBS and MPS diodes.

### 2.2 SiC Power Switch Devices

In this section, the main features of SiC FETs including the JFETs and MOSFETs as unipolar power switches are briefly described. In the continuation, the SiC-based bipolar switch devices e.g. bipolar junction transistors (BJTs), gate turn-off thyristors (GTOs), and insulated-gate bipolar gate transistors (IGBTs) are shortly discussed.

**Table 2.1. Summary of the state-of-the-art SiC rectifiers including the PiN, SBD, JBS, and MPS devices.**

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{BR}$ (kV)</th>
<th>$V_F$ (V)</th>
<th>$R_{ON}$ (mΩ·cm$^2$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBD</td>
<td>1.2</td>
<td>1.35 @ 200 A/cm$^2$</td>
<td>---</td>
<td>[30]</td>
</tr>
<tr>
<td>SBD</td>
<td>1.7</td>
<td>2 @ 126 A/cm$^2$</td>
<td>8.7</td>
<td>[31]</td>
</tr>
<tr>
<td>SBD</td>
<td>5</td>
<td>2.4 @ 25 A/cm$^2$</td>
<td>17</td>
<td>[32]</td>
</tr>
<tr>
<td>SBD</td>
<td>6.7</td>
<td>4 @ 60 A/cm$^2$</td>
<td>43</td>
<td>[33]</td>
</tr>
<tr>
<td>SBD</td>
<td>10</td>
<td>11.75 @ 20 A/cm$^2$</td>
<td>97.5</td>
<td>[34]</td>
</tr>
<tr>
<td>PiN</td>
<td>0.6</td>
<td>3.1 @ 100 A/cm$^2$</td>
<td>---</td>
<td>[35]</td>
</tr>
<tr>
<td>PiN</td>
<td>4.3</td>
<td>3.25 @ 100 A/cm$^2$</td>
<td>---</td>
<td>[36]</td>
</tr>
<tr>
<td>PiN</td>
<td>10-13</td>
<td>3.75 @ 100 A/cm$^2$</td>
<td>3.3</td>
<td>[37]</td>
</tr>
<tr>
<td>PiN</td>
<td>10</td>
<td>3.87 @ 100 A/cm$^2$</td>
<td>38</td>
<td>[38]</td>
</tr>
<tr>
<td>PiN</td>
<td>10</td>
<td>3.44 @ 100 A/cm$^2$</td>
<td>2.1</td>
<td>[39]</td>
</tr>
<tr>
<td>PiN</td>
<td>&gt;10</td>
<td>3.3 @ 100 A/cm$^2$</td>
<td>3.4</td>
<td>[40]</td>
</tr>
<tr>
<td>PiN</td>
<td>13</td>
<td>4.9 @ 100 A/cm$^2$</td>
<td>12</td>
<td>[41]</td>
</tr>
<tr>
<td>PiN</td>
<td>13</td>
<td>3.22 @ 100 A/cm$^2$</td>
<td>1.87</td>
<td>[42]</td>
</tr>
<tr>
<td>PiN</td>
<td>15</td>
<td>9.68 @ 100 A/cm$^2$</td>
<td>62</td>
<td>[43]</td>
</tr>
<tr>
<td>PiN</td>
<td>15</td>
<td>4.1 @ 100 A/cm$^2$</td>
<td>25.5</td>
<td>[44]</td>
</tr>
<tr>
<td>PiN</td>
<td>27</td>
<td>4.72 @ 100 A/cm$^2$</td>
<td>9.72</td>
<td>[42]</td>
</tr>
<tr>
<td>PiN</td>
<td>15</td>
<td>9.1 @ 100 A/cm$^2$</td>
<td>41.4</td>
<td>[45]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>1.2</td>
<td>1.2 @ 100 A/cm$^2$</td>
<td>3.1</td>
<td>[46]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>1.6</td>
<td>1.4 @ 100 A/cm$^2$</td>
<td>7.5</td>
<td>[47]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>1.7</td>
<td>1.6 @ 100 A/cm$^2$</td>
<td>2.9</td>
<td>[48]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>5</td>
<td>3.5 @ 100 A/cm$^2$</td>
<td>25.2</td>
<td>[49]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>6.5</td>
<td>4 @ 100 A/cm$^2$</td>
<td>---</td>
<td>[50]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>10</td>
<td>3.37 @ 100 A/cm$^2$</td>
<td>100</td>
<td>[41]</td>
</tr>
<tr>
<td>JBS &amp; MPS</td>
<td>&gt;10</td>
<td>4.5 @ 100 A/cm$^2$</td>
<td>~150</td>
<td>[51]</td>
</tr>
</tbody>
</table>

32
2.2.1 SiC FETs (JFETs and MOSFETs)

The schematic of a SiC JFET structure is shown in Fig. 2.5.a. The current passes through the channel, which can be pinched by applying the voltage to the gate to turn off the device. No gate oxide layer is required for JFETs and the process is rather simple compared to other SiC power switch devices. Normally-on JFETs provide lower on-resistance but have higher leakage current, which is not desirable for power applications. SiC JFETs are popular devices for mid-range voltage applications due to their high frequency switching, low switching loss, and simpler driver circuitry with voltage-controlled drivers. The advent of SiC enabled thinner drift layer for the desired breakdown voltage compared to silicon.

Currently, 4H-SiC power metal-oxide-semiconductor field effect transistors (MOSFETs) are the most attractive power switches on the market [14]. The MOSFETs are unipolar devices with high switching frequency. The SiC MOSFET on-resistance consists of the channel and drift layer. The main challenges in SiC MOSFETs are the gate oxide breakdown and the channel mobility. The oxide process is a key factor to minimize the SiC/SiO$_2$ interface charges, which degrades the channel mobility [52], [53]. Fig. 2.5.b and Fig. 2.5.c illustrate the schematic cross-sectional view of two different SiC MOSFET technologies known as DMOSFET and UMOSFET. Currently, 1200-V MOSFETs are commercially available from different companies [7], [8], [10]. There is an increasing demand for higher blocking capability of the SiC devices for the next generation of power electronics. Some progress have been made to extend the potential of SiC unipolar devices to high-voltage and ultra-high-voltage classes [54]–[56]. However, the high resistance of the lowly-doped drift region limits the performance of the unipolar devices, particularly for >15 kV devices. Hence, bipolar devices are going to play the main role in such voltage range due to the conductivity modulation of the drift region. This can significantly reduce the $R_{ON}$ of
Table 2.2. Some of the advanced power SiC FETs including the JFETs and MOSFETs.

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{BR}$ (kV)</th>
<th>$R_{ON}$ (mΩ⋅cm²)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFET</td>
<td>0.6</td>
<td>2.6</td>
<td>[57]</td>
</tr>
<tr>
<td>JFET</td>
<td>1.2</td>
<td>5</td>
<td>[58]</td>
</tr>
<tr>
<td>JFET</td>
<td>1.68</td>
<td>5.5</td>
<td>[59]</td>
</tr>
<tr>
<td>JFET</td>
<td>1.73</td>
<td>3.6</td>
<td>[60]</td>
</tr>
<tr>
<td>JFET</td>
<td>1.9</td>
<td>2.8</td>
<td>[61]</td>
</tr>
<tr>
<td>JFET</td>
<td>2.05</td>
<td>5.7</td>
<td>[62]</td>
</tr>
<tr>
<td>JFET</td>
<td>3.5</td>
<td>390</td>
<td>[63]</td>
</tr>
<tr>
<td>JFET</td>
<td>4.2</td>
<td>454</td>
<td>[64]</td>
</tr>
<tr>
<td>JFET</td>
<td>9</td>
<td>96</td>
<td>[65]</td>
</tr>
<tr>
<td>JFET</td>
<td>9.4</td>
<td>127</td>
<td>[66]</td>
</tr>
<tr>
<td>JFET</td>
<td>11</td>
<td>130</td>
<td>[67]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>0.95</td>
<td>8.4</td>
<td>[68]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>1.6</td>
<td>40</td>
<td>[69]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>2.6</td>
<td>200</td>
<td>[70]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>6.5</td>
<td>40</td>
<td>[54]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>10</td>
<td>123</td>
<td>[71]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>13.1</td>
<td>169</td>
<td>[56]</td>
</tr>
<tr>
<td>DMOSFET</td>
<td>15</td>
<td>250</td>
<td>[54]</td>
</tr>
<tr>
<td>UMOSET</td>
<td>1.4</td>
<td>74</td>
<td>[72]</td>
</tr>
<tr>
<td>UMOSET</td>
<td>3.3</td>
<td>9.4</td>
<td>[73]</td>
</tr>
<tr>
<td>VMOSFET</td>
<td>1.2</td>
<td>2</td>
<td>[74]</td>
</tr>
</tbody>
</table>

The device in forward conduction mode and take the SiC performance beyond the unipolar limits. Table 2.2 summarizes the properties of the state-of-the-art SiC FETs.

### 2.2.2 SiC BJTs

The schematic of the 4H-SiC vertical and lateral BJT structures is shown in Fig. 2.6. The BJT consists of two back-to-back pn diodes invented in 1947. The first SiC-based BJT was reported in 1977 [75] in which the pn junctions were epitaxially grown and etched by means of dry etching to form the emitter and base regions. In 2001, the first high-voltage SiC BJT with blocking voltage of 200 V and current gain of 4 was reported [76]. Two different approaches were used to form the emitter and base regions: (1) using ion implantation to form either the emitter or base or both regions; (2) using epitaxial emitter and base that were then isolated by dry etching. Since then, several studies to improve the performance of SiC BJTs have been done [76]–[137]. In spite of their excellent performance in high-voltage and high-temperature applications, the SiC BJTs have not received much attention. One of the main reasons is that the BJT is a current-controlled device while the market development is mostly focused on voltage-based drivers. However, as mentioned earlier, eventually power electronics have to switch to ultra-high-voltage bipolar devices, particularly with the recent development of the lifetime enhancement process, which will improve the conductivity modulation in the device drift layer. The properties of the most advanced SiC BJTs are summarized in Table 2.3.
2.2. SiC Power Switch Devices

Figure 2.6. Cross-sectional view of a 4H-SiC BJT with (a) vertical structure (b) lateral structure.

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{BR}$ (kV)</th>
<th>$\beta$</th>
<th>$R_{ON}$ (mΩ·cm²)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJT</td>
<td>3.2</td>
<td>28</td>
<td>28</td>
<td>[87]</td>
</tr>
<tr>
<td>BJT</td>
<td>2.8</td>
<td>55</td>
<td>4</td>
<td>[100]</td>
</tr>
<tr>
<td>BJT</td>
<td>2.8</td>
<td>52</td>
<td>6.8</td>
<td>[100]</td>
</tr>
<tr>
<td>BJT</td>
<td>1.8</td>
<td>40</td>
<td>4.4</td>
<td>[111]</td>
</tr>
<tr>
<td>BJT</td>
<td>2.3</td>
<td>35</td>
<td>4.5</td>
<td>[77]</td>
</tr>
<tr>
<td>BJT</td>
<td>6</td>
<td>---</td>
<td>28</td>
<td>[86]</td>
</tr>
<tr>
<td>BJT</td>
<td>23.5</td>
<td>7</td>
<td>321</td>
<td>[130]</td>
</tr>
<tr>
<td>BJT</td>
<td>10.5</td>
<td>75</td>
<td>110</td>
<td>[91]</td>
</tr>
<tr>
<td>BJT</td>
<td>2.7</td>
<td>132</td>
<td>4</td>
<td>[78]</td>
</tr>
<tr>
<td>BJT</td>
<td>15</td>
<td>139</td>
<td>579</td>
<td>PAPER I</td>
</tr>
<tr>
<td>BJT</td>
<td>5</td>
<td>40</td>
<td>33</td>
<td>PAPER II</td>
</tr>
<tr>
<td>BJT</td>
<td>5.65</td>
<td>44</td>
<td>18.8</td>
<td>PAPER III</td>
</tr>
<tr>
<td>BJT</td>
<td>5.85</td>
<td>40</td>
<td>28</td>
<td>PAPER IV</td>
</tr>
</tbody>
</table>

2.2.3 SiC Thyristors and GTOs

Power thyristors rapidly gained much interest for power applications and became commercially available in the 50s. The capability to function in both forward and reverse modes in the same range makes them a favorable device for high power switching operations. These devices can be triggered by a voltage, current, light, induction etc. to switch between on- and off states. Among several types of SiC thyristors, GTOs are the most attractive devices for SiC technology since the device can be switched from on-state to off-state under gate bias control, which is desirable for AC applications. The structure of a GTO is presented in Fig. 2.7.a. The 4H-SiC GTO benefits from high breakdown capability and high thermal conductivity. Also, it shows excellent turn-off behavior and high current capability. Moreover, it offers low forward voltage drop at high current densities, which results in low power dissipation in the on-state mode. However, the bipolar degradation originating from the material quality and the large turn-off gate drive are the main challenges for SiC GTOs in high power applications. Besides, the switching speed of the thyristors is limited due to the high amount of stored charges in the layers.
2.2.4 SiC IGBTs

The insulated-gate bipolar transistors (IGBTs) were firstly presented in 80s to marry a BJT with a MOSFET to benefit from the advantages of both technologies. Different types of MOSFET structures e.g. DMOSFET, UMOSFET, trench MOSFET etc. can be implied to realize the IGBTs. The structure of SiC n- and p-IGBTs based on a

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{BR}$ (kV)</th>
<th>$R_{ON}$ (mΩ·cm$^2$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTO</td>
<td>0.4</td>
<td>---</td>
<td>[138]</td>
</tr>
<tr>
<td>GTO</td>
<td>3.1</td>
<td>---</td>
<td>[139]</td>
</tr>
<tr>
<td>GTO</td>
<td>7.8</td>
<td>5.3</td>
<td>[140]</td>
</tr>
<tr>
<td>GTO</td>
<td>8.1</td>
<td>6</td>
<td>[141]</td>
</tr>
<tr>
<td>GTO</td>
<td>9</td>
<td>---</td>
<td>[142]</td>
</tr>
<tr>
<td>GTO</td>
<td>12.7</td>
<td>---</td>
<td>[141]</td>
</tr>
<tr>
<td>GTO</td>
<td>20</td>
<td>11</td>
<td>[143]</td>
</tr>
<tr>
<td>GTO</td>
<td>22.1</td>
<td>7.7</td>
<td>[71]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>2</td>
<td>500</td>
<td>[144]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>12.5</td>
<td>5.3</td>
<td>[145]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>13</td>
<td>22</td>
<td>[146]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>15</td>
<td>---</td>
<td>[147]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>16</td>
<td>11.3</td>
<td>[148]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>17</td>
<td>25.6</td>
<td>[149]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>20</td>
<td>177</td>
<td>[150]</td>
</tr>
<tr>
<td>n-IGBT</td>
<td>27</td>
<td>---</td>
<td>[151]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>2.7</td>
<td>161</td>
<td>[152]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>5.8</td>
<td>580</td>
<td>[153]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>7.5</td>
<td>26</td>
<td>[154]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>10.2</td>
<td>24</td>
<td>[155]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>12</td>
<td>18.6</td>
<td>[156]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>15</td>
<td>24</td>
<td>[145]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>15</td>
<td>41</td>
<td>[149]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>15</td>
<td>33</td>
<td>[151]</td>
</tr>
<tr>
<td>p-IGBT</td>
<td>15</td>
<td>148</td>
<td>[157]</td>
</tr>
</tbody>
</table>

Figure 2.7. Cross-sectional view of a high-voltage SiC (a) GTO, (b) n-IGBT, and (c) p-IGBT.
DMOSFET structure are presented in Fig. 2.8.b and 2.8.c, respectively. As discussed earlier, the BJTs offer a low forward voltage drop and on-state characteristics. A high current gain is required to avoid a complicated drive circuit. Back in the years, BJTs were suffering from relatively low current gain leading to lose the attention from the markets. Hence, the IGBTs were proposed to monolithically integrate a BJT with a MOSFET to make a voltage-controlled device with low on-resistance. In recent years, progress have been made to develop ultra-high-voltage SiC IGBTs. Thanks to the maturity of the epitaxial growth processes to grow thick n- and p-epitaxial layers [157] and also some novel fabrication technologies [144], [148], [150], [158], both SiC n-IGBTs and p-IGBTs have been realized.

Table 2.5. Some of the most recent reported GaN-based power devices.

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{BR}$ (kV)</th>
<th>$R_{ON}$ (mΩ·cm²)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlGaN/GaN HEMT</td>
<td>1050</td>
<td>3.4</td>
<td>[159]</td>
</tr>
<tr>
<td>AlGaN/GaN HEMT</td>
<td>900</td>
<td>---</td>
<td>[160]</td>
</tr>
<tr>
<td>AlGaN/GaN HFET</td>
<td>8300</td>
<td>200</td>
<td>[161]</td>
</tr>
<tr>
<td>AlGaN/GaN</td>
<td>1100</td>
<td>1.5</td>
<td>[162]</td>
</tr>
<tr>
<td>AlGaN/GaN</td>
<td>1900</td>
<td>2.2</td>
<td>[163]</td>
</tr>
<tr>
<td>AlGaN/GaN</td>
<td>1600</td>
<td>3.4</td>
<td>[164]</td>
</tr>
<tr>
<td>AlGaN/GaN</td>
<td>10400</td>
<td>200</td>
<td>[165]</td>
</tr>
<tr>
<td>InAlN/GaN MOSHEMTs</td>
<td>3000</td>
<td>4.3</td>
<td>[166]</td>
</tr>
<tr>
<td>GaN on Si</td>
<td>700</td>
<td>4.5</td>
<td>[167]</td>
</tr>
<tr>
<td>GaN on Diamond</td>
<td>1100</td>
<td>3.4</td>
<td>[168]</td>
</tr>
<tr>
<td>AlGaN/GaN HEMT</td>
<td>1500</td>
<td>5.3</td>
<td>[169]</td>
</tr>
<tr>
<td>GaN polarization super HFET</td>
<td>1100</td>
<td>6.1</td>
<td>[170]</td>
</tr>
<tr>
<td>InAlN/AlN/GaN MISHEMT</td>
<td>460</td>
<td>2.3</td>
<td>[171]</td>
</tr>
<tr>
<td>AlGaN/GaN HEMT</td>
<td>1100</td>
<td>1.8</td>
<td>[172]</td>
</tr>
<tr>
<td>AlGaN/GaN on Si HEMT</td>
<td>1410</td>
<td>2.3</td>
<td>[173]</td>
</tr>
<tr>
<td>AlGaN/GaN SBD</td>
<td>1500</td>
<td>3.37</td>
<td>[174]</td>
</tr>
<tr>
<td>Vertical GaN PN Diode</td>
<td>3700</td>
<td>2.95</td>
<td>[175]</td>
</tr>
<tr>
<td>Vertical AlGaN/GaN 2DEG</td>
<td>1500</td>
<td>2.2</td>
<td>[176]</td>
</tr>
<tr>
<td>Al2O3/AlGaN/GaN-on-Si MISFET</td>
<td>860</td>
<td>1.2</td>
<td>[177]</td>
</tr>
<tr>
<td>AlGaN/GaN lateral SBD on Si</td>
<td>1900</td>
<td>5.1</td>
<td>[178]</td>
</tr>
<tr>
<td>Vertical GaN pn</td>
<td>2600</td>
<td>1</td>
<td>[179]</td>
</tr>
<tr>
<td>Vertical GaN pn</td>
<td>3900</td>
<td>0.9</td>
<td>[180]</td>
</tr>
<tr>
<td>Vertical GaN-on-Si pn</td>
<td>500</td>
<td>0.8-1</td>
<td>[181]</td>
</tr>
<tr>
<td>GaN-on-GaN pn</td>
<td>1000</td>
<td>3</td>
<td>[182]</td>
</tr>
<tr>
<td>GaN-on-GaN pn</td>
<td>3480</td>
<td>0.95</td>
<td>[183]</td>
</tr>
<tr>
<td>GaN MOSFET</td>
<td>1200</td>
<td>1.8</td>
<td>[184]</td>
</tr>
<tr>
<td>GaN polarization super FET</td>
<td>4000</td>
<td>7</td>
<td>[185]</td>
</tr>
<tr>
<td>GaN polarization super FET</td>
<td>1500</td>
<td>2</td>
<td>[185]</td>
</tr>
<tr>
<td>Vertical GaN Schottky</td>
<td>1100</td>
<td>0.71</td>
<td>[186]</td>
</tr>
<tr>
<td>Vertical GaN MPS</td>
<td>2000</td>
<td>3.1</td>
<td>[187]</td>
</tr>
<tr>
<td>Normally-off Vertical GaN FET</td>
<td>1700</td>
<td>1</td>
<td>[188]</td>
</tr>
<tr>
<td>InAlN/GaN HEMT</td>
<td>2300</td>
<td>4.6</td>
<td>[189]</td>
</tr>
<tr>
<td>Vertical GaN pn</td>
<td>4700</td>
<td>1.7</td>
<td>[190]</td>
</tr>
<tr>
<td>Vertical GaN pn</td>
<td>4000</td>
<td>2.8</td>
<td>[191]</td>
</tr>
<tr>
<td>GaN-on-GaN pn</td>
<td>1400</td>
<td>0.12</td>
<td>[192]</td>
</tr>
</tbody>
</table>

37
the SiC IGBTs takes them beyond the SiC unipolar limits, it seems that the wafer-scale development of SiC IGBTs for industrial applications takes longer. The properties of the most advanced SiC GTOs and IGBTs are summarized in Table 2.4.

As mentioned earlier, in recent years GaN-based devices gained much interest as the main competitor for SiC devices, particularly in the low-voltage and mid-voltage class [193]. Table 2.5 summarizes the properties of the state-of-the-art GaN-based devices. In spite of the significant progress in development of GaN devices and their superior performance, GaN technology is still suffering from the material quality, process cost, immature fabrication process, and low thermal conductivity of GaN for power applications.

Fig. 2.8 compares the $V_{BR}$-$R_{ON}$ characteristic of the most advanced SiC power devices. As can be seen, SiC bipolar performance is extended beyond the SiC limits due to the conductivity modulation in the drift region. This is mainly owing to the recent progress in SiC epitaxial process to grow high-quality thick a- and p-epilayers and lifetime enhancement process. It is worth noting that the minimum on-resistance of the device is limited to the resistivity of the Ohmic contacts, which is about 0.1 m$\Omega$·cm$^2$. A higher contact resistivity of 0.1 m$\Omega$·cm$^2$ can result in a low injection and high on-resistance for high power devices. Therefore, there is a demand to improve the Ohmic contact technology to SiC, particularly for the p-Ohmic contact.

![Figure 2.8. Comparison of the $V_{BR}$-$R_{ON}$ characteristic of the most advanced SiC and GaN power devices.](image-url)
2.3 Development of SiC BJTs

Ultra-high-voltage SiC bipolar devices seem to be the game-changers in the future of power electronics. The SiC BJT technology has been improved and developed over the years. As mentioned above, high-voltage and ultra-high-voltage SiC BJTs with superb blocking and conducting electrical characteristics have been reported. The simplicity of the fabrication process, absence of gate oxide, low on-resistance, and the temperature stability of the device are the main advantages of 4H-SiC BJTs. As a result of the continuous development of the implantation-free process at KTH, 4H-SiC BJTs have been developed for many years and their excellent electrical characteristics are improved and verified for high-voltage and ultra-high-voltage [15], [16]. To benefit from the bipolar advantages, it is essential to use lifetime enhancement process to achieve a better $V_{BR}$-$R_{ON}$ trade-off.

2.4 BJT Principle

Fig. 2.9.a and 2.9.b schematically illustrate BJTs with npn and pnp configurations. BJTs are three-terminal switches consisting of two np and pn junctions. The npn type is more common due to higher mobility of the n-type. In this thesis, what is simply referred as BJT is meant to be an npn BJT. The p-base region is surrounded by the n-emitter and n-collector regions on the sides. As mentioned earlier, the BJT is a bipolar device in which both minority and majority carriers are involved in the current flow. As shown in Fig. 2.10 the highly doped n-emitter injects the electrons in the base region. In the forward mode, the electrons partially recombine in the base and the reverse-biased n-collector collects in most of the injected electrons.

Depending on the bias of the emitter-base and collector-base layers, the BJT function changes. Table 2.6 shows the biasing condition and the corresponding operation modes. Among these modes, the forward, reverse, and the saturation modes are of great interest for analog electronics, whereas the forward and reverse modes are attractive for power electronics. In the forward mode, the ratio of the $I_C$ to $I_B$ is known as current gain and the ratio of the $I_C$ to $I_E$ is known as common-base current gain ($\alpha$).

![Electrical schematic symbol of a (a) npn and (b) pnp BJT.](image-url)
Table 2.6. The biasing conditions and corresponding operating modes of a BJT.

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Emitter-base</th>
<th>Collector-base</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward (Active)</td>
<td>Forward</td>
<td>Reverse</td>
</tr>
<tr>
<td>Saturation</td>
<td>Forward</td>
<td>Forward</td>
</tr>
<tr>
<td>Reverse (Cut-off)</td>
<td>Reverse</td>
<td>Reverse</td>
</tr>
<tr>
<td>Reverse Active</td>
<td>Reverse</td>
<td>Forward</td>
</tr>
</tbody>
</table>

Figure 2.10. Current components of a npn BJT in the forward conduction mode.

The total currents between the emitter, base, and collector can be related as below:

\[
I_C = \beta I_B \tag{2.1}
\]

\[
I_E = I_C + I_B = (\beta + 1) I_B \tag{2.2}
\]

\[
\alpha = \frac{I_C}{I_E} \tag{2.3}
\]

\[
\alpha = \frac{I_C}{I_C + I_B} = \frac{\beta}{\beta + 1} \tag{2.4}
\]

where the \( I_E \), \( I_C \), and \( I_B \) are the emitter, collector, and the base currents, where the \( I_B \) and \( I_C \) are usually considered as the input and output currents, respectively.

The current components inside a SiC BJT in the forward mode is shown in Fig. 2.10. The highly-doped emitter layer injects the electrons into the p-base layer, and the base injects the holes into emitter region. Most of the injected electrons from the emitter pass through the base and diffuse into the collector region whereas small portion of electrons recombine with holes in the base region. The emitter, base, and collector current can be calculated as follows:

\[
I_E = I_{nE} + I_{pE} + I_R \tag{2.5}
\]

\[
I_B = I_{pE} + I_{RB} + I_{RS} + I_R + I_{CO} \tag{2.6}
\]

\[
I_C = I_{nE} - I_{RB} - I_{RS} + I_{CO} \tag{2.7}
\]

where the currents are as follows:
\( I_{dE} \): Injection of minority carrier electrons to the base.
\( I_{pE} \): Injection of minority carrier holes to the emitter.
\( I_{R} \): Recombination current in the space charge region (SCR) of the emitter-base junction.
\( I_{RB} \): Bulk recombination current in the base region.
\( I_{RS} \): Surface recombination current at the SiC interface.
\( I_{C0} \): The generation of carriers in the reverse-biased base-collector junction. It is negligible below avalanche breakdown.

The Equation 2.3 can be rewritten as below:

\[
\alpha = \frac{I_C}{I_E} = \frac{I_C}{I_{nC}} \times \frac{I_{nC}}{I_{nE}} \times \frac{I_{nE}}{I_E} = \gamma_C \times \alpha_T \times \gamma_E
\]  

(2.8)

where \( \gamma_C \), \( \alpha_T \), and \( \gamma_E \) are known as the collector efficiency, base transport factor, and emitter injection efficiency, respectively. The emitter efficiency depends upon the design of emitter and base regions and can be calculated as follow:

\[
\gamma_E = \frac{I_{nE}}{I_E} = \left(1 + \frac{N_B W_B D_E}{N_E W_E D_B}\right)^{-1}
\]

(2.9)

where \( N \), \( W \), and \( D \) are the doping concentration, width, and minority carrier diffusion constant of the regions. Therefore, it is desirable to design the BJT with highly doped emitter layer and lowly doped thin base layer to approach the emitter injection efficiency of 1 and consequently achieve a high current gain. However, a too lowly-doped base layer can result in base punch-through and premature breakdown voltage, which will be described in Chapter 3. As was already mentioned above, small portion of injected electrons from the emitter recombine in the base region, which decreases the collector current. The ability of injected electrons to diffuse to the base without recombining is defined by \( \alpha_T \). The recombination rate in the base region can be calculated from the following equation:

\[
\alpha_T = \frac{1}{\cosh(W_B/L_n)}
\]

(2.10)

where \( L_e \) is the electron diffusion length in the base. For a lowly-doped base layer, the \( L_e \) is much larger than \( W_B \), and the base transport can be estimated as:

\[
\alpha_T = 1 - \frac{W_B^2}{2L_n^2}
\]

(2.11)

In the forward mode, the collector-base is biased in reverse. Hence, the collector collects almost the electrons transported through the base region, which makes the \( \gamma_C \) value close to 1.
Chapter 3. SiC BJT Design Consideration

At KTH, we have developed 4H-SiC BJTs from low-voltage to ultra-high voltage ranges in different sizes and current rates [15]–[17], [194]. To fully gain from the potential of 4H-SiC material and approach the material limits, it is necessary to enhance the material quality and properties, improve the fabrication process, and optimize the device design. In this chapter, we focus on the design consideration of 4H-SiC BJTs whereas the fabrication process will be discussed in details in Chapter 4. A comprehensive design optimization and investigation for 4H-SiC BJTs is performed. The measurement results from each batch are used to optimize and find the optimum design for the next batch by means of TCAD simulation. The final design is implemented on large-area BJTs to tailor the high-voltage and high-current characteristics.

3.1 Application and Device Specification

The first step in device design is to know the device specification, particularly the desired current-rating and blocking capability. The current-rating mainly determines the device active area. The edge termination is surrounding the conduction area to terminate the electric field and ensure the blocking capability. The total device size is the active area plus the termination area. A higher ratio of the active area to the total die size is an important factor for a more efficient design leading to a lower cost per chip. This is more important for higher voltage classes in which a much wider termination is required. Therefore, to industrialize the high-voltage and ultra-high-voltage devices, it is essential to fabricate larger devices. Currently, the quality of the SiC bulk material and epitaxial process as well as the fabrication yield is still one of the main limiting factors to realize large-size (> 1 cm\(^2\)) high-voltage devices. In addition, there are always some variations in the epitaxial growth and uncertainties in the fabrication process like the etching step. Hence, the characterization and measurement results from the epilayer growth and the fabrication process specifications like the etching profiles, surface passivation properties, and metal contacts behavior are the feedbacks to calibrate the simulation and modeling and optimize the device design.
These variations and uncertainties are critical considerations for the device design procedure to tailor the targeted specifications with a high yield.

The current naturally flows in the least resistive and shortest distances. In a SiC power BJT, the emitter current flow is close to the edge of the emitter resulting in emitter current crowding (see Fig. 3.1). The fabrication process, the cell scaling and geometry, and the device layout influence the current distribution and can improve the emitter crowding effect.

To realize a SiC power BJT, the base and emitter regions can be formed either by etching epitaxial layers or by implanting ions in the epilayers, which each has advantages and drawbacks [195]. In the fully epitaxial process, the emitter and base regions are formed by dry etching of SiC epilayers. The fabrication process is rather simple and cheap. The ion implantation makes defects in the epilayers, which causes degradation. Also, a high-temperature annealing (~1600 °C) is required to activate the implanted ions for the full activation of the implanted ions. This affects the carrier lifetime in the epilayers leading to reduction of the maximum current gain. On the other hand, the dry etching of the epilayers damages the SiC surface. This introduces defects and results in severe increase of the interface charges, particularly at the etched mesa sidewalls, which significantly degrades the forward performance as well as the blocking behavior. It is known that the emitter-base spacing changes the amount of surface charge density. Therefore, the cell pitch is limited, either by the etching profile and fabrication process limits or the mesa sidewall charge density. Therefore, a high-quality etching and surface passivation are required for high-performance 4H-SiC BJTs. The fabrication process and the enhanced surface treatment is described in Chapter 4.

Another approach is to perform a shallow high-dose p+ implanted layer underneath the p-type metal contact to improve the contact resistance. This introduces defects around the p+ implanted regions that increases the recombination rate and degrades the current gain. In this thesis, we selected the fully epitaxial approach. All
design consideration in conduction and blocking modes from epilayers, fabrication steps, and device layout are modified to be fully free of ion implantation process. For a SiC high-voltage BJT, the collector sustains the high-voltage. For the lateral low-voltage BJT, a highly-doped n-layer is epitaxially grown as the buried collector. The emitter and base layers mostly play role in the forward performance like the current gain. The BJT characteristics, including the maximum current gain, specific on-resistance, and current density depend on the doping concentration and thickness of these epilayers. Moreover, the device cell geometry and scaling affect the device behavior. Finally, the device layout design should be optimized to use the area efficiently. Hereby, the design consideration is described in detail and the characterization results of the realized devices will be presented in Chapter 5.

3.2 Design of Epitaxial SiC BJT

It is known that the epitaxial pn junctions offer much higher charge injection than the implanted pn junctions [9], [195]. Therefore, a full epitaxial process is more suitable to form the emitter-base pn junction. In this thesis, we will exclusively focus on the design consideration of the full epitaxial 4H-SiC BJTs due to their superior performance and a mature in-house fabrication process technology.

3.2.1 Collector Region

As already mentioned, the collector, also known as the drift region, sustains the blocking voltage in 4H-SiC vertical BJTs. Fig. 3.2.a shows a basic pn junction and the electric field profile in the layers in reverse condition, assuming that the depletion occurs on the n−side. The reverse voltage can be increased until the avalanche breakdown occurs at the critical electric field of SiC. The integral of the electric field with triangular profile at this point determines the breakdown voltage (Equation 3.1). This is a so-called non-punch-through (NPT) design.

\[
V_{BR} = \frac{E_c \cdot x}{2}
\]  

(3.1)

In another approach called punch-through (PT) design, the electric field is terminated by an n+ region underneath the drift as shown in Fig. 3.2.b. In the PT design, the depletion region reaches the n+ layer before the breakdown occurs in the drift region. This results in a different electric field distribution in the drift region, and thus the NPT triangular electric field profile becomes trapezoidal for the PT design. The trapezoidal electric field profile transforms to a rectangular-shape for a higher doping concentration of the drift layer. Equation 3.2 represents the breakdown voltage for the PT design when the p-region is biased at zero.
Figure 3.2. The simplified electric field distribution in a pn junction for a (a) non-punch-through (NPT) design and (b) punch-through (PT) design.

\[ V_B = E_C \cdot d - \frac{qN_D d^2}{2\varepsilon_{SiC}} \quad (3.2) \]

where \( N_D \) is the doping concentration of the drift layer and \( \varepsilon_{SiC} \) is the permittivity of the silicon carbide. The specific on-resistance of the drift layer can be calculated by:

\[ R_{ON} = \frac{d}{qN_D \mu_n} \quad (3.3) \]

where \( \mu_n \) is the electron mobility in the collector layer. By elimination of \( N_D \) from Equation 3.2 and 3.3, the optimum thickness of the collector to reach minimum \( R_{ON} \) and the minimum \( R_{ON} \) can be achieved from Equation 3.4 and 3.5, respectively.

\[ d_{optimum} = \left( \frac{3}{2} \right) \frac{V_B}{E_C} \quad (3.4) \]

\[ R_{ON,min} = \left( \frac{27}{8} \right) \frac{V_B^2}{\mu_n \varepsilon_{SiC} E_C} \quad (3.5) \]

### 3.2.2 Base Region

The base is the intermediate layer between the emitter and collector. The design of the base layer is very important for the performance of a SiC BJT. In conduction mode, the base directly affects the current gain. To obtain a high current gain, the thickness of the base layer should be lower than the minority carrier diffusion length \( L_n \). \( L_n \) depends upon the minority carrier lifetime in the base layer \( (\tau_n) \) which can be reduced for higher doping concentration. Therefore, a thinner base with lower doping concentration is favorable to obtain higher current gain. On the other hand, a high enough dose of the base layer is required to support high electric field in the blocking mode and avoid the emitter-collector punch-through. Moreover, additional condition
is considered in our implantation-free design since the edge termination is formed by multi-step etching of the base layer. Hence, a thicker base layer for the controlled multi-step etched process is needed. This results in better control of the etching to obtain higher uniformity and eliminates the risk of the over-etching through a thin base layer. Finally, a lower-resistive base layer to obtain higher switching performance is desirable. One has to consider the trade-off between a lower-dose for the conducting mode and a higher-dose base layer for the blocking mode to meet the conditions. A dose of $\sim 10^{13}$ cm$^{-2}$ is the optimum value for the base layer.

### 3.2.3 Emitter Region

The emitter layer injects the current to the collector and base. Even though a highly-doped layer is favorable to have a low-resistive n-Ohmic contact, however, a too highly-doped emitter layer results in bandgap narrowing. Therefore, the emitter layer with doping concentration of $10^{18}$-$10^{19}$ cm$^{-3}$ is chosen, which is capped by a thin n$^{++}$ ($\sim 3 \times 10^{19}$ cm$^{-3}$) layer to obtain low-resistive n-Ohmic contact. On the other hand, a too thick emitter layer causes complexity in the fabrication process. Also, a higher emitter mesa side-wall results in more defects after the emitter dry etching. This leads to higher recombination of the electron and hole carriers that degrades the current gain. As mentioned earlier, an epitaxial grown emitter layer is preferred due to much higher injection efficiency and lower defects. Considering these points, the optimum thickness of $1 \mu m$ – $2 \mu m$ for the emitter layer is selected. The schematic cross-sectional view of a 4H-SiC BJT cell is illustrated in Fig. 3.

### 3.3 Scaling and Dimension Effects

It is known that the dimension of the emitter and base influences the forward characteristics of 4H-SiC BJTs [112], [196]. Hereby, the effect of emitter and base dimensions and the cell pitch is investigated and optimized to find the best trade-off between current density, maximum current gain, and specific on-resistance.

#### 3.3.1 Emitter Width

We comprehensively investigated the scaling effect of the emitter cells on the forward performance of the 4H-SiC BJTs [PAPER II, V, VI]. It is presented that a wider emitter results in a higher maximum current gain, though leading to higher on-resistance and lower current density. The emitter cell dimensions, cell geometries, and cell pitch are dependent. Therefore, we analyzed the effect of emitter cell scaling for different geometries in order to find the optimum layout design for the 4H-SiC BJTs. The influence of the emitter width on the maximum current gain of the SiC BJTs with different emitter finger designs is shown in Fig. 3.4. Although, wider emitter fingers
3.3.2 Emitter Length

The influence of the emitter length and emitter finger width on the maximum current gain of the interdigitated 4H-SiC BJTs is shown in Fig. 3.5. As can be seen, a longer emitter finger increases the maximum current gain, though it saturates for too long emitter fingers due to the voltage drop along the finger [100]. This might be due to the periphery to area ratio, which changes the density of sidewalls and consequently the recombination rate in the device. A higher current gain is obtained for the BJTs with wider emitter fingers whereas a higher maximum current gain and current density is achieved for longer emitter fingers. This behavior saturates for too wide and too long
3.3.3 Emitter-Base Spacing

As described earlier, the emitter mesa is formed by dry etching process. The etching process damages the emitter mesa sidewalls and the p-layer base surface, which influences the maximum current gain in the 4H-SiC BJTs. The sacrificial oxidation is performed to improve the surface roughness. The passivation oxide covers the distance between the emitter n-Ohmic and base p-Ohmic contacts ($W_n$-$W_p$). The major part of carrier recombination occurs in this area, particularly at the oxide/SiC surface. The sidewall profile, etching process, surface profile, and the area between the base and emitter covered by the passivation oxide determine the surface defect density in the device. This consequently degrades the maximum current gain. For a comprehensive investigation, various BJTs with different cell geometries and emitter-base spacing were designed and fabricated. Fig. 3.6 represents the influence of the emitter-base spacing on the maximum current gain of 4H-SiC BJTs with different cell geometries. As expected, the lowest maximum current gain is achieved for the tightest cell pitch. This is mainly due to the density of defects and the total recombination in
the device. The best result is measured for the emitter-base distance of 6 μm. It should be noted that the optimum emitter-base spacing changes for different geometries. The main reason is that the periphery to area ratio varies for different geometries. This leads to variation of the surface defect density, which directly affects the maximum current gain.

### 3.4 Unit Cell Design

To perform a comprehensive study to find an optimum design for the 4H-SiC BJTs, we designed and fabricated different cell geometries including hexagon, square, circle, and triangle shapes. The main goal is to have the highest possible cell pitch at a reasonable current gain. This leads to higher current density due to the more efficient usage of the area. Fig. 3.7 illustrates the realized 4H-SiC BJTs with different emitter cell geometries. Several BJTs with the area of 300×300 μm² and different widths of 10 μm to 50 μm are realized. Fig 3.8 depicts the measured on-resistance and current
density versus the maximum current gain of devices. It is apparent that the hexagon-cell geometry show 42% higher current density and 21% lower specific on-resistance at a given maximum current gain compared to the interdigitated finger. On the other hand, the maximum current gain is slightly higher for the interdigitated fingers. This might be due to the different geometry and higher density of sidewalls for the new designs. One could expect to reach higher maximum current gain by further widening of hexagon and square cells.

Moreover, square- and circle-cell geometries with diagonally-aligned cells were designed and fabricated (see Fig. 3.9). No significant difference is observed for different cell alignments. Since the cell width, cell pith, and number of cells are identical, the cell alignment does not affect the density of surface charges resulting in comparable performance. One could expect to observe different current distribution along the device that needs further investigation.

Figure 3.7. The optical microscopic images of the 4H-SiC BJTs with different emitter cell geometries. All devices have identical forward area size of 300×300 μm².

Figure 3.8. (a) The current density and (b) the on-resistance versus the maximum current gain for 4H-SiC BJTs with different geometries compared to the interdigitated design.
3.5 Edge Termination

As described earlier, a desirable high voltage SiC device should withstand a large reverse voltage at minimal leakage current. The so-called blocking voltage is the maximum reverse voltage that the device can sustain, which is determined by the material properties and the device design. The breakdown behavior of power devices is mainly attributed in the following mechanisms:

- Punch-through of the base region in a BJT, MOSFET, IGBT, or thyristor
- Avalanche breakdown in a reverse-biased pn or Schottky junction, either as a discrete rectifier or as a part of a switching transistor or thyristor
- Excessive leakage current in a reverse-biased pn or Schottky junction
- Excessive electric field in the oxide of an MOS-based power device such as a MOSFET or IGBT

Although, the SiC critical electric field determines the theoretical breakdown voltage, the electric field crowding can occur inside the device in operational blocking conditions. The electric field stress results in early breakdown at sensitive regions of the device and deteriorates the device performance. This declines the efficiency of the device without using the full potential of the SiC material. The electric field crowding usually happens at the corner of a mesa or the asymmetric points like etched or implanted regions inside the drift region. To avoid this, designs so-called edge termination techniques have been proposed to share the electric field stress along the device and modulate the high field peaks. The edge termination expands the depletion region along the device, and hence a larger die size is required. This becomes an important factor for high- and ultra-high-voltage devices in which the termination can occupy a major portion of the die. Few main factors are known to evaluate the edge termination design as following:
1. The termination efficiency that is the ratio of estimated breakdown to the theoretical breakdown voltage for a specific doping concentration and thickness of the drift
2. The achieved blocking voltage capability per each μm of the drift epilayer
3. The total termination length, which determines the ratio of the inactive area of the device to the total die size
4. A wide process window to increase the fabrication yield
5. The process complexity in terms of fabrication process and number of lithographic steps

The total cost to realize a device highly depends upon the total die size, fabrication process, the epitaxial material, and the process yield. Some edge termination designs show a high efficiency at a certain dose, but a slight process variation can significantly affect their performance. It is worth noting that a wide process window along with a process simplicity is rather important factor for the termination design.

Edge termination techniques like floating guard rings [198]–[203], multi-zone JTEs [204]–[209], bevel edge termination [210], space modulated [211], and hybrid or combined rings+JTE [212]–[215] are using ion implantation with certain doses to change the electric field distribution in the drift region. In another approach, ion implantation-free termination techniques are designed in which the remaining dose of the p-layer is gradually decreasing from the innermost toward the outermost of the device [140], [216]–[218]. At KTH, a double-step etched JTE has been designed and successfully implemented on 4.3 kV 4H-SiC PiN diodes [36] and 2.8 kV 4H-SiC BJTs [100]. To realize 4.5-kV and 15-kV class BJTs, the same design concept is employed. By using the TCAD simulation, different multi-step etched termination techniques are implemented in order to improve the termination efficiency and increase the breakdown voltage [PAPER I-IV]. Table 3.1 compares some of the recent reported termination techniques in high-voltage and ultra-high-voltage devices. Moreover, it should be noted that the edge termination together with a field stopper terminates the high electric field inside the device to protect the neighbor circuits or elements from the high-voltage device. A high electric field close to the outermost edge of the device can destroy the polyimide or oxide passivation layer or the molding material in the package. This can result in an early breakdown, and thus shorten lifetime of the device.

3.6 Current Distribution

The current distribution in power devices is an important factor to increase the device lifetime and improve the switching performance. Current crowding at some corners of the device generates hot spots inside the device that leads to reliability issues and performance degradation. In a power SiC BJT, the base is the input that
Chapter 3. SiC BJT Design Consideration

### Table 3.1. Summary of Comparison between Recent Reported Edge Termination Techniques in Most Advanced High-Voltage and Ultra-High-Voltage SiC Devices.

<table>
<thead>
<tr>
<th>Termination [Ref.]</th>
<th># of Lithographic Step / Ion Implantation</th>
<th>( V_{br} ) (kV)</th>
<th>( V/\mu m )</th>
<th>Efficiency</th>
<th>Termination Length / Drift Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double-JTE [36]</td>
<td>2 / No</td>
<td>4.3</td>
<td>148</td>
<td>80 %</td>
<td>100 ( \mu m ) / 29 ( \mu m )</td>
</tr>
<tr>
<td>Double-JTE [100]</td>
<td>2 / No</td>
<td>2.8</td>
<td>112</td>
<td>75 %</td>
<td>100 ( \mu m ) / 25 ( \mu m )</td>
</tr>
<tr>
<td>Graded-Etched [140]</td>
<td>4 / No</td>
<td>7.8</td>
<td>130</td>
<td>96 %</td>
<td>350 ( \mu m ) / 60 ( \mu m )</td>
</tr>
<tr>
<td>Etched rings JTE [217]</td>
<td>1 / No</td>
<td>6.3</td>
<td>105</td>
<td>78 %</td>
<td>200 ( \mu m ) / 60 ( \mu m )</td>
</tr>
<tr>
<td>3-step JTE [218]</td>
<td>3 / No</td>
<td>7.6</td>
<td>127</td>
<td>90 %</td>
<td>300 ( \mu m ) / 60 ( \mu m )</td>
</tr>
<tr>
<td>MD-JTE [80]</td>
<td>2 / No</td>
<td>5</td>
<td>113</td>
<td>80 %</td>
<td>210 ( \mu m ) / 44 ( \mu m )</td>
</tr>
<tr>
<td>ST-JTE [88]</td>
<td>2 / No</td>
<td>5.85</td>
<td>133</td>
<td>93 %</td>
<td>185 ( \mu m ) / 44 ( \mu m )</td>
</tr>
<tr>
<td>O-JTE [194]</td>
<td>4 / No</td>
<td>15</td>
<td>120</td>
<td>---</td>
<td>900 ( \mu m ) / 125 ( \mu m )</td>
</tr>
<tr>
<td>O-JTE [94]</td>
<td>3 / No</td>
<td>5.65</td>
<td>128</td>
<td>92 %</td>
<td>200 ( \mu m ) / 44 ( \mu m )</td>
</tr>
<tr>
<td>SM-JTE [130]</td>
<td>2 / Yes</td>
<td>23.5</td>
<td>126</td>
<td>78 %</td>
<td>500 ( \mu m ) / 186 ( \mu m )</td>
</tr>
<tr>
<td>Rings [151]</td>
<td>2 / Yes</td>
<td>27.5</td>
<td>120</td>
<td>---</td>
<td>1500 ( \mu m ) / 230 ( \mu m )</td>
</tr>
<tr>
<td>JTE+Rings [203]</td>
<td>2 / Yes</td>
<td>&gt;14</td>
<td>140</td>
<td>&gt; 90 %</td>
<td>500 ( \mu m ) / 100 ( \mu m )</td>
</tr>
<tr>
<td>MFZ-JTE [208]</td>
<td>1 / Yes</td>
<td>&gt; 10</td>
<td>84</td>
<td>88 %</td>
<td>500 ( \mu m ) / 120 ( \mu m )</td>
</tr>
<tr>
<td>Multi-Zone [209]</td>
<td>1 / Yes</td>
<td>6.4</td>
<td>152.4</td>
<td>93 %</td>
<td>250 ( \mu m ) / 42 ( \mu m )</td>
</tr>
<tr>
<td>Bevel-JTE [210]</td>
<td>1 / Yes</td>
<td>1.6</td>
<td>155</td>
<td>95 %</td>
<td>65 ( \mu m ) / 10 ( \mu m )</td>
</tr>
<tr>
<td>SM-JTE [211]</td>
<td>2 / Yes</td>
<td>16.4</td>
<td>137</td>
<td>94 %</td>
<td>600 ( \mu m ) / 120 ( \mu m )</td>
</tr>
<tr>
<td>Hybrid [212]</td>
<td>2 / Yes</td>
<td>5.45</td>
<td>136</td>
<td>&gt;99 %</td>
<td>200 ( \mu m ) / 40 ( \mu m )</td>
</tr>
<tr>
<td>Combined [215]</td>
<td>2 / Yes</td>
<td>1.8</td>
<td>120</td>
<td>&gt; 90 %</td>
<td>100 ( \mu m ) / 15 ( \mu m )</td>
</tr>
</tbody>
</table>

Figure 3.10. The layout designs of the small-area 4H-SiC BJTs with different topologies.

feeds the emitter. As described in Chapter 2, the base and emitter Ohmic metal contacts are covered by a thick metal layer to improve the current spreading inside the device. However, in large-area high-current BJTs, it is desirable to design a symmetric layout to have uniformly-distributed current path and consequently a low voltage drop. Different layout designs have been modelled and studied and it has been found that the center-base layout design provides significantly more uniform current distribution in 4H-SiC high current BJTs [219]. Hereby, 4H-SiC BJTs with conventional corner-base, edge-base, and center-base layout designs are fabricated on square-cell
geometries (Fig. 3.10). Identical forward performance is observed for different layouts whereas the center-base design is expected to be cooler in the stress condition.

3.7 Area Efficiency

As mentioned above, it has been shown that a center-base design provides much more uniform current distribution along the device. In large-area high-current SiC high power BJTs, the base metal pad can occupy part of the forward area. This part is inactive in current conduction mode due to elimination of the emitter cells underneath. In the interdigitated design, long emitter fingers connected from one end to the emitter metal contacts were used to solve the issue [100][129], but they are not fully active due to the high voltage drop along the long emitter fingers. Hence, it is desirable to find a method that solves this issue without adding cost of extra lithography and fabrication process complexity. In this thesis, we designed a novel structure called intertwined design, which can be implemented on different cell geometries or even on the other type of devices [PAPER VII]. This novel method combines the center-base structure with the square and hexagon cells with no extra lithographic step, and converts the region underneath the base contact to active transistor area. The key point of this design is its ability to connect two layers (e.g. metal contacts, interconnections, epilayers etc.) at different levels with no intersection. This relies on different features in the mask layout design of the intertwined structure.

3.7.1 Mask Layout and Realization of Intertwined Design

Fig. 3.11 presents the mask layout design of center-base 4H-SiC BJTs with intertwined design with the hexagon- and square-cell geometries. As can be seen from the figure, 100% of the area is used to form the emitter and base regions. This efficient design can decrease the total cost of the device by saving the device area. The fabrication process steps remain the same as in the conventional one. The design is successfully implied on center-base 4H-SiC BJTs to connect the inner and outer base-emitter networks. To realize the center-base intertwined design, inverted masks inside the inactive area was used (see Fig. 3.11). Instead of emitter cells surrounded by the base networks, the base holes in the center area are surrounded by the emitter networks. Dumbbell-shape structures at the edge of this area are used as the piers of the metal bridge connections (see Fig. 3.12). To form the intertwined design, the top metal contact is used as a bridge to connect the inactive area to the main base and emitter networks. As shown in Fig. 3.12, the top metal layer covers the Ohmic contacts on the dumbbell-shape structures (see Fig. 3.12.a and 3.12.b) at the edge of the inner area. The outer emitter cells (inner base cells) are connected to the inner emitter networks (outer base contacts) with top metal contacts (see Fig. 3.12.a and 3.12.b). These structures play a key role to connect two different metal levels of the
Figure 3.11. The layout designs of the small-area hexagon- and square-cell 4H-SiC BJTs with center-base intertwined design. The Blue, Orange, Black, and Magenta layouts are the p-Ohmic, n-Ohmic, oxide openings, and top metal layers, respectively.

Figure 3.12. (a) 3D-schematic view of the emitter and base contact layers in the center part of the intertwined design with square cell geometry. (b) magnified optical microscopic images of the center area (dashed square) of an intertwined BJT design with hexagon-cell in the center area (left) after forming the n- and p-Ohmic contacts and (right) after top metallization. Dumbbell-shape structures (dashed ovals) at the edge of inner area were used as the piers of the metal bridges connected by the top metal contact. The outer emitter cells (inner base cells) are connected to the inner emitter networks (outer base contacts) with top metal contacts. (c) microscopical images of the top view of the fabricated intertwined design BJTs with hexagon (left) and square (right) cell geometries. (d) microscopical image of the top view of the fabricated Darlington with intertwined design BJTs with square-cells.
3.7. Area Efficiency

Figure 3.13. (a) $I_C-V_C$ characteristic of a BJT with center-base intertwined design. Higher current with comparable current gain is achieved for the intertwined design compared to the conventional design. (b) the $\beta-I_C$ plot of the fabricated BJTs with different emitter cell geometries. The maximum current gain is measured at 10% higher collector current for the intertwined design with equal die size.

The $I_C-V_C$ characteristic of the fabricated intertwined BJTs is shown in Fig. 3.13.a. A comparable maximum current gain of 22 and 20 is obtained for the conventional and intertwined BJTs with the hexagon and square cells, but at a higher collector

3.7.2 Characteristics of the Intertwined Design

The $I_C-V_C$ characteristic of the fabricated intertwined BJTs is shown in Fig. 3.13.a. A comparable maximum current gain of 22 and 20 is obtained for the conventional and intertwined BJTs with the hexagon and square cells, but at a higher collector
current for the intertwined designs. Results follow the same trend as in [84], [92] since the devices are fabricated in the same wafer. Fig. 3.13.b presents the Gummel plot of the fabricated BJTs with different layout designs and emitter cell geometries. The maximum current gain is found at about 10% higher collector current for the intertwined designs whereas the device sizes are equal. This proves the former explanation for the measured $I_C-V_C$. To have a reasonable comparison between different designs, an accurate value of the actual active area is required. The current flow in the thick collector drift layer is simulated and the current spreading effect is considered in order to find the accurate equivalent active area. To evaluate this method, we compared our simulation and calculation with experimental small- and large-area results [100] and a good agreement was achieved.

![Figure 3.13](image1)

**Figure 3.14.** Current gain as a function of emitter width for different cell geometries. Comparable gain is measured for the intertwined designs with equal cell size.

![Figure 3.15](image2)

**Figure 3.15.** The (a) current density and (b) specific on-resistance as a function of emitter width for hexagon- and square-cell with different layout designs and cell sizes. A higher current density and lower on-resistance are achieved for the intertwined designs with equal size. The current density is measured at the maximum current gain at $V_{CB} = 5$ V whereas the corresponding specific on-resistance is obtained at $I_C = 0.1$ A.
3.7. Area Efficiency

![Image of comparison graphs]

Figure 3.16. Comparison of the (a) current density at $V_{CB} = 5 \text{ V}$ and (b) specific on-resistance at $I_C = 0.1 \text{ A}$ versus the maximum current gain for intertwined layout designs and conventional hexagon- and square-cell geometries with different emitter widths. A higher current density and lower on-resistance at a given current gain are measured for the intertwined designs.

Fig. 3.14 shows the emitter size effect on the maximum current gain for the different cell designs compared with as of the intertwined designs. A comparable maximum current gain is achieved for the conventional and intertwined layout designs for the equal emitter width. The gain is decreasing as the $W_E$ reduces below 40 $\mu\text{m}$ for all emitter cell geometries. As expected, the wider emitter ($> 40 \mu\text{m}$) does not result in higher current gain due to the saturation behavior discussed in [196].

Fig. 3.15.a and 3.15.b present the dependency of the current density (at the maximum current gain) and specific on-resistance (at $I_C = 0.1 \text{ A}$) to the emitter width for different cell geometries and the intertwined designs, respectively. The maximum current gain is measured at $V_{CB} = 5 \text{ V}$ whereas the corresponding on-resistance is obtained at $I_C = 0.1 \text{ A}$. A higher current density and a lower on-resistance are measured for the intertwined designs, which are mainly due to the efficient usage of the forward area. It is worth noting that the difference between the hexagon- and square-cell designs is mainly due to the area to periphery ratio [PAPER VI].

Fig. 3.16.a and 3.16.b illustrate the current density and specific on-resistance as a function of the maximum current gain for hexagon- and square-cell geometries compared to the intertwined designs with different emitter widths. About 15% higher $J_C$ and lower $R_{ON}$ are achieved for the intertwined designs compared to the conventional layout design. This is obtained by efficiently employing 100% of the forward area. Therefore, at a given maximum current gain, the intertwined layout designs are more suited for high-power SiC devices.
3.8 High-Current Darlington Pairs

In most of the industrial applications and high power operations, a high current is required to drive a load. For a single BJT, the output current is a multiplication of input current multiplied by the factor of current gain that is achievable at a certain voltage drop. Therefore, driver circuit is required to provide a sufficient $I_B$ to achieve the maximum $I_C$. This results in a higher input power dissipation and more complexity of the driver circuit design. Darlington pairs are well-known double stage BJTs in series in which the output of the first stage is the input of the second stage.

A Darlington pair with isolated input and output BJTs as shown in Fig. 3.17. If both the driver and output BJTs are biased in their maximum current gain, the output current can be calculated as below:

\[ I_{C1} = \beta_1 I_B \]  
\[ I_{C2} = \beta_2 I_B = \beta_2 I_{E1} = \beta_2 (I_{C1} + I_B) = \beta_2 ((\beta_1 + 1)I_B) \]  
\[ I_C = I_{C1} + I_{C2} = \beta_1 I_B + (\beta_1 \beta_2 + \beta_2)I_B = (\beta_1 \beta_2 + \beta_1 + \beta_2)I_B \approx (\beta^2 + 2\beta)I_B \]  
\[ I_C \approx \beta^2 I_B \]

where the $I_C$ and $I_B$ are the output and input current of the Darlington pairs, respectively.

To achieve the optimum performance of a Darlington pair, it is important to consider different points as follow:

- Since the output current density is much higher than a BJT, a thick enough metallization to handle the high current is required.
- The current of the output BJT is almost $\beta$ times higher than the driver BJT. Hence, the same area factor should be considered between the output and driver BJTs. This is important to achieve the highest current density and to bias the driver and output BJTs close to their maximum current operating points. To
achieve this, the maximum current gain of the BJTs should be achieved at a high current density. It is worth noting that a too small driver results in low current injection into the output BJT. This is due to the late biasing of the output BJT leading to a lower maximum current gain at low output current. On the other hand, a too large input BJT injects too high current in the output BJT leading to early bias of the output BJT. As a result, the early saturation occurs in the output BJT, which decreases the total maximum current gain.

- The input resistance of the output BJT is an important factor. It is desirable to have the lowest input resistance to drive the Darlington at its maximum performance.

3.9 Layout Design

As mentioned earlier, a stepper lithography with a frame size of $7 \times 7 \text{ mm}^2$ is used. In this thesis, three different batches including several devices are fabricated. Since a minimum $1-\mu\text{m}$ feature size in some structures is used, resolution marks and rotational alignment structures so-called Vernier marks are added for each lithographic steps. We checked and verified the alignment and resolution marks during the fabrication process steps to minimize the misalignment and realize the structures with the minimum feature sizes.

Fig. 3.18.a and 3.18.b show the layout design and the microscopic image of the fabricated die of the 4.5-kV high-voltage batch. In this work, different termination designs are implemented to find the optimum termination design. Moreover, several test structures are added to optimize the forward performance including the current gain, current density, and on-resistance. Small-area 0.5 A BJTs ($\sim 0.1 \text{ mm}^2$), medium-size 3-A BJT (1 mm$^2$), large-area 10-A BJT (4 mm$^2$), and small-area 1.5-A Darlington pairs (0.5 mm$^2$) are drawn. Fig. 3.18.c and 3.18.d represent the layout design and the microscopic image of the fabricated die of the 15-kV high-voltage batch. Several optimized parameters extracted from the previous batch are used in this work. Other than some test structures, a large-area 5-A PiN diode, a large-area 4-A BJT, and different Darlington pairs (0.1 A – 4 A) are realized. Fig. 3.18.e and 3.18.f depict the layout design and the microscopic image of the fabricated die of the high-temperature lateral 4H-SiC BJTs. Different high-current lateral BJTs and a Darlington pair are implemented.
Figure 3.18. The (a) layout design and (b) microscopical image of the fabricated die of the 4H-SiC 4.5-kV devices; the (c) layout design and (d) microscopical image of the fabricated die of the 4H-SiC 15-kV devices; (e) the layout design and (f) the microscopical image of the fabricated die of the 4H-SiC high-temperature lateral BJTs.
Chapter 4. SiC Fabrication Technology and Process Development

In this chapter, the process technology of the fabricated SiC devices is discussed and the process flow of the high-voltage and high-temperature BJTs is briefly explained. All processes are designed to be fully implantation-free and the devices are formed by etching, deposition, and metallization processes. Although most of the process steps including the lithography, etching process, and metallization are similar for different devices, essential modifications are considered due to their difference for high-voltage, high-current, and high-temperature applications. Afterward, special attention is dedicated to the surface passivation oxidation and Ohmic-contact technology with a wafer-scale process. This simplifies the fabrication, improves the BJT performance, and enables the scalability of our integrated devices and circuits.

A similar fabrication process is used for the high-voltage devices and high-temperature devices and integrated circuits unless otherwise stated. The main differences are the number of etching steps, thickness of oxide layers and the interconnection metal layers, interconnection metal stack, and the number of metallization layers. An already established etching, sacrificial oxidation, surface passivation, and Ohmic metal contact is used in the first two batches. Later on, a further investigation and improvement in the SiC surface engineering and SiC contact process technology will be discussed.

4.1 Ion Implantation-Free Technology

As mentioned earlier, it is known that SiC BJTs with epitaxial emitter and base regions offer excellent performance due to better emitter injection efficiency, lower degradation, and lower base resistance. The crystalline damages caused by ion implantation process degrade the current gain. Also, a high-temperature annealing to activate the implanted ions is required, which lowers the carrier lifetime during the fabrication process. The estimated carrier lifetime between 1 µs to 3 µs for the drift layer was reported by the supplier. So it is preferred to avoid any high temperature
annealing. On the other hand, no ion implanter is available in-house and the process is
time-consuming and costly. Therefore, we decided to use epitaxial emitter and base
layers and we fully eliminated the ion implantation process, even to implement the
dge termination to avoid high temperature annealing. As a result, an ion implantation-
free process flow is designed in which the emitter mesa, base region, the multi-step
etched junction termination extension, and the channel stopper are formed by SiC dry
etching. Hence, to achieve high yield and reasonable uniformity, a controlled etching
process is developed that will be discussed in the coming sections.

4.2 Lithography and Fabrication Process Flow

Lithography is the fundamental process of the fabrication technology to pattern and
realize a design. The more number of lithographic steps increases the complexity and
total cost of the fabrication process. It is highly recommended to add no extra
lithographic step or even desired to reduce them by applying novel designs or
fabrication technologies. The established lithographic process is based on the ALS
2035 G-line stepper tool, which limits the design and process to ~1 μm. To obtain the
minimum feature size, one has to consider the thickness of photoresist, exposure time,
topology and the coverage of the wafer surface, and the corresponding process step.
Regarding these points, lithographic process is developed and established for the
typical 700-1.2 positive photoresist with different thickness and exposure time. A well-
known developer CD-26 with different development time (mostly 60 sec) is used to
develop the photoresist. Some treatments like soft-, post-, and hard-baking at different
temperatures (100 to 115 °C) and durations (1 to 2 minutes) are necessary to achieve
the best possible resolution as well as a clean and smooth pattern that exactly
follows the mask layout design.

Considering the lithographic limit, all devices and integrated circuits are designed
with minimum feature size of 1 μm. Though it is simpler and safer to have more
relaxed designs and keep safe margin from the lithographic limit, however reaching 1-
μm is inevitable since finer structures is useful in the termination design [PAPER IV],
which will be discussed later. Also, there is a demand to have more aggressive designs
to further approach the scaling of the high-temperature integrated circuits to enable
the realization of more advanced SiC integrated circuits. 10, 11, and 9 lithographic
steps are used for high-voltage BJTs, high-temperature integrated devices, and
recessed-gate MOSFETs. Additional lithographic steps in the high-temperature
integrated circuit BJTs and recessed-gate MOSFETs are due to presence of extra
metallization layer and gate poly-silicon layer.

As mentioned earlier, the SiC BJT technology and fabrication process has been
developed in our group at KTH for several years. We had an established technology
for medium-voltage range 4H-SiC BJTs as the starting point [100]. The overall process step of the high-voltage BJTs is schematically presented in Fig. 4.1. As represented in Fig. 4.1, it includes 10 different lithographic masks and two metal layers, acting as over-layer metallization as current spreading layer for device contacts and the final metal layer. It should be noted that an additional metal layer on the oxide close to the termination zones can affect the device blocking behavior that results in early breakdown. Therefore, the total thickness of oxide layer and the metal paths are carefully designed to avoid this. Later on, the high temperature BJT technology is also developed to realize the SiC BJTs and integrated circuits for harsh environment [17]. This process originated from the high-voltage BJT process in which a few process steps were added and modified. Fig. 4.2 illustrates the process flow of the high-temperature integrated circuits. This process includes 10 different lithographic masks and two metal layers, acting as over-layer metallization as current spreading layer for device contacts and the final metal layer. As mentioned earlier, basic fabrication steps of high-voltage BJTs and high-temperature devices are similar except for the thickness of oxide layers and the final metallization, that will be explained later. The process details of the established procedures as well as the new developed processes for the SiC etching, surface passivation, and Ohmic metal contact technology both for the n- and p-type SiC will be discussed in the next sections. Special attention is dedicated to develop wafer-scale fabrication processes in order to make the whole procedure simpler and more reliable.

### 4.3 Dry Etching of SiC

Wet etching of a chemically inert material like SiC is very difficult and results in a rough surface, which is not suitable for devices and integrated circuits. Hence, dry etching processes like inductively coupled plasma (ICP) and reactive ion etching (RIE) become popular alternatives to pattern SiC. The RIE is mostly used for etching below 1 μm whereas the ICP is more suitable for deep etching of SiC. It should be noted that the sidewall profile of the etching and the surface roughness and damages are different for the ICP and RIE process. One can control these parameters with the power, gases pressure and flux, mask patterning etc. with specific recipes for each tools. In our established process, the etch rate of 4H-SiC in RIE is about 125 nm/min and the selectivity is about 0.9. The RIE process allows us to use photoresist as the mask. This saves time and simplifies the process. However, it should be noted that it can produce polymer particles during the etching. These polymer particles can be locally redeposited and work as microscale masks leading to tiny pillar shape or islands in the open areas. To solve the problem, a modified RIE process with higher O2 pressure was used, which on the other hand increases the etching of photoresist. The RIE is used, which on the other hand increases the etching of photoresist. The etch rate of
Figure 4.1. The schematic of the process flow for the high-voltage and ultra-high voltage SiC BJT technology. (*) The batch of 4.5-kV-class devices was fabricated with 3-zone JTE and has one less lithographic and dry etching step compared to the 15-kV BJT with 4-zone JTE.
4.3. Dry Etching of SiC

SiC in the modified RIE is about 145 nm/min with the selectivity of about 1.2. The RIE is using DC power in which a higher etch rate could be obtained by higher power, but it can result in more surface damage. Unlike RIE, metal or SiO$_2$ should be used as a hard mask for ICP etching. Using a metal mask leading to steeper angle and better selectivity but can result in trenching effect on the bottom of the etched mesa [15].
Therefore, SiO$_2$ is used as a hard mask for ICP etching. The etch rate of SiC in the ICP is about 125 nm/min with the selectivity of about 1. The ICP coil is supplied by RF power, that produces high plasma density with lower ion energies. As a result, it introduces less surface damage compared to the RIE etching [15]. The rough surface can significantly hamper the BJT current gain and produce early breakdown in the termination area [17][15]. The sidewall angle of 50° and 75° are measured for the RIE an ICP etching, respectively. The ICP etching is used for high-voltage BJTs in which the etching of the emitter and termination mesa steps are deeper than 1.5 μm. Other etching steps in high-voltage and high-temperature integrated circuits are done by mean of the improved RIE dry etching. Since the emitter, base, collector, and gate are formed by etching through the epilayers, the uniformity and controllability of the etching process is critical in this thesis, particularly for the thin base layer. Beside, an over-etching is needed to compensate the epilayer variations to ensure reaching the next epilayer. Moreover, the etching controls the remaining dose of the junction termination extension area. This affects the termination efficiency and the breakdown voltage of the device. Taking the sensitivity of the device performance to the etching process into consideration, the etchings are divided in few steps and the etch depth and the rate is traced to approach the targeted value with minimum variation. The uniformity of ±7 % is achieved with this process.

4.4 4H-SiC Surface Engineering and Treatments

As mentioned earlier, the SiC surface quality affects the device performance both in forward and reverse characteristics. Several studies have been reported to improve the quality of SiC/SiO$_2$ interface. Presence of interface traps significantly influences the channel mobility and consequently the performance of the SiC [52], [220]–[222]. In SiC BJTs, the surface between the emitter and base, that is directly exposed by the first etching process plays the key role in the current gain due to the presence of the surface recombination [223]. In the reverse, the introduction of large variation in the junction termination areas can change the efficiency of the termination technique [224], [225]. Also, the presence of charges at the SiC interface changes the electric field distribution in the termination, which should be considered in the device design and process variability study. The sacrificial oxidation reduces the surface damages, and hence decreases the surface recombination current [223]. The advantage of SiC is the presence of Si atom that allows a thermally grown oxidation process. The sacrificial oxidation process is performed to smoothen the damaged surface of the SiC after the dry etching steps. The thermal oxidation rate of SiC is much lower than Si and requires relatively high temperature. The thermal oxidation of SiC leaves carbon clusters at the surface of SiC due to out-diffusion of C atoms. A portion of these carbon atoms react with O$_2$ [226], whereas some C clusters remain and introduce as interface traps
The growth rate of the dry and wet oxidation is about 10 nm per min. This is much lower than Si even at higher temperatures about 1250 °C. After removal of the sacrificial oxidation, employing a passivation oxide is known to be a fine method to improve the surface charges to resolve the problems. The annealing ambient, the time, and the temperature have great influences on the surface treatment both in the sacrificial oxidation and surface passivation [83], [222], [224].

In this thesis, we firstly used the established process in high-voltage BJTs [16]. To prepare the SiC surface after the etching process, the wafers are cleaned in RCA to remove the organic contaminations and in Piranha and HF:H2O2 baths to remove the non-organic contaminations and possible native oxide. Then, a dry sacrificial oxidation at 1100 °C for 1 hour [PAPER II-VII] is performed, that forms the thermally grown oxide with the thicknesses of ~10 nm. The oxide is removed by hydrofluoric acid (HF). Afterward, a PECVD oxide with a thickness of 50 nm is deposited as the surface passivation. The post-deposition annealing in N2O ambient at 1100 °C for 3 hours is performed. The established passivation process results in relatively high interface density of states, which degrades the current gain.

In the past decade, several works have been performed to improve the quality the SiC/SiO2 interface either by introduction of external atoms to occupy the dangling bonds or by reduction of the surface roughness by surface treatments. In the first approach, it has been shown that introduction of nitrogen (N) atoms at the SiC/SiO2 interface can passivate the dangling Si bonds and eliminate the interstitial C and C clusters during nitridation. The high-temperature annealing cracks the NO or N2O molecules and release the nitrogen atoms that can penetrate into the PECVD deposited oxide and reach the SiC interface and passivate the Si dangling bonds. Therefore, it results in a lower density of interface traps and a higher channel mobility [227]. To generate N atoms at the SiC/SiO2 interface, other methods have been used such as thermal oxidation in nitric oxide (NO) or nitrous oxide (N2O) [224], nitrogen implantation [229][230], high-temperature annealing in NO or N2O [222] and thermally grown SiO2 followed by annealing in Argon (Ar) and NO ambient [93]. Moreover, high-temperature annealing in POCl3 [220], [231] and hydrogen (H) [232] ambient can reduce the interface trap density. The effect of etching process on the surface roughness is studied and an improved sacrificial oxidation is performed to smoothen the SiC surface, which improves the deposition quality of the PECVD SiO2. In the next step, improved dry etching, sacrificial oxidation technique, and surface passivation are developed. The enhanced surface treatments [17], [194] are developed and used in 15-kV-class 4H-SiC BJTs [PAPER I].

A dry sacrificial oxidation at 1100 °C for 3 hours [PAPER II-VII] is performed. This forms ~20 nm of thermally grown oxide. The oxide is removed by hydrofluoric
acid (HF). Afterward, a PECVD oxide with a thickness of 100 nm is deposited as the surface passivation. The post-deposition annealing in N$_2$O ambient at 1250 °C for 3 hours is performed. The enhanced passivation oxidation significantly improved the current gain. It is worth noting that a low-temperature (300 °C) PECVD oxidation is used to deposit the SiO$_2$. The low-temperature oxide deposition make it porous that later helps the diffusion of nitrogen atoms to reach the SiC interface.

### 4.5 Ohmic Metal Contact Technology

#### 4.5.1 Established Lift-off Process

Forming low-resistive and uniform Ohmic contact to 4H-SiC is an important part of the process for all kind of devices including the BJTs and MOSFETs. To achieve a proper device performance, contact resistivity below 0.1 mΩ.cm$^2$ is required. A high contact resistance increases the forward voltage drop and the device total power loss. Several metals with different temperatures and thicknesses have been studied to form a low-resistive and uniform Ohmic contact to SiC. Reasonable Ohmic contact technologies are currently available for n-type SiC, however the p-type is still suffering from high contact resistance. On the other hand, depending on the metal type and the available process technology, different processes such as metal lift-off, reactive ion etching, and ion milling etching have been used to pattern the metal layer. However, the SiC Ohmic metal technology is still not as mature as of Si.

In the first and second batches in this thesis, an established metal contact technology for n- and p-type SiC by means of the lift-off process to pattern the metal layers was used. In the following, an effort is made to eliminate the lift-off and exchange it with etching process. As will be discussed, a wafer-scale self-aligned Ohmic metal contact process was developed and investigated. The lift-off free process was tested and verified for the n- and p-Ohmic contacts.

To form a desirable Ohmic contact, it is essential to do a surface preparation and cleaning to remove any contamination, photoresist residues, native oxide etc. In the lift-off process, metal evaporation is used to deposit the metal layers. The metal evaporation is done in an ultra vacuum clean chamber. The deposition rate is usually low (1-2 nm per sec) with a poor step coverage. A thick photoresist (more than 1.5 µm) is chosen to make the lift-off easier and finer. The lift-off process leaves jagged metal edges and metal residues on the wafer, which is the main disadvantage of this process. Finishing the process in a fine lift-off ultra-sonic bath can improve the process. Using metal sputtering is not fine for the lift-off process since it can create photoresist particles and harden or even burn the photoresist. On the other hand,
using a sample with photoresist is not very welcome in the sputtering tools due to the possibility of contaminating the chamber.

In the lift-off process, the oxide is opened and nickel (Ni) with thickness of 100 nm is deposited for n-type 4H-SiC. After the lift-off process, a high temperature RTA annealing at 950 °C in nitrogen ambient for 60 sec is performed to form the n-Ohmic contact. A metal stack of Ni-Ti-Al with the thickness ratio of 10-15-85 nm is deposited for p-type 4H-SiC. A p-contact is formed by high temperature RTA annealing at 825 °C in argon ambient for 120 sec. The contact resistivity is measured by TLM structures. It should be noted that no vacuum chamber was currently available in our facilities for RTA annealing. The contact resistivity of 5×10⁻⁶ and 5×10⁻⁴ Ω.cm² for the n- and p-type 4H-SiC are achieved, respectively. A reason for the slightly high p-contact resistance is the lowly-doped p-layer that is designed to increase the current gain and make the JTE etching more controllable. It should be noted that a local high dose ion implantation in the p-contact area has been reported to improve the contact resistivity, however in this process we avoid using ion implantation to protect the devices from the damages and defects caused by ion implantation. To avoid oxidation of the metal contact top surface, the chamber is purged with nitrogen to cool down the sample before unloading. An oxidized rough metal surface can cause bad adhesion of the overlayer metallization and metal interconnections. This is critical for uniform current distribution in the device.

4.5.2 Wafer-Scale Ni-SALICIDE n-Ohmic Contact Technology

For further improvement of the process technology as well as simplifying the fabrication, a wafer-scale self-aligned Ni SALICIDE for 4H-SiC contact technology is developed [PAPER VIII]. The self-aligned silicide process (SALICIDE) has been developed in Si technology for many years. The Ti- and Co-based SALICIDE process with two-step annealing process was developed in silicon CMOS technology, specifically to reduce the resistivity of the contacts. As mentioned earlier, unlike the Si technology, forming a good Ohmic contact to SiC requires high temperature annealing. SiC contact technology suffers from the lack of a simple and clean self-aligned Ni process particularly on wafer-scale. Moreover, downscaling of SiC-based devices and circuits is hampered by a lack of reliable self-aligned process to form the metal contacts and short channels. High temperature annealing of metal/SiO₂ increases the risk of diffusion-reaction of metal and oxide layer. This could affect the functionality of large area devices and circuits. Furthermore, the quality of silicide surface and coverage significantly affects the device behavior. The two-step annealing has been previously used for SiC technology to form Co-based contacts to n-type and for Ni-Al contacts to p-type. Nickel (Ni) silicide is shown to be a good choice for the
n-type Ohmic contacts. For SiC, Ni$_2$Si is rectifying until annealed at 950 °C, without any obvious phase-change.

In Paper IV, a wafer-scale self-aligned n-contact with a two-step rapid thermal annealing (RTA) is demonstrated. The electrical and physical properties of the contacts are studied. The key point is to perform a first step annealing (FSA) of Ni layer at low-temperature (550-700 °C) to form one phase of Ni$_3$Si$_x$ and removing the unreacted Ni by a selective wet etch in Piranha (H$_2$SO$_4$+H$_2$O$_2$ (3:1)). Afterward, the second step annealing (SSA) at high temperature (950 °C) produces a low contact resistance. This eliminates the effect of high temperature annealing of Ni/SiO$_2$ layer, which could affect the quality of oxide at higher temperatures. This method is successfully employed on a 4-inch SiC wafer process and the surface quality and the coverage of silicide in the oxide openings is significantly improved in comparison with the lift-off process. This method improves the yield and reduces the process complexity. Unlike the lift-off process, the thin oxide opening could simply be shrunk, filled in by the sputtered metal and annealed to form the contact. Also, no underlap in the contact openings to improve the silicide coverage is required. The proposed self-aligned technology could widely be used for all kind of SiC devices and integrated circuits to form the n-type Ohmic contacts.

The wafer surface is cleaned in Piranha, HF:H$_2$O, and the RCA baths to remove the organic contaminant and the native oxide. A 100-nm layer of SiO$_2$ is conformally formed at 350 °C on the surface of the SiC samples and the contact windows are opened by dry etching process. An O$_2$ cleaning for 10 minutes and conditioning process for 10 minutes is consequently done in the oxide deposition chamber, which significantly improves the oxide quality and uniformity. A 100-nm Ni layer is sputtered using a pre-sputtering process. The pre-sputtering is done for 20 sec on the wafer to remove the possible formed oxide at the SiC surface and on the Ni target to remove any contamination from the target. Fig. 4.3 presents the process step flow and annealing profile of the self-aligned n-contact. The FSA is performed to form one phase of Ni silicide in the contact openings. Temperature steps from 450 to 1000 °C in N$_2$ ambient to find the optimum temperature of the FSA are performed. To protect the formed silicide and the Ni layer from oxidation after the annealing steps, a continuous purging with N$_2$ for 3 minutes is done in the chamber to cool down the wafer to below 200 °C before unloading the wafer. Then, the sample is dipped into the Piranha to remove the unreacted Ni. The SSA at 950 °C for 1 min in N$_2$ ambient to form the low-resistivity Ohmic contacts is performed. The contact characteristics as a function of the annealing temperature profiles are evaluated in terms of electrical and structural properties. In order to measure the contact resistivity ($\rho_C$), linear transmission line model (TLM) structures with rectangular pads with spacing from 5
to 25 μm are fabricated. Finally, 1-μm Al/TiW was sputtered and patterned to form the final metal pads. For further investigation, the structural analyses at the interface of Ni/4H-SiC and the formation of Ni$_x$Si$_y$ silicide phases by X-ray diffraction (XRD) are done. The morphology of the contacts by atomic-force microscopy (AFM) is studied.

The proposed self-aligned process is based on two annealing steps. The formation of Ni-silicide (Ni$_x$Si$_y$) compounds is an important factor to form a low-resistive electrical contact between Ni and 4H-SiC. The silicide phase at the Ni/4H-SiC interface changes at different annealing temperature. To find the optimum temperature range of the FSA, the formation of Ni$_x$Si$_y$ silicide at different temperatures is investigated by X-ray diffraction (XRD). Fig. 4.4 presents the XRD spectra of the Ni silicide contacts after the FSA at different temperatures. A 4H-SiC reference and an as-deposited Ni sample are added as references in which a peak of single-crystalline 4H-SiC and poly-crystalline Ni are visible. A phase transformation of Ni-silicide is obvious for different annealing temperatures. This interaction between Ni and Si is the key point in this self-aligned process that allows the following wet removal of the unreacted Ni and the consequent SSA. Ni$_{31}$Si$_{12}$ at below 600 °C and Ni$_2$Si for higher temperatures are the main phases while no trace of Ni is observed after the FSA and removal of unreacted Ni. The SSA at 950 °C is essential to produce low-resistive Ohmic contacts. The silicide formation starts at 550 °C and its phase transformation continues at higher temperatures. The intensity of the Ni$_2$Si peak is dramatically increased at above 700 °C. The contact surface became rougher at higher annealing temperatures. Due to presence of Ni atoms, different phases of Ni$_x$Si$_y$ could be formed due to diffusion and reaction of these atoms. The silicide starts to agglomerate when the temperature increases and the silicide islands become visible. The AFM images of the samples after FSA and wet removal step and after the SSA at 950 °C compared with the as-deposited Ni are shown in Fig. 4.5. The annealing
process influences the surface morphology of the samples. This is attributed to the reaction of Ni and Si and the phase transformation of Ni-silicide. The short annealing time in RTA and the thickness of Ni film could affect the formation of the silicide and its morphology. The formation of silicide in larger areas is much more uniform than in the smaller openings. This might be attributed to the immediate expansion of the Ni layer surrounded by oxide sidewalls during the RTA process. The annealing process affects the quality of oxide, which could be a passivation layer of BJT’s, gate oxide of MOSFET’s, side-wall oxide of JFETs and trench devices, etc. Fig. 4.6 illustrates the scanning electron microscopy (SEM) image of the Ni-contacts formed by the lift-off process and the double-step annealing SALICIDE process. The contact with lift-off has metal residues and jagged edges whereas the one with the silicide process has smoothed metal edges and clean oxide surface.

In the Ni-SALICIDE process, after opening the oxide by dry etching, Ni sputtering with pre-sputtering process is used to deposit 100 nm of Ni. The pre-sputtering on the sample removes the contaminations and possible formed oxide at the 4H-SiC surface. The FSA is performed to form one phase of Ni silicide in the contact openings. Temperature steps from 450 to 1000 °C in nitrogen ambient to find the optimum temperature of the FSA are performed. Then, the sample is dipped into the Piranha to remove the unreacted Ni. The SSA at 950 °C for 1 min in N₂ ambient to form the low-resistivity Ohmic contacts is performed. The contact characteristics as a function of the annealing temperature profiles are evaluated in terms of electrical and structural properties. In order to measure the contact resistivity ($\rho_C$), linear transmission line model (TLM) structures with rectangular pads with spacing from 5 to 25 μm are fabricated. Finally, 1-μm Al/TiW was sputtered and patterned to form the final metal pads. For further investigation, the structural analyses at the interface of Ni/4H-SiC and the formation of NiₓSiᵧ silicide phases by X-ray diffraction (XRD) are done.
Figure 4.5. The AFM images of the silicide contact surface after removal of the unreacted nickel at different temperatures of the FSA. The AFM scanning size is 20×20 μm².

Figure 4.6. The SEM images of Ni n-contacts on 4H-SiC formed by (bottom) lift-off and (top) SALICIDE process. The proposed Ni- SALICIDE technology results in a smoother metal edge and cleaner oxide surface.

Fig. 4.7.a presents the I-V electrical characteristic of the Ni contacts after the FSA from 450 to 950 °C. The typical Schottky behavior of the contacts at lower annealing temperatures gradually changes to Ohmic behavior at higher annealing temperatures. All samples with FSA > 500 °C become Ohmic after the SSA at 950 °C (see Fig. 4.7.b). However, the lower annealing temperature of Ni/SiO₂ saves the oxide quality. The FSA range between 550 to 700 °C results in low-resistive Ohmic behavior after the SSA at 950 °C. Moreover, it is found that the annealing time between 45-90 seconds is sufficient for the FSA and SSA steps. Hence, the proposed two-step self-aligned process benefits from a wide process window for the annealing temperature and time that makes it a reliable contact technology. The influence of the proposed process on the oxide quality is investigated and no significant effect is observed.
Figure 4.7. The I-V characteristic of the Ni contacts (a) after the FSA at different temperatures and removal of unreacted Ni and (b) after the SSA at 950 °C. All samples with FSA > 500 °C become Ohmic after the SSA at 950 °C.

The TLM plots with different FSA temperatures and SSA at 950 °C are shown in Fig. 4.8.a. To fairly measure the contact characteristics, the total resistance of different samples is calculated by differentiation of the I-V curves for distances of TLM pads. All samples with FSA > 500 °C shows $\rho_C$ below $1 \times 10^{-5} \, \Omega \cdot cm^2$ whereas the samples with the FSA in the range of 550 to 700 °C shows $\rho_C$ below $5 \times 10^{-6} \, \Omega \cdot cm^2$, which is comparable to that of the conventional single-step annealing at 950 °C. It should be noted that the difference between contact resistances is mainly attributed to the doping variation of the samples. As mentioned earlier, the $\rho_C$ decreases for higher annealing temperatures of FSA. The wafer mapping of the measured contact resistivity is shown in Fig. 4.8.b. Among the 112 measured dies with TLM structures, above 50 has a contact resistivity below $5 \times 10^{-6} \, \Omega \cdot cm^2$ and more than 80 has a contact resistivity below $6 \times 10^{-6} \, \Omega \cdot cm^2$. A high uniformity for the contact resistivity is achieved.

4.5.3 Wafer-Scale Lift-Off-Free p-Ohmic Contact Technology

After successful development of the wafer-scale Ni- SALICIDE process for n-type SiC, we started to develop an Ohmic contact technology for the p-type. In the next step, by employing a similar concept, we demonstrated a wafer-scale lift-off-free process for both n- and p-Ohmic contacts on 4H-SiC with no additional lithographic or fabrication process step. The fabrication process step of the proposed p-Ohmic contact technology is presented in Fig. 4.9. The key step to make the p-Ohmic contact is to deposit a Ti/Al stack on the Ni-silicide and transform it to a low-resistive Ohmic contact with a final annealing. The low-temperature (FSA) Ni-SALICIDE process as such described above is used to form a silicide on the n- and p-type 4H-SiC layers. Since the initial low-temperature silicide phase is used for the p-contact, the oxide via are opened for the n- and p-Ohmic contacts in the same lithographic step. A 50-nm Ni layer is deposited and annealed at >700 °C. Afterward, the unreacted Ni is removed
by wet-etching in Piranha. The stable silicide phases (Ni$_x$Si$_y$) remain in the openings after the wet-etching process. A Ti/Al stack with thickness of 30/120 nm is deposited and patterned on the p-Ohmic contact openings by dry etching process. The final annealing is performed at >900 °C, which transforms the silicide to Ohmic contact both on the n- and p-type 4H-SiC layers. Thanks to the Ni-SALICIDE process, no wet etching or ion milling of Ni is required.

Figure 4.8. (a) The total resistance measured for the TLM structures with different pad distances at various FSA temperatures 500 to 900 °C followed by the SSA temperature at 950 °C. The transfer length ($L_T$) is extracted for each sample. (b) The wafer mapping of the measured n-contact resistivity on the wafer with 112 dies.

Figure 4.9. Schematic fabrication process flow of the wafer-scale lift-off-free process to form the n- and p-Ohmic contact to 4H-SiC.
A 4-inch 4H-SiC n\textsuperscript{+}-substrate with n- and p-type epilayers is used. Reactive ion etching (RIE) process is used to etch the top n-layer and form the mesa to reach the p-layer. It has been shown that the surface roughness can degrade the Ohmic contact quality [15]. Therefore, a sacrificial oxidation in O\textsubscript{2} for 3 h is performed to improve the surface damages caused by the ion etching process. The n-contacts are formed on highly-doped (> 1×10\textsuperscript{19} cm\textsuperscript{-3}) epilayers whereas the p-Ohmic contacts are made on an epilayer with doping concentration of ~1×10\textsuperscript{18} cm\textsuperscript{-3}. This lower doping concentration can degrade the quality of Ohmic contact. To improve the measurements and eliminate the current debiasing effect on the metal contacts, a 1-\textmu m TiW/Al stack was sputtered and patterned on the Ohmic contacts. A specific contact resistivity of 6×10\textsuperscript{-4} \Omega cm\textsuperscript{2} for the p-type 4H-SiC is obtained. The wafer mapping of the measured p-contact resistivity is shown in Fig. 4.10. Among the 112 measured dies with TLM structures, more than 70 have a contact resistivity below 7×10\textsuperscript{-4} \Omega cm\textsuperscript{2}. Although the contact resistivity is slightly high, the advantage of eliminating the lift-off, simultaneous annealing process, and no need for extra lithography makes it a reasonable process for many devices. It is worth noting that a compatible process with other metal stacks like Ni/Al may improve the contact resistivity [233]–[237].
Chapter 5. Characterization

As discussed earlier, the BJT performance in conduction and blocking modes are influenced by various terms including the epilayer properties, fabrication process parameters, layout design and device geometry, and device dimensions and scaling. In Chapter 3, epilayer thickness and doping concentrations are chosen by considering the targeted specifications. Then, the device layout and dimensions are optimized to reach the specified properties. Moreover, the termination design is optimized to decrease the total area of the device with minimum lithographic steps. The BJT on-state characteristics such as the maximum current gain, current density, on-resistance, and current distribution are improved. The optimized results are implemented in high- and low-voltage devices with small- and large-area.

In this chapter, the characteristics of the fabricated BJTs in 4.5 kV-class and 15 kV-class BJTs in conducting and blocking modes are presented. In the following, the measurement results of the high-current BJTs for high-temperature integrated circuits are presented. As described in Chapter 3, the effect of emitter geometry and scaling on the maximum current gain, current density, and on-resistance are studied and the optimum design is implemented for the large-area high-voltage and ultra-high-voltage devices. Different junction termination extensions, including the double-JTE, modified double-JTE, area-optimized multi-step etched-JTE, and multiple-shallow-trench junction termination extension (ST-JTE) are fabricated for different voltage ratings. The maximum termination efficiency of 93 % with a wide process window is achieved. The effect of etching process and fabrication uncertainties is considered in the design and investigated by measuring the etching steps and the corresponding breakdown voltages. By optimizing the termination technique in multiple shallow trenches, a higher blocking voltage with smaller termination length without any additional lithographic step is achieved. Finally, the characteristics of the high-temperature lateral BJTs will be presented.
Chapter 5. Characterization

5.1 High-Voltage and Ultra-High-Voltage 4H-SiC BJTs

In this section, we explain the measurement results of the fabricated 4.5-kV class and 15-kV class BJTs. The conducting and blocking $I_C-V_C$ characteristics as well as the Gummel plot of the BJTs provided a complete set of data required for the evaluation of the structures. In addition, the temperature dependency of the BJTs is investigated.

5.1.1 Conducting Characteristics

As explained in Chapter 3, several parameters affect the BJT conduction performance. In the first batch for high-voltage 4H-SiC BJTs, we used the established process as explained in Chapter 4. Therefore, by implementing the TCAD simulation and comparing the results with old batches [100], we expected to obtain relatively low current gain due to the surface recombination particularly in the emitter-base region. Fig. 5.1.a shows the $I_C-V_C$ forward characteristics of the 4.5-kV class 4H-SiC BJT with interdigitated finger design. The collector current versus maximum current gain plotted for the corresponding BJT is presented in Fig. 5.1.b. The maximum current gain of 40 at 250 mA (310 A/cm$^2$) is achieved.

In the next batch for ultra-high-voltage 4H-SiC BJTs, we optimized several parameters in the device design by the feedbacks of the measurement results of the first batch into the simulation and device design. Also, we performed the enhanced passivation process [17] to improve the BJT characteristics. Therefore, it was expected to achieve a higher maximum current gain due to significantly lower surface recombination in the emitter-base region. Fig. 5.2.a represents the $I_C-V_C$ forward characteristics of the 15-kV class BJTs with interdigitated finger design and hexagon-cell design with identical device size. The Gummel plot of the 15-kV class BJTs with interdigitated finger is presented in Fig. 5.2.b. The maximum current gain of 139 at $V_{BE} = 3.15$ V is achieved.

Figure 5.1. The measured (a) $I_C-V_C$ forward characteristics and (b) $\beta-I_C$ of the 4.5-kV class BJT.
5.1. High-Voltage and Ultra-High-Voltage 4H-SiC BJTs

Figure 5.2. (a) The $I_C-V_C$ forward characteristics and (b) the Gummel plot of the 15-kV class 4H-SiC BJTs.

Figure 5.3. The $\beta-I_C$ forward characteristics of the 15 kV-class 4H-SiC BJTs in (a) linear and (b) logarithmic scales.

This is in agreement with Fig. 5.2.a. Fig. 5.3 represents the $\beta-I_C$ of the devices at different collector-base voltages both in linear and logarithmic scales. As expected, the maximum current gain increases by raising the $V_{CB}$ from 0 V to 20 V. This is due to the base width modulation effect in the base region. The maximum current gain is measured at 50 mA which corresponds to a current density of 50 A/cm².

5.1.2 Blocking Voltage and Edge Termination Techniques

The junction termination extension is an important part of a high-voltage device that terminates the electric field at the edges of the device. The termination design and efficiency ensures the functionality of the termination in blocking behavior. The process variation dependency of the termination is another key factor in the design. It is desirable to have less sensitivity to the process uncertainties like etching and ion implantation variations. This will result in wider process window and higher wafer yield.
At KTH, an established edge termination technique based on double-step etching has been reported [36]. It is known that a higher number of etching steps could result in better electric field distribution. However, it requires more lithographic steps, which increases the total process cost and complexity. By employing TCAD simulation, we designed and optimized different termination techniques. Then different terminations were fabricated and measured and the results are compared in terms of termination efficiency, breakdown voltage, and total length of termination. More details on the properties and comparison of different termination techniques is described for better understanding of the value of the termination design in Chapter 3.

The influence of charges at the SiC/oxide interface on the breakdown voltage of SiC devices has been reported [224]. The presence of charges can change the electric field distribution and shift the electric field peaks toward the innermost edge for positive charges and outermost edge for negative charges [225]. The amount of charges in a certain area is affected by the etching process. This effect is considered in the simulation to optimize the JTE zones and their corresponding remaining doses. The electric field peak shifts occurs at the mesa edge and base edge for too high dose and too low dose, respectively. This effect is clearly investigated in TCAD simulation and has been experimentally observed with electroluminescence imaging of the device in reverse biased mode [36]. This type of measurement is useful to investigate the reliability of the device and to find the actual location in the device that the breakdown happens. It is worth noting that a controlled etching process is used for the etching steps of the termination area. The RIE etching is used to form \( \sim 50^\circ \) tilted angle with no trenching effect. The JTEs are formed from the innermost mesa toward the outermost mesa. This is found easier and more controllable to etch each JTE step separately.

As initial design for the edge termination, the same established concept is employed and modified for the 4.5 kV class. The total termination length of 210 \( \mu \)m with the equal length of the first and second JTEs and the remaining dose of \( 1 \times 10^{13} \) cm\(^-2\) and \( 2 \times 10^{13} \) cm\(^-2\) are the optimal values. The maximum breakdown voltage of 4.25 kV is measured for the conventional double-JTE. The breakdown voltage variation of 1900 V is measured when the JTE\(_1\) remaining dose varies from 0.9 to \( 1.4 \times 10^{13} \) cm\(^-2\). Although the double-JTE termination offers a wider dose range for the targeted breakdown voltage and hence wider process window compared with the single-JTE, it is desirable to have higher efficiency and less process sensitivity.

As mentioned earlier, it has been a common study to optimize the depths of the JTEs to find the optimum remaining dose for the JTEs whereas the JTEs mostly have equal lengths [36], [100], [132], [140], [238]. We investigated the effect of the length of the JTEs and it is found that the first JTE is the most effective one in the distribution.
of the electric field. We found that for a given total termination length ($\sum_{\text{JTE},i}$), a decremental JTE length ($L_{\text{JTE},i}$) from the innermost edge to the outermost mesa edge of the device will result in better modification of the electric field. Therefore, we demonstrated the JTE termination technique with descending length of the JTEs. In the next step, this concept is studied and implemented on the double-JTE, 3-zone, and 4-zone JTE terminations.

The schematic cross-sectional view and the microscopic image of the fabricated 4H-SiC with double-JTE is shown in Fig. 5.4. As explained in Chapter 4, the deep emitter and field stopper mesas are formed by ICP dry etching whereas the JTEs are realized by RIE etching. The fabrication process steps Fig. 5.5 compares the simulated electric field for the asymmetric double-JTE with different length of the JTE1 and JTE2 compared with the conventional double-JTE structure at their optimum dose for the applied reverse voltage of 6 kV. The electric field distribution is more uniform for the double-JTE with the descending length of the JTEs, which modulates the field crowding at the JTE and mesa corners. Consequently, it results in higher efficiency of the termination technique and higher breakdown voltage.

![Schematic Cross-Sectional View and Microscopic Image of 4H-SiC BJT with Double-JTE](image)

Figure 5.4. (a) the schematic cross-sectional view and (b) the microscopic image of the 4H-SiC BJT with modified double-JTE.

![Simulated Electric Field of 4H-SiC BJT with Double-JTE at the Cutline of AA'](image)

Figure 5.5. Simulated electric field of the 4H-SiC BJT with double-JTE at the cutline of AA'.
The dependency of the breakdown voltage to the length and dose of the JTEs is studied by TCAD simulations and the results are presented in Fig. 5.6. For the total termination length of 210 μm, the optimum length for the JTE\textsubscript{1} and JTE\textsubscript{2} are found to be 140 μm and 70 μm, respectively.

4H-SiC BJTs with different JTE length and remaining dose were fabricated. The actual depth and length of the JTE\textsubscript{1} and JTE\textsubscript{2} and the measured breakdown voltages are summarized in Table 5.1. At a remaining dose of 1.15×10\textsuperscript{13} cm\textsuperscript{-2} and 0.75×10\textsuperscript{13} cm\textsuperscript{-2} for the JTE\textsubscript{1} and JTE\textsubscript{2}, a maximum open-base breakdown voltage of 4975 V is achieved for the SiC BJT with the modified JTE length compared to a 4270 V for the equal length. By this modification, we obtained the $V_{BR}$ of 4.95 kV by improving the termination efficiency from 68 to 85 for no extra cost or fabrication process step. This technique can be employed for multi-step etched-JTE to minimize the total termination length and total device area. Moreover, it can be combined with other termination techniques such as etched rings, implanted field rings, bevel-JTE etc. (see Chapter 3) to further improve the termination efficiency.

We implemented the same descending length concept on the 3-zone and 4-zone junction termination extensions to realize 5.6 kV and 15 kV BJTs, respectively. A 3-zone JTE is designed to reach higher breakdown voltage by improving the termination efficiency. The microscopic image of the area optimized 3-zone JTE (O-JTE) is shown in Fig. 5.7. The 3-zone JTE with three different remaining doses of JTEs improves the electric field distribution inside the device. Then the concept of descending JTE length is applied to minimize the total area of the termination. Several designs with different length and remaining dose of the JTEs are simulated to find the optimum values. It is found that the descending length of 100 μm, 75 μm, and 25 μm with the remaining dose of 1.3×10\textsuperscript{13} cm\textsuperscript{-2}, 1.2×10\textsuperscript{13} cm\textsuperscript{-2}, and 1.1×10\textsuperscript{13} cm\textsuperscript{-2} are the optimized value for the JTE\textsubscript{1}, JTE\textsubscript{2}, and JTE\textsubscript{3}, respectively. The electric field distribution of the O-JTE.
TABLE 5.1. SUMMARY OF THE TERMINATION DESIGNS IMPLEMENTED ON 4H-SiC BJTs.

<table>
<thead>
<tr>
<th>L_{JTE1} (μm)</th>
<th>D_{JTE1} (×10^{13} cm^{-2})</th>
<th>L_{JTE2} (μm)</th>
<th>D_{JTE2} (×10^{13} cm^{-2})</th>
<th>V_{BR} (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>105</td>
<td>1.15</td>
<td>105</td>
<td>0.75</td>
<td>4270</td>
</tr>
<tr>
<td>140</td>
<td>1.15</td>
<td>70</td>
<td>0.75</td>
<td>4975</td>
</tr>
<tr>
<td>105</td>
<td>1.025</td>
<td>105</td>
<td>0.65</td>
<td>3850</td>
</tr>
<tr>
<td>140</td>
<td>1.025</td>
<td>70</td>
<td>0.65</td>
<td>4350</td>
</tr>
<tr>
<td>105</td>
<td>1.4</td>
<td>105</td>
<td>0.9</td>
<td>4125</td>
</tr>
<tr>
<td>140</td>
<td>1.4</td>
<td>70</td>
<td>0.9</td>
<td>4685</td>
</tr>
</tbody>
</table>

Figure 5.7. (a) the schematic cross-sectional view and (b) the microscopic image of the 4H-SiC BJT with modified 3-zone JTE.

compared with the asymmetric double-JTE and conventional double-JTE is shown in Fig. 5.8. A more uniform electric field distribution with lower field crowding is obtained for the O-JTE. The maximum breakdown voltage of 5.65 kV with the termination efficiency of 92 % for the O-JTE is measured. Thanks to the O-JTE design, a higher termination efficiency and higher breakdown voltage with 10 μm smaller total termination length is achieved at the expense of one additional lithographic step and etching process.

Figure 5.8. Simulated electric field along the BJT with O-JTE termination at the cutline of AA’.
Figure 5.9. The dependency of the breakdown voltage of a 4H-SiC O-JTE BJT to the dose of the JTEs.

The dependency of the breakdown voltage to the remaining dose of the JTEs for the O-JTE is shown in Fig. 5.9. As can be seen, the O-JTE design with three-step etchings provides wider process window and less sensitivity to the etching process. A 4-zone JTE is simulated and designed for this voltage class. Though a slightly more uniform electric field is obtained for the cost of additional lithographic and etching steps, however we skipped to implement it on 4.5-kV class and employed it for 15-kV ultra-high voltage class, which will be discussed later.

As mentioned earlier, it is well-known to implement structures such as floating guard rings in the termination to share the electric field peaks and alleviate the electric field crowding. In this section, by employing the same concept, a 4H-SiC BJT with multiple-shallow-trench JTE (ST-JTE) termination is demonstrated. Compared with multi-implanted or graded-etched JTEs, the trench structures are simultaneously formed by the first JTE with no extra mask. This makes the fabrication simpler and cheaper; while avoiding any further misalignment. The maximum \( V_{BR} \) of 5.85 kV is obtained that corresponds to 93 % of the theoretical value [239][240]. Even higher termination efficiency is yet achievable by increasing the number of trenches and squeezing the trenches, which requires lithography with higher resolution. Furthermore, the total termination length is shrunk to 180 µm compared to 200 µm and 210 µm for the O-JTE and double-JTE designs.

The cross-sectional schematic and the microscopic image of the ST-JTE are shown in Fig. 5.10. Trench structures, gradually decreasing in dimensions, have been formed on the first JTE. Depending on the design, the depth of the trenches can be controlled by the etching of the other layers with no additional mask. Considering the lithography limit to 1 µm, the number, width, and spacing of the trenches are optimized to reach the optimized electric field spreading. The optimized result is obtained for the ST-JTE
5.1. High-Voltage and Ultra-High-Voltage 4H-SiC BJTs

Figure 5.10. (a) the schematic cross-sectional view and (b) the microscopic image of the 4H-SiC BJT with modified ST-JTE.

Figure 5.11. The charge distribution in the ST-JTE design at the cutline of AA'.

with seven trenches as deep as 300 nm; whereas the spacing gradually increases from 1 μm to 7 μm and the width is gradually decreasing from 9 μm to 3 μm.

As already mentioned, the presence of charges at the oxide/SiC interface affects the electric field distribution in the termination area. The amount of charges in a certain area varies by forming the trenches. The optimum effective dose of $1.15 \times 10^{13}$ cm$^{-2}$ is found for the first JTE by simulation. Fig. 5.11 shows the space charge distribution at the oxide/SiC interface. Fig. 5.12 compares the simulated electric field for the ST-JTEs with different number of trenches with conventional double-JTE structure at their optimum dose for the applied reverse voltage of 6 kV. It is apparent that the electric field is shared and alleviated by the multiple trenches. Therefore, these trenches prevent the field crowding and shield the high field at the JTE and mesa corners. Hence, the electric field in the ST-JTE is more uniform. This results in higher efficiency of the edge termination.
It is apparent that higher number of trenches with smaller widths results in better electric field distribution. Considering the lithography limit to 1 μm, the optimized result is obtained for the ST-JTE with seven trenches. The smallest dimension required for realizing the ST-JTE with 14 trenches is 0.5 μm compared with 1 μm for the device with seven trenches. Although a finer photolithography improves the termination efficiency and sensitivity to the etching and doping variation (remaining dose) of the p-layer, it is recommended not to design too narrow trenches with dense spacing.

The remaining dose of the dopants in the JTEs is controlled by the dry etching process. Fig. 5.13 illustrates the $V_{BR}$ versus the p-layer dose for ST-JTE compared with conventional double-JTE. It is apparent that the ST-JTE BJTs have much less
5.1. High-Voltage and Ultra-High-Voltage 4H-SiC BJTs

Figure 5.14. The blocking I-V characteristics of the fabricated 4.5-kV-class 4H-SiC BJTs with different termination designs.

<table>
<thead>
<tr>
<th>Termination Design</th>
<th>$V_{BR}$</th>
<th>Efficiency</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Double-JTE [PAPER II]</td>
<td>4200</td>
<td>75</td>
<td>210</td>
</tr>
<tr>
<td>Modified Double-JTE [PAPER II]</td>
<td>4650</td>
<td>80</td>
<td>210</td>
</tr>
<tr>
<td>3-Zone O-JTE [PAPER III]</td>
<td>5600</td>
<td>92</td>
<td>200</td>
</tr>
<tr>
<td>Multiple-Shallow-Trench [PAPER IV]</td>
<td>5850</td>
<td>93</td>
<td>180</td>
</tr>
</tbody>
</table>

sensitivity to the etching variation. Moreover, simulation results show that higher number of trenches results in wider stable dose range, which will result in higher yield of the wafer. The maximum breakdown voltage variation ($\Delta V_{BR}$) of 700 V and 1700 V is measured for the ST-JTE and conventional double-JTE for 20 % variation in the remaining dose of the p-layer, respectively. Among the 26 measured ST-JTE devices, 80 % blocks more than 4.5 kV and the yield of high blocking ST-JTE BJTs (higher than 5 kV) is about 55 %. Fig. 5.14 illustrates the measured breakdown voltages for all fabricated BJTs with different termination structures. Table 5.2 summarizes the properties of the realized termination techniques. The ST-JTE design has the highest termination efficiency and shortest termination length.

As mentioned earlier, the four-step O-JTE design is designed and implemented to realize ultra-high-voltage 4H-SiC BJTs. The cross-sectional view and the layout design of the area optimized 4-zone O-JTE is shown in Fig. 5.15. By implementing the same concept of JTEs with descending length, the optimum length and dose of the JTEs are found by TCAD simulation, which are summarized in Table 5.3. The electric field distribution of the four-step O-JTE is shown in Fig. 5.16a. The dependency of the breakdown voltage to the remaining dose of the JTEs is presented in Fig. 5.16b. Due to the wide process window of the termination design, reasonable safe margin in the device design, and the controlled etching process [194], it is expected to achieve a high yield for the blocking voltage. It should be noted that the termination is slightly oversized to ensure the blocking capability of the BJTs. Therefore, optimization and
Figure 5.15. (a) the schematic cross-sectional view and (b) the layout design of the 15-kV 4H-SiC BJT with modified four-step O-JTE termination.

Table 5.3. The properties of the JTEs for the 15-kV 4H-SiC BJTs with 4-step O-JTE termination design.

<table>
<thead>
<tr>
<th>Step</th>
<th>Length (μm)</th>
<th>Etching Depth (nm)</th>
<th>Dose (x10^{13} cm^{-2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTE₁</td>
<td>350</td>
<td>260</td>
<td>1.1</td>
</tr>
<tr>
<td>JTE₂</td>
<td>263</td>
<td>80</td>
<td>0.9</td>
</tr>
<tr>
<td>JTE₃</td>
<td>175</td>
<td>80</td>
<td>0.7</td>
</tr>
<tr>
<td>JTE₄</td>
<td>87</td>
<td>120</td>
<td>0.45</td>
</tr>
<tr>
<td>Mesa</td>
<td>80</td>
<td>1500</td>
<td>---</td>
</tr>
</tbody>
</table>

Figure 5.16. (a) The simulated electric field along the 15-kV 4H-SiC BJT with 4-zone etched termination at the cutline of AA’ and (b) the dependency of the breakdown voltage of the 15-kV 4H-SiC BJT to the dose and length of the first JTE.

The reduction of the total termination length is necessary to do in the next batches in order to reduce the total device size or increase the forward area to total area ratio. As mentioned in the previous section, a high yield for the conducting characteristics of the 15-kV 4H-SiC BJTs is achieved thanks to the uniformity of the controlled etching process. Since the same process is used for the JTEs, it is expected to have less sensitivity and uncertainties in the etching depth. Fig. 5.17 illustrates the simulated and measured breakdown voltage for the fabricated BJTs. At the moment, our measurement setup is limited to 13 kV.
5.2 High-Temperature Lateral SiC BJTs

As mentioned earlier, SiC is an attractive material for high-temperature applications owing to its unique electrical and physical properties. In recent years, SiC lateral BJTs are shown to be a good candidate for high-temperature integrated circuits [17], [84]. Also, SiC integrated circuits based on field effect transistors (FETs) including MOSFETs, MESFETs, and JFETs operating at high temperatures have been demonstrated [241]–[249]. The advantages and disadvantages of each type is comprehensively discussed in [17], [250]. In recent years, monolithic integration of SiC high temperature lateral devices and circuits for high temperature applications has gained much interest and led to implementation of power integrated circuits such as linear voltage regulators and drivers [246], [249], [251]–[255]. This could result in smaller chip size, less power dissipation, and consequently lower total cost of the devices and modules. Moreover, monolithic integration decreases the total cost of process steps to design a process to accommodate both low- and high-voltage electronics or to eliminate the need of wire-bonding between the two chips. In this thesis, 4H-SiC lateral BJTs with different areas are designed and optimized for high temperature monolithic integrated circuits.

Although power devices are usually designed to high current and high voltage switches, there are plenty of uses for a power device that is not designed to be a switch or do not have a high blocking voltage. Such devices, in SiC bipolar, have extensive potentialities to be integrated together with other integrated circuits in this technology. Monolithic integration is an important concern for high-temperature systems. In design of a controlled switched-mode power supplies, for example, the controller can be fully built as an integrated circuit in a low-power process. However, the switching devices have to be built on a high-power process, maintaining a thick isolation layer.
above the substrate. This is where the high blocking voltage requirement comes as a limiting factor. An ultimate solution is to design a single fabrication process for both low-power and high-power circuits, considering the power isolation between the two. However, many process steps will be added that substantially contribute to the overall cost of the system. Moreover, having two different processes for low-power and high-power, implies that the connection between the low-power and high-power should be made externally. A usual way for connection is to use wire bonding. Bonding wires, however, introduce stray parasitics to the switching loop and add to the losses. Integration of lateral high-current SiC BJT can be made on the same process as of the low-power SiC bipolar circuits, and therefore provides a low cost and high-efficiency solution for some power management solutions. A circuit that can benefit a lot from a lateral high-current BJT is a linear voltage regulator in bipolar SiC [252]–[254]. The lateral high-current BJT can be used as the pass device of the linear voltage regulator. The pass device is never used in switching mode and therefore there is no need for high reverse blocking voltage and neither a thick isolation layer. Development of a high current lateral device is a cornerstone in achieving higher current ratings for the linear voltage regulator in bipolar SiC. Also, lateral high-current BJTs are genuine candidates to realize the output stage of the drivers driving power switches [246], [249], [255]. Such drivers normally need output currents in the range of 0.2–3 A depending on the power switch, however they do not require high blocking voltages (< 100 V). Therefore, high-current lateral BJTs can perfectly be fit for this application.

The lateral BJT technology for SiC-based integrated circuits has been developed [17]. Hereby, the established technology is used to realize the lateral 4H-SiC BJTs for high-temperature and high-current operations [PAPER IX]. Fig. 5.18 represents the schematic cross-sectional view of the lateral 4H-SiC BJT specifically developed for high-temperature electronics. To design a high-current BJT for this application, the optimization of cell geometry and device dimensions are taken into consideration. The influence of emitter width and geometry in SiC BJTs has been described in [80], [84], [92]. It has been shown that a wider emitter width results in a higher current gain though leads to higher on-resistance and lower current density. Depending on the application, a finger width of 30 μm to 50 μm is a good choice to save the area and to obtain a reasonable current gain and current density. On the other hand, two different layout designs are possible to scale an interdigitated BJT to achieve higher current capability: (1) parallelization of BJTs array with small emitter fingers connected with metal interconnections (2) comb-shape large BJT with long-fingers. The first approach was implemented in [197]. As described in Chapter 3, there is a trade-off between the on-resistance and maximum current gain of the BJTs with different width and length of the emitter fingers. On the other hand, it has been shown that a triple-sided lateral 4H-SiC BJTs provide significantly lower collector resistance than the single-sided
5.2. High-Temperature Lateral SiC BJTs

Figure 5.18. (a) The schematic cross-sectional view of the 4H-SiC lateral BJT. (Inset left) 3D-schematic view of the layout design and (inset right) the fabricated 4H-SiC BJT.

lateral 4H-SiC BJTs [17]. To combine the advantage of triple-sided design with the comb-shape layout design, a winding base region was designed. The base is surrounded by the comb-shape emitter fingers and the surrounding complementary comb-shape collector regions. The layout is such designed that each of the emitter, base, and collector regions are formed as single monolithic regions, which are individually covered by a metal layer for uniform current distribution to avoid voltage drop along its edges. The optimized layout design is implemented as low-voltage high current BJTs (see Fig. 5.18). A higher maximum current gain and higher current density are obtained for the BJTs with wider and longer emitter fingers. It should be noted that the metal contact is formed along the long fingers to diminish the voltage drop in the fingers. Considering the cell pitch and the maximum current density, the emitter length and width of 500 μm and 40 μm is selected for the high current BJTs.

Based on the optimized finger design, BJTs with three different sizes are fabricated and compared with the small-size (0.1 mm²) current driver (Chapter 3). Fig. 5.19 presents the forward characteristic of the fabricated 4H-SiC lateral BJTs. A comparable maximum current gain of >60 is measured for the BJTs. A breakdown voltage of >50 V is measured for the BJTs. Compared to the conventional BJT array design, significantly higher current density for the new BJT designs with optimized finger design is achieved. The on-resistances of 19 and 34 mΩ·cm² for the medium- and large-area BJTs compared to the 39 mΩ·cm² of the conventional BJT array design are measured.

To measure the current capability of the devices, the current gain of the fabricated BJTs is measured at different collector currents, as shown in Fig. 5.20.a. The β for the large-, medium-, and small-area BJTs is achieved at 11, 4, and 1.3 A compared to 0.25 A for the conventional BJT array design. The lower β of the large-area device is attributed to the self-heating effect caused by the high current drive of the BJT.
Figure 5.19. The measured $I_C-V_C$ characteristic of the fabricated (a) small-, (b) medium-, and (c) large-area 4H-SiC BJTs compared with (d) the BJT array fabricated as in [197]. Compared to the conventional design, a much higher current density and lower on-resistance is achieved for the new BJTs, which is due to the triple-sided layout design and optimized scaling.

Figure 5.20. The collector current versus maximum current gain plot of (a) the fabricated lateral 4H-SiC BJTs with different sizes at room temperature and (b) the medium- and large-size BJTs from room temperature to 500 °C.
5.3 High-current Darlington pairs

Table 5.4. Comparison of the different lateral BJT s and MOSFETs compared to the BJT-array design.

<table>
<thead>
<tr>
<th>BJT design</th>
<th>Active Area (mm²)</th>
<th>β</th>
<th>$J_C$ at β (A/cm²)</th>
<th>I (A)</th>
<th>$R_{ON}$ (mΩ·cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array</td>
<td>0.11</td>
<td>62</td>
<td>242</td>
<td>0.25</td>
<td>38.8</td>
</tr>
<tr>
<td>Small</td>
<td>0.26</td>
<td>62</td>
<td>504</td>
<td>1.3</td>
<td>14.2</td>
</tr>
<tr>
<td>Medium</td>
<td>0.98</td>
<td>62</td>
<td>409</td>
<td>4</td>
<td>19.2</td>
</tr>
<tr>
<td>Large</td>
<td>3.04</td>
<td>53</td>
<td>378</td>
<td>11</td>
<td>34.3</td>
</tr>
<tr>
<td>MOSFET [252]</td>
<td>0.76</td>
<td>--</td>
<td>263</td>
<td>2</td>
<td>--</td>
</tr>
<tr>
<td>MOSFET [253]</td>
<td>4</td>
<td>--</td>
<td>300</td>
<td>12</td>
<td>--</td>
</tr>
</tbody>
</table>

The high temperature performance of the medium- and large-size BJT s measured from room temperature to 500 °C is presented in Fig 5.20.b. The temperature-dependence behavior of BJT s is discussed in [17], [92], [136]. Table 5.4 summarizes the characteristics of the new BJT designs with three different areas compared to the BJT array design and MOSFETs. A significantly higher current density and lower on-resistance is achieved for the new BJT designs.

5.3 High-current Darlington pairs

As mentioned in Chapter 3, Darlington pair BJT s are attractive devices for high-current and high-power applications. Three different configurations for Darlington pairs for high-voltage, ultra-high-voltage, and high-temperature operations are designed and fabricated. In this section, we explain the measurement results of the high-voltage isolated Darlington pairs with intertwined design and high-temperature isolated lateral Darlington pairs.

5.3.1 Isolated Darlington with Intertwined Design

As mentioned earlier, the intertwined design is implemented on Darlington pairs in which the design is used to connect the driver and output BJT s. Fig. 5.21 shows the microscopic image of the fabricated Darlington pairs with the conventional corner-base topology and the center-base intertwined design.

The $I_C-V_C$ characteristic of the fabricated intertwined Darlington pair is shown in Fig. 5.22. To have the optimum design of the driver and output BJT s, the ratio of 1:8 was chosen for the active area of the driver and output BJT s. A comparable current gain of 380 is measured for the Darlington pairs whereas the intertwined design has about 14% higher current drive. The high current gain of Darlington pairs is achieved at a high current density, which results in self-heating of the device. This limits the drivability of the device at higher current rate and hence its safe operating area of the device at high powers.
Figure 5.21. (a) the microscopic image of the fabricated 4H-SiC Darlington pairs with (a) conventional corner-base topology and (b) center-base intertwined design. Both devices have equal die size of 700×700 μm².

Figure 5.22. $I_C-V_C$ characteristic of the Darlington pairs with center-base intertwined design. About 14% higher current with comparable current gain is achieved for the intertwined design compared to the corner-base design.

Figure 5.23. The (a) 3-D schematic layout design and (b) the fabricated lateral 4H-SiC Darlington pair for high-temperature application.
5.3. High-current Darlington pairs

5.3.2 High-Temperature Isolated Lateral Darlington Pair

As described earlier, lateral high-current 4H-SiC BJTs are required for a linear voltage regulator in bipolar SiC [254]. One can further improve it by using a lateral Darlington pair to provide higher current for the load. Due to this need, an isolated lateral Darlington pair was designed and realized as the output stage of a linear voltage regulator for the high-temperature applications. Fig. 5.23 presents the fabricated Darlington pair. The $I_C-V_C$ characteristic of the Darlington is presented in Fig. 5.24.a. A high current gain of 3300 at the output collector current of 15 A and forward voltage drop of 13 V at room temperature is achieved.

To further investigate the Darlington pair behavior, the current gain of the driver and output BJTs at different collector currents is also individually measured. As shown in Fig. 5.24.b, the maximum current gain of 62, 50, and 3300 for the driver BJT, output BJT, and the Darlington pair at 0.6 A, 11 A, and 15 A are achieved, respectively. It is worth noting that such high current density can melt down the metal interconnections, which should be considered during the device design and fabrication.
Chapter 6. Conclusion and Future Outlook

In this thesis, implantation-free 4H-SiC bipolar junction transistors (BJTs) have been designed, realized, and characterized for high-voltage, ultra-high-voltage, and high-temperature applications. The optimization and development was done for epilayer design, device design, and fabrication process. A special attention was dedicated to development of high-yield wafer-scale process steps as well as large-area device design to enable further realization of high-current devices for the real applications. The main achievements involved in this thesis are summarized in device design and fabrication process development:

Device design: Regarding the device design, a comprehensive study has been performed to optimize the device design in terms of epilayer design, cell geometry and scaling, edge termination techniques, and device layout design.

✓ Ultra-high-voltage (15-kV) 4H-SiC BJTs with a maximum current gain of 139 and a specific on-resistance of 579 mΩ·cm² at the current density of 89 A/cm² were realized, respectively. High-voltage (4.5-kV class) 4H-SiC BJTs with various cell designs including interdigitated finger, hexagon-, square-, circle-, and triangle-cell geometries were fabricated and compared. A maximum current gain of 40 and a specific on-resistance of 20 mΩ·cm² at the current density of 330 A/cm² for the high-voltage 4H-SiC BJTs have been achieved. The hexagon-cell geometry showed 42% higher current density and 21% lower specific on-resistance at a given maximum current gain compared to the interdigitated finger design. Several design topologies have been fabricated to investigate the current distribution in the device. Diagonally-aligned cells, corner-base, edge-base, and center-base topologies were designed and characterized. Also, a novel lithographic design called intertwined design has been developed to extend the forward area usage to 100%. In a small-area BJT, ~15% higher current drive was obtained from a center-base intertwined design. The intertwined design benefits from a center-base design, which provides significantly more uniform current distribution.

✓ Different edge termination techniques including a modified double-JTE, area-optimized 3-zone-JTE (O-JTE), and multiple shallow trench-JTE (ST-JTE) have
been designed and fabricated and a termination efficiency of $> 90\%$ was measured for the BJTs. Even though the ST-JTE has $10\%$ shorter length and one less lithographic step compared to O-JTE, a higher blocking voltage of 5.85 kV for the ST-JTE was achieved compared to 5.65 kV for the O-JTE, respectively.

- High-current 4H-SiC lateral BJTs and Darlington pairs (up to 15 A) have been demonstrated for high-temperature applications. The BJT characteristics were measured at elevated temperatures up to 500 °C and the devices were operational. The current gain decreased to $\sim 30\%$ of its maximum at room temperature.

Fabrication process development: Two main developments in fabrication process have been performed in this thesis: (1) improvement of the fabrication process steps that affect the performance of the 4H-SiC BJTs; (2) development of metal Ohmic contact technology for n- and p-type 4H-SiC.

- An enhanced surface passivation process has been developed to improve the SiC BJT performance. A maximum current gain of 139 for the 15-kV-class BJTs is achieved compared to 40 of the 4.5-kV-class BJTs with the established passivation.

- To stride toward industrialization of the SiC-based devices and ICs, we developed lift-off-free processes for the n- and p-Ohmic contact technologies. A wafer-scale self-aligned Ni-silicide (SALICIDE) process with two step annealing process for n-Ohmic contact technology for SiC has been developed. Also, a Ni-SALICIDE-based lift-off-free p-Ohmic contact technology for SiC has been developed. By simultaneous second annealing step for the n- and p-Ohmic contacts, no extra lithographic step was required. A contact resistivity of $5 \times 10^{-6} \, \Omega \cdot \text{cm}^2$ and $7 \times 10^{-4} \, \Omega \cdot \text{cm}^2$ for the n- and p-Ohmic contacts were measured, respectively.

Further works are required in this field to develop and industrialize the ultra-high-voltage SiC bipolar devices:

- Optimization of the base and collector designs to reduce the on-resistance and increase the current gain. Improving the edge termination design to reduce the total length and increase the termination efficiency for ultra-high-voltage devices.

- Investigation of the sacrificial oxidation and surface passivation in terms of oxide type, annealing ambient, annealing temperature, and annealing time. A comprehensive study of the lift-off-free p-Ohmic contact with different metal stacks to obtain a lower contact resistivity.

- Lifetime enhancement process is highly required to improve the device on-resistance with conductivity modulation in the device.

- Packaging of the large-area devices and evaluating the devices in high-current and switching conditions to evaluate the device performance in realistic conditions.
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“Yesterday This Day’s Madness did prepare;
To-morrow’s Silence, Triumph, or Despair:
Drink! for you know not whence you came, nor why:
Drink! for you know not why you go, nor where.”

Omar Khayyám