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The impact of atomic layer depositions on high quality Ge/GeO₂ interfaces fabricated by rapid thermal annealing in O₂ ambient

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Abstract

This work demonstrates high quality Ge/GeO₂ interfaces fabricated by O₂ RTA that are degraded by a good quality SiO₂ layer deposited by ALD. However, neither O₃ and H₂O precursors commonly used during subsequent high-k ALDs nor Si precursor AP-LTO-330 do not degrade the interface. Thus D_{it} increase after SiO₂ deposition is likely due to intermixing. Therefore, the effect of subsequent ALDs on the interface quality has to be considered while designing Ge-based gate stacks.

(Keywords: Germanium, GeO₂, high-k, ALD, D_{it})

Introduction

One of the most crucial challenges in realizing high-performance Ge devices is the gate stack formation. GeO₂ provides the lowest interface state density D_{it} values [1] and can be combined with high-k dielectrics to achieve low equivalent oxide thickness (EOT) [2]. However, the gate process conditions are important, e. g. O₃-based atomic layer deposition (ALD) on a thin GeO₂ layer has been shown to cause oxidation of Ge surface [3]. In this work we show that subsequent ALD on thermally grown GeO₂ layers can influence the Ge/GeO₂ interface quality.

Experimental

The fabrication process of Ge MOS capacitors is displayed in Fig. 1. After the cleaning of the n-Ge substrate native germanium oxide was removed with aqueous HF and HCl solutions. The samples were immediately loaded into the rapid thermal anneal (RTA) chamber and oxidation was carried out at 550°C for 5 s to 5 min. Then either SiO₂ layer was deposited by ALD at 350°C employing O₃ and AP-LTO-330 precursors or vacuum, H₂O, O₃ or AP-LTO-330 anneals were performed in ALD reactor at 350°C. Reference samples without SiO₂ deposition and annealing were also fabricated. Al gate metal was deposited by PVD and patterned.

Results and discussion

GeO₂ layer thermally grown by RTA displays an increasing growth characteristic with time (Fig. 2). Well-behaved capacitance-voltage (CV) curves with almost no frequency dispersion in accumulation obtained from n-Ge/GeO₂ gate stacks are shown in Fig. 3. D_{it} at the midgap was estimated from the CV curves in the following way. Theoretical CV curves [4] that assume a parabolic D_{it} distribution within

the bandgap were fitted to the measured curves. The parabolic distribution with a minimum at the midgap was employed due to the close resemblance to the symmetrical D_{it} distribution for GeO₂ observed in literature [1]. A good agreement between the measured and the theoretical curves from midgap to accumulation can be judged from Fig. 4. The influence of the D_{it} value at the midgap on low frequency CV characteristics is displayed in Fig. 5 where theoretical curves are plotted for a 5 nm EOT MOS capacitor showing an increase of the capacitance minimum with a rising D_{it} value. The lowest interface state density at the midgap that can be estimated using this method is around $1 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Measured CV characteristics of the n-Ge/GeO₂ MOS capacitors were used to extract low D_{it} at the midgap values in the range of $2.5 \cdot 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ which are shown in Fig. 6 at different GeO₂ CETs. However, a subsequent ALD of a high quality SiO₂ layer can damage the Ge/GeO₂ interface and to a greater extent for thinner GeO₂ as shown in Fig. 6 where a D_{it} increase is displayed after SiO₂ deposition. The following experiments were performed to investigate a possible source of the interface degradation in Ge/GeO₂/SiO₂ gate stacks as well as the effects other ALDs could have on good quality interfaces.

For scaled Ge channel MOSFETs GeO₂ is commonly integrated with high-k dielectrics that are deposited by ALD at elevated temperature. To investigate the effect of the main precursors employed during the high-k ALDs, H₂O and O₃ anneals were performed at 350°C on n-Ge/GeO₂ gate stacks that were fabricated by O₂ RTA at 550°C for 2 min. A vacuum anneal was also performed at 350°C to examine a possible effect of GeO desorption that has been reported to occur at elevated temperature in vacuum [5] and might take place during the deposition. Finally, the influence of the Si precursor AP-LTO-330 employed in SiO₂ ALD was investigated by performing an AP-LTO-330 anneal at 350°C. Almost no change in D_{it} was observed regardless of the anneal ambient (see Fig. 7).

Another factor that can cause the defects in the gate stack is metal deposition, i.e., if the metal reacts or intermixes with the oxide, or the deposition itself damages the underlying layers. The latter can be ruled out because Ge/GeO₂ gate stacks with good

interface quality and employing a rather thin oxide of ~ 3 nm CET were achieved while Ge/GeO₂/SiO₂ gate stacks are much thicker and thus would be affected less. To examine if the interface degradation in Ge/GeO₂/SiO₂ gate stacks was caused by the employment of Al as a gate metal, TiW/Al stack was used instead. The results are summarized in Fig. 8 showing that employing TiW instead of Al as a gate metal does not reduce D_{it} . Therefore, the choice of metal is not likely to be the factor that increases the interface state density in Ge/GeO₂/SiO₂ MOS capacitors.

A cross sectional scanning transmission electron microscope (STEM) bright field image of a Ge/GeO₂/SiO₂/Al MOS capacitor is displayed in Fig. 9a. Separate GeO₂ and SiO₂ layers (thicknesses of 6-7 nm and 7-7.5 nm respectively) can be distinguished as indicated in the figure. Another important feature of the image is an interfacial layer of Ge/GeO₂ that can be more distinctively seen as a bright line in the high resolution transmission electron microscope (HR TEM) image in Fig. 9b. This 3-4 nm thick layer is both crystalline and amorphous, and can appear this way due to the surface roughness since the information is gathered from a ~ 100 nm thick lamella. We have observed a RMS surface roughness of ~ 1.8 nm measured by AFM after HF and HCl dips. Moreover, GeO₂ and SiO₂ layers displayed in the HR TEM image are less distinguishable than in STEM image, and of slightly different thicknesses (6.5-7.5 nm and 8.5-9.5 nm respectively). This can be due to the surface roughness or an indication of an intermixture between layers.

Intermixing between GeO₂ and SiO₂ might be responsible for D_{it} degradation in Ge/GeO₂/SiO₂ gate stacks. If Si atoms are diffusing to Ge/GeO₂ interface and causing defects, the decreasing D_{it} with increasing GeO₂ thickness trend could be explained since less Si atoms would be able to reach Ge/GeO₂ interface if GeO₂ thickness is higher. Furthermore, Ge atoms could be diffusing into SiO₂ layer and leaving broken bonds at Ge/GeO₂ interface. This effect has been reported in Ge/GeO₂/HfO₂ gate stacks [6] where Ge diffused through HfO₂ layer and gathered at the surface. Ge diffusion would also explain D_{it} vs. GeO₂ thickness trend because more diffusion would occur from parts of GeO₂ layer that are closer to SiO₂ layer and thus further from the

interface for thicker GeO₂ layers. Therefore, it is likely that either Si or Ge diffusion is responsible for the D_{it} degradation in Ge/GeO₂/SiO₂ gate stacks.

Conclusion

Ge/GeO₂ gate stacks fabricated by O₂ RTA exhibit low D_{it} at the midgap in the range of $2.5\text{--}5\cdot 10^{11}$ cm⁻²eV⁻¹. The interface is not degraded by further vacuum, O₃, H₂O or AP-LTO-330 anneals in ALD chamber but a D_{it} increase is observed after a SiO₂ deposition that employs O₃ and AP-LTO-330 precursors. This degradation is likely to be caused by either Si diffusion to the interface or Ge diffusion towards SiO₂ layer. Therefore, the effect of subsequent ALDs on the interface quality has to be considered while designing Ge-based gate stacks.

Acknowledgments

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Fig. 1: Process flow of Ge MOS capacitor fabrication. Schematic view of the final structures is displayed on the right.

Fig. 2: GeO₂ CET versus O₂ oxidation time for n-Ge/GeO₂ MOS capacitors.

Fig. 3: Well-behaved CV characteristics of n-Ge/GeO₂ MOS capacitors oxidized by O₂ RTA. Inversion response is observed at room temperature.

Fig. 4: Comparison between a measurement and a theoretical CV curve that assumes a parabolic D_{it} distribution for: a) Ge/GeO₂ and b) Ge/GeO₂/SiO₂. Good agreement is observed around the midgap.

Fig. 5: Simulated CV characteristics of 5 nm EOT MOS capacitor with varying D_{it} in the midgap displaying an increase in midgap capacitance with increasing D_{it} .

Fig. 6: High D_{it} at midgap values for n-Ge/GeO₂/SiO₂ MOS capacitors decreasing with GeO₂ thickness in reference to n-Ge/GeO₂ MOS capacitors with good quality interface.

Fig. 7: D_{it} at midgap for as deposited, vacuum, H₂O, O₃ and AP-LTO-330 annealed n-Ge/GeO₂ gate stacks.

Fig. 8: D_{it} at midgap for Ge/GeO₂/Al, Ge/GeO₂/SiO₂/Al and Ge/GeO₂/SiO₂/TiW/Al stacks showing higher D_{it} for stacks with SiO₂ regardless of the gate metal employed.

Fig. 9: a) STEM Bright Field and b) HR TEM cross sectional images of Ge/GeO₂/SiO₂/Al MOS capacitor with comprising layers indicated.