<http://www.diva-portal.org>

Postprint

This is the accepted version of a paper presented at *19th International Conference on Solid-State Sensors, Actuators and Microsystems, TRANSDUCERS 2017, 18 June 2017 through 22 June 2017*.

Citation for the original published paper:

Wang, X., Bleiker, S J., Antelius, M., Stemme, G., Niklaus, F. (2017)
Narrow footprint copper sealing rings for low-temperature hermetic wafer-level packaging
In: *TRANSDUCERS 2017 - 19th International Conference on Solid-State Sensors, Actuators and Microsystems*, 7994077 (pp. 423-426). Institute of Electrical and Electronics Engineers (IEEE)
<https://doi.org/10.1109/TRANSDUCERS.2017.7994077>

N.B. When citing this work, cite the original published paper.

Permanent link to this version:

<http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-216276>

NARROW FOOTPRINT COPPER SEALING RINGS FOR LOW-TEMPERATURE HERMETIC WAFER-LEVEL PACKAGING

Xiaojing Wang¹, Simon J. Bleiker¹, Mikael Antelius², Göran Stemme¹, and Frank Niklaus¹

¹Department of Micro and Nanosystems, KTH Royal Institute of Technology, Sweden and

²APR Technologies AB, Sweden

ABSTRACT

This paper reports a narrow footprint sealing ring design for low-temperature, hermetic, and mechanically stable wafer-level packaging. Copper (Cu) sealing rings that are as narrow as 8 μm successfully seal the enclosed cavities on the wafers after bonding at a temperature of 250 $^{\circ}\text{C}$. Different sealing structure designs are evaluated and demonstrate excellent hermeticity after 3 months of storage in ambient atmosphere. A leak rate of better than 3.6×10^{-16} mbarL/s is deduced based on results from residual gas analysis measurements. The sealing yield after wafer bonding is found to be not limited by the Cu sealing ring width but by a maximum acceptable wafer-to-wafer misalignment.

INTRODUCTION

Wafer-scale hermetic packaging is indispensable for high-volume manufacturing of various MEMS devices such as inertial sensors and resonators [1]. Wafer bonding techniques including direct bonding, anodic bonding, and intermediate layer bonding have been developed to achieve hermetic sealing of MEMS devices [2]. Direct bonding is typically demanding in terms of process temperatures and quality of the surfaces to be bonded [3, 4]. For intermediate layer bonding, materials including polymers, glasses, and metals have been investigated, among which metals offer the lowest permeability to gases and moisture [5]. The excellent hermeticity and mechanical strength of metals allow significant reduction of the footprint of sealing ring, which ultimately facilitates die-size miniaturization, thus making metal-based wafer-level hermetic packaging an advantageous choice compared to the other technologies.

Much effort has been devoted to minimize the metal sealing structure footprint for reducing die-size and process cost. Wafer-level encapsulation is reported to be achieved with 1.5 – 7 μm -wide sealing rings of Au, but the mechanical support needs to be enhanced by additional solder pads featuring dimensions of over 100 μm [6] or by polymer underfill [7, 8]. 3 μm -wide Al sealing rings have been reported for wafer-level hermetic packaging at a high temperature of 450 $^{\circ}\text{C}$ [9]. However, low-temperature processing is desired in the packaging of thermally sensitive MEMS structures and CMOS circuits. Cu is a preferred material used in state-of-the-art 3D integration and has been reported to yield hermetic wafer-level packaging at a low temperature of 250 $^{\circ}\text{C}$ using 3 – 50 μm -wide sealing rings [10]. However, additional large surrounding bonding areas are incorporated to ensure mechanical stability. On the other hand, Cu has higher mechanical strength than Au and Al, which promises further reduction of the sealing ring footprint. We have reported a wafer-scale vacuum packaging method based

on plastic deformation and low-temperature welding of Cu sealing rings without additional mechanical enhancement of the bond [11]. In this paper, we present an extended analysis of the sealing yield distribution on the bonded wafers and the influence of the sealing ring width and number of grooves on the sealing yield.

CONCEPT AND WAFER PROCESS

The sealing concept is illustrated in Figure 1. The Cu sealing rings on the device wafer are compressed with the annular grooves (covered by a thin Cu layer) in the cap wafer, inducing very high local pressures at the small overlapping areas between the Cu rings and cap wafer. The high localized pressures exceed the yield stress of the Cu and result in plastic deformation of the Cu rings and low-temperature welding of Cu-Cu interfaces, thus achieving hermetic sealing of the enclosed cavities [11].

Figure 1: Schematic drawing of the Cu sealing ring structures. The close-up images indicate the three basic sealing ring designs with 1, 2, and 3 grooves in the cap wafer, respectively.

Table 1: Primary dimensions and variations of the different sealing ring designs shown in Figure 1.

Number of grooves	1 / 2 / 3
Overlap width	1 μm / 2 μm / 3 μm
Height of Cu ring	5.2 μm
Width of Cu ring	6 – 21 μm
Width of groove	3.25 μm / 4 μm
Groove wall thickness	1.5 μm / 3 μm
Total number of design variations	15

Different sealing ring designs are incorporated on the same wafer. The key design variables are the number of grooves and overlap width at the edges of the Cu sealing rings, as specified in the Table 1. These variations translate into the width of the Cu rings, reflecting different potential overall overlapping areas for distinct designs.

The proposed wafer-level process scheme is depicted in Figure 2. The cap wafer was firstly process by Si deep reactive ion etching (DRIE) to form the annular grooves and cavities to be sealed with a depth of 8 μm . Next, a 10 nm/300 nm-thick Ti/Cu layer was deposited by sputtering to cover the annular grooves. For the device wafer, 5.2 μm -high Cu sealing rings were electroplated on top of a 10 nm/30 nm-thick sputtered Ti/Cu seed layer, as shown in Figure 2(a). After alignment of the two wafers, the wafer stack was transferred into a wafer bonder (CB8, Suss MicroTec). The bond-chamber was pumped down to a pressure of 7×10^{-5} mbar, and then the wafer chucks were heated up to 250 $^{\circ}\text{C}$. A bonding force of 20 kN was applied to the wafer stack and was kept constant for 25 minutes, as explained in Figure 2(b). This force translates into a high local pressure of ~ 550 MPa at the small overlapping Cu-Cu areas, which is nearly 2.4 times the reported yield strength of electroplated Cu [12] and thus facilitates plastic deformation of the Cu rings and sealing by Cu-Cu welding. After this, the wafer chucks were cooled down and the bonding force was removed. Finally, the chamber was vented to atmospheric pressure.

Figure 2: Process scheme for wafer-level vacuum sealing. (a) Cap wafer preparation by Si DRIE of annular grooves and cavities and subsequent Cu deposition by sputtering. Electroplating of the Cu rings on the device wafer. (b) Wafer bonding and vacuum sealing inside a vacuum chamber at 250 $^{\circ}\text{C}$. (c) Cap wafer thinning to induce cavity diaphragm deflections for hermeticity evaluation.

In order to assess the sealing yield after wafer bonding, the cap wafer was thinned down by isotropic Si

dry etching to form thin diaphragms (75 – 95 μm thick) on top of the cavities, as illustrated in Figure 2(c). The diaphragms will deflect when placed in atmospheric pressure if the vacuum cavities have been successfully sealed. This method offers a direct way to observe the sealing yield distribution on the bonded wafers, and can be used to evaluate long-term leak rate of the seals [13].

RESULTS AND DISCUSSION

Sealing Yield Evaluation

The distribution of the sealing yield on the bonded wafers is illustrated in Figure 3. 93 out of the 124 cavities were successfully sealed after wafer thinning. After 3 months of storage in ambient atmosphere, only 1 of the 93 sealed cavities failed, demonstrating the excellent reliability of the narrow Cu sealing rings.

Figure 3: Top view of the distribution of the sealing yield on the wafers after bonding and after 3 months of storage in ambient atmosphere, respectively.

As can be seen from Figure 3, many failed cavities appear near the edges of the wafers. These cavities feature the narrowest sealing design, which contain 6 μm -wide Cu rings with only 1 μm overlap width at the edges of the Cu rings. The failure of these seals is most probably due to their low tolerance of only 1 μm for wafer-to-wafer misalignment. Except for this design-related tendency, we have not observed any significant failure dependency on the location of the cavity on the wafers. There is a region in the lower half of the wafers in Figure 3 where many failed cavities are clustered together. This is possibly attributed to irregularities in thickness of the Cu rings from electroplating process or caused by surface contamination from other sources, which might impair the complete formation of the hermetic Cu-Cu bond.

In order to evaluate the dependency of the sealing yield on the Cu ring design, the corresponding yield after 3 months of storage is plotted in Figure 4. The best yield

of up to 100% was achieved with the 2-groove design and Cu ring widths between 11.5 and 15.5 μm . However, no significant dependency on the width of Cu rings was observed, which indicates that the sealing yield is not limited by the Cu ring width. As discussed previously, the complete failure of 6 μm -wide sealing rings can be explained by their low wafer-to-wafer alignment tolerance of only 1 μm . A sufficient alignment tolerance therefore enables very narrow sealing structures, as demonstrated by the 8 μm -wide sealing ring providing a good sealing yield of 75%.

Figure 4: Sealing yield with respect to Cu ring width and number of grooves after 3 months of storage in ambient pressure.

After 3 months of storage in ambient pressure, the wafer stack was diced into individual dies, as shown in the close-up images in Figure 3. Different sealing ring designs experienced decreases in the sealing yield after dicing to different extents, but still no significant dependency on the Cu ring width was observed. The fact that all the seals with 8 μm -wide sealing rings survived the dicing procedure indicates again that this bonding technique enables very narrow sealing footprint.

Cross-sections of the bond interfaces of different sealing ring designs were inspected by scanning electron microscopy (SEM), as shown in Figure 5. They show a uniform, welded Cu layer where part of the Cu has been pressed into the grooves, as intended. The dashed line in Figure 5(d) indicates a 1.2 μm -wide (designed as 1.5 μm) broken wall between grooves, while the 2.7 μm -wide groove walls are all intact. This local breakage is probably ascribed to shear stresses induced during the wafer bonding process. On the other hand, this also implies that the aspect ratio of the groove wall should be relatively small to ensure the mechanical integrity of the sealing structures.

To investigate more precisely the vacuum levels inside the sealed cavities, residual gas analysis (RGA) (SAES Getters S.p.A, Italy) was conducted for the diced individual cavities 146 days after bonding. The achieved sealed pressure was as low as 2.6×10^{-2} mbar, which indicates a leak rate better than 3.6×10^{-16} mbarL/s [11]. This conservatively calculated leak rate is much smaller than the reported data for seals using other packaging

methods including Cu-Cu thermo-compression bonding [10], Ni/Sn solder bonding [14], Au-Sn eutectic bonding [15], and our previous work based on Au sealing rings [6] and Au bumps [16].

Figure 5: Cross-sectional SEM images of the bonding interfaces of different sealing ring designs. (a) 1-groove design (2 μm overlap width). (b) 2-groove design (3 μm overlap width). (c) and (d): 3-groove designs (3 μm overlap width) with 3 μm and 1.5 μm -thick walls between the grooves.

In terms of the hermeticity of different sealing ring structures, designs with 3 grooves tend to provide smaller leak rates than 2-groove designs based on the results from the RGA. However, the limited data from only 3 chips is not sufficient for drawing any firm conclusions. Nevertheless, multi-groove sealing ring designs could potentially induce larger Cu-Cu bond areas than single-groove designs, thus resulting in better hermeticity, although associated with higher bonding forces and larger sealing footprints. In addition, multi-groove designs have higher tolerance to wafer-wafer misalignment since not all of the grooves have to be closed to achieve successful sealing.

Design Reference

Table 2: Influence of the key sealing ring design variables on packaging performance.

Packaging performance	Overlap width of the Cu ring $\uparrow$	Number of grooves / Cu ring width $\uparrow$
Die size reduction	–	–
Hermeticity & Mechanical robustness	+	+
Tolerance towards wafer misalignment	+	+
Bonding force reduction	–	–

Based on the results and discussion above, we can summarize a general design reference specifying the

influence of the key designs variations on the packaging performance, as listed in Table 2. For the sake of die size miniaturization (smallest sealing ring footprint), the design with 1 groove in the cap wafer and 2 μm overlap width at the edges of Cu rings is recommended for typical wafer-wafer alignment tool capabilities. All other basic parameter values are shown in Table 3. Multi-groove structures can be designed using the same groove dimensions from the single-groove design in combination with a proper groove wall thickness.

Table 3: Recommended design parameter values for typical sealing structures under similar bonding conditions as described in this paper.

Design parameter values		Typical Values
Cu ring	Overlap width	2 μm
	Height of Cu ring	4 – 5 μm
	Width of Cu ring	8 μm
	(Single-groove design)	
Single-groove design	Width of groove	4 μm
	Depth of groove	6 – 8 μm
Multi-groove design	Groove wall thickness	3 μm

CONCLUSION

A Cu-based sealing ring design featuring a small footprint for wafer-scale hermetic packaging is described and evaluated. In our university clean-room environment and using a process that has not been optimized, we demonstrate a vacuum sealing yield of 75% for cavities with Cu sealing rings that are as narrow as 8 μm even after wafer dicing. Residual gas analysis indicates a leak rate better than 3.6×10^{-16} mbarL/s. A design reference is proposed for practical applications. The proposed narrow footprint sealing ring design and process offer a very attractive approach for low-temperature hermetic wafer-scale packaging of a wide variety of MEMS and IC devices.

REFERENCES

- [1] R. Gooch, T. Schimert, W. McCardel, B. Ritchey, D. Gilmour, and W. Koziarz, "Wafer-level vacuum packaging for MEMS", *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 17, no. 4, pp. 2295-2299, 1999.
- [2] M. A. Schmidt, "Wafer-to-wafer bonding for microstructure formation", *Proc. IEEE*, vol. 86, no. 8, pp. 1575–1585, 1998.
- [3] C. Harendt, H. G. Graf, B. Hofflinger, and E. Penteke, "Silicon fusion bonding and its characterization", *J. Micromech. Microeng.*, vol. 2, no. 3, pp. 113-116, 1992.
- [4] F. Niklaus, G. Stemme, J.-Q. Lu, and R. J. Gutmann, "Adhesive wafer bonding", *J. Appl. Phys.*, vol. 99, no. 3, p. 031101, 2006.
- [5] S. Farrens, "Metal based wafer level packaging", *Proc. 5th Int. Wafer-Level Packag. Conf. (IWLPC)*, Oct. 2008, pp. 8-14.
- [6] M. Antelius, G. Stemme, and F. Niklaus, "Small footprint wafer-level vacuum packaging using compressible gold sealing", *J. Micromech. Microeng.*,

- vol. 21, no. 8, p. 085011, 2011.
- [7] F. J. Aparicio et al., "Dye-based photonic sensing systems", *Sens. Actuators B: Chem.*, vol. 228, pp. 649-657, 2016.
- [8] M. Lapisa, M. Antelius, A. Tocchio, H. Sohlström, G. Stemme, F. Niklaus, "Wafer-level capping and sealing of heat sensitive substances and liquids with gold gaskets", *Sens. Actuators A: Phys.*, vol. 201, pp. 154-163, 2013.
- [9] C. H. Yun, J. R. Martin, E. B. Tarvin, and J. T. Winbigler, "Al to Al wafer bonding for MEMS encapsulation and 3-D interconnect", *Proc. IEEE 21st Int. Conf. Micro Electro Mech. Syst. (MEMS)*, Jan. 2008, pp. 810-813.
- [10] J. Fan, D. F. Lim, L. Peng, K. H. Li, and C. S. Tan, "Low temperature Cu-to-Cu bonding for wafer-level hermetic encapsulation of 3D microsystems", *Electrochem. Solid-State Lett.*, vol. 14, no. 11, pp. H470-H474, 2011.
- [11] X. Wang, S. J. Bleiker, M. Antelius, G. Stemme, and F. Niklaus "Wafer-level vacuum packaging enabled by plastic deformation and low-temperature welding of copper sealing rings with a small footprint", *J. Microelectromech. Syst.*, vol. PP, no. 99, pp. 1-9, 2017, in print.
- [12] D. T. Read, Y. W. Cheng, and R. Geiss, "Morphology, microstructure, and mechanical properties of a copper electrodeposit", *Microelectron. Eng.*, vol. 75, no. 1, pp. 63-70, 2004.
- [13] A. Goswami and B. Han, "On ultra-fine leak detection of hermetic wafer level packages", *IEEE Trans. Adv. Packag.*, vol. 31, no. 1, pp. 14-21, 2008.
- [14] W. Yu-Chuan, Z. Da-Peng, X. Wei, and L. Luo, "Wafer-lever hermetic package with through-wafer interconnects", *J. Electron. Mater.*, vol. 36, no. 2, pp. 105-109, 2007.
- [15] S.-H. Choa, "Reliability study of hermetic wafer level MEMS packaging with through-wafer interconnect", *Microsyst. Technol.*, vol. 15, no. 5, pp. 677-686, 2009.
- [16] M. Antelius, A. C. Fischer, N. Roxhed, G. Stemme, and F. Niklaus, "Wafer-level vacuum sealing by coining of wire bonded gold bumps", *J. Microelectromech. Syst.*, vol. 22, no. 6, pp. 1347-1353, Dec. 2013.

CONTACT

*X. Wang, tel: +46-737652387; xiawang@kth.se.