Fabrication of Group IV Semiconductors on Insulator for Monolithic 3D Integration

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Abstract

The conventional 2D geometrical scaling of transistors is now facing many challenges in order to continue the performance enhancement while decreasing power consumption. The decrease in the device power consumption is related to the scaling of the power supply voltage ($V_{dd}$) and interconnects wiring length. In addition, monolithic three dimensional (M3D) integration in the form of vertically stacked devices, is a possible solution to increase the device density and reduce interconnect wiring length. Integrating strained germanium on insulator (sGeOI) pMOSFETs monolithically with strained silicon/silicon-germanium on insulator (sSOI/sSiGeOI) nMOSFETs can increase the device performance and packing density. Low temperature processing (<550 ºC) is essential as interconnects and strained layers limit the thermal budget in M3D. This thesis presents an experimental investigation of the low temperature (<450 ºC) fabrication of group IV semiconductor-on-insulator substrates with the focus on sGeOI and sSiGeOI fabrication processes compatible with M3D.

To this aim, direct bonding was used to transfer the relaxed and strained semiconductor layers. The void formation dependencies of the oxide thickness, the surface treatment of the oxide and the post annealing time were fully examined. Low temperature SiGe epitaxy was investigated with the emphasis on the fabrication of Si$_{0.5}$Ge$_{0.5}$ strain-relaxed buffers (SRBs), etch-stop layer, and the device layer in the SiGeOI and GeOI process schemes. Ge epitaxial growth on Si as thick SRBs and thin device layers was investigated. Thick (500 nm-3 µm) and thin (<30 nm) relaxed GeOI substrates were fabricated. The latter was fabricated by continuous epitaxial growth of a 3-µm Ge (SRB)/Si$_{0.5}$Ge$_{0.5}$ (etch stop)/Ge (device layer) stack on Si. The fabricated long channel Ge pFETs from these GeOI substrates exhibit well-behaved IV characteristics with an effective mobility of 160 cm$^2$/Vs.

The planarization of SiO$_2$ and SiGe SRBs for the fabrication of the strained GeOI and SiGeOI were accomplished by chemical mechanical polishing (CMP). Low temperature processes (<450 ºC) were developed for compressively strained GeOI layers (# ~ -1.75 %, < 20 nm), which are used for high mobility and low power devices. For the first time, tensile strained Si$_{0.5}$Ge$_{0.5}$ (# ~ 2.5 %, < 20 nm) films were successfully fabricated and transferred onto patterned substrates for 3D integration.

Keywords

monolithic three dimensional (M3D) integration, strained germanium on insulator (sGeOI) pMOSFETs, silicon/silicon-germanium on insulator (sSOI/sSiGeOI) nMOSFETs, Si$_{0.5}$Ge$_{0.5}$ strain-relaxed buffer (SRB), direct bonding, chemical mechanical polishing (CMP), compressively strained GeOI, tensile strained Si$_{0.5}$Ge$_{0.5}$OI