Area-Efficient Switched-Capacitor Integrator with Flicker Noise Cancellation

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Abstract—A fully differential switched-capacitor circuit that combines the functionality of a voltage buffer and an integrator is proposed. The employed switching scheme exhibits intrinsic flicker noise canceling properties, whereas conventional techniques require additional circuit components. The circuit has been designed in a 0.18 μm CMOS process for 1.8 V supply. The estimated power consumption is 13.5 μW, while the occupied area is 121x442 μm^2. Area-efficient design is achieved by exploiting the correlation between the effective noise bandwidth and noise floor density in the proposed circuit. The sampled input referred noise floor is -133 dBV/$\sqrt{Hz}$, which is remarkably low when considering that the sampling capacitance is just 1.8 pF.

Keywords—*switched-capacitor integrator, flicker noise canceling, thermal noise limit.*

I. INTRODUCTION

Switched-capacitor (SC) circuits are the critical blocks of discrete-time systems, which are used for implementing various transfer functions in precision analog and high dynamic range mixed-signal applications [1], [2]. However, due to their sampling nature, they are prone to out-of-band noise-folding that originates from the noisy switches and CMOS amplifiers. Consequently, SC circuits are plagued with a larger noise floor density than an equivalent continuous-time circuit [2].

Thermal noise is recognized as the dominant noise contributor in SC circuits, which is commonly referred to as the kT/C limit. Recently, limit breaking techniques have been proposed to circumvent this trade-off [3], [4]. For instance, in [3], the correlation between the sampling bandwidth and the dominant noise source is weakened by introducing extra design freedom between them. Additionally, the active thermal noise cancellation techniques, presented in [3], [4], show even better noise reduction at the cost of higher complexity.

Although thermal noise contribution is considerable over a wide frequency band, flicker noise can be an overwhelming source at low frequencies if it is not suppressed. Flicker noise canceling techniques, such as correlated double sampling or chopping [5]–[10], usually require additional capacitors and switches for their implementation.

In this paper, we propose a simple area-efficient SC integrator with built-in flicker noise suppression. Moreover, compared to conventional techniques, the proposed integrator does not require any additional circuitry. Also, we show that instead of breaking the thermal noise limit it can be advantageous to exploit it for significant capacitor area reduction at the cost of small deterioration in the noise performance.
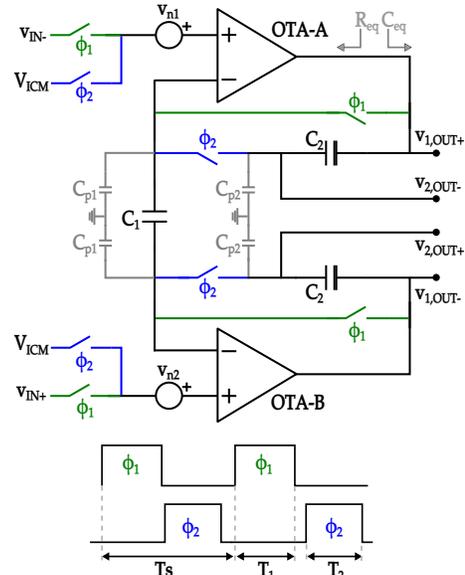

Fig. 1. Proposed integrator circuit and switching waveform diagrams.

II. CIRCUIT DESCRIPTION

The proposed SC integrator circuit is shown in Fig. 1. The main principle behind the proposed circuit is that it combines the functionalities of a voltage buffer and an integrator. Compared to [11], in which a single source-follower with a three-phase switching scheme was used to achieve the same principle, in this work we employ a simpler two-phase switching scheme with OTAs, which can provide a comparatively better performance in terms of gain, voltage headroom and linearity.

The operation of the proposed integrator is as follows. During the sampling phase, ϕ_1, the two OTAs are configured as unity-gain amplifiers, which provide voltage buffering and storage of v_{in} across the sampling capacitor C_1. Since v_{in} is stored differentially, the sampling capacitance is effectively double.

During the integration phase, ϕ_2, the capacitor C_2 is switched to form an inverting integrator with C_1, while the non-inverting input of the OTAs is connected to the input common-mode voltage, V_{ICM}. The role of V_{ICM} is to provide a virtual ground reference for controlling the charge transfer between C_1 and C_2, such that only the differential signal is integrated. By using the same OTAs in both clock phases, the

power consumption can be reduced when a dedicated buffer is needed to drive the SC circuits [10]. Consequently, the mismatch between the OTAs should be minimized in order to achieve good common-mode rejection.

Depending on the active phase, the circuit has two different outputs: $v_{1,\text{out}}$ at the end of ϕ_2, and $v_{2,\text{out}}$ at the end of ϕ_1. The transfer function for $v_{1,\text{out}}$ output is given by

$$\frac{V_{1,\text{out}}}{V_{\text{in}}}(z) \approx \frac{-\left(\frac{C_1^*}{C_2}\right)z^{-T_2/T_s}}{1 + \frac{C_1^*+C_{p2}}{C_2(1+A_0)} - \left(1 + \frac{C_{p2}}{C_2(1+A_0)}\right)z^{-1}}, \quad (1)$$

while $v_{2,\text{out}}$ is given by

$$\frac{V_{2,\text{out}}}{V_{\text{in}}}(z) \approx \frac{1 + \frac{C_1^*+C_{p2}}{C_2(1+A_0)} - \left(1 - \frac{C_1^*}{C_2}\right)z^{-1}}{\left(1 + \frac{C_1^*+C_{p2}}{C_2(1+A_0)}\right)\left(1 + \frac{C_{p2}}{C_2}\right) - z^{-1}}, \quad (2)$$

where $C_1^* = 2C_1 + C_{p1}$, $C_{p1,2}$ are the parasitic plate capacitances, while A_0 is the amplifier DC gain.

Expressions (1) and (2) show that the proposed circuit can be used for example as a delaying or as a delay-less integrator depending on the values of C_1 and C_2. The accuracy of the charge transfer is sensitive to C_{p1} in both cases, while C_{p2} has a significant impact on the low frequency gain of (2), as it can be seen from the example shown in Fig. 2a for $C_1 = C_2$ and $T_1 = T_2 = 0.45T_s$. This can introduce a limitation on the maximum routing capacitance, depending on the accuracy requirements for the ratio C_1/C_2. Therefore, the proposed integrator is limited to applications with moderate DC gain requirements (e.g. 40-50 dB).

Although (1) and (2) have a similar frequency response with respect to v_{in}, the OTA$_{A,B}$ noise, $\bar{v}_{n1,2}$, is treated differently at the two outputs. For instance, at the $v_{1,\text{out}}$, the noise is integrated by the following transfer function

$$\frac{V_{1,\text{out}}}{V_{n1,2}}(z) \approx \frac{1 + \frac{C_1^*+C_{p2}}{C_2} - \left(\frac{C_1^*}{C_2}\right)\left(z^{-T_2/T_s} - z^{-1}\right)}{1 + \frac{C_1^*+C_{p2}}{C_2(1+A_0)} - z^{-1}\left(1 + \frac{C_{p2}}{C_2(1+A_0)}\right)}, \quad (3)$$

while, in the case of $v_{2,\text{out}}$, the $\bar{v}_{n1,2}$ is high-pass filtered by

$$\frac{V_{2,\text{out}}}{V_{n1,2}}(z) \approx \frac{1 + \frac{C_1^*+C_{p2}}{C_2(1+A_0)} - z^{-1} - \left(\frac{C_1^*}{C_2}\right)\left(z^{-T_1/T_s} - z^{-1}\right)}{\left(1 + \frac{C_1^*+C_{p2}}{C_2(1+A_0)}\right)\left(1 + \frac{C_{p2}}{C_2}\right) - z^{-1}}, \quad (4)$$

as it is shown in Fig. 2b. The cancellation of $\bar{v}_{n1,2}$ at low frequencies is achieved by storing the previous noise sample across C_2, during $\phi_2(nT - T/2)$, and then comparing it against the present sample, which is buffered to $v_{1,out}$ output during $\phi_1(nT)$. In principle, the slowly changing $\bar{v}_{n1,2}$ samples are differentiated in time, which is more commonly referred to as correlated double-sampling (CDS) [7]. The ratio of expressions (4) and (2) represents $\bar{v}_{n1,2}$ referred to the v_{in} input, and it's magnitude is shown in Fig. 2c. Note that the frequency response in Fig. 2c is insensitive to the parasitic plate capacitances $C_{p1,2}$. For higher frequencies, specifically at the multiples of the sampling frequency (f_s), the successive noise samples occur in-phase, and are integrated over time. As a result, the aliased high-frequency thermal noise will down-convert to DC and it will increase the noise floor, while the
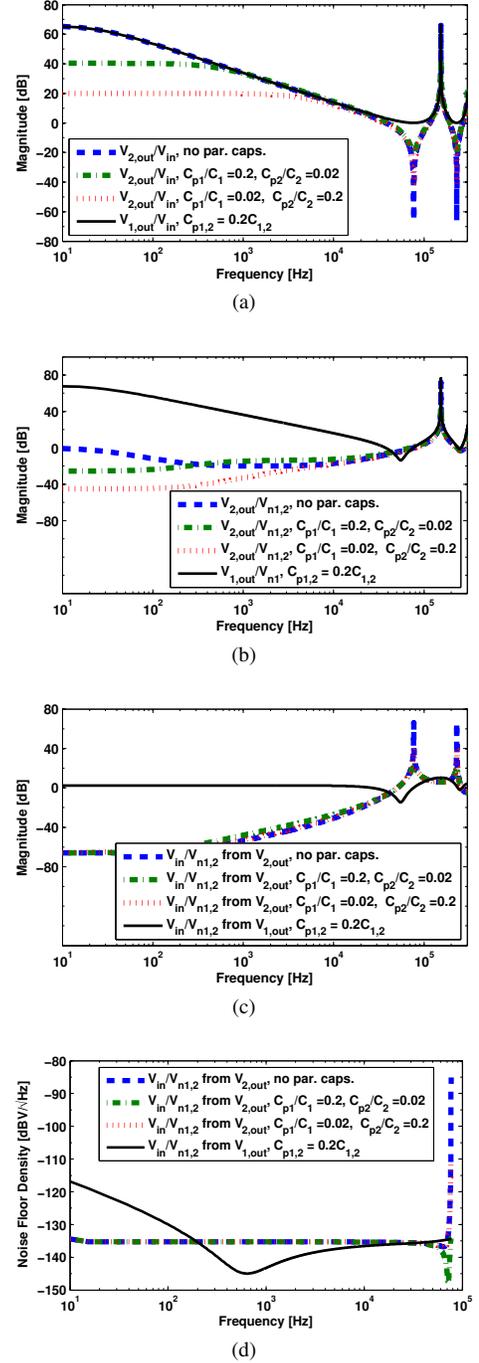

(a)

(b)

(c)

(d)

Fig. 2. Frequency responses of: a) the magnitude of the signal transfer functions (1) and (2); b) The magnitude of the noise transfer functions (3) and (4); c) Transfer function of the OTA noise referred to the input of the integrator; d) Input noise floor after aliasing.

flicker noise will be suppressed at the $v_{2,out}$ output, as it is can be seen in Fig. 2d. Contrarily, in the case of $v_{1,out}$, the flicker noise is not attenuated. However due to the numerical simplifications in (3), a zero occurs very close to DC and it creates a notch in the noise floor, which is not noticeable in the simulations. To demonstrate how the thermal noise folding can be exploited for area reduction, a detailed noise analysis of the OTA$_{A,B}$ implementation is presented.

A. Differential Difference Amplifier

The two OTAs, which are shown in Fig. 1, are implemented as a single differential difference amplifier (DDA) to avoid large slewing transients that can occur in the output common-mode voltage due to charge injection at the $OTA_{A,B}$ input terminals. The DDA consists of a pair of two-stage amplifiers cross-coupled at the intermediate nodes, V_x and V_y, as shown in Fig. 3. Compared to a conventional two-stage amplifier, the symmetry of the differential pair is improved due to matching current-mirror loads. The mirroring ratio controls the equivalent transconductance at node V_x, $g_{ds,x} \approx g_{m3,B}(W_{4B} - W_{3B})/(W_{4B} + W_{3B})$. The ratio is made less than unity to maintain stable operation and $W_{3,4,B}$ are made relatively large (22.4 μm and 24μm) to account for device tolerance. A SC common-mode feedback (CMFB), which is not fully shown in Fig. 3, regulates only a fraction of the common-source biasing current to reduce the simulation time needed to enter steady-state operation.

B. Constant Effective Noise Bandwidth Approach

The DDA is divided into two identical half-circuits, as shown in Fig. 3, to simplify the noise analysis. Before aliasing, the DDA input referred noise floor is given by

$$\bar{v}_{nf,DDA}^2 = 16kT\left(1 + \frac{f_c}{f}\right)\left(\frac{1}{g_{m1}} + \frac{1}{g_{m5}}\frac{g_{ds,x}^2}{g_{m1}^2}\right), \quad (5)$$

where f_c is the OTA flicker noise corner, while g_{m1} and g_{m5} are the transconductance of transistors M_{IA} and M_{5A}, respectively. In continuous-time operation, the noise floor density, of the designed DDA, is approximately 45 nV/$\sqrt{Hz}$ with a flicker noise corner of 7 kHz. After aliasing, the resulting noise floor increases by approximately 9 dB, as it can be seen in Fig. 2d. The aliasing is accounted for by performing convolution in the frequency domain with a finite Dirac pulse train $\sum_{n=1}^{N}\delta(nf_S)$. The length (N) is defined by the ratio of the effective noise-bandwidth, f_{ENBW}, and the sampling frequency, f_S=153.6 kHz. In a single pole system, the f_{ENBW} can be approximated as one-fourth of ω_u. Since ω_u is chosen based on the settling time requirements, which are adopted from [10], choosing $N = 3$ should be sufficient for an accurate estimation. Considering the circuits shown in Fig. 1 and Fig. 3, the ω_u is defined by

$$\omega_u = \frac{1}{R_{eq}C_{eq}} = \left(\beta\frac{g_{m5}g_{m1}}{g_{ds,x}}\right)\left(\frac{1}{C_1^*\beta}\right). \quad (6)$$

Thus, the total sampled noise at the $OTA_{A,B}$ input is then found by

$$\bar{v}_{n,DDA}^2 \approx \frac{4kT}{C_1^*}\left(\frac{g_{m5}}{g_{ds,x}} + \frac{g_{ds,x}}{g_{m1}}\right). \quad (7)$$

Based on (7), the most efficient manner of reducing the total sampled noise, in terms of area and power, is to increase g_{m1}, while decreasing g_{m5} to maintain a constant ω_u and stable operation.

C. Stability Considerations

As it can been seen in Fig. 3, the Miller compensation has not been used since it would require a considerably large capacitor. Instead, the DDA is stabilized by defining the dominant pole at the $v_{1,out}$ node while adjusting the position
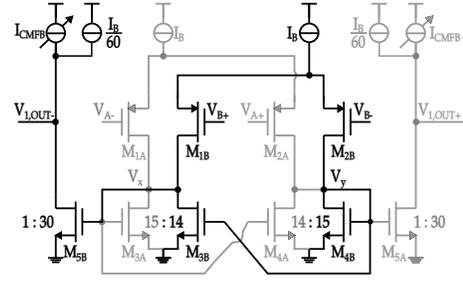

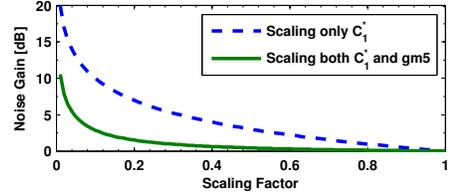Fig. 3.   Schematic of the differential difference amplifier.

Fig. 4.   The change in noise with respect to the scaling factor.

of the second pole at the intermediate nodes V_x and V_y. To achieve the desired phase margin, assuming that the first pole is contributing to a 90° phase shift, the following expression has to be fulfilled

$$tan(90° - PM) = \frac{\omega_u C_x}{g_{ds,x}}, \quad (8)$$

where C_x is the cumulative parasitic capacitance at the intermediate node V_x. Note that (8) puts a constraint on the maximum size of the transistors in the cross-coupled current mirrors (M_{3-5}), which has to be balanced with the tolerance to process and device variation due to the small mirroring ratio.

D. Area-Efficient Approach

It is apparent from (6) and (7) that to achieve low noise it is not sufficient to simply increase C_1^* since other parameters are negatively affected. In fact, increasing the capacitance size to lower the noise is ineffective unless g_{m1} is increased simultaneously to maintain a constant ω_u. However, by doing so, both area and power consumption are penalized. Alternatively, decreasing $g_{ds,x}$ to offset for the change in C_1^* would introduce instability in (8) and even increase the total noise ($g_{m5}/g_{ds,x} \gg g_{ds,x}/g_{m1}$), while increasing g_{m5} would not affect (7). On the other hand, if we scale both C_1^* and g_{m5} simultaneously, we can aggressively reduce the capacitance area for a small noise penalty, as shown in Fig. 4. For instance, by scaling both parameters by a factor of 0.2, the capacitance area reduces by 5x and the noise increases by only 1.5 dB, compared to an increase of 7 dB when g_{m5} remains constant in a conventional kT/C limited system.

III.   POST-LAYOUT SIMULATION RESULTS

The proposed circuit is designed in a 0.18 μm CMOS process, and occupies an area of 121x422 μm², as shown in Fig. 5. Less than half of the total area is used by C_1 and C_2, which are equal to 1.8 pF. The CMFB error amplifier is incorporated in the layout due to the matching considerations in the biasing currents. At this stage, the switched-capacitors,
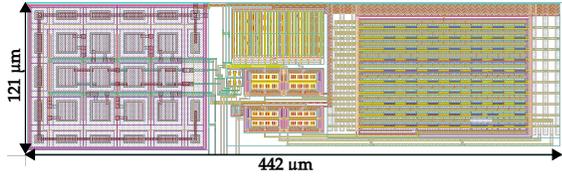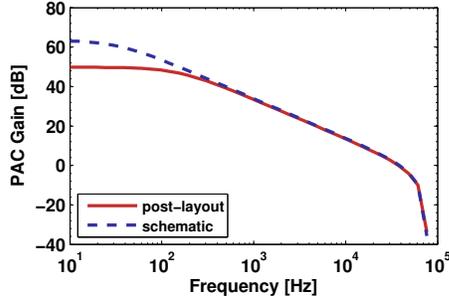
Fig. 5. Layout of the proposed integrator.

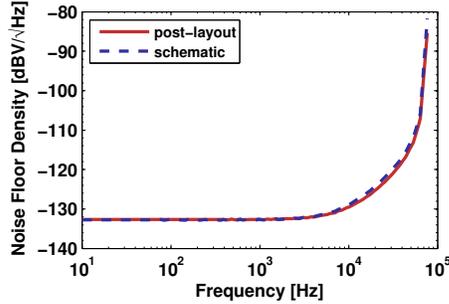Fig. 6. Simulation results of the *pss/pac* analysis.

Fig. 7. Simulation results of the *pss/pnoise* analysis.

which are used to sense the average output common-mode voltage, have not been included in the layout since they have a minor impact on the performance.

The total DC current consumption is 7.5 μA from a 1.8 V supply of which 3.65 μA is used to bias a single differential pair and 61.4 nA in the common-source stage. The chosen biasing distribution complies with the theoretical analysis for constant f_{ENBW}, but it also limits the maximum input signal swing due to the poor slew-rate performance. For these biasing conditions, the open-loop DC gain of the DDA is 66 dB with a unity gain frequency of 418 kHz and a phase margin of 46° for a loading capacitance of 1.8 pF. The unity-gain frequency is slightly larger than $2f_s$ due to process and device variations, while the phase margin can be improved by additional loading capacitance at $v_{1,out}$ or by adjusting the scaling factor.

The transfer function given by (2) and the sampled input noise floor of the integrator were simulated with *Spectre* by using *pss/pac* and *pss/pnoise* analysis, respectively. The clock frequency was set to 153.6 kHz based on the adopted system specifications [10]. The maximum noise frequency was made ten times larger to accurately model the aliasing effects in the simulation. The schematic and post-layout simulation results are given in Fig. 6 and Fig. 7. The main difference is in the decrease of low frequency gain due to the routing parasitics

introduced by C_{p2}. The simulation results match with the presented theoretical analysis at low frequencies, since the OTA gain was assumed constant. Moreover, as it can be seen from Fig. 7, the input referred noise floor is white at lower frequencies and remarkably low when considering that the sampling capacitance is only $C_1 = 1.8$ pF. At frequencies larger than $f_S/4$, the noise floor rapidly increases due to a drop in gain, as it can be seen in Fig. 6.

IV. CONCLUSION

A simple and area-efficient implementation of a switched-capacitor integrator with flicker noise canceling properties has been presented. Based on the theoretical and simulation results, we have shown that the noise cancellation is insensitive to stray parasitic capacitances, which is not the case for the charge transfer accuracy. Additionally, we demonstrated that by maintaining a constant effective noise bandwidth, the sampling capacitance can be significantly reduced, at the cost of a small noise and slew-rate performance degradation. The post-layout simulation results show a constant noise floor of -133 dBV/$\sqrt{Hz}$ at low frequencies, which makes the proposed integrator suited for feed-forward $\Delta\Sigma$ modulator architectures with high oversampling ratios.

REFERENCES

[1] R. Gregorian and G. Temes, *Analog MOS integrated circuits for signal processing*. New York: Wiley-Interscience, 1986.

[2] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2358–2368, Nov 2005.

[3] R. Kapusta, H. Zhu, and C. Lyden, "Sampling circuits that break the kT/C thermal noise limit," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1694–1701, Aug 2014.

[4] B. D. Sahoo and A. Inamdar, "Thermal-noise-canceling switched-capacitor circuit," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 63, no. 7, pp. 628–632, July 2016.

[5] W. H. Ki and G. C. Temes, "Offset-compensated switched-capacitor integrators," in *IEEE Int. Symp. Circuits Syst.*, May 1990, pp. 2829–2832 vol.4.

[6] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov 1996.

[7] O. Oliaei, "Noise analysis of correlated double sampling SC integrators with a hold capacitor," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 50, no. 9, pp. 1198–1202, Sept 2003.

[8] O. Rajaee, Y. Hu, M. Gande, T. Musah, and U. K. Moon, "An interstage correlated double sampling technique for switched-capacitor gain stages," in *IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 1252–1255.

[9] X. Zheng, F. Li, X. Wang, and C. Zhang, "A current-to-voltage integrator using area-efficient correlated double sampling technique," in *IEEE Int. Symp. Circuits Syst.*, May 2012, pp. 2167–2170.

[10] N. Ivanisevic, S. Rodriguez, and A. Rusu, "A 96.4 dB high-pass delta-sigma modulator with dynamic biasing and tree-structured DEM," in *14th IEEE Int. New Circuits Syst. Conf.*, June 2016, pp. 1–4.

[11] I. Seo and R. M. Fox, "Low-power switched-capacitor filters using charge transfer integrators," in *IEEE Int. Symp. Circuits Syst.*, vol. 1, May 2003, pp. 609–612.