Design and Implementation of 4-Stroke Topology in Electric Drives

DARIAN VERDY RETIANZA
Design and Implementation of 4-Stroke Topology in Electric Drives

DARIAN VERDY RETIANZA
Abstract

The 4-Stroke inverter topology is investigated and implemented in this thesis as a method to damp the oscillation at the MOSFET drain-source voltage when reverse recovery occurs. The aim is lower Electromagnetic Interference source level from the power inverter. The design process is coming from analyzing the appropriate inductor, making a simulation in LTSPICE and making a high-performance six-layer PCB for the high current application. Finally, the prototype is tested in different control timing, radiated emission test and conducted emission test.

Key words: 4-stroke design, LTSPICE, PCB design, EMI.
Sammanfattning

4-taktsomvandlarens topologi undersöks och implementeras i denna avhandling som en metod för att dämpa oscillation när reverse recovery sker i slutstegets MOSFET. Syftet är att dämpa elektromagnetisk störning från kraftomvandlaren. Designprocessen är att analysera lämplig induktans, göra en simulering i LTSPICE och designa ett högpresterande 6-lager PCB för kraftiga strömmar. slutligen testas prototypen med olika kontrolltider, elektromagnetisk emission och elektromagnetisk konduktion.

Nyckelord: 4-taktsomvandlarens, LTSPICE, PCB-design, elektromagnetisk störning.
Acknowledgments

The present thesis conducted at Inmotion Technologies AB, Stockholm, Sweden.

First of all, I would like to thank my supervisor Johan Lans for entrusting me with such an interesting and challenging topic. He gives me much feedback that is very important in during all of the stage of the thesis. Most importantly, he taught me that the industry work is really different from Academia which pushes me to work for perfection. In addition, I would like to thank my examiner Oskar Wallmark for giving me a chance to conduct this master thesis.

Moreover, I would like to especially thank Ulf Karlsson for the continuous supervision from the idea and guidance in the project. I am also thankful to Lars Lindberg for giving me any advice on the way I am doing the thesis which makes me grow further as a person during my thesis time.

I would also like to thank to I am also grateful to Anders Björklund for the time to teach me about LTSPICE and help in the gate driver model and transistor modeling. Also, I would like to thank Benn Frisk and Christer Thomson for relentless help and guidance in Capture CIS and Allegro for designing PCB.

Furthermore, I would like to thank KTH Formula Student team as for giving me a chance to become an electric powertrain member for these past two years. Moreover, I would like to express my gratitude to Vehicle Engineering Department to entrust me as a winner of KTH Master Challenge 2016 which let me get a scholarship in vehicle engineering department for following two years of my study.

Finally, I would like to express my deepest gratitude to my family for encouraging me to follow my passion and supporting me in all of the condition.
## Contents

1 Introduction  
1.1 Background and objectives ........................................... 1  
1.2 Thesis outline .......................................................... 2  
  
2 4-Stroke Topology  
2.1 Conventional Two-Level Inverter .................................... 3  
  2.1.1 Topology description .............................................. 3  
  2.1.2 Modulation techniques .......................................... 4  
2.2 Electromagnetic Compatibility ....................................... 5  
2.3 MOSFET ................................................................. 7  
  2.3.1 Brief introduction ................................................ 7  
  2.3.2 Model in Simulation ............................................. 8  
2.4 Introduction to 4-Stroke Topology .................................. 11  
  2.4.1 Problem Formulation .............................................. 11  
  2.4.2 4-Stroke Topology ................................................. 13  
  2.4.3 Preliminary Comparison in Simulation ......................... 16  
2.5 Inductor ................................................................. 18  
  2.5.1 Ferrite core inductor ........................................... 19  
  2.5.2 Air Coil Inductor ................................................ 22  
  
3 4-Stroke Design ........................................................... 24  
3.1 Design Introduction .................................................... 24  
3.2 4-Stroke PCB ........................................................... 25  
  3.2.1 Design Challenge ................................................ 26  
3.3 PCB Design .............................................................. 30  
3.4 Gate Driver .............................................................. 34  
  3.4.1 Component Selection ............................................. 34  
  3.4.2 Gate Driver Circuit ............................................. 35  
3.5 Short Circuit Protection ............................................... 36
4 Experiment and Validation 39
  4.1 4-Stroke vs 2-Stroke ................................. 39
  4.2 Simulation vs Experiment ............................... 41
  4.3 Loss Experiment ....................................... 47
  4.4 Impact of auxiliary switch timing ..................... 49
    4.4.1 Rise Time Control Variation of Auxiliary Switch . 50
    4.4.2 Overlap Time Control Variation of Auxiliary Switch 51
  4.5 Radiated Emission Test ................................. 53
  4.6 Conducted Emission Test ............................... 55
    4.6.1 Differential-Mode Emission Test .................. 55
    4.6.2 Common-Mode Emission Test ....................... 57

5 Conclusion and Future Works 60
  5.1 Conclusion ............................................. 60
  5.2 Future Works .......................................... 61
## List of Figures

2.1 Two-Level Inverter [8] ........................................ 3  
2.2 Sinusoidal Pulse Width Modulation .......................... 5  
2.3 Blue line shows SPWM, red line shows the third harmonic injection, and yellow line shows the THPWM  .......... 6  
2.4 Electromagnetic Capability Classification .................... 6  
2.5 Typical frequency range of power electronics perturbations .................................................. 7  
2.6 Typical output characteristics [2] ............................ 8  
2.7 The Mosfet Model in One Leg Switching. The first picture is the MOSFET initial condition. The (1) – (3) sign indicates the MOSFET model in the transition period. (1) is the condition when $V_{GS}<V_{TH}$. (2) is the condition when $V_{GS}-V_{TH}<V_{DS}$. (3) is the condition when $V_{GS}-V_{TH}>V_{DS}$ ........................................ 9  
2.8 Representation of MOSFET body diode ......................... 10  
2.9 Timing diagram of MOSFET body diode during reverse recovery ........................................ 10  
2.10 MOSFET model simulation during the transition from turn off to turn on, conduction and transition from turn on to turn off  ........................................ 12  
2.11 MOSFET reverse recovery condition ........................ 13  
2.12 Drain-Source Voltage when reverse recovery occurs ......... 13  
2.13 4-Stroke one leg .............................................. 14  
2.14 Switching Stage when $I_L$ goes in ............................ 15  
2.15 Switching Stage when $I_L$ goes out ............................ 16  
2.16 Switching diagram when load current flow out from inverter ........................................ 17  
2.17 Switching diagram when current flow goes in to inverter 17  
2.18 $V_{ds}$ Voltage in LTSPICE when reverse recovery occur .......... 18
2.19 Inductor current in LTSPICE when reverse recovery occur
2.20 Ferrite core inductor model with airgap
2.21 Ferrite core inductor circuit model with airgap
2.22 The φ − H curve. The black line shows the ferrite core with no gap while the red line shows the ferrite core with an air gap.
2.23 B-H Curve [6]
2.24 Inductor Current [6]
2.25 Inductor current measurement with pulse current injection
2.26 Inductor Voltage measurement with pulse current injection
3.1 The design scheme. The blocks inside the big dashed block are the parts which is designed in this thesis
3.2 First Design
3.3 Second Design
3.4 Third Design
3.5 Fourth Design
3.6 Fifth Design
3.7 Sixth Design
3.8 Seventh Design
3.9 The final look of PCB Design
3.10 Circuit Segmentation
3.11 Layout Consideration
3.12 Plane Separation
3.13 Component placement
3.14 Confidential Information
3.15 Confidential Information
3.16 Output Current Comparison between each driver
3.17 Timing Comparison between each driver
3.18 Simplified Gate Driver circuit schematic
3.19 Simplified Short Circuit Protection Schematic
3.20 BUS Voltage when Short Circuit occur
3.21 BUS voltage when no Short Circuit
4.1 Experiment of the 4-stroke and 2-stroke comparison
4.2 $V_{ds}$ main comparison of 4-stroke(blue) and 2-stroke(red)
4.3 $V_{gs}$ main voltage of 4-stroke(blue) and 2-stroke(red)
4.4 $V_{ds}$ 2-stroke high frequency content
### LIST OF FIGURES

- **4.5** $V_{gs}$ 2-stroke high frequency content .......................... 40
- **4.6** Experiment setup to compare simulation and experimental data .................................................... 41
- **4.7** $T_{A+}$ switch $V_{ds}$ and current during reverse recovery period in experiment ................. 42
- **4.8** $T_{A+}$ switch $V_{ds}$ and current during reverse recovery period in Simulation .................. 42
- **4.9** Losses comparison between experiment and simulation in 2-stroke ........................................ 43
- **4.10** $T_{A+}$ switch $V_{ds}$ and current during turn-on transition period in Simulation .................. 43
- **4.11** $T_{A+}$ switch $V_{ds}$ and current during turn-on transition period in Experiment .................. 43
- **4.12** Simulation in turn on transition period ................................. 44
- **4.13** $T_{A+}$ switch $V_{ds}$ and current during reverse recovery in experiment for 4-stroke ................. 45
- **4.14** $T_{A+}$ switch $V_{ds}$ and current during reverse recovery in simulation for 4-stroke .................. 45
- **4.15** Losses comparison between experiment and simulation during reverse recovery for 4-stroke drives .................. 45
- **4.16** $X_{A-}$ switch $V_{ds}$ and current during reverse recovery of $T_{A+}$ in Experiment for 4-stroke .................. 46
- **4.17** $X_{A-}$ switch $V_{ds}$ and current during reverse recovery of $T_{A+}$ in simulation for 4-stroke .................. 46
- **4.18** Losses comparison between experiment and simulation during reverse recovery in $M_{A-}$ .................. 46
- **4.19** Measurement Setup of the losses measurement .................. 47
- **4.20** Inverter Setup ........................................ 47
- **4.21** Inverter Losses of 4-stroke and 2-stroke in 2,4,8 kHz switching frequency .................. 48
- **4.22** 4-stroke and 2-stroke switching losses of different frequency ........................................ 48
- **4.23** Measurement Setup of Auxiliary control experiment .................. 49
- **4.24** 4-stroke timing diagram ........................................ 49
- **4.25** The control scheme of the auxiliary switch of 4-stroke inverter .................. 49
- **4.26** upper main switch $V_{ds}$ with different inductance value .................. 50
- **4.27** Auxiliary Switch $V_{ds}$ with different inductance value .................. 50
- **4.28** Inductor current with different inductance value .................. 51
4.29 upper main switch $V_{gs}$ with different inductance value .......................... 51
4.30 Upper main switch $V_{ds}$ ................................................................. 52
4.31 Auxilliary Switch $V_{ds}$ ........................................................................... 52
4.32 Gate-source voltage with overlap value 10 .............................................. 52
4.33 Gate-source voltage with overlap value 40 .............................................. 52
4.34 A schematic of Radiated emission test setup ........................................... 53
4.35 Radiated emission test between 4-stroke and 2-stroke 
for lower frequency test (1MHz to 30MHz) .............................................. 54
4.36 Radiated emission test between 4-stroke and 2-stroke 
for higher frequency test (30MHz to 120MHz) ....................................... 54
4.37 Radiated Emission between 4-stroke and 2-stoke in 8kHz 
and 4kHz switching frequency at higher frequency test(50MHz to 
100MHz) ........................................................................................................ 55
4.38 Radiated Emission between 4-stroke and 2-stroke in 8kHz 
and 4kHz switching frequency at lower frequency ................................... 55
4.39 A functional schematic of differential emission conduction test ............. 56
4.40 Differential-Mode Emission for 4-stroke and 2-stroke in 
lower frequency range .................................................................................. 56
4.41 Differential-Mode Emission for 4-stroke and 2-stroke in 
higher frequency range ................................................................................ 56
4.42 A schematic of common mode conduction test ..................................... 57
4.43 Common-Mode emission test comparison for 4-stroke 
and 2-stroke in lower frequency range ....................................................... 58
4.44 Common-Mode emission test comparison for 4-stroke 
and 2-stroke in higher frequency range ...................................................... 58
4.45 Illustration of parasitic element created by MOSFET switching 
in one leg ......................................................................................................... 58
List of Tables

3.1 Gate Driver Comparison . . . . . . . . . . . . . . . . . . . 34
Acronyms

BJT  Bipolar Junction Transistor. 4

DUT  Device Under Test. 53

EMC  Electromagnetic Compatibility. 5, 60

EMI  Electromagnetic Interference. 5

EMS  Electromagnetic Susceptibility. 5

IGBT  Insulated-Gate Bipolar Junction Transistor. 4

LBEV  low Voltage Battery Electric Vehicles. 1, 52

LISN  Line Impedance Stabilization Networks. 52

MOSFET  Metal-Oxide Semiconductor Field-Effect Transistor. 4

PCB  Printed Circuit Board. 7

PWM  Pulse Width Modulation. 4

SPWM  Sinusoidal Pulse Width Modulation. 4

THIPWM Third Harmonics Pulse Width Modulation. 4
Chapter 1

Introduction

The motive behind the thesis subject is given in this first chapter together with the project goals. A summary of the report layout is also presented.

1.1 Background and objectives

As the electric vehicle technology advances, the need to place more efficient electrical and electronic systems into the electric vehicle has increased rapidly. In low Voltage Battery Electric Vehicles (LBEV) such as forklift, the use of cheap electronic component in the motor controller is needed to lower the production cost. The MOSFET transistor is used as the power electronics switch as it has sufficient power and fast switching characteristic. However, due to the intrinsic body diode of the MOSFET, the motor controller will produce higher electromagnetic interference (EMI) when increasing switching performance.

The thesis has an aim to design and develop the new concept of two-level inverter topology and control strategy to increase the switching speed while keeping the electromagnetic interference at the low level. This topology is done based on Inmotion Technologies Patent (EP293667281). [13] It is implemented by using additional switches to damp the ringing effect due to reverse recovery in MOSFET body diode. A prototype is built and tested to show its operational principle and benefit.
1.2 Thesis outline

The thesis report is separated in five chapters as follows:

- **Chapter 1**: Short presentation of the thesis purpose and the report structure.

- **Chapter 2**: Investigation of 4-Stroke topology and the introduction of additional components.

- **Chapter 3**: Detailed description in the building of 4-Stroke topology.

- **Chapter 4**: Validation of the 4-Stroke topology through experimental testing. Comparative study between conventional two-level topology, 4-Stroke, and LTSPICE simulation.

- **Chapter 5**: Brief discussion over the experimental results and suggestions for further design improvements.
Chapter 2

4-Stroke Topology

In this chapter, the theoretical background of 4-Stroke topology from analyti-
cally approach, simulation, and preliminary component design is presented

2.1 Conventional Two-Level Inverter

2.1.1 Topology description

Nowadays, two-level voltage source inverter is the most common way for three-phase motor control application. Each consist of three legs which produce an output of 120 degrees displacement concerning each other. These legs are connected with DC Voltage supply in the parallel connection with the large capacitors. The inverter is depicted in the figure 2.1

![Two-Level Inverter Diagram](image)

Figure 2.1: Two-Level Inverter [8]

Each leg is consist of two switches in connection with an anti-parallel diode for letting the power to flow in the reverse direction. The pri-
primary control rule of the switches is not letting the MOSFET in one leg to be on together since it will short-circuit the DC Voltage Source. The choice of the switches can be either Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET), Insulated-Gate Bipolar Junction Transistor (IGBT), or Bipolar Junction Transistor (BJT). Since at every moment, one of the two switches in each leg is always on, the output voltage is independent of the output load.

2.1.2 Modulation techniques

To control the duration of each switch to conduct, a Pulse Width Modulation (PWM) technique is used. Several ways of PWM has been developed which have some objectives in minimizing the dc voltage and current ripple, inverter losses, and harmonic output content.

In order to designate the switching state for each semiconductor in a power inverter, a switching pattern is needed. The selected modulation technique is responsible for creating the current and voltage waveforms in the output stage by deciding which switches, and for how long will be conducting. During the past years, numerous techniques have been developed aiming at minimizing the inverter losses, reducing the dc voltage and current ripple and adjusting the output depending on the load. [8]

The modulation technique that used in this project is Sinusoidal Pulse Width Modulation (SPWM) with third harmonic injection or Third Harmonics Pulse Width Modulation (THIPWM). The SPWM is a PWM technique based on the comparison between three sinusoidal voltage which shifted 120 degrees phase on each other and triangular carrier voltage with a fixed frequency.

The comparison of these two signals will give each of switch a duty ratio D. When \( V_{\text{control}} < V_{\text{tri}} \) the \( T_{A+} \) switch is on while the \( T_{A-} \) is off. The reverse condition is applied for \( V_{\text{control}} > V_{\text{tri}} \) which \( T_{A+} \) is off. The output pole voltage \( V_A, V_B, V_C \) of the inverter switch is between \(-\frac{V_d}{2}\) and \( \frac{V_d}{2} \) where \( V_d \) is the DC Voltage. It is important to note that the frequency of carrier voltage is the one who decides the switching frequency of the system. As the reason, the proper choice of the carrier frequency is needed to have an optimum inverter performance. However, the SPWM technique does not have an optimum DC Bus utilization. To improve it, the optimum the Third Harmonic Injection PWM (THIPWM) used. The idea is to inject the triple frequency term in the
control signal which can be seen in the term below:

\[ y(\omega t) = \sin(\omega t) + A\sin(3\omega t) \]  

(2.1)

Where \( y \) is the control signal amplitude concerning the time, and \( A \) is the constant amplitude of the third harmonics. To get the maximum value of \( y(\omega t) \), the equation of \( y(\omega t) \) should be derived concerning \( (\omega t) \) equal to zero. The extensive calculation can be seen in the [18]. From the derivative, the maximum value happens when the third harmonics amplitude is \( \frac{1}{6} \) which makes the required control signal waveform is

\[ y(\omega t) = \sin(\omega t) + \frac{1}{6}\sin(3\omega t) \]  

(2.2)

Figure 2.3 shows the illustration of the THIPWM control signal

### 2.2 Electromagnetic Compatibility

Electromagnetic Compatibility (EMC) is the ability of an electrical and electronics system to function and operate properly in their intended electromagnetic environment with a defined safety margin and not be a source of pollution to that electromagnetic environment. EMC is consist of Electromagnetic Interference (EMI) and Electromagnetic Susceptibility (EMS) which the classification is shown in figure 2.4
Figure 2.3: Blue line shows SPWM, red line shows the third harmonic injection, and yellow line shows the THIPWM.

Figure 2.4: Electromagnetic Capability Classification
CHAPTER 2. 4-STROKE TOPOLOGY

EMI is the disruptive electromagnetic energy transmitted from the source to another electronic device which can be a conducted and radiated emission. Conducted emission is propagated from the electrical source along a power line such as cables and Printed Circuit Board (PCB) traces while the radiated emission is transmitted as an electromagnetic wave through free space. [4] In the other hand, EMS is representing the capability of the device to response the unwanted disturbances such as Electrostatic Discharge (ESD) and electromagnetic waves.

These problems can occasionally cause malfunction of their local electronics environment. Hence, it is essential to understand the origin of the EMI phenomena to have an optimal design to obey the EMC standards.

In the power electronics, the conducted and emitted electromagnetic perturbation can be classified into specific frequency range shown in figure 2.5

![Figure 2.5: Typical frequency range of power electronics perturbations](image)

For electric drives, it is essential to consider the frequency range from $10^4$ to $10^8$ since this is the range of frequency that performed to the switches and the frequency oscillation during switching process occurs. [5]

### 2.3 MOSFET

#### 2.3.1 Brief introduction

MOSFET is a three-terminal device where the input, gate, control the current flow at the output in drain and source. When a voltage is applied between gate and source, the MOSFET is conducting, and the
current will flow between drain and source. The output characteristics $i_D$ as a function of gate-source voltage $V_{GS}$ and drain-source voltage $V_{DS}$ is given on figure 2.6. The MOSFET operation points are divided into three regions called cut-off, linear and saturation region. The MOSFET is in a cut-off region when $V_{GS}$ is lower than threshold voltage $V_{TH}$ which means that the device is in open circuit condition. The other two states happen after $V_{GS}$ level is surpassing $V_{TH}$ with linear region following the condition below [17]

$$V_{GS} - V_{TH} > V_{DS} \quad (2.3)$$

The condition for saturation region is following the condition

$$V_{GS} - V_{TH} < V_{DS} \quad (2.4)$$

In power electronics application, MOSFET is desired to operate in a linear region when the conduction occur since it has the lowest energy dissipation while in the transition of the turn-off and turn on, MOSFET will operate in saturation condition. This phenomenon is modeled in LTSPICE and will be discussed in the next sub-chapter.

2.3.2 Model in Simulation

Under transition period, The initial condition of one leg of the three-phase bridge can be modeled by first figure at 2.7.

The load current can be treated as a DC source since the computation time only last a short time. In addition, the physical phenomena
of MOSFET can be described as input capacitance \( C_{iss} = C_{gd} + C_{gs} \) and output capacitance \( C_{oss} = C_{gd} + C_{gs} \). When MOSFET in the transition period, the phenomena can be modeled into the equivalent circuit by figure 2.7 [12]

Figure 2.7: The Mosfet Model in One Leg Switching. The first picture is the MOSFET initial condition. The (1) – (3) sign indicates the MOSFET model in the transition period. (1) is the condition when \( V_{GS} < V_{TH} \). (2) is the condition when \( V_{GS} - V_{TH} < V_{DS} \). (3) is the condition when \( V_{GS} - V_{TH} > V_{DS} \).

Each equivalent circuit is modeled with anti-parallel connection with a modeled diode. The diode model refers to Lauritzen and Ma [15] which is based on lumped charge control by following the equations:

\[
\begin{align*}
    i_D(t) &= \frac{q_e - q_m}{T_m} \\
    0 &= \frac{dq_m}{dt} + \frac{q_m}{\tau} - \frac{q_e - q_m}{T_m} \\
    q_e &= I_S \tau \left[ \exp \left( \frac{v_d}{nV_T} \right) - 1 \right]
\end{align*}
\]

Where, \( i_D(t) \) is the diode current, \( q_m \) is injected charge of the total forward bias, \( q_e \) is the junction injected charge level, \( T_m \) is the drift region transit time, \( \tau \) is the lifetime, \( I_s \) is the diode saturation current, \( v_D \) is the diode junction voltage, \( V_T \) is the thermal voltage and \( n \) is the emission coefficient. To speed up the computational time, Natan and Sam [14]
simplified model is used by disregarding the exponential dependency between $q_e$ and $v_D$. The simplification diode model circuit is shown in figure 2.8

![Figure 2.8: Representation of MOSFET body diode](image-url)

Figure 2.8: Representation of MOSFET body diode during reverse recovery

The equation 2.6 is represented by $R\tau C\tau$ as shown in the figure 2.8 which in reality, it reflects the first stages phenomena during $0 < t < t_a$. For the second $t > t_a$, the phenomena is emulated by RC network $R_{rr}C\tau$ which the value of $R_{rr}$ is coming from curve fitting between experiment and simulation. The switch in the middle is controlling which stages should be active. An extensive calculation in the simplification can be found in [14]

From figure 2.7, the transition period is described in the explanation below [17]

- When $V_{GS} < V_{TH}$, the constant input voltage $V_{IN}$ is injected to the MOSFET to charge the input capacitance. As the MOSFET is not active, no power loss occurs in this period.

- The second period occurs when $V_{GS} < V_{TH} < V_{DS}$. Based on the equivalent circuit, the dynamics of the voltage and current can be obtained by solving the Laplace transform equation 2.8 to 2.12.

$$V_{gs}(s) = V_{ds}(s) + V_{gd}(s)$$

Equation 2.8 shows the correlation between MOSFET gate-source voltage, drain-source, and gate-drain by examining the voltage
mesh loop of MOSFET.

\[ V_{IN} - V_R(s) = sL_g I_g \]  

(2.9)

\[ I_g = \frac{V_R(s) - V_{gs}}{R_g} = sC_{gd}V_{gd}(s) + sC_{gs}V_{gs}(s) \]  

(2.10)

Where \( V_{IN} \) is PWM input, \( V_R \) is the voltage between resistors and inductors, \( L_g \) is the gate inductance, \( I_g \) is the gate driver current. \( R_g \) is gate resistance, \( C_{gd} \) gate-drain capacitor, \( C_{gs} \) gate-source capacitor.

Equation 2.9 and 2.10 shows the gate current equation which is formed from the definition of current flow in the inductor for equation 2.9 and Kirchhoff current law for equation 2.10.

\[ I_D(s) = I_d(s) - sC_{ds}(s)V_{ds} - sC_{gd}V_{gd}(s) \]  

(2.11)

Where \( I_D \) is the current flow through MOSFET, \( I_d \) is the dependent current source inside MOSFET, and \( C_{ds} \) is the drain-source capacitor. Equation 2.11 shows one bridge leg current equation which is formed from the Kirchhoff current law.

\[ I_d(s) = g_{fs}(V_{gs}(s) - V_{TH}) \]  

(2.12)

Equation 2.11 shows the transconductance equation which the value of \( g_{fs} \) is extracted from the datasheet.

- The third period occurs when \( V_{GS} - V_{TH} > V_{DS} \). Since in this period the dynamics are highly non-linear, from (citation) the simplified equation is used as shown below [21]

\[ I_d(s) = K_p(V_{gs}(s) - V_{TH} - \frac{V_{ds}}{2})V_{ds} \]  

(2.13)

The capacitance, diode, and resistance data is non-linear and extracted from MOSFET datasheet and injected into LTSPICE model. It is important to notice that the turn-off transition period of MOSFET is just an inverse sequence of the turn-on transition. The result of simulation is depicted in figure 2.10.

**2.4 Introduction to 4-Stroke Topology**

**2.4.1 Problem Formulation**

In low voltage application, MOSFET is widely used as the chosen switch of the inverter because of the low prices. In two-level inverter when
Figure 2.10: MOSFET model simulation during the transition from turn off to turn on, conduction and transition from turn on to turn off.
the MOSFET is in the process of changing states from on to off, the reverse recovery of body diode will occur and cause high-frequency oscillation in high frequency on the drain-source MOSFET voltage. Reverse recovery is a phenomena which the current through diode are still conducting after reaching zero current but in the reverse direction for a small time due to minority carriers stored semiconductor materials. The complete analysis of reverse recovery can be seen in [7]. In the inverter, the reverse recovery occurs when the MOSFET is in the transition from turn on to turn off when the load current flow direction is able to pass through the MOSFET body diode which is shown in figure 2.11.

Since the power inverter is the source of EMI, the production of high-level frequency content will generate EMI. The drain-source voltage when reverse recovery is measured in conventional two-level drives and shown in figure 2.12.

![Figure 2.11: MOSFET reverse recovery condition](image1)

![Figure 2.12: Drain-Source Voltage when reverse recovery occurs](image2)

From the measurement, $V_{DS}$ produce high-frequency oscillation when turn-off period which is the source of EMI. This oscillation is caused by the non-linearity of MOSFET body diode when reverse recovery occurs. To overcome this problem, the new topology to mitigate oscillation is done and will be presented in the next section.

### 2.4.2 4-Stroke Topology

From the problem formulation, the ringing effect occurs in drain-source voltage when and after the reverse recovery happen. To overcome, the
4-stroke topology is developed. This topology is shown in figure 2.13

![Figure 2.13: 4-Stroke one leg](image)

The main switch which is represented by S1 and S2 do the main switching while S3 and S4 are the auxiliary switches which have the main responsibility for helping the switching of main switches. The inductor between auxiliary switches and main switches is chosen in an optimum way by considering some aspects which will be discussed in the next section. As mentioned in the previous section, the reverse recovery produces a high-frequency oscillation of $V_{ds}$ which is the source of EMI. By using the helper and inductor, it will give a damping effect during the reverse recovery switching since it will reduce the current that flows through the MOSFET body diode into the inductor which makes the MOSFET can be turned off in lower current. Figure 2.14 shows the circuit switching scheme of the 4-stroke topology when the current goes in into the inverter.

Since the MOSFET commutation time is sufficiently short, the current that goes into the inverter can be inferred as a DC current source $I_L$. Note that the auxiliary switches will work either when the $I_L$ goes in and the main upper switch still on the on state or when the $I_L$ goes out and the main lower switch still on the on state. When the load current goes into inverter, The 4-stroke switching works by following the sequence below:

1. The stage started when S1 is turned on and the load current goes into the inverter
2. The first stroke occurs when S4 start to conduct which makes the current flow divided into S1 and through the inductor
3. The second stroke occurs when S1 open while keeping S4 conducting. In this process, damping occurs since the current which flows through S1 is small which also makes the S1 able to do the soft switching.

4. The third stroke occurs when S2 will turn on while still keeping S4 to conduct to make sure that the change state of S4 will not affect the transient response.

5. The fourth stroke occurs when S2 is the only switch that conducting.

For the load current goes out from the inverter, the 4-stroke topology will have the same procedure but is applied for helping main switch S2 by using auxiliary switch S3.

Figure 2.15 shows the circuit switching scheme of the 4-stroke topology when the current goes out of the inverter.

The inductor is designed to be linear in all operating condition so that the auxiliary switch can be controlled with the linear correlation of inductor which follows the equation below.

$$t = \frac{L I_{\text{load}}}{V_{\text{bus}}}$$  \hspace{1cm} (2.14)

Where L is the inductance value of the auxiliary inductor, $I_{\text{load}}$ is the load current and $V_{\text{bus}}$ is the DC bus voltage. This approach is chosen...
since the auxiliary switch is only switched on in maximum around 5 $\mu$s which means the control calculation should be really fast. The control time is divided into two parts, the first part is called Time Rise which infers how long the switch is on the extended time is determined from the inductor-time correlation from previous equation. The second part is called Dead Time Overlap which infers how long the switch is still maintaining the on position. If the switch on in such a long time it will give the current increase in inductor and MOSFET which makes higher losses, on the other hand, if the timing is short, the system still cannot reduce the high frequency oscillation content due to reverse recovery optimally.

Figure 2.16 shows the circuit switching scheme of the 4-stroke topology when the current goes out of the inverter while figure 2.17 shows the switching scheme when the current goes into the inverter.

### 2.4.3 Preliminary Comparison in Simulation

Based on the MOSFET modeling in the previous discussion, the preliminary comparison of 4 stroke and conventional two-level topology
Figure 2.16: Switching diagram when load current flow out from inverter

Figure 2.17: Switching diagram when current flow goes in to inverter
is made. Figure 2.18 and 2.19 shows the MOSFET voltage and inductor current of SPICE simulation result when the reverse recovery occurs.

From the figure, it is shown that the emergence of auxiliary switches is helping the upper main MOSFET switching performance. They can damp the oscillation and lower the overshoot.

From figure 2.19, since the 4-stroke commutation is in microseconds order, it can be inferred that the inductor should be chosen with the capability of low losses in high frequency. Also, the RMS current that flows in the inductor is 41.8 Ampere which mean for the inductor design it is important to choose value about 1.5 times higher.

### 2.5 Inductor

The inductor is a critical part of the 4-stroke design. To achieve the research goal, Inductor analysis is needed. The requirements of inductor are listed below.

- Capability to deliver 60 A RMS.
- Small size since it will be implemented in the compact design PCB
- Low losses in high-frequency switching
• Operate as a linear device in the high current application (not saturate)
• 150nH inductance

2.5.1 Ferrite core inductor

In this design, the ferrite core inductor with an air gap is used. Figure 2.20 show the picture of the inductor. The inductor can easily be analyzed by using magnetic circuit model which is represented in figure 2.21

![Figure 2.20: Ferrite core inductor model with airgap](image)

![Figure 2.21: Ferrite core inductor circuit model with airgap](image)

In the magnetic circuit model, the ferrite core element can be represented as core reluctance $\mathcal{R}_c$ and the air gap can be represented as air reluctance $\mathcal{R}_g$. [6]

There are two reasons for the air gap employment. The first one is the addition of air gap makes the inductance not directly proportional to the core permeability, which depends on the temperature and the operating point. This addition makes the inductor non-linear so that it is difficult for the control of 4-stroke topology since the current estimation that flow through the inductor is needed. The addition of air gap makes sure that the value of inductance is less sensitive to variations of core permeability.

The second reason for air gap is allowing the inductor to operate in the higher region of saturation. This happen because now the flux is depend not only on the $\frac{N_i l_c \mu_c A_c}{l_c}$ but now is depend on the $\frac{N_i l_c \mu_c A_c + \mu_0 A_g}{l_c}$ which makes the gradient between flux and magnetic field strength lower. It is shown in figure 2.22 $\phi$ is flux, $A_c$ is core area, $A_g$ is air gap area, $l_c$ is core length, $l_g$ is length of air gap, $N$ is the number of turn, $B$
is magnetic density, $B_{sat}$ is magnetic density saturation value, and $H_c$ is the magnetic intensity.

However, there is another problem with calculation above. Note that there are two core losses which lowering the inductor efficiency. The first one is due to the characteristic of core materials that not ideal. To change the magnetization of a core material, some of the required value of energy is needed. However, in a non-ideal core, not all the energy is recovered into electrical energy which means it also converted into heat. These losses are called hysteresis losses of B-H loop Figure 2.23 shows the example of a non-ideal B-H curve, The energy loss can be calculated by examining the area inside the curve which can be formulated in the equation below.
\[ W = V_c \int_{\text{onecycle}} H dB \]  

(2.15)

Where \( V_c \) is the core volume and \( H \) is the magnetic field strength. The power loss due to the hysteresis can be calculated by multiplying the energy loss with switching frequency which can be shown in the equation below.

\[ P = fV_c \int_{\text{onecycle}} H dB \]  

(2.16)

The second losses are due to the fact that the core materials are made from the good electrical conductor. As a result due to the magnetic flux that flew inside the core, there will be rotating electrical current that flows through the material itself. This current is called eddy current which can be seen in figure 2.24

\[ P_{\text{eddy}} = I_{\text{eddy}}^2 R_{\text{core}} \]  

(2.17)

Where \( P_{\text{eddy}} \) is the core loss due to the eddy current, \( I_{\text{eddy}} \) is the rotating current inside the core (eddy current) and \( R_{\text{core}} \) is the resistive value of the core. The current that flows into the conductor will induce the magnetic flux which introduces the eddy current according to the Lenz’s law. It can be seen that the emergence of eddy current tend to increase the current density on the conductor surface while it lowers the current density on the conductor center. The current density will decay in a function of the distance into the conductor with such fixed distance length called skin depth. The skin depth is formulated by the equation below [6]
\[
\delta = \sqrt{\frac{\rho}{\pi \mu f}}
\]  
(2.18)

Where \(\delta\) is the skin depth, \(\mu\) is conductor permeability, \(\rho\) is material resistivity, and \(f\) is the current frequency. From the equation, the increase of frequency is lowering the skin depth. The increasing of frequency makes the current only flow on the surface of the wire so that the effective cross-sectional area of the wire is reduced. This reduction will increase resistive losses since the conductor resistance is represented by equation

\[
R = \rho \frac{l_c}{A_c}
\]  
(2.19)

Where \(R\) is the resistance, \(\rho\) is material resistivity, \(l_c\) is the conductor length, and \(A_c\) is conductor cross section area. From the objectives, the inductor is used in high frequency which makes the application of core will give additional core losses. Also, the ferrite core inductor will give non-linearity in the high current application which makes the 4-stroke control is more difficult. The choice of Air coil inductor is considered which will be presented in next section.

### 2.5.2 Air Coil Inductor

In a simple case the inductance of air coil inductor can be estimated by using wheeler formula [3]

\[
L = \frac{0.001N^2r^2}{228r + 254l}
\]  
(2.20)

Where \(L\) is the inductance in H, \(l\) is the coil length in meters, \(N\) is the number of turns and \(r\) is the coil radius.

Since it does not depend on the core permeability, the correlation between flux and magnetic strength field is linear which gives an advantage in 4-stroke operation to operate in higher switching frequency. As mentioned in the design objectives, the need for small inductance and small size packaging makes the using of air coil inductor is more advantageous compared to the core based inductor. For the implementation, the air coil inductor from Wurth electronics is used which has the nominal value 117nH with 20% tolerance and maximum 1.43m\(\Omega\).
DC resistance. To verify the datasheet result, the inductance measurement is done by injecting pulse current through the inductor. The measurement result is shown in figure 2.25 and 2.26. The calculation of inductance is taken by taking two points when the inductor has constant voltage. By taking the same points in the inductor current, the inductance can be solved by the following equation:

\[ L = \frac{V_{\text{ind}} \cdot \Delta t}{\Delta i} \]  \hspace{1cm} (2.21)

where \( L \) is inductance, \( V_{\text{ind}} \) is the inductor voltage, \( \Delta t \) is the time difference between two points, and \( \Delta i \) is the current difference between two points.

By putting the value from figure 2.25 and 2.26, the inductance is 147nH which follow the datasheet and passed the design requirement.
Chapter 3

4-Stroke Design

The 4-Stroke design is discussed in the details. The detailed PCB design is presented and analyzed

3.1 Design Introduction

In the making of the 4-stroke inverter, there are several hardware parts which need to be done. Figure 3.1 shows the parts of 4-Stroke Inverter. In this thesis, the designed board is Power Stage, Gate Driver, and

![Diagram of 4-Stroke Inverter]

Figure 3.1: The design scheme. The blocks inside the big dashed block are the parts which is designed in this thesis

Short circuit protection. These parts are designed into one PCB. The Power Stage is the circuit which contains the 4-Stroke topology, the gate driver is a circuit which converts input signals from the microcontroller into the signals which can drive high-power switches, and
the short circuit protection is the circuit to make the system off when the short circuit happen by sensing the Voltage drop in the inverter.

This design can be operated either as 4-Stroke or conventional two-level inverter.

3.2 4-Stroke PCB

The 4-stroke topology was designed under several specifications to ensure the performance optimization regarding fast switching, high current output, safety, and flexibility during testing. It means this prototype board should be able to handle the thermal increase of the power component in a high current test, save from any electrical failure, and able to suppress the electromagnetic interference (EMI). Note that by having comfortable access design, means that it should easily handle the change in the microcontroller unit software. There are several objectives of the PCB design to get the maximum performance of 4-stroke:

**Mechanical Properties:**

- Component placement of each phase is identical to get the equal performance.
- For cooling in the high current test, a mechanical spring press is used.
- Board should easily to be accessed for measurement.

**Electrical Properties:**

- inverter is used for low voltage application, which is 48 V DC.
- PCB has six layers which consist of 4 conductor layer and two plane layer.
- Capability to deliver 400 A peak current per phase.
- The design should consider EMI.
- Galvanic isolation between MCU and Power inverter.
• Low switching delay in Auxiliary switch.
• Negative voltage gate input for switching test.

3.2.1 Design Challenge

The most challenging problem of the design is to make the component placement as close as possible to the design requirement. Since it should deliver the capability in high current, the several cooling techniques either from system level and component level are implemented. In the component level, the MOSFET and Inductor trace is designed with appropriate thermal via and create an etch opening of power component in the bottom layer for the contact with the cooling plate.

Another important aspect of the design is how to get a good component placement to get an optimum distance between each power component, the gate driver to MOSFET and power component to power input output. Since it is critical to get high performance in switching by faster charging of input capacitance and keeping the EMI in low level, it is important also important to consider the layer stack-up for encountering those problems. Therefore, the design iteration is done and has been compared. There are seven iteration designs that have been done in this project which can be summarized below:

• 1st and 2nd Design
  The first proposed design is the straight power component placement. It consists of 3 high-low side main switch, 2 inductors in series and 2 high-low side auxiliary switch which is placed in straight. This design let the distance between gate driver output close to the MOSFET, and it is equally distributed in all phase. These equal distributions will make the switching output performance between each gate driver equal. Moreover, it is easy from cooling perspective since there is a clear separation between the surface mounted and through-hole component. However, this design has a problem with too much distance between components which make the board produce higher losses. Meanwhile, it only occupied 3 MOSFET for the main switch which will lower the current output.
  The second proposed design is the T-shape design on each power
inverter phase. It consists of 4 pair main switches, two pair auxiliary switches and four inductors (two series and two parallel). It has distributed gate driver output to the power switch, and the distance between Power component is not far compared to the previous design which makes this design is more compact. However, this design is still not solving the problem of an undistributed input-output power source to the component.

- 3rd and 4th Design
  The third design is the triangular design with the negative input in the middle of the main switches, and the auxiliary switch is located in the outer edge of the triangle. By implementing this design, the inverter has a distributed distance between power component, distributed distance between the component to power input-output and comfortable in cooling arrangement. However, since the design is closed, it makes the connection between gate driver and power component is more difficult.
  To make the design that has more distributed distance between gate driver and the power component, instead of using closed power component placement, the open diamond design is used. It has most of the advantage of the previous design, but it possesses much more prominent space in the middle of the design which means bigger PCB design and higher losses since the distance between power component will be much more significant.

- 5th and 6th Design
To accommodate the disadvantage in the previous design, instead of making the diamond in the middle design, the circular design is introduced. By placing the all the power phase output in the middle, it will make the distance between each power component much more compact. However, since all the input-output power is located in the middle, the risk of short circuit arises and makes the safety in the design not achieved. Furthermore, it also gives a difficulty to connect the power output with the respective MOSFET phase.

In design 6th, instead of placing all the input-output power in the middle, the placement is done in a distributed way but still keeping the circular shape. However, by placing the power output tower in the middle of power component, it will give more spacing which makes higher losses.

• 7th Design

The last design is the distributed semicircular design. It combines all the previous design advantages wit distributed input-output power, comfortable access gate driver to power component, and short design between driver to auxiliary switch the smaller size compared to the diamond design make the power component placement is more compact which lower the losses. However, since this design is semi-circular, the manufacture of pressure plate will be more complicated.
CHAPTER 3. 4-STROKE DESIGN

Figure 3.6: Fifth Design

Figure 3.7: Sixth Design

Figure 3.8: Seventh Design

Figure 3.9: The final look of PCB Design
Since the 7th design is the most optimum way in power component placement, this design is used on the final PCB design for the 4-stroke inverter.

### 3.3 PCB Design

The printed circuit Board (PCB) of the inverter with gate driver and its protection circuit is made on FR-4 board with 6-layer and (confidential information) dielectric material between each layer. Important objectives need to be solved to prevent EMI problem:

- Physical segmentation from sources of and susceptors of EMI
- Y-capacitors to reduce common mode noise between electric drives and chassis [1]
- Having solid multilayer ground plane [1]
- Avoid current loops
- Good selection of Bypass and decoupling capacitors

Since all the components are placed in one PCB, the circuit segmentation is needed in order to classify the sources and susceptors of EMI. The segmentation is shown in the Figure 3.10

![Figure 3.10: Circuit Segmentation](image)

Besides, the inverter layouts are essential to minimize the radiated noise and spike voltage and also to get better control of noise to the IC gate driver for ensuring the proper turn-on/off for the MOSFETs. The basic layout idea is coming from the design reference from [10],[20],[4]
and optimized in-house. This layout is used to handle parasitic element which appear unintentionally on the PCB. Parasitic element is a resistance, inductance, or capacitance that possess by electrical component which is not desirable for the intended application [19].

The layout designs consideration for the 4-stroke design is shown in figure 3.11

Figure 3.11: Layout Consideration

Note that one leg is representing auxiliary and main switch. The figure is analyzed in the points below

1. The gate driver should be as short as possible. If it is not possible to make it short, the trace should be made as wide as possible. In the design, the drive has (confidential information) width trace for short trace while (confidential information) width for long trace. This procedure will reduce gate driver impedance which makes faster switching performance since wider and shorter trace will reduce the resistance and inductance value.

2. Confidential Information

3. The DC side stray inductance (L1 and L14) is decreased by using low-ESR decoupling capacitor which connected as central and close as possible to the MOSFET terminals for limiting the voltage transient on the DC bus.
4. DC loop Residual inductance (L2, L3, L6, L7, L8, L10, L11, L12) and AC loop (L13, L9, L4, L5) will give a response such as voltage overshoot.

5. Minimize the distance between the signal ground and power ground for lowering L11 and L12 stray inductance by minimizing the distance between each signal ground and driver ground.

6. Connect all of the driver signal ground in star connection by using a ground plane. The star connection will not make a ground loop which will increase the EMI because the current flow through ground loops can radiate energy to sensitive components. In addition, the fluctuation of true ground reference potential can happen if there are external magnetic sources inducted to the ground loop. [20]

7. Give some distance between the line which sensitive to the electrical noise and lines with high switching voltage transition which means the output gate driver which carrying high current is separated from sensing circuit and comparator. That is one of the reasons the circuit segmentation is needed for EMC.

8. Put as much as possible via in the power component to lower the impedance created by one via component. One via connection will give additional parasitic impedance between each layer. By putting many vias, the lower parasitic impedance will be achieved since the vias is connected as a parallel connection.

Based on the segmentation before, the board is divided into two segments. The first one is power plane and the second is a signal plane. The separation is shown in figure 3.12 while the component placement based on the segmentation is shown in figure 3.13 The signal is consist of input port to the board, short circuit protection, regulator which regulates from $+15V$ to $+5V$ and Flip-Flop circuit for the logic input to the gate driver from short circuit protection while the power plane is consist of gate driver and inverter circuit. In addition to the separation, layer stack up is also important for reducing the EMI production. In this board, 6-layer PCB is used with (confidential information) copper layer thickness for greater current carrying capability and (confidential information) dielectric thickness. The layer stack up is divided
into two parts which is power parts and signal parts as shown in figure (confidential information) and (confidential information) respectively.

From figure 3.14, the positive and negative DC bus is placed closely and coupled together to reduce the capacitive coupling since the distance between both is only (confidential information). Moreover, the multiple ground plane will lower the board ground impedance. In addition, the second layer is used to accommodate the return path to be placed exactly beneath the outgoing path.

On the other hand, the signal plane which is shown in figure 3.15 have a different stack-up the arrangement with the power plane. There is separation between vertical and horizontal routing which the long connection is placed on 3rd and 4th layer while the short one is placed in top and bottom layer with the first, 2nd, 5th, and bottom layer is fully covered by copper of power and ground plane. This arrangement has a function to make the power plane as a shield to reduce the radiation from the long trace connection which is PWM signals.
3.4 Gate Driver

3.4.1 Component Selection

To examine the gate driver that will be used for the circuit, the several solutions is compared. The comparison is tabulated on the table 3.1.

<table>
<thead>
<tr>
<th>Driver Name</th>
<th>Isolation Type</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>1EDC60I12</td>
<td>UL galvanic</td>
<td>-Desaturation protection - Enable - Fault reporting - Over-current protection (ITRIP) - Soft over-current shutdown - Two-level turn-off</td>
</tr>
<tr>
<td>1EDS20I12</td>
<td>Reinforced Isolation UL galvanic</td>
<td>-Separate pin for logic ground, -Separate sink/source outputs</td>
</tr>
<tr>
<td>AUIRS2127</td>
<td>Functional levelshift</td>
<td>- Fault reporting - Single input</td>
</tr>
<tr>
<td>1EDC60H12</td>
<td>UL galvanic</td>
<td>-Separate pin for logic ground - Separate sink/source outputs</td>
</tr>
<tr>
<td>1EDI60N12</td>
<td>Galvanic Isolation</td>
<td>-Separate pin for logic ground - Separate sink/source outputs</td>
</tr>
<tr>
<td>IR2125</td>
<td>Functional levelshift</td>
<td>-Adjustable Shutdown - Current sense - Enable - Fault reporting - Over-current protection (ITRIP) - Single input</td>
</tr>
</tbody>
</table>

From the comparison table, the gate driver based on EDS Family has an advantage since it has a reinforced isolation features, fault reporting, and overcurrent protection. However, this IC is still not available in the market which makes the possibility to use the gate driver based on EDS Family. The other possibility is the using of IC AUIRS2127 or IR2125. Although these drivers have the capability of...
current sense and fault reporting, they only have functional level shift isolation which means it is not electrically isolated. The others are the IC from EDI family which is an isolated gate driver. It is also important to be noted that the UL galvanic is the galvanic isolation that is specified for North America standard. However, they do not share the fault reporting and current sense features. To compare these drive, figure 3.16 and 3.17 shows the comparison between output current and timing of the circuit. [9]

From the current diagram, the AUIRS and IR212 have a low current output which makes the buffer circuit connection in cascade with the gate driver is needed. The addition of buffer circuit will increase the delay which will lower the driver precision. On the other hand, the IC from EDC family has the highest current output which makes it is the best candidate to become the 4-stroke gate driver. From figure 3.17, 1EDI60N12 has the lowest delay which makes this IC is chosen to drive 4-stroke. The gate of the MOSFET is driven by 1EDI60N12 which is an isolated gate driver from Infineon. As mentioned before, it has the capability have a gate output source and sink current around 10 Ampere and has a fast propagation delay and rise/fall time. Since the need for fast and precision switching for the auxiliary switch, those capabilities are necessary since it can charge input capacitance quickly and fast delay means it increases the switching precision.

3.4.2 Gate Driver Circuit

As mentioned before, the gate driver is based on 1EDI60N12AFXUMA1 which is isolated gate driver with current output up to 10 Ampere. The
schematic of the gate driver circuit for one switch is shown in figure 3.18. The gate driver circuit input is run with 5V logic PWM and driven by the 15V voltage at output driver. The output ground is connected with the additional supply voltage for making a faster turn off timing. The bootstrap capacitor is connected to the driver ground and placed as close as possible to the driver output. To prevent under voltage due to the switching, the bootstrap capacitor is charged with oscillator circuit which is rectified by half-bridge diode.

### 3.5 Short Circuit Protection

Since the 4-stroke topology has a short computation time, the short circuit protection is needed to prevent hardware damage when the short-circuit fault occurs. The short circuit occurs when two switches in one leg is conducting in the same time. The comparator circuit based on LM2901D is used in this application. Figure 3.19 shows the protection circuit.

The circuit will sense a short circuit if the condition in figure 3.20. From the simulation, the short circuit occur when the positive DC bus ($B^+$) has higher voltage compared to phase voltage and the phase voltage is higher than negative DC bus ($B^-$) at the time when the switching signals are high. This condition is sensed by circuit 3.19 in some stages. The first one is the circuit senses the voltage at $B^+, B^-$, and Phase by using voltage divider to lower the voltage input into the comparator. Then, IC LM2901D make a comparison whether if the condition of phase voltage is higher than $B^-$ or $B^+$ is higher than

![Simplified Gate Driver circuit schematic](image-url)
Figure 3.19: Simplified Short Circuit Protection Schematic

Figure 3.20: BUS Voltage when Short Circuit occur
Figure 3.21: BUS voltage when no Short Circuit occur
$B-$ is satisfied. If the condition is achieved, the IC will generate 15V voltage output since a 15V system powers the IC. The second stage is the circuit will sense whether this condition is met when the switching signals are high. If the signal from PWM is high while the output from the first comparator is high, the circuit gives short circuit signals to the system and will shut down the operation of the inverter.
Chapter 4

Experiment and Validation

The simulation and experiment will be compared. The test is consist of complete set up explanation, result, and analysis.

4.1 4-Stroke vs 2-Stroke

In chapter 2, the comparison between 4-stroke topology and conventional two-level or 2-stroke has been shown in the simulation. The mock-up inverter is used as Device Under Test (DUT). In the simulation, the drain-source voltage contains high frequency oscillation which is the source of EMI. The Inverter experiment is depicted in figure 4.1.

![Figure 4.1: Expeiment of the 4-stroke and 2-stroke comparison](image)

The comparison between 4-stroke and 2-stroke experiment is shown in figure 4.2 and 4.3.

From figure 4.2, the addition of 4-stroke gives a smoother step response when switching. It matches the preliminary result from the
simulation that the 4-stroke can damp the high-frequency content during the reverse recovery period. Due to the high-frequency content in the drain-source voltage, there is a conducted emission which also high-frequency content oscillation in gate-source voltage. To examine the high frequency content characteristic, figure 4.4 and 4.5 shows the zoom with $50\,\text{ns/div}$ version of high frequency content for $V_{ds}$ and $V_{gs}$ respectively.

The high-frequency content can be estimated roughly by taking two half wave signal points. From figure 4.4 the time difference between two points is $0.012\,\mu\text{s}$ which means the frequency is $83\,\text{MHz}$.

![Figure 4.2: $V_{ds}$ main comparison of Figure 4.3: $V_{gs}$ main voltage of 4-stroke(blue) and 2-stroke(red)](image)

![Figure 4.3: $V_{gs}$ main voltage of 4-stroke(blue) and 2-stroke(red)](image)

![Figure 4.4: $V_{ds}$ 2-stroke high frequency content](image)

![Figure 4.5: $V_{gs}$ 2-stroke high frequency content](image)
mentioned in chapter 3, the driver and inverter circuit is the source of EMI, which means within the frequency range of 83MHz the inverter highly potential candidate in producing a high level of EMI. The EMI discussion will be discussed later in the EMI test section.

4.2 Simulation vs Experiment

In this section, the comparison between model calculation in the simulation will be compared with the measurement result from the experiment. The objectives are to estimates the switching losses generated by switches in 4-Stroke and 2-Stroke. The experiment setup is shown in figure 4.6

![Experiment setup to compare simulation and experimental data](image)

In this test, the load current is set to 60 Ampere constant current. From figure 4.6, $T_{A+}$ represent the upper main switch, $T_{A-}$ represent the lower main switch, and $X_{A-}$ represent the lower auxiliary switch. The Rogowski coil is placed in MOSFET drain for measuring a current through lower auxiliary and upper main switches. Rogowski coil is a current probe for measuring AC current which has thin coil design so that it can be placed to measure drain-source current. Then, the differential probe is used to measure the drain-source voltage to those switches. The differential probe is a probe to measure a floating ground and gives isolation capability between measurement point and
oscilloscope. Note that the 4kHz switching frequency is used during the experiments.

Figure 4.7 and 4.8 shows the $T_{A+}$ drain source voltage and current in 2-stroke from experiment and simulation during reverse recovery period respectively.

From figure 4.8, the simulation can resemble the big picture of the problem which is the drain-source voltage contain high-frequency oscillation. However, the huge difference comes from the current simulation. It can happen because the diode model is simplified to reduce the computational time which makes the model cannot capture high-frequency content like in the experiment from figure 4.7. To compare the power loss in switching between simulation and experiment, the multiplication between voltage and current is done and presented in one figure. Figure 4.9 shows the losses comparison between experimental data and simulation for 2-stroke drives.

From figure 4.9, the power losses from the simulation is much higher compared to the experiment. The reverse recovery in the simulation causes this is slower compared to the experiment. The reverse recovery switching loss is computed at the time when the loss starts to increase until the loss goes back to zero. From the figure, switching loss calculation starts from $1.5 \mu s$ to $1.65 \mu s$. To calculate the switching loss, the trapezoid numeric method is used to calculate the area under the losses to find the energy which is formulated in the equation below

$$E_{sl} = \frac{S_L(k) + S_L(k + 1)}{2} (t(k + 1) - t(k)) \quad (4.1)$$
Figure 4.9: Losses comparison between experiment and simulation in 2-stroke

Where $E_{sl}$ is energy loss during the switching, $S_L$ is the switching power loss, $k$ is the iteration step, and $t$ is time. To calculate the total power loss during the reverse recovery period, the energy should be multiplied by switching frequency. From the calculation, the simulation has total reverse recovery loss 2.31 W where the experiment has 1.234 W.

Figure 4.10 and 4.11 shows the $T_{A+}$ drain source voltage and current in 2-stroke experiment and simulation during when turn-on transition Note that 4-stroke has the same turn-on characteristic since the difference is only when reverse recovery occurs. From both figures, it
can be seen the turn-off response between simulation and experiment is almost same. There is also the small crossed area between current and voltage which indicates the switching loss in this period is small. To verify, the same losses calculation from the previous experiment is done. Figure 4.12 shows the losses comparison between experimental data and simulation during turn-on transition period.

![Figure 4.12: Simulation in turn on transition period](image)

Since the voltage and current measurement has high noise, it makes the losses comparison between experiment and simulation is hard to be done. However, the highest loss peak from the experiment is 150W while 50W for simulation. It verifies the hypothesis that the losses during the turn-off period are small. As the reason of this, this period can be neglected in total losses calculation.

Figure 4.13 and 4.14 shows the $T_{A+}$ drain source voltage and current in 4-stroke from experiment and simulation during reverse recovery period respectively. Although it can be seen that is simulation also reduce the high-frequency content in drain-source voltage during reverse recovery, There is a vast difference in the simulation in a 4-stroke case for both voltage and current during the reverse recovery period. The experiment has faster transient response compared to the simulation. These phenomena confirm that the diode model during reverse recovery cannot capture high-speed transient well. The same losses calculation is conducted which is presented in figure 4.9

Since the calculation result of experiment gives high oscillation due to sensor reading, it is not included in figure 4.15. However, the loss peak of the loss is slow which is not comparable to the simulation. By
Figure 4.13: $T_{A+}$ switch $V_{ds}$ and current during reverse recovery in experiment for 4-stroke

Figure 4.14: $T_{A+}$ switch $V_{ds}$ and current during reverse recovery in simulation for 4-stroke

Figure 4.15: Losses comparison between experiment and simulation during reverse recovery for 4-stroke drives
using the same calculation method to calculate the losses, the simulation gives 1.3419 W.

Figure 4.16 and 4.17 shows the $X_{A-}$ drain source voltage and current in 4-stroke from experiment and simulation during reverse recovery period respectively.

Figure 4.16: $X_{A-}$ switch $V_{ds}$ and Figure 4.17: $X_{A-}$ switch $V_{ds}$ and current during reverse recovery of current during reverse recovery of $T_{A+}$ in Experiment for 4-stroke  

During reverse recovery of $T_{A+}$, the $X_{A-}$ is not undergo reverse recovery. As the result, from figure 4.17, the simulation almost resemble the experiment result. The loss calculation is also done and shown in figure 4.9

Figure 4.18: Losses comparison between experiment and simulation during reverse recovery in $M_{A-}$
From figure 4.18, since the turn-off and turn-off of $X_{A-}$ is a bit faster in experiment compared to the simulation, the loss is increasing and decreasing faster in the experiment. By using the same calculation, the Experiment gives 1.5 W loss while simulation gives 2.75W loss.

### 4.3 Loss Experiment

The loss measurements were done with the measurement and inverter setup shown in figure 4.19 and 4.20

![Measurement Setup of the losses measurement](image1)

![Inverter Setup](image2)

Figure 4.19: Measurement Setup of the losses measurement

Figure 4.20: Inverter Setup

In figure 4.19, the inverter is connected to a variable rectifier DC source with a voltage dc output kept to be constant at 48Vdc. The output is connected with inductor with low resistive losses to represent the low-speed condition in motor control operation. The inverter also kept in the running as a one phase system to specifically seen the switching transient different between 4-stroke and 2-stroke. While keeping the DC input constant, the output current was gradually raised from 30 A to 200 A. Inside the inverter, and the setup is one phase inverter with three main MOSFET and two auxiliary MOSFET in parallel as depicted in figure 4.20

Since the load is purely inductive, the power produced in output is mostly reactive power. To calculate the inverter loss, the active power from the output is measured by measuring the filtered output voltage and true RMS current by using true RMS multimeter. By measuring those, the inverter losses directly can be calculated by following equation below

$$P_{input} = P_{inverter} + P_{output} \quad (4.2)$$

The inverter loss measurement is plotted in three different switching frequency for 2-stroke and 4-stroke which depicted in figure 4.21 with
Figure 4.22 shows the switching losses for each measurements

\[ P_{\text{conduction}} = I_{\text{MOSFET}}^2 R_{\text{dson}} \] (4.3)

By subtracting either 2-stroke and 4-stroke measurements in all frequency range with conduction loss calculation, the switching loss of each measurement can be seen in figure 4.22. The 4-stroke has slightly higher switching losses compared to 2-stroke in all frequency tested. As mentioned before, in this test the auxiliary MOSFET rise and overlap time is high which contributes higher auxiliary MOSFET conduction loss. It is important to consider that inductor conduction loss makes the 4-stroke switching loss higher.
4.4 Impact of auxiliary switch timing

The next step is to test the impact of auxiliary switch timing on the response of drain-source voltage at the main switch. The test is using the same load setup from the previous section which is the use of inductive load. The inverter is operated in single phase and one direction which for the MOSFET and inductor current measurement is using CWT Rogowski coil ultra mini while the measurement of the Upper main switch and the lower auxiliary switch is using a differential probe. Figure 4.23 shows the measurement setup and 4.24 shows the control scheme. The control scheme is divided into the rise and overlap time as mentioned in chapter 2. The control scheme setup is shown in figure 4.25. The phase currents are sensed $V_{DCBUS}$ and $I_{phase}$.

![Figure 4.23: Measurement Setup of Auxiliary control experiment](image)

![Figure 4.24: 4-stroke timing diagram](image)

![Figure 4.25: The control scheme of the auxiliary switch of 4-stroke inverter](image)

from the inverter. If the current sensor senses the direction of the current which match the stages when reverse recovery occurs, the MCU will start to calculate the Overlap and Rise Time. The Overlap time is a constant value which is inputted by the user while the rise time value depends on the Inductance value, phase current and dc bus voltage.
which will be discussed later. The inputted value for overlap time is overlap value which is the value range from 0 to 32767. 0 represents the overlap time always off while 32767 represents the auxiliary switch is always on. In the experiment, the output current is going into the inverter, and it is kept constant during the control time variations. The next section will discuss the impact of the different timing of rising time and overlap time.

### 4.4.1 Rise Time Control Variation of Auxiliary Switch

In this subsection, the impact of overlap timing variation will be discussed. Figure 4.26 to 4.27 shows the experiment result of overlap time variation. The control of the rise time depends linearly on the current by following the equation

\[
t = \frac{LI_{\text{load}}}{V_{\text{bus}}}
\]  

(4.4)

Where \( L \) is the inductance value of the auxiliary inductor, \( I_{\text{load}} \) is the load current and \( V_{\text{bus}} \) is the DC bus voltage. In the experiment, the inductance value is varied to see the effect of the additional on time of the auxiliary switch. From figure 4.26 there is still low amplitude high-frequency content when the applied inductance value is 150nH and 100nH. In addition, there is small voltage dip if the inputted inductance values are small. These phenomena is described later in the

![Figure 4.26: upper main switch \( V_{ds} \) with different inductance value](image1)

![Figure 4.27: Auxiliary Switch \( V_{ds} \) with different inductance value](image2)
next subsection. The different rise time of the auxiliary switch can be seen in figure 4.27 which also in line with equation 4.4.

Figure 4.28 and 4.29 shows the inductor current and upper main switch $V_{gs}$

![Figure 4.28: Inductor current with different inductance value](image)

![Figure 4.29: Upper main switch $V_{gs}$ with different inductance value](image)

From figure 4.28, the inductor RMS current is increasing while the rise time increase, this will give higher conductive loss in the inductor. It also the inductor current is not directly going to zero after auxiliary switch turn-off, and the current is circulates back through the other auxiliary switch body diodes. From figure 4.29 it also can be seen that there still also high-frequency content oscillation in gate-source voltage at the same time with figure 4.26

### 4.4.2 Overlap Time Control Variation of Auxiliary Switch

In this subsection, the impact of overlap timing variation will be discussed. Figure 4.30 to 4.31 shows the experiment result of overlap time variation.

From figure 4.30, if the given overlap value is 10, there is a drop voltage at main switch $V_{ds}$. Besides, there also small voltage dip when the overlap value is 20. It can happen because the auxiliary MOSFET is already turn off when the 4-stroke is still in the dead-time period. This makes the current that goes to inverter should flow through the MOSFET body diode of an upper main switch and upper auxiliary switch. This makes the drain-source voltage will have a voltage drop until the lower main switch on.
Figure 4.30: Upper main switch $V_{ds}$  

From figure 4.30 the upper main switch $V_{ds}$ has a different on time. It is because the output current is kept as constant. To keep output current as a constant while the overlap time is changing, the rise time is also changing. Figure 4.32 and 4.33 shows the gate source voltage of all working switch with overlap value 10 and 40 respectively.

Figure 4.31: Auxiliary Switch $V_{ds}$

From figure 4.31 the auxiliary switch $V_{ds}$ has a different on time. It is because the output current is kept as constant. To keep output current as a constant while the overlap time is changed, the rise time is also changing. Figure 4.32 and 4.33 shows the gate source voltage of all working switch with overlap value 10 and 40 respectively.

Figure 4.32: Gate-source voltage with overlap value 10

Figure 4.33: Gate-source voltage with overlap value 40

From figure 4.32, the auxiliary switch $V_{gs}$ voltage lower than the threshold voltage when still in the dead-time period which makes phenomena in the previous discussion happen. In both cases, it can be seen that the gate-source voltage is not reaching steady state in 15V since the gate resistance is high. The objective of choosing the high gate resistance in an auxiliary switch is to lower the turn off spike os-
4.5 Radiated Emission Test

The next step is to test the radiated emission test from the inverter when the inverter is operated as 4-stroke and 2-stroke. The measurement setup is shown in figure 4.34.

![Figure 4.34: A schematic of Radiated emission test setup](image)

To represent the actual condition when the setup is implemented in LBEV instead of DC rectifier. The battery is fully charged and has 52 V voltage during all the test. Because of this reason the artificial Line Impedance Stabilization Networks (LISN) is not used in the connection between Voltage input and Inverter. Furthermore, the output of the battery does not contain a noise from AC grid which means less significance of using LISN. Also, to represent the actual load during the vehicle operation, the two-phase of PMSM motor is connected to the inverter load to make a single-phase inductive load. The log-periodic antenna is placed one meter from the DUT which is the inverter. Normally, for low voltage truck drives (EN 12895), the radiation test should be done with the antenna for 10m. However, since there is no space for conducting 10m radiation test, the one-meter test is used. The difference between 10m and a one-meter test is the amplitude reduction of $-6$ dB (Inmotion standard) value on each frequency from 30MHz to 1GHz. However, It is essential to be known that the objectives are not to compare the experiment with standard but to com-
pare between radiated EMI produced by 4-stroke and 2-stroke. The emission data is collected from the spectrum analyzer. Note, the measurement should be done in a closed chamber to protect the test from a noisy environment. Figure 4.35 and 4.36 shows the radiated emission measurement result between 4-stroke and 2-stroke for lower frequency and higher frequency respectively.

In high frequency, the performance of 4-stroke is much better compared to 2-stroke. The highest emission reduction can be seen in the frequency around 60MHz until 100MHz. This result match initial assumption that 4-stroke can decrease the emission level on these frequency ranges. The radiated test is also conducted in 8kHz switching frequency. Figure 4.37 and 4.38 shows the measurement result in higher and lower frequency.

At higher frequency, The 2-stroke 8kHz has the highest radiated emission. Interestingly, the 2-stroke 4kHz almost has the same emission compared to 4-stroke 8kHz. From figure 4.38 at the frequency between 1MHz to 6 MHz the 4-stroke in both frequency has higher radiated emission compared to 2-stroke emission.
4.6 Conducted Emission Test

In this section, the conducted emission test is done which consist of two different test, the first one is differential emission test and later is common mode test. Differential-mode is defined to be disturbances concerning line-to-line while the common-mode is disturbance from line to ground. [16]

4.6.1 Differential-Mode Emission Test

The measurement setup for differential-mode emission test is depicted in figure 4.39. The electrical connection between differential mode emission and radiated emission test is almost same. However, the difference is in here the measured property is current noise which is measured by the current probe and a spectrum analyzer collects the emission data. The current sensor is only measured in one line which is in this test the positive DC voltage is measured.

From both figures, there are two measurements presented in this test which are peak and average emission value. From figure 4.40 4-stroke has higher differential-mode emission compared to 2-stroke. In low frequency, the 2-stroke has better differential emission performance. It happens because the introduction of air coil inductor in the

Figure 4.37: Radiated Emission between 4-stroke and 2-stoke in 8kHz and 4kHz switching frequency at a higher frequency test (50MHz to 100MHz)

Figure 4.38: Radiated Emission between 4-stroke and 2-stoke in 8kHz and 4kHz switching frequency at a lower frequency
Figure 4.39: A functional schematic of differential emission conduction test

Figure 4.40: Differential-Mode Emission for 4-stroke and 2-stroke in lower frequency range

Figure 4.41: Differential-Mode Emission for 4-stroke and 2-stroke in higher frequency range
design which gives higher emission in low frequency since the magnetic path is big. Better coil mounting in the drives can reduce this problem.

From figure 4.41 4 stroke has a better emission suppression in the range of 40MHz to 100MHz. This differential-mode emission test also confirms that the high-frequency content during reverse recovery is causing EMI.

### 4.6.2 Common-Mode Emission Test

The measurement setup for common-mode emission test is depicted in figure 4.42. Notice that the measurement setup is almost same with differential-mode emission. However, instead of measuring current in one line, the current sensors are placed to measure both positive and negative line. Figure 4.43 and 4.44 shows the common-mode emission test result for lower and higher frequency respectively. From figure 4.43 averagely, 4-stroke produce lower emission performance compared to 2-stroke. It can happen because the additional switch which switches fast makes a parasitic capacitance to chassis(ground). This parasitic capacitance exists due to the emergence of the switched voltage potential across the MOSFET drain and ground. This phenomenon can be drawn in the figure 4.45.

The noise current that goes through the parasitic capacitance is following equation

$$I_c(t) = C_p \frac{dv(t)}{dt}$$

(4.5)

Where $I_c(t)$ is the current flow through parasitic capacitance, $C_p$ is the parasitic capacitance, and $\frac{dv(t)}{dt}$ is the switching voltage of the MOSFET.
Figure 4.43: Common-Mode emission test comparison for 4-stroke and 2-stroke in lower frequency range.

Figure 4.44: Common-Mode emission test comparison for 4-stroke and 2-stroke in higher frequency range.

Figure 4.45: Illustration of parasitic element created by MOSFET switching in one leg.
It means that this current will increase with the increase of switching speed. Since in 4-stroke has auxiliary switches, the common-mode noise is increasing. To overcome, the proper choice of Y-capacitor and placed it between positive and negative DC bus to the ground which makes lower impedance path from ground to voltage source.

On the other hand, at the 40MHz to 100MHz, it is expected that 4-stroke has better performance in emission suppression due to the high-frequency oscillation damping when reverse recovery occurs.
Chapter 5

Conclusion and Future Works

5.1 Conclusion

The goal of this thesis is to design and implement the new inverter topology patented by Inmotion Technologies named 4-stroke which can give damping at MOSFET due to reverse recovery period occurs. The thesis is done by model the 4-stroke topology in LTSPICE which the MOSFET model was made based on the datasheet. The other important aspects of 4-stroke design are choosing the inductor value. The air coil inductor is chosen due to its capability not to saturates or always linear regardless of the flown current.

In this thesis, the inverter is designed in FR-4 6-layer PCB with (confidential information) thickness and (confidential information) dielectric thickness between each layer. Several guidelines and techniques have been implemented to reduce the parasitic effect that reducing inverter switching performance. The inverter design also includes the gate driver and short circuit protection design.

The experiments shows that the conventional two-level inverter (2-stroke) produce high-frequency oscillation which is the source of EMI in the frequency range 60MHz to 100MHz. Comparative study between simulation and experiment result has been done. All and all, the simulation depicts a big picture of the 2-stroke problem and gives the insight of the advantages of 4-stroke. However, the simplified diode model gives the limited capability to capture high-frequency oscillation phenomena. From the experiment and simulation, the turn-on transition period of MOSFET gives low MOSFET losses compared to the turn-off period. 4-stroke can reduce the switching losses of the
main switch during reverse recovery but gives the additional switching losses in the auxiliary switch. The inverter losses experiments have been done by connecting inverter output to inductive load to represent vehicle at low speed. From the measurement result, 4-stroke gives a slight increase in switching losses compared to 2-stroke. It is happening because, in the experiment, the auxiliary on time is set to be extended which increase the losses in the inductor in auxiliary switches. The auxiliary switch timing control which consists of rising and overlap time is also done in the experiment. The experiment is conducted by keeping the output current constant. The result shows that the shorter rise time, the high-frequency content in drain-source voltage is more apparent. However, the increasing of rising time gives higher conduction loss in the auxiliary switches. For the overlap time, the lower overlap time will give voltage dip in the drain-source voltage. It happens because the auxiliary switch is turned off when the dead-time period is not over which makes the load current should flow through MOSFET body diode.

The EMC experiment which consists of radiated emission test and conducted emission test has been done. In radiated emission test, 4-stroke is better to damp the emission in the frequency range of 60MHz to 100MHz. For conducted emission test, two different type of test has been performed which are differential-mode and common-mode emission test. In differential-mode emission test, 2-stroke has better performance in low-frequency range while 4-stroke has better performance in the high-frequency range. The lower performance happens because of the air coil inductor which has significant magnetic path since the inductor placement is not optimal in the prototype. For common-mode emission, 2-stroke also has better performance compared to 4-stroke in lower frequency range due to the auxiliary switch gives additional unwanted parasitic capacitance. This problem can be solved by proper choice and placement of common-mode Y-capacitor to lower impedance path from ground to the voltage source.

5.2 Future Works

The making of an algorithm for implementation in three phase is needed to test the 4-stroke performance in running the motors. The diode model can be improved by better tuning or makes another model to
represent reverse recovery periods better. Also, the better algorithm for controlling the auxiliary performance is needed to gain better trade-off for lowering inverter loss and EMI.
Bibliography


