Improvements in Power Line Communication Reliability for Electric Drives by Random PWM Techniques

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Abstract—Power line communication (PLC) techniques seem a worthwhile research issue not only in civil applications, but also into the industrial scenario. The realisation of a communication network using the already existing electrical network is attractive for cost benefits, even though it represents a real challenge. Major problems concern communication reliability, effectiveness of transmission modulation methods and algorithms for error correction. EMC issues also must be taken into account, considering the consequences of injecting high-frequency harmonics into the AC power distribution system. This paper deals with the application of PLC techniques to the harsh and noisy environment of electrical drives. This study points out how the improvements in communication reliability can be achieved not only by a smart choice of the communication protocol, but also by using proper inverter modulation techniques, as Random Space Vector Modulation. The experimental results of transmission tests with both conventional and random space vector modulation techniques are here presented and discussed.

I. INTRODUCTION

In typical industrial motion systems, electrical drives share a common power supply and are located far from the control supervisor. Bright examples are represented by industrial systems in which many inverter-fed ac motors share a common DC bus, or specific applications in which the drive location is critical, as in the case of submerged pumps with on-board electronic. In these applications, a dedicated bus is often used for information exchange between each drive and the remote supervisor.

The data transferred through the bus are either reference signals to the control units, or supervisor actions directed to the management of status alarms coming from the drive location.

Wired systems obviously increase installation and maintenance costs, while reducing the overall system reliability. This is especially true when a slow data flow between the parts may suffice. A dedicated bus for a low 32 kbit/s rate, which is enough to transmit, every millisecond, a word (16 bit) containing a speed reference and a word (other 16 bit) for a general-purpose status register, represents a non-negligible factor in the overall system cost. Removing the data bus between supervisor and drives should be a significant improvement in terms of both economic savings and reliability.

The actual trend of embedding intelligence in every remote component, particularly on electrical drives, can be capitalized with the purpose of creating a communication network based on the already existing

power supply network. This should lead to a strong reduction in wiring costs, although the complexity of the transmission methods should increase. Besides, nowadays power line communication techniques are already adopted by several power energy distributors, to realize a data exchange between elements supplied from the main line (automatic measure and remote control, [1]).

Many studies have been conducted on noise modelling in low voltage mains for civil/residential purposes [2] and signal propagation modelling in general PLC communication networks [3]-[5], although industrial system PLC applications have not been specifically investigated yet.

One of the major challenges in the use of PLC techniques into the electrical drives scenario is represented by the communication reliability and the countermeasures for its improvement. Actually, reliability (as trade-off with bit rate) is the key factor in an extremely noisy environment, as that of power lines feeding PWM inverters. Signal transmission among these lines suffers the presence of conducted noise due to the inverter switching activity. Moreover, in an industrial system with several inverters, each with its own switching frequency, and all sharing a common DC bus, harmonics can be predicted neither in amplitude nor in frequency.

Communication reliability on power lines can be improved not only providing a robust transmission technique with good error correction algorithms [6], [7], but also by using proper inverter modulation techniques.

As a practical example, in a shared DC bus configuration with different switching frequencies originated by an unknown number of inverters, a Random Space Vector Modulation (RSWM) technique [8], [9] should lead to consistent benefits, because of its capability of spreading the power spectrum over a broad frequency range.

With these premises, a laboratory bench has been implemented with the purpose of exploring the benefits of RSVM techniques on a Frequency Shift Key (FSK) transmission between two industrial PLC transceivers, located at the ends of the power cable that connects an inverter-fed induction motor to the main supply.

The expected advantages are confirmed by the experimental results, which show a statistical report of various transmission tests using classical Space Vector Modulation (SVM) techniques compared with a RSVM technique.

II. THE PROPOSED RSVM TECHNIQUE

An ideal RSVM technique should vary the switching frequency or the pulse position within the switching period in a continuous and random manner. However, digital implementations of RSVM techniques must cope with the limits of fixed-point hardware and memory size. In order to obtain a simplified RSVM technique, which is suitable to be implemented on low-cost drives, a digital frequency-span RSVM algorithm has been adopted. The basic concept lies in the relation between a pseudo-random generated number and the output switching frequency range that, in this case, has been chosen between 6.3 kHz and 11.2 kHz.

One of the simplest ways of obtaining m pseudo-random numbers is to use a pseudo-random generator, which can be implemented by the following recursive expression:

$$x_{k+1} = (ax_k + c) \bmod m \quad (1)$$

in which the mod operator represents the rest of the division of $(ax_k + c)$ by m .

Different initial conditions x_0 leads to different sequences; moreover, there are some constraints on the values of a and c in order to obtain a good sequence of uniformly distributed random numbers, as reported in [10]:

$$\begin{aligned} \sqrt{m} &\leq a \leq m - \sqrt{m} \\ a \bmod 8 &= 5 \\ \frac{c}{m} &= \frac{1}{2} - \frac{1}{6}\sqrt{3} \end{aligned} \quad (2)$$

For the implemented RSVM technique, the following values have been selected:

$$\begin{cases} m = 1024 \\ a = 517 \\ c = 217 \end{cases} \quad (3)$$

Moreover, considering the minimum time interval that can be represented on the microprocessor used for the RSVM algorithm implementation, that in this work was $Q = 160$ ns, the number of different switching frequencies is equal to:

$$N_f = \frac{\frac{1}{f_{\min}} - \frac{1}{f_{\max}}}{Q} = \frac{\frac{1}{6300} - \frac{1}{11200}}{160 \cdot 10^{-9}} = 434 \quad (4)$$

The length m of the pseudo-random sequence reflects a compromise with the required microprocessor storage space. A value of $m=1024$ has been selected in this work. However, the following procedure allows the virtual stretch of the sequence, with benefits in terms of power spectral density of the resulting RSVM. Three pseudo-random sequences have been created off-line by using (1) with the following initial conditions:

$$\begin{cases} x_0 = 0 \\ y_0 = 1 \\ v_0 = x_0 \end{cases} \quad (5)$$

The sequences have been stored as three vectors X , Y and V respectively. During the on-line execution of the random sequence, the vector elements are combined following three steps (Fig. 1):

- For $i=1..m$, generation of the index $j=Y(i)$;
- extraction of the final value from the scramble vector $u=V(j)$;
- substitution of $V(j)$ with a new value from the sequence stored in X , $V(j)=X(u)$.

Fig. 1. Pseudo-random sequence generation.

It can be shown that, if boundaries (2) are fulfilled, the resulting pseudo-random sequence has a repetition length of m^2 .

Each pseudo-random number must be associated to each of the N_f frequency (4). It is worth to note that a direct relation between $V(j)$ and N_f would lead to uniformly distributed frequencies in the frequency domain, but not in the time domain (i.e. lower frequencies are applied for a higher time with respect to higher frequencies).

Although there are no significant advantages in the experimental tests, theoretical analysis of the RSVM spectrum is simplified if the frequencies are uniformly distributed in the time domain [11, 12]. To get that feature, the output sequence (which span between 1 and m) has been mapped into the N_f frequencies by setting N_f intervals of variable length, computed by

$$I_h = \frac{mf_h}{\sum_{i=1}^{N_f} f_i} \quad (h = 1, \dots, N_f) \quad (6)$$

In this way, the theoretical interval length related to each of the N_f frequencies assumes the linear outline, represented by the dotted line of Fig. 2.

It can be interpreted by considering that a time-uniform sequence of switching frequencies would require that, for example, the frequency 7 kHz should appear twice in the m -elements vector which maps the output $V(j)$ to the randomly selected switching frequency.

On the other hand, a higher frequency, for example 8 kHz, should appear a fractional number of times in the aforementioned mapping vector (dotted line in Fig.2), and this is practically unfeasible.

Fig. 2. Mapping vector for the random sequence.

In practice, a quantization of the interval length has become necessary. Fig. 2 indicates that the length of the intervals can be split between two and three elements. Therefore, the output frequency vector has been divided into "a" intervals of two elements and "b" intervals of three elements, satisfying the following constraints:

$$\begin{cases} 2a + 3b = 1024 \\ a + b = 434 \end{cases} \quad (7)$$

which returns $a = 278$ and $b = 156$. Consequently, the output vector of switching frequencies has been divided in 278 intervals of two elements and 156 intervals of three elements, associating the lower frequencies (higher switching periods) with the 2-elements intervals, and the higher frequencies (lower switching periods) with the 3-elements intervals (continuous line, Fig.2).

Approximately, (7) yields the desired uniform frequency distribution in the time domain.

III. TEST-BED IMPLEMENTATION

The experimental laboratory setup consists of a variable transformer, an inverter-fed IM motor, and a couple of PLC transceivers, for a master-slave communication on the U-V phase lines, as depicted in Fig. 3.

Fig. 3. Laboratory setup general scheme.

The inverter is controlled by means of a card equipped with a Texas Instruments TMS320C31 floating-point DSP, for fast control prototyping. By means of a C-written code, the control card allows an easy change of the PWM parameters characteristics, as switching frequency and type of modulation (classical PWM or RPWM).

The PLC board is based on ST7538 Frequency Shift Keying (FSK) transceiver, whose block diagram is reported in Fig. 4. It is an integrated modem chip

specifically designed for PLC applications on low voltage (220V) and medium voltage (2KV) main supply.

It realizes the interface from an electrical network and a system (usually a microprocessor with some sensors), which manages the main control procedure and the upper layers of the communication protocol.

Fig. 4. ST7538 FSK transceiver block diagram.

The transceiver is organized in three main sections: the modem section, the serial interface with control logic section and the microprocessor supervisor section. For several reasons, which are linked to the topology of the electrical network, the noise and the low impedance of the line, the transmission is realised by means of a half duplex Frequency Shift Key modulation (FSK).

Shortly, it is worth to recall that the FSK modulation technique translates a digital signal into a sinusoidal signal that can have two different frequency values, one for the logic high-level of the digital signal (f_h), the second one for the low level (f_l) [13]. The average value of the two tones is the carrier frequency (f_c). The difference between the two frequencies is a function of the baud rate b_r of the digital signal (the number of symbols transmitted in one second), as follows:

$$f_h - f_l = dev \cdot b_r \quad (8)$$

where dev is the deviation, a user-selectable parameter.

The PLC board is able to communicate using one of 8 different channels (60, 66, 72, 76, 82.05, 86, 110, 132.5 kHz), selecting for the chosen channel four baud-rates (600, 1200, 2400, 4800) and two different deviations (1 and 0.5). These parameters are configured writing the internal control register (Status Register, Fig. 4).

It has been found that the transmission reliability is hardly affected by the choice of a correct parameter set, whose selection is not trivial [13, 14].

The modem provides the possibility of inserting a preamble and the reception operated by the slave card can be conditioned on the recognition of a predefined characters pattern, to limit as much as possible the retransmissions, with the consequent reduction of the baud rate.

Actually, the influence of noise is critical in power lines connected to PWM inverters. The preamble uses only a 16-bit sequence but reduces the reception of wrong messages or, in the worst case, the lost of the entire message. As a matter of fact, experimental results have shown an increase in communication immunity if the transmission uses the preamble detection combined with carrier detection.

The PLC board is equipped with a power line interface,

which filters out all the environment noise except the band of the modulated signal. All filters' sections that compose the board circuitry interface are shown in Fig. 5. It is worth to note that the Rx Band Pass (BP) filter must be tuned according to the selected carrier frequency.

Fig. 5. PLC board interface with the main line.

The topology of the Rx BP filter is that of a resonant parallel circuit: C_{36} , L_7 and R_{11} realize a 2nd order passive filter with cut-off frequency of

$$f_0 = \frac{1}{2\pi \cdot \sqrt{C_{36} \cdot L_7}} = 132.5 \text{ kHz} \quad (9)$$

To limit the cross coupling with the transmission circuit, R_{11} has been selected as higher as possible. The chosen components also influence the quality factor of the filter, which is equal to:

$$Q \cong R_{11} \sqrt{\frac{C_{36}}{L_7}} = 2.85 \quad (10)$$

Finally, a proprietary software supervisor runs on two PCs connected via RS232 with the master and the slave PLC transceivers, allowing transmission of arbitrary sequences of maximum 127 bytes with three transmission modes (continuous, one-shot or repeated N times), or ping (Packet InterNet Groper) operations between the cards. A photo of the PLC board is shown in Fig. 6.

Fig. 6. The PLC transceiver board.

IV. EXPERIMENTAL RESULTS

The experimental stage of the work is essentially divided in two parts: a spectrum analysis and a statistic test using the ST7538 ping protocol with the correction bit error algorithm.

A. Spectrum Analysis

For the spectrum analysis, the phase-to-phase voltage has been measured utilizing a differential probe and a digital oscilloscope, as sketched in Fig. 3. FFT signals have been directly created with the oscilloscope math facilities, and then saved and post-processed in the Matlab environment.

For the following experiments, a 4800 baud-rate has been chosen, and a unit coefficient for the deviation frequency ($dev=1$). The selected carrier frequency was $f_c=132.5 \text{ kHz}$ so that, according to (8), the FSK algorithm uses

$$f_l = 130.1 \text{ kHz} \quad f_h = 134.9 \text{ kHz} \quad (11)$$

The measured FSK modulation spectrum, with an inverter DC bus of 250 V and no inverter activity, is shown in Fig. 7.

Fig. 7. FSK spectrum ($f_c=132.5 \text{ kHz}$, $b=4800 \text{ Hz}$, $dev=1$)

FSK transmissions have been performed while the inverter was feeding the IM motor with either a symmetric 12 kHz SVM [15] or with the RSVM described in Sect. I.

Fig. 8 and Fig. 9 show the phase-to-phase main supply voltage spectrum of the 12 kHz SVM and the RSVM respectively, with a 250V DC bus voltage and a modulation index of about 40%.

Fig. 8. Main supply, SVM phase-to-phase voltage spectrum. ($x=26.4 \text{ kHz/div}$, central freq. 132.5 kHz ; $y=36.3 \text{ dB/div}$)

The switching frequency at 12 kHz has been selected because its eleventh harmonic nearly matches the selected carrier frequency, and therefore it is a clear case in which the noise conducted into the mains can hardly affect the reliability of the PLC. As expected, SVM shows sharp

harmonic peaks at specific frequencies, while the RSVM exhibits a spread and smooth spectrum.

Fig. 9. Main supply, RSVM phase-to-phase voltage spectrum. ($x=26.4$ kHz/div, central freq. 132.5 kHz; $y=36.3$ dB/div)

In particular, as highlighted by red circles in Fig. 8 and Fig. 9, the amplitude of the noise at the central frequency of 132.5 kHz, with RSVM, is almost 12 dB lower than that of SVM, and this has positive effects in the percentage of successful power line transmissions, as shown in the next paragraph.

B. Ping Test

Using the RS232 serial port interface facility of the PLC boards and two PCs (one for each PLC board), it is possible to realize a ping test, to investigate on the statistics of transmitted and received data through the transmission line.

The ping test architecture implemented on the PLC board is realized by transmitting data frames through the line with redundant bytes, used for error detection and correction. In principle, several slaves are able to respond to the master, through an addressable protocol. In this specific case, only a board-to-board configuration has been used for the communication tests, as shown in Fig. 3. The ping protocol master frame is composed of a total of 20 bytes, as shown in Table I.

TABLE I.
MASTER FRAME STRUCTURE FOR PING TESTS

Preamble	Header	Slave address	Master address	Message Number	Auxiliary byte	FCS
AAAAh	9B58h	8 bit +FEC	8 bit +FEC	(8 bit +FEC) x3	8bit +FEC	(8 bit +FEC) x2

Once a PLC board, acting as a master, has sent the 20 bytes frame, another PLC board, acting as a slave, detects the data and answers with an ACK frame of the same size, which composition is reported in Table II.

TABLE II.
ACK (SLAVE) FRAME STRUCTURE FOR PING TESTS

Preamble	Header	Slave address	Master address	Message Number	Auxiliary byte	FCS
AAAAh	E958h	8 bit +FEC	8 bit +FEC	(8 bit +FEC) x3	8bit +FEC	(8 bit +FEC) x2

Meanwhile, the master board waits for any slave response, for 200 ms. Then, a timeout routine is triggered, and the master reports to the PC a Not Acknowledged

(NA) message, through the serial line.

Different tests have been performed using different DC bus voltages, comparing the percentage of the correct received messages with either the classical SVM or the RSVM. Fig. 10 shows a histogram of the results.

Fig. 10. Percentage of correct messages as function of DC bus.

The higher the DC bus voltage, the higher the percentage of NA messages. Likely, this is because it is higher the noise conducted to the mains. Nevertheless, the percentage of correct data frames is in any case better with RSVM (62.29% mean, 86% peak, 44% worst case) with respect to conventional SVM (53.52% mean, 79% peak, 28% worst case).

Fig. 11 reports another trend: among correct received messages, the percentage of messages corrected by the error correction algorithm, with respect to all acknowledged messages. Consistently with the results of Fig. 11, the number of corrected messages is generally higher as the DC bus voltage increases, while the differences between RSVM and classical SVM are not relevant in this case.

Fig. 11. Messages handled by the error correction algorithm.

V. CONCLUSIONS AND FUTURE WORKS

In this paper, the application of power line communication in the noisy environment of electric drives has been proposed. In particular, the influence of voltage inverter modulation technique on transmission reliability has been carefully investigated.

The experimental results, carried out on laboratory setup with evaluation power communication boards have confirmed that random Space Vector Modulation, with its spread frequency spectrum, greatly improve the data integrity. The mean percentage of corrected data frames,

under different working condition, passes from the 53.52% of conventional space vector modulation to the impressive 62.29% of random modulation. Future works will include the possible implementation of the PLC system into a low-cost FPGA component, for easier integration with the drive system.

VI. ACKNOWLEDGMENTS

The authors gratefully acknowledge the contribution of E.Saccani, for his precious advice during the experimental stage of this work.

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