Carrier-less fault-tolerant stochastic synthesis in multi-cell multi-level converters: a central limit approach to highly-dimensional power electronic systems

Pierluigi Tenca¹, Luca Peretti² ✉

¹ABB Corporate Research, Munich D-80802, Germany*

²Department of Electrical Systems, ABB Corporate Research, Forskargränd 7, 72178 Västerås, Sweden

*Author's Former Institution

✉ E-mail: luca.peretti@se.abb.com

ISSN 1755-4535

Received on 26th June 2015

Revised on 1st November 2015

Accepted on 7th November 2015

doi: 10.1049/iet-pel.2015.0503

www.ietdl.org

Abstract: As the number of cells in multi-level converters increase, issues related to the high number of subsystems enter the power electronics area. Within this frame, this study presents a carrier-less approach to the voltage synthesis across the series of several voltage-source cells in multi-level converter topologies. The key idea is the exploitation of a stochastic-based choice of the discrete cell output voltage, operating according to a local, independent random variable. When the number of cells is sufficiently high, the law of large numbers and the central limit theorem (CLT) of the probability theory guarantee that the synthesis of the total voltage lies in a known interval with high probability. Because of the CLT stochastic properties, an increased number of cells inherently leads to more robust and fault-tolerant waveforms, also due to the reduced capacitors required in each cell. The absence of deterministic modulation reduces the hardware cost (cabling and control) and requires no reconfiguration in case of cell failures. This work focuses on the theoretical and hardware-in-the-loop validation of the main principle, including an analysis of the capacitance requirements for each cell. The method could be also applied to current-source multi-level converters based on parallel connections of current-source cells.

1 Introduction

The conventional approach for the synthesis of voltage waveforms in high-power voltage-source multi-level converters (MMCs), based on several cells connected in series, is deterministic and it relies on a multitude of synchronised carriers. A well-known example of such class of converters is the MMC structure proposed in [1–4]. In such deterministic synthesis concepts [5–7], the higher the number of cells, the greater the complexity of the command chain, which is realised in practice with optical fibres and optoelectronic transmitter/receivers for the feedback, acknowledgement, and switching signals. By either generating the switching signals inside the cells upon reception of the voltage command, or by letting the central controller to generate directly each single switch command, the number of communication channels easily reach the order of hundreds, even when multiplexing techniques together with addressing schemes of the cells are employed [8]. In other words, deterministic approaches impose significant reliability requests and increase costs, which are critical aspects in modern power system applications [9]. In addition to that, envisioning even greater ratings for HVDC and DC-grid converters would demand a very large number of cells, where deterministic synthesis approaches could lead to increasingly complex control hardware.

One of the many possibilities to reduce critical issues, improve system availability and reduce life cycle costs [4, 9] could be represented by an alternative approach of voltage synthesis. To this aim, this paper describes a non-deterministic approach to the voltage synthesis of multi-level waveforms, whose basic principles were already disclosed in [10, 11]. Its conceptual roots are based on the law of large numbers and the central limit theorem (CLT) from the probability theory [12]. The CLT is a well-known fundamental law of nature describing systems where the behaviour is ruled by the additive effect of a multitude of similar, yet independent, elementary entities. Indeed, in the case of MMCs, several voltage-source cells connected in series form a physical

system composed by many elementary entities, and the total voltage at the two terminals of the series becomes the sum of all cell voltages. Thus, this system could produce the total voltage in a stochastic way, by relying on the CLT. Each single cell should behave as a discrete random variable, independent from all others yet identically distributed, with an output voltage distribution related to the desired total arm voltage.

Such methodology is different from random pulse-width modulation (PWM) methods based on probabilistic distributions of the switching intervals, which are well known in literature [13–15] and were also applied to MMCs [16]. Random PWMs have been used to typically achieve spread-spectrum waveforms for mitigation of electromagnetic interferences and/or structure-borne mechanical noise. In this work, the proposed synthesis does not introduce randomness in the switching instants, but truly in the voltage values generated by each cell.

This paper is organised as follows. Section 2 is devoted to the description of the main principle of the proposed approach, followed by considerations on the minimum capacitance required by each cell, reported in Section 3. A real-case analysis is discussed in Section 4, while hardware-in-the-loop (HIL) evidence is given in Section 5. Some final remarks will conclude the paper.

2 Main principle

2.1 Stochastic-based synthesis

The voltage network composed by the series of N_c cells resembling an arm of a voltage-source MMC is shown in Fig. 1. The single cell structure considered in this work is reported in Fig. 2. The cell is a conventional H-bridge with a local random number generator and a controller, whose functions are explained in Sections 2.4 and 2.5.

The main principle of the stochastic synthesis is inspired by a corollary of the CLT [12]. When a multitude of equally

Fig. 1 Structure of a voltage-source multi-cell arm with N_c cells. Each cell can generate a discrete set of voltage values, with at least two elements

distributed, yet independent random variables are added together, as in the network of Fig. 1 when N_c is large, the distribution of the sum approximates a Gaussian law. Its expected value equals the sum of the expected values of the single variables, whereas its variance becomes smaller as the number of variables increases [12]. This concept applies both to the sum of the voltages of several series-connected cells of a voltage-source MMC arm, and to the sum of the currents of several parallel-connected cells of a current-source MMC arm [17].

The simplest case is represented by the series of N_c independent voltage-source two-level cells, each synthesising an output voltage of either $+v_{c,j}$ or $-v_{c,j}$, according to Fig. 2. The j th cell internally generates a uniform independent (pseudo-)random sequence $R_j(t) \in [0, 1]$, and it receives from a central controller a 'reference probability' $p^*(t)$, which represents the probability of the event: ' $v_j = +v_{c,j}$ at the instant t '. The signal $p^*(t)$ is sent identical to all cells.

The cell voltage synthesis occurs at discrete time instants kT_s , $k \in \mathbb{N}$, where T_s – possibly variable – is the time interval between two successive generations of a random number, different for each independent cell. At each kT_s , the j th cell generates its own $R_j(kT_s)$, independently from all other cells, and it compares $R_j(kT_s)$ to $p^*(kT_s)$. The comparison determines the output of the j th cell according to the rule (1). The cell voltage is kept constant for the interval $[kT_s, (k+1)T_s]$. The same algorithm is executed independently and locally for all N_c cells.

$$\begin{cases} v_j = +v_{c,j} & \text{if } R_j(kT_s) < p^*(kT_s) \\ v_j = -v_{c,j} & \text{if } R_j(kT_s) > p^*(kT_s) \end{cases} \quad (1)$$

The output voltages can be considered as discrete-time independent stochastic processes, with the following ensemble expectation

$$E[v_j(kT_s)] = (2p^*(kT_s) - 1)v_{c,j} \quad (2)$$

When $p^*(kT_s) = 1$, all cells synthesise $v_j = v_{c,j}$ with probability 1, while for $p^*(kT_s) = 0$ all cells synthesise $-v_{c,j}$ with probability 1. For $p^*(kT_s) \in]0, 1[$ some cells synthesise $+v_{c,j}$ and some others $-v_{c,j}$ without any possibility to determine each cell behaviour in advance. Nevertheless, when N_c is sufficiently large and with the assumption of equal $v_{c,j}$ for all cells, the CLT ensures the following ensemble expectation of the total arm voltage process (the subscript j is removed for simplicity of notation)

$$E[v_{arm}(kT_s)] = v_{arm}^*(kT_s) = (2p^*(kT_s) - 1)N_c v_c \quad (3)$$

and most importantly its variance is monotonically and non-linearly

Fig. 2 Full H-bridge cell considered as the reference cell for this work

decreasing with N_c [12]. For larger values of N_c , it is more probable that the arm voltage $v_{arm}(t)$ remains close to its expected value (3), which is a deterministic signal since the probability $p^*(t)$ is a deterministic signal. By solving (3) for $p^*(t)$, one obtains the expression for the deterministic signal $p^*(t)$ from the desired arm voltage reference $v_{arm}^*(t)$ (with $|v_{arm}^*(t)| \leq N_c v_c$)

$$p^*(t) = \frac{v_{arm}^*(t)}{2N_c v_c} + \frac{1}{2} \quad (4)$$

2.2 Cost considerations on the proposed principle

The signal $p^*(t)$ is the only deterministic signal sent from the central controller to all cells, which implies that no centralised deterministic switching commands and no communication among cells are required. Moreover, the proposed approach does not require any carrier, hence no reconfiguration of deterministic modulation patterns is required in case of failure. This is a main difference with respect to deterministic schemes, which must guarantee reliable centrally-calculated switching signals, including a carrier reconfiguration scheme in case of cell failure. Furthermore, differently from the stochastic syntheses, the complexity and the real-time computational requirements of deterministic schemes increases with larger values of N_c , while the CLT ensures that the stochastic synthesis becomes more robust and less sensitive to variations of N_c when N_c is large, also without increasing the computational burden.

This can have some influence on the initial cost as well as on the maintenance of a MMC control architecture through its lifetime. However, it is important to underline the life cycle cost estimation of high-power installations (such as HVDC ones) is a rather complex matter involving decade-long business models where financing, profits, stocks, equities, assets depreciation, penalties for trips towards transmission system operators and service contracts must be considered. The component and commissioning cost of the control hardware is a minor fraction of the initial cost of the plant. For this reason, it is not straightforward to quantify the impact on the life-cycle cost of control solutions based on the proposed principle – nevertheless, it is interesting to observe that such methods could bring greater cabling simplicity, higher robustness and fault tolerance, which possibly translates into greater availability of the installation, lighter maintenance duties through its typical 30-years (or more) lifespan, hence lowering life-cycle costs for the customers.

2.3 Loss considerations on the proposed principle

The stochastic synthesis is performed at kT_s intervals, each independent from any other. The interval T_s might be interpreted as the equivalent period of carrier-based PWM schemes, and objections might arise regarding losses when T_s assumes relatively small values.

As a matter of fact, the method does not imply a greater number of commutations, because the more $p^*(t)$ is different from 1/2, the more likely any cell will remain in the same switching state of the preceding T_s interval. The likelihood of a commutation is maximum when $p^*(t) = 1/2$, but still the cells do not experience a commutation every T_s seconds [11].

Moreover, as regards to possible circulating currents among different arms of a MMC, it should be noted that the corrective actions can be commanded to the reference voltage, hence to the reference probability of the stochastic synthesis in the same way as it is usually done for deterministic carrier-based voltage syntheses.

On a larger system perspective and a broader technological horizon, it should also be considered that the continuous development of materials and production technologies brings to a steadily reduction of the component losses. In an imaginable future framework where the loss differences between different control solutions might be minimised and almost levelled out by the advances in materials science and technology, still, the question on how to reach a satisfactory robust, fault-tolerant

Fig. 3 Local controller in each j th cell

control of an increasingly complex modular system will remain a fundamental and very relevant aspect.

2.4 Generation of the random numbers

One of the key aspects of the stochastic voltage synthesis is the independent pseudo-random number generation inside each cell. Achieving a uniform pseudo-random sequence generation while keeping a low computational profile at the cell level is not straightforward. However, simple 32-bit integer-based generators can be found in literature [18], with a long-term behaviour which seems aligned for the need of this application. This class of random number generators have been successfully used in some electrical drives applications [19, 20]. In particular, Peretti *et al.* [20] discusses the schematic of the simplest uniform pseudo-random generator from [18], including an experimental validation of its uniform probability density. The same generator has been used in this work.

It is important to highlight that a uniform pseudo-random sequence is not strictly necessary, as the CLT is valid for other distributions too, provided that they are equal among the cells and independent from each other. An interesting path for future research activities may consider the exploitation of other distributions. Their evaluation should also consider the practical implementation in modern microprocessors/FPGAs, an aspect that classify the uniform distributions among the easiest solutions available.

2.5 Local alteration of the probability distribution

One of the main issues in the practical implementation of the stochastic synthesis is related to component non-linearities, tolerances and control inaccuracies due to digitalisation and rounding effects of integer variables. These effects could lead to diverging DC-link capacitor voltages, if no countermeasures are taken. The problem can be tackled by introducing a local controller in each cell [10], whose schematic is shown in Fig. 3.

The controller is based on a PI regulator, and it operates independently using only local information, therefore not violating the assumption of independent random variables which is required by the CLT. The PI regulation modifies the global reference probability $p^*(t)$ by processing the desired cell DC-link voltage v_c^* and its actual value $v_{c,j}$ and by multiplying its output by the sign of the arm current. The latter is essential to assess which state of the cell switches should be 'more probable' in order to dynamically minimise the voltage error. For example, for positive currents and positive DC-link voltage errors, it is beneficial to increase the probability of closing the switches T_1 and T_4 in Fig. 2, that is, increasing $p^*(t)$ towards 1.

The sum of $p^*(t)$ and the PI regulation output is subsequently limited in $[0, 1]$ and compared with the locally-generated random number, according to the rule (1). In probabilistic sense, it is 'more likely' that the switching events will lead to a bounded stochastic process for the cell DC-link voltage, with an expectation value equal to the desired DC-link voltage reference. However, the action of the PI regulation is kept within ± 0.07 while bounding the total corrected probability inside $[0, 1]$, in order not to modify excessively the intrinsic random distribution and independence of the output voltage cell.

3 Minimum capacitance requirements

Before continuing the analysis of the stochastic voltage synthesis, the minimum capacitance requirements for each cell are investigated. Section 3.1 analyses the conditions for ensuring a non-negative energy in the converter arm, independently from the adopted control structure, while Section 3.2 calculates the necessary conditions for synthesising the required arm voltage.

3.1 Limits for a non-negative energy in the arm

When the capacitance of all N_c cells in the arm is assumed linear and time invariant and equal to C_c , the total instantaneous energy in the arm is expressed by

$$\frac{C_c}{2} \sum_{j=1}^{N_c} v_{c,j}^2(t) = \int_{t_0}^t v_{\text{arm}}^*(\tau) \cdot i_{\text{arm}}^*(\tau) d\tau + \frac{C_c}{2} \sum_{j=1}^{N_c} v_{c,j}^2(t_0) \geq 0 \quad (5)$$

where $v_{c,j}(t)$ is the DC-link instantaneous voltage of the j th cell, v_{arm}^* and i_{arm}^* are the arm voltage reference and the arm current reference, respectively, while the integral represents the instantaneous energy variation from instant t_0 . The functions v_{arm}^* and i_{arm}^* are the desired references, assumed periodical in T , and chosen such that the average power entering the arm over T is zero. This is a necessary condition to ensure the boundness of all capacitor voltages within the arm. When no cell exchanges energy with any external source, this constraint must be always satisfied, otherwise the steady-state conversion would not be physically possible. From (5), the value of the minimum capacitance for a non-negative arm energy can be obtained

$$C_{c,\min} = \frac{-2 \left[\min_{\substack{t \in [t_0, t_0+T] \\ t_0 \in [0, T]}} \left(\int_{t_0}^t v_{\text{arm}}^*(\tau) \cdot i_{\text{arm}}^*(\tau) d\tau \right) \right]}{\sum_{j=1}^{N_c} v_{c,j}^2(t_0)} \quad (6)$$

In the special case where $v_{c,j}(t_0) = v_{\text{DC}}(t_0)$ for all cells, then $\sum_{j=1}^{N_c} v_{c,j}^2(t_0) = N_c v_{\text{DC}}^2(t_0)$. Equation (6) has general validity, since it is independent from any control strategy. It is worth highlighting that the minimum of the integral in (6) should be calculated for all possible values of t_0 within T , since the arm could be requested to start the synthesis at any instant. Moreover, the opposite of the term in square brackets visible in (6) represents the absolute minimum total energy that must be stored in the arm, which is depending exclusively on its desired operation as defined by the functions $v_{\text{arm}}^*(t)$, $i_{\text{arm}}^*(t)$. No arm operation would be possible if the design did not allow for at least the storage of such minimum energy.

3.2 Limits for the synthesis of a desired arm voltage

When the arm is composed by N_c series-connected cells, a necessary (yet not sufficient) condition for the minimum capacitance required for the synthesis of v_{arm}^* can be obtained when the following definitions are introduced

$$\begin{aligned} v_{\text{EXP}}(t) &\triangleq \frac{1}{N_c} \sum_{j=1}^{N_c} v_{c,j}(t) \\ \sigma v^2(t) &\triangleq \frac{1}{N_c} \sum_{j=1}^{N_c} [v_{c,j}(t) - v_{\text{EXP}}(t)]^2 \\ \Delta E(t, t_0) &\triangleq \int_{t_0}^t v_{\text{arm}}^*(\tau) \cdot i_{\text{arm}}^*(\tau) d\tau \end{aligned} \quad (7)$$

where v_{EXP} is the average cell voltage computed over the ensemble of all cells at the instant t and σv^2 is the mean quadratic error of the cell voltages with respect to v_{EXP} , again computed over the ensemble

of all cells at the instant t . The following expression holds

$$\frac{1}{N_c} \sum_{j=1}^{N_c} v_{c,j}^2(t) = v_{\text{EXP}}^2(t) + \sigma v^2(t) \quad (8)$$

The energy formula in (5) can therefore be transformed in

$$\underbrace{v_{\text{EXP}}^2(t)}_{\text{Dependent on the arm internal control strategy}} + \underbrace{\sigma v^2(t)}_{\text{Dependent on the arm internal control strategy}} = \frac{\overbrace{\frac{2}{C_c} \Delta E(t, t_0) + \sum_{j=1}^{N_c} v_{c,j}^2(t_0)}^{\text{Independent from any arm internal control strategy}}}{N_c} \quad (9)$$

where the following limit holds

$$\lim_{C_c \rightarrow +\infty} [v_{\text{EXP}}^2(t) + \sigma v^2(t)] = \frac{\sum_{j=1}^{N_c} v_{c,j}^2(t_0)}{N_c} \quad (10)$$

When the constraint $v_{c,j}(t) \geq 0$ holds (e.g. by the presence of a free-wheeling diode in conventional voltage-source H-bridge cells), a necessary (yet not sufficient) condition for the synthesis of $v_{\text{arm}}^*(t)$ is the following

$$\sum_{j=1}^{N_c} v_{c,j}(t) \geq |v_{\text{arm}}^*(t)| \quad (11)$$

where the absolute value indicates that the H-bridge cells can synthesise voltages of both signs. The condition (11) is not sufficient, because even with enough DC-link voltage available in each cell, the internal control strategy of the arm might not be able, or could not afford, to exploit it well. In some instants, priority might be given to correct capacitor voltages which are close to their maximum limits, or to reduce the number of commutations. Having non-negative terms on both sides, (11) can be squared, and by substituting the first of (7) it follows

$$v_{\text{EXP}}^2(t) \geq \frac{|v_{\text{arm}}^*(t)|^2}{N_c^2} \quad (12)$$

Equation (12) can be used in (9) to derive (13), where $C_{c,\text{synth}}$ is the minimum required capacitance.

$$1 + \frac{\Delta E(t, t_0)}{(C_{c,\text{synth}}/2) \sum_{j=1}^{N_c} v_{c,j}^2(t_0)} \geq \frac{|v_{\text{arm}}^*(t)|^2}{N_c \sum_{j=1}^{N_c} v_{c,j}^2(t_0)} + \frac{N_c \sigma v^2(t)}{\sum_{j=1}^{N_c} v_{c,j}^2(t_0)} \quad (13)$$

For the special case $v_{c,j}(t_0) = v_{\text{DC}}(t_0) \forall j$, the inequality becomes

$$1 + \frac{\Delta E(t, t_0)}{\left(\frac{C_{c,\text{synth}}}{2} N_c v_{\text{DC}}^2(t_0) \right)} \geq \left[\frac{|v_{\text{arm}}^*(t)|}{N_c v_{\text{DC}}(t_0)} \right]^2 + \frac{\sigma v^2(t)}{\underbrace{v_{\text{DC}}^2(t_0)}_{\text{RelVarCells}(t)}} \quad (14)$$

If $C_{c,\text{synth}}$ is given, (14) can be used to determine the achievable total arm voltage, although such a voltage could not be guaranteed because (14) remains a necessary condition.

No assumption on the internal control strategy of the series-connected cells was introduced up to this point. However, an analysis of (14) can lead to some considerations related to the control strategy. The left-hand side of (14) is dependent only on N_c , $C_{c,\text{synth}}$ and the desired operating conditions at the arm

terminals, but not on its control strategy. Conversely, the right-hand side is dependent on the control strategy via the variance σv^2 , which then influences $v_{\text{EXP}}(t)$ through (9). This simple analysis reveals the existence of two fundamental families of design philosophies and arm control strategies:

- family A: strategies which pose significant effort in reducing as much as possible the ‘voltage spread’ $\sigma v^2(t)$ with a limited number of cells N_c and an optimal capacitance C_c . These strategies focus on reducing the oscillations in the left-hand side of (14) under the ideal target of becoming closer to the limit (10), possibly with further reduced $\sigma v^2(t)$ as a consequence of an optimal C_c . The strategies belonging to this family [6, 21–23] emphasise the balancing of the capacitor voltages as its effect is the reduction of $\sigma v^2(t)$. It is important to recall that the balancing of the capacitor voltages should not be interpreted as forcing all $v_{c,j}(t)$ voltages to be as close as possible to $v_{\text{DC}}(t_0)$ at any instant, but that all capacitors should equally share the evolution of the total energy contained in the arm as determined by the combination of $v_{\text{arm}}^*(t)$, $i_{\text{arm}}^*(t)$ and $v_{\text{DC}}(t_0)$. A good balancing means a reduction of $\sigma v^2(t)$ so that all capacitor voltages can become as close as possible to $v_{\text{EXP}}(t)$.
- family B: strategies which choose to allow a priori a significant ‘spread’ of capacitor voltages around $v_{\text{EXP}}(t)$ – caused also by a possibly smaller C_c – and compensate for the greater local variability by using a large number of cells N_c . Owing to the inverse-squared dependence on N_c in the right-hand side of (14), these strategies focus on reducing the term $\text{FracCells}^2(t)$ while leaving more possible oscillations in the left-hand side of (14). Since (14) must be satisfied as a necessary condition, the oscillations on the left-hand side term must have a minima not lower than the maxima of the oscillations on the right-hand side term, which are mainly caused by $\sigma v^2(t)$. The strategies belonging to this family do not emphasise the balancing of the capacitor voltages, considering the instantaneous sharing of the total arm energy among capacitors as a second priority, but nevertheless pursuing the long-term sharing of the total arm energy, avoiding improper arm operation. Greater importance is given to possibly smaller capacitance, less need of strongly deterministic control, simpler/cheaper control architectures and better fault tolerance through higher redundancy. As further observation, it should be also noted that the CLT does not rule $\sigma v^2(t)$, since it applies only to the variance of the sum of all cell voltages. The stochastic synthesis proposed in this paper and in [10, 11] falls within this second family of strategies.

4 Application to a realistic case

This section analyses a case study of stochastic synthesis for an arm with realistic parameters considering the technological state of the art. Details about the configuration can also be found in [10]. A conventional reference pair $\{v_{\text{arm}}^*(t), i_{\text{arm}}^*(t)\}$ for a high-power MMC converter for grid applications (such as HVDCs) is assumed, and it is expressed by the following relationships, where the third one imposes the necessary condition for zero average power entering the arm

$$\begin{cases} i_{\text{arm}}^*(t) = I_{\text{arm,DC}}^* + I_{\text{arm,AC}}^* \sin(\omega t) \\ v_{\text{arm}}^*(t) = V_{\text{arm,DC}}^* + V_{\text{arm,AC}}^* \sin(\omega t + \gamma) \\ \cos(\gamma) = -\frac{2V_{\text{arm,DC}}^* I_{\text{arm,DC}}^*}{V_{\text{arm,AC}}^* I_{\text{arm,AC}}^*} \end{cases} \quad (15)$$

Each cell has the full H-bridge structure of Fig. 2, where the switches are realised with a controllable device and a free-wheeling diode in parallel. With a non-negative capacitor voltage constraint, the cell allows the synthesis of voltages with both polarities at the cell output terminals. It is very important to underline that both $i_{\text{arm}}^*(t)$ and $v_{\text{arm}}^*(t)$ in (15) possess non-zero DC components $I_{\text{arm,DC}}^*$ and $V_{\text{arm,DC}}^*$. The parameters used for the case study are: $\omega = 2\pi 50$ rad/s, $I_{\text{arm,DC}}^* = -130$ A, $I_{\text{arm,AC}}^* = 466$ A, $V_{\text{arm,DC}}^* = 320$ kV and $V_{\text{arm,AC}}^* = 400$ kV, which leads to $\gamma = 1.10$ rad in order to ensure the required zero average power entering the arm. Respecting this

Fig. 4 Surfaces of the left-hand side of (14) and the first term of the right-hand side of (14) with $N_c = 512$ and $C_{c,min} = 0.78$ mF. Their intersection demonstrates that the capacitance is largely insufficient for the synthesis of the desired $v_{arm}^*(t)$

condition during the arm actual operation is a responsibility of the internal arm control. Still, if the reference values did not already satisfy this requirement *a priori*, no meaningful operation of the arm would be possible.

The number of cells N_c is maintained at the value of 512, while the initial value $v_{c,j}(t_0)$ of all DC-link voltages is chosen equal to 2133 V, a conventional value for present switches characterised by 4.5 kV breakdown voltage [10]. 2133 V is also the value of v_c^* in the local controller of Fig. 3. With the chosen system parameters, the absolute minimum capacitance $C_{c,min}$ from (6) is equal to 0.78 mF, hence no operation of the arm with the desired pair $\{v_{arm}^*(t), v_{arm}^*(t)\}$ is physically possible for cell capacitances below this value.

As regards to the voltage synthesis condition, Fig. 4 shows the relation between the left-hand side of the inequality (14) and the first term $FracCells(t)^2$ in the right-hand side of the same inequality. Both expressions are considered functions of two independent variables t and t_0 ranging in $[0, T]$. With $N_c = 512$ cells and $C_{c,min} = 0.78$ mF, the surface representing the left-hand side of (14) goes significantly below the surface representing the first term of the right-hand side. This means that even in the ideal case of $\sigma v^2(t) = 0$ the value $C_{c,min} = 0.78$ mF would be insufficient for synthesising $v_{arm}^*(t)$ at all-time instants.

Conversely, when the cell capacitance is increased to 1.48 mF the synthesis of $v_{arm}^*(t)$ may become possible, also for a non-negligible variance $\sigma v^2(t)$. The proof is given in Fig. 5, which shows the same two surfaces for $C_c = 1.48$ mF. In this case, the left-hand side of (14) remains significantly greater than the first term of the right-hand side of the same inequality for all pairs (t, t_0) .

As a counter-example, Fig. 6 shows the case of $N_c = 700$ with $C_c = 0.78$ mF, which is a choice belonging to the second family of

Fig. 5 Surfaces of the left-hand side of (14) and the first term of the right-hand side of (14) with $N_c = 512$ and $C_c = 1.48$ mF. The surface of the left hand side of (14) is entirely above that of $Frac Cells(t)$ squared, thereby indicating that the capacitance might be sufficient for the synthesis of the desired $v_{arm}^*(t)$

Fig. 6 Surfaces of the left-hand side of (14) and the first term of the right-hand side of (14) with $N_c = 700$ and $C_c = 0.78$ mF. The surface of the left hand side of (14) is entirely above that of $Frac Cells(t)$ squared, therefore indicating that the increase of N_c may allow the synthesis of the desired $v_{arm}^*(t)$

strategies described in the last part of Section 3. In this case, the synthesis might be possible. The two aforementioned surfaces remain apart due to the large increase of N_c which affects more the right-hand side of (14) than its left-hand side. Indeed, with $N_c = 700$ and all other parameters kept identical, (6) returns a minimum capacitance of $C_{c,min} = 0.53$ mF.

Fig. 7 shows another example where a choice towards the first family of strategies is assumed. Here $N_c = 400$ cells and $C_c = 10$ mF are chosen, that is, larger capacitances are privileged over a larger number of cells. The effect of a larger C_c is to flatten significantly the left-hand side of (14), whereas the first term of the right-hand side assumes even greater values due to the reduction of N_c . With this design choice, (6) returns $C_{c,min} = 1$ mF.

It is worth observing that, for a given $v_{DC}(t_0)$, the stored energy in the arm at t_0 is linear both with N_c and with C_c . Conversely, when it comes to the synthesis capability, N_c shows greater influence because it scales the first term in the right-hand side of (14) with $1/N_c^2$, whereas C_c scales the left-hand side of (14) with $1/C_c$ only. Therefore, in principle (and without considering other real implications related to the technological state of the art) with the same $v_{DC}(t_0)$, an increase of N_c instead of C_c has potentials that should not be underestimated in terms of synthesis.

Although (14) might seem trivial (i.e. for better voltage synthesis, an increase of the number of cells is required), the message it sends is broader. It reveals that an increased number of cells, each one characterised by lower capacitance, may open another way of performing the voltage synthesis. This is based on a greater system dimensionality that spreads the energy over a large number of cheaper, simpler and more loosely controlled subsystems. It is different from the most intuitive attempt to instantaneously balance the DC-link voltages, as long as the second term of the right-hand side of (14) is kept to reasonable levels. In this perspective, the CLT in combination to the large arm dimensionality is a helping hand, by exploiting the cells as an energy storage with more degrees of freedom.

Fig. 7 Surfaces of the left-hand side of (14) and the first term of the right-hand side of (14) with $N_c = 400$ and $C_c = 10$ mF. The surface of the left hand side of (14) is entirely above that of $Frac Cells(t)$ squared due to the increase of C_c

Fig. 8 HIL setup OPAL-RT OP5600 real-time system and a Yokogawa DL750 oscilloscope / recorder

5 Results from the HIL implementations

5.1 Implementation of the stochastic voltage synthesis

A real-time verification of the case in Section 4, with $N_c = 512$ and $C_c = 1.48$ mF, was performed on an OPAL-RT OP5600 system, composed by a 2.4-GHz 4-cores processor and a Virtex 6 FPGA. The series of cells as in Fig. 1 were implemented along with the random number generation and the local PI regulation, and the significant signals were routed on the analogue output board of the system with an update rate of $1 \mu\text{s}$. The signals were recorded at $50 \mu\text{s}$ rate for a total of 50 s, by using a Yokogawa DL750 digital oscilloscope. A picture of the HIL setup is shown in Fig. 8.

The values of v_{arm}^* and i_{arm}^* were the same as those reported in Section 4. The discrete sample time of the stochastic synthesis (i.e. of the random number generation) was set to $250 \mu\text{s}$. The local controller parameters in Fig. 3 were set to $K_p = 7 \cdot 10^{-5}$ and $K_i = 1.4 \cdot 10^{-3}$. The reference probability signal was sent identical to all cells, according to (4). For this particular value of v_{arm}^* , the reference probability $p^*(t)$ ranged in the interval $[0.170, 0.830]$.

Fig. 9 reports the most relevant quantities measured from the system. Fig. 9a shows the trace of the arm current $i_{\text{arm}}^*(t)$. Fig. 9b shows the desired reference $v_{\text{arm}}^*(t)$ together with the stochastically-synthesised actual voltage, which follows the reference very well. Fig. 9c the total instantaneous power entering the arm, together with its moving average. Its value proves that the action of the internal controllers inside each cell is capable of respecting the required condition of a zero average power entering the arm. The same graph shows a dashed horizontal line representing the product $v_{\text{arm,DC}}^* \cdot i_{\text{arm,DC}}^*$. Finally, Fig. 9d depicts two selected DC-link capacitor voltages of two cells within a magnified time interval towards the end of the run. In order to explore two distant positions in the arm, the 20th and the 380th cell have been chosen.

Fig. 9 HIL results of the stochastic synthesis with $N_c = 512$ cells and $C_c = 1.48$ mF

- a i_{arm}^*
- b v_{arm}^* and v_{arm}
- c Total instantaneous power entering the arm with its moving average and the product $V_{\text{arm,DC}}^* \cdot I_{\text{arm,DC}}^*$
- d DC-link capacitor voltages of the 20th cell and the 380th cell

Fig. 10 HIL DC-link voltages of the 20th cell and the 380th cell under stochastic synthesis with $N_c = 512$ cells and $C_c = 1.48$ mF

a Complete time window
b Zoomed time window

Fig. 10 details the DC-link voltages of the 20th and the 380th cell over the whole interval of 50 s, as well as a magnified sub-interval where their deviation from 2133 V is particularly significant. Large variations of the DC-link voltages with respect to the reference $v_{c,j}^* = 2133$ V are observed, but still the voltages do not diverge. Despite of the individual large excursions of all DC-link voltages, owing to the CLT the stochastically-synthesised total arm voltage is well following the given reference with limited variance.

In another test, the system was reprogrammed with larger capacitor voltages for all cells, by setting $C_c = 7.8$ mF which corresponds to 10 times the minimum capacitance $C_{c,min}$ obtained from (6). Figs. 11 and 12 present the results in the same form of Figs. 9 and 10. As expected, the DC-link voltages exhibit a reduced deviation with respect to $v_{c,j}^* = 2133$ V. Still, the

stochastically-synthesised voltage is not comparatively better than the one obtained for the case $C_c = 1.48$ mF. This result is coherent with the considerations reported at the end of Section 3 applied to the stochastic synthesis approaches, which choose to synthesise waveforms by relying more on a higher number of loosely-controlled contributions rather than fewer, more accurate ones.

5.2 Comparative analysis with a deterministic voltage synthesis

For the sake of comparative investigation, additional HIL results have been included considering the implementation of a traditional deterministic synthesis based on regular-sampled PWM, in the

Fig. 11 HIL results of the stochastic synthesis with $N_c = 512$ cells and $C_c = 7.4$ mF

a i_{arm}
b v_{arm}^* and v_{arm}
c Total instantaneous power entering the arm with its moving average and the product $V_{arm,DC}^* \cdot I_{arm,DC}^*$
d DC-link capacitor voltages of the 20th cell and the 380th cell

Fig. 12 HIL DC-link voltages of the 20th cell and the 380th cell under stochastic synthesis with $N_c = 512$ cells and $C_c = 7.4$ mF
a Complete time window
b Zoomed time window

same operating conditions as the ones of Section 5.1. The multi-level modulation scheme is the conventional one using N_c symmetrical triangular carriers, shifted by $1/N_c$ -th of the fundamental period and characterised by a pulse number of 3.37 with respect to the fundamental frequency of the reference voltage [4]. Each cell is modulated according to a shifted carrier, and it also contains a local PI controller similar to the one shown in Fig. 3, which slightly modifies the PWM switching instants with the aim of improving the balance between the DC-link voltages of the different cells. This modulation and balancing choice is among the simplest ones within the class of deterministic syntheses for a MMC arm [24]. Willingly, no sorting algorithm of the DC-link voltages has been implemented in order to render the deterministic method as comparable as possible with the straightforward implementation of the stochastic synthesis.

The results for $N_c = 512$ cells and $C_c = 1.48$ mF, as well as those for $N_c = 512$ cells and $C_c = 7.4$ mF, are reported in Figs. 13, 14 and 15, respectively. Table 1 summarises the most important indexes of the different modulations.

It should be noted that the arm reference voltage has a third harmonic superimposed to its fundamental, and therefore the THD of the arm reference voltage is already equal to 11.79%. It must be also highlighted that with the stochastic synthesis, all waveforms are stochastic processes and therefore typical figures of merit such as THD, RMS and voltage ripple must be interpreted within the probabilistic context of the stochastic process theory. Their evaluation, which is often based on the expectation of functional operators over the stochastic processes, must be performed over ensembles of process realisations. In the case of ergodic processes (a common practical assumption), the expectation can be

Fig. 13 HIL results of the deterministic synthesis with $N_c = 512$ cells and $C_c = 1.48$ mF
a i_{arm}
b v_{arm}^* and v_{arm}
c Total instantaneous power entering the arm with its moving average and the product $V_{arm,DC}^* \cdot I_{arm,DC}^*$
d DC-link capacitor voltages of the 20th cell and the 380th cell

Fig. 14 HIL results of the deterministic synthesis with $N_c = 512$ cells and $C_c = 7.4$ mF

- a i_{arm}
b v_{arm}^* and v_{arm}
c Total instantaneous power entering the arm with its moving average and the product $V_{arm,DC}^* \cdot I_{arm,DC}^*$
d DC-link capacitor voltages of the 20th cell and the 380th cell

Fig. 15 FFT of v_{arm} with $N_c = 512$ cells

- a Stochastic method, $C_c = 1.48$ mF
b Deterministic method, $C_c = 1.48$ mF
c Stochastic method, $C_c = 7.4$ mF
d Deterministic method, $C_c = 7.4$ mF

Table 1 Stochastic vs. deterministic synthesis comparison (THD of the reference voltage = 11.79%)

	Arm voltage THD, %	DC voltage ripple 20th cell	DC voltage ripple 380th cell
stochastic synthesis, $C_c = 1.48$ mF	17.18	655 V_{rms}	654 V_{rms}
deterministic synthesis, $C_c = 1.48$ mF	17.84	320 V_{rms}	320 V_{rms}
stochastic synthesis, $C_c = 7.4$ mF	16.33	282 V_{rms}	271 V_{rms}
deterministic synthesis, $C_c = 7.4$ mF	9.29	61 V_{rms}	62 V_{rms}

approximated with a time average over a long time window. Nevertheless, the analysis leads to the following considerations:

- The THD of the simple deterministic synthesis with $C_c = 1.48$ mF seems worse than the stochastic one, although better in terms of DC-link voltage variation.
- The simple deterministic synthesis with $C_c = 7.4$ mF is not markedly better than the stochastic one in terms of THD, still deforming the reference voltage.
- Although the stochastic synthesis benefits of a reduced DC-link voltage ripple by a larger capacitance value, the THD of the stochastically-synthesised total arm voltage remains approximately the same of the case with smaller capacitance. Indeed, this is an indication that the voltage deformation is tightly related to the arm energy variation caused by the change of the current and the voltage at its terminals, and to the total number of cells acting in the arm. The stochastic modulation does not 'entangle' the voltage dynamic evolution, as in the deterministic control schemes.
- From an implementation point of view, the stochastic synthesis requires a random number generation and a switching decision at each T_s interval, where T_s values are in the order of hundreds of microseconds. Conversely, the deterministic synthesis requires the implementation of a rising/falling carrier signal, which must sweep the entire PWM period with a finer time base. As a consequence, the stochastic synthesis requirements on the control hardware are relaxed.

6 Conclusions

The paper has presented an unconventional stochastic approach to the synthesis of the arm voltage in modular voltage-source multi-level converters targeted for high-power HVDC and FACTS applications. The presented approach is carrier-less, eliminating the critical structuralism of switching patterns sent through several command lines to the switches, therefore increasing tolerance against cells failures and reducing the cost for the control architecture. Moreover, as a natural consequence of the CLT, the greater the number of cells, the more robust the voltage synthesis algorithm becomes. In addition, there is no need of reconfiguring any deterministic modulation pattern in case of cell failures. This is a key difference compared with the typical deterministic carrier-based syntheses, where complexity and reliability issues increases with greater system modularity, because of the required determinism.

A section was devoted to the analysis of the physical assumptions for applying the method to MMC arms structured as the series connection of cells without any external energy supply. Two large families of arm control strategies were discussed: the conventional deterministic ones and the proposed stochastic ones. The latter ones seem to allow the use of cells with lower capacitance values, thereby further improving the fault tolerance of the converter because less energy is stored in the single cell, hence released in case of cell failure.

The HIL validation of the proposed strategy has been performed and compared with a conventional deterministic strategy, confirming the potential of the approach in realistic operating

conditions. The tests have confirmed that the capacitor voltages are bounded even under complete random operation of the cells, while a correct synthesis of the reference arm voltage is obtained. Applications of the method to a multi-stage MMC converter as well as a variant of the synthesis algorithm, conceived for a reduced number of cells, can be found in [10, 11].

7 References

- 1 Marquardt, R.: 'Modular multilevel converter: an universal concept for HVDC-networks and extended DC-bus-applications'. Proc. of the Int. Power Electronics Conf. (IPEC 2012), Sapporo, Japan, 21–24 June 2010, pp. 502–507
- 2 Glinka, M., Marquardt, R.: 'A new AC/AC multilevel converter family', *IEEE Trans. Ind. Electron.*, 2005, **52**, (3), pp. 662–669
- 3 Allebrod, S., Hamerski, R., Marquardt, R.: 'New transformerless, scalable modular multilevel converters for HVDC-transmission'. Proc. 39th Power Electronics Specialists Conf. (PESC 2008), Rhodes, Greece, 15–19 June 2008, pp. 174–179
- 4 Jacobson, B., Karlsson, P., Asplund, G., *et al.*: 'VSC-HVDC transmission with cascaded two-level converters'. Proc. of Cigré 2010, Paris, France, 22–27 August 2010, vol. B4, (110)
- 5 Adam, G.P., Anaya-Lara, O., Burt, G.M., *et al.*: 'Modular multilevel inverter: pulse width modulation and capacitor balancing technique', *IET Power Electr.*, 2010, **3**, (5), pp. 702–715
- 6 Zhang, Y., Adam, G.P., Lim, T.C., *et al.*: 'Analysis of modular multilevel converter capacitor voltage balancing based on phase voltage redundant states', *IET Power Electr.*, 2012, **5**, (6), pp. 726–738
- 7 Nademi, H., Norum, L.: 'Analytical circuit oriented modelling and performance assessment of modular multilevel converter', *IET Power Electr.*, 2015, **8**, (9), pp. 1625–1635
- 8 Kirby, N.M., MacLeod, N.M., Stidham, D., *et al.*: 'Tres Amigas: A flexible gateway for renewable energy exchange between the three asynchronous AC networks in the USA'. Proc. of Cigré 2012, Paris, France, 26–31 August 2012, vol. B4, (309)
- 9 Tenca, P.: 'Theoretical and practical aspects characterizing the research on multilevel converters'. Proc. European Center for Power Electronics (ECPE) Workshop on Advanced Multilevel Converter Systems, Västerås, Sweden, 28–29 September 2010
- 10 Tenca, P.: 'Stochastic waveform synthesis for multilevel converters via the central limit theorem of the theory of probability'. Ireland Research disclosure 586 020, 9 January 2013. Available at <http://www.researchdisclosure.com>
- 11 Tenca, P., Peretti, L.: 'Fault tolerant cost-effective carrierless stochastic synthesis of voltages and currents in multi-cell multilevel converters via the central limit theorem'. Proc. of the Energy Conversion Congress and Exposition (ECCE), Denver, Colorado, USA, 15–19 September 2013, pp. 1732–1739
- 12 Gnedenko, B.V.: 'The theory of probability' (Chelsea Publishing, New York, 1966)
- 13 Boys, J.T.: 'Theoretical spectra for narrow-band random PWM waveforms', *IEE El. Power Appl. Proc. B*, 2002, **140**, (6), pp. 393–400
- 14 Stankovic, A., Verghese, G., Perreault, D.: 'Analysis and synthesis of randomized modulation schemes for power converters', *IEEE Trans. Power Electron.*, 1995, **10**, (6), pp. 680–693
- 15 Stankovic, A., Verghese, G., Perreault, D.: 'Randomized modulation of power converters via Markov chains', *IEEE Trans. Control Syst. Technol.*, 1996, **5**, (1), pp. 61–73
- 16 George, D.S., Baiju, M.R.: 'Space vector based random pulse width modulation scheme for a 3-level inverter in open-end winding induction motor configuration'. Proc. of the Int. Symp. on Industrial Electronics (ISIE 2012), Hangzhou, China, 28–31 May 2012, pp. 742–747
- 17 Liang, J., Nami, A., Dijkhuizen, F., *et al.*: 'Current source modular multilevel converter for HVDC and FACTS'. Proc. 15th European Conf. on IPower Electronics and Applications (EPE 2013), Lille, France, 3–5 September 2013, pp. 1–10
- 18 Marsaglia, G.: 'Yet another RNG. Posted on sci.stat.math, 1 August 1994. Available at <https://groups.google.com/forum/#!topic/sci.stat.math/p7aLW3TsJys>
- 19 Bolognani, S., Peretti, L., Zigliotto, M.: 'Online MTPA control strategy for DTC synchronous-reluctance-motor drives', *IEEE Trans. Power Electron.*, 2011, **26**, (1), pp. 20–28
- 20 Peretti, L., Särkimäki, V., Fabér, J.: 'A wind turbine emulator for generator control algorithm development'. Proc. Int. Conf. on Industrial Technology (ICIT), Cape Town, South Africa, 25–27 February 2013, pp. 228–233
- 21 Zhang, Y., Adam, G., Finney, S., *et al.*: 'Improved pulse-width modulation and capacitor voltage-balancing strategy for a scalable hybrid cascaded multilevel converter', *IET Power Electr.*, 2013, **6**, (4), pp. 783–797
- 22 Merlin, M.M.C., Green, T.C.: 'Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter', *IET Power Electr.*, 2015, **8**, (3), pp. 350–360
- 23 Konstantinou, G., Ciobotaru, M., Agelidis, V.: 'Selective harmonic elimination pulse-width modulation of modular multilevel converters', *IET Power Electr.*, 2013, **6**, (1), pp. 96–107
- 24 Xiaojian, L., Qiang, S., Jianguo, L., *et al.*: 'Capacitor voltage balancing control based on CPS-PWM of modular multilevel converter'. Proc. Energy Conversion Congress and Exposition (ECCE), Phoenix, AZ, USA, 17–22 September 2011, pp. 4029–4034