Advanced Test Circuit for DC Circuit Breakers

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Keywords

≪HVDC≫, ≪Multiterminal HVDC≫, ≪Power transmission≫, ≪Fault handling strategy≫, ≪Test bench≫

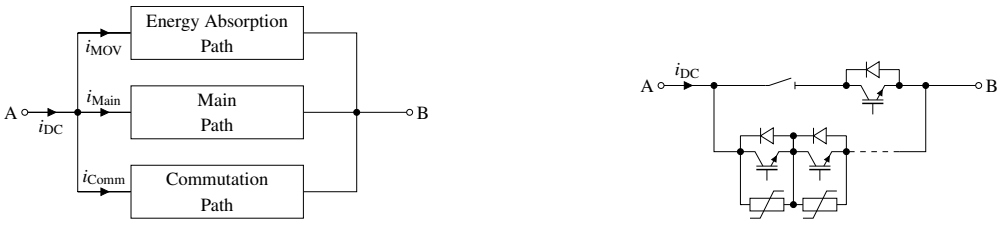
Abstract

In future HVDC systems, many DC circuit breakers (DCCBs) will be required. In this paper, an advanced test circuit for DCCBs is described. A DC source is combined with a capacitor bank. In contrast to other test circuits, the proposed test circuit allows to replicate constant DC and temporary faults. In addition to conventional faults, this enables testing of auto-reclosing, proactive commutation, and complex test sequences combining all of these modes. The test circuit is easy to setup and also suitable for smaller research facilities. Experimental results from a down-scaled mock-up are included to demonstrate the capabilities of the test circuit.

Introduction

Direct current circuit breakers (DCCBs) will play an important role in future high-voltage direct current (HVDC) systems with non-fault-blocking voltage source converters (VSCs) to handle DC line faults. DCCBs are needed in meshed HVDC grids to ensure safe grid operation [1]. Even in HVDC point-to-point links DCCBs are advantageous, as the stress on the converter during a DC line fault is reduced and VSCs can provide reactive power to the AC grids again after fault separation [2]. In case overhead lines are used, temporary faults may occur and DCCBs with auto-reclosing capability are a viable solution [3].

Several DCCB concepts for HVDC have been proposed [4–8]. In general, DCCBs have a structure as shown in Fig. 1a with a main path, a commutation path, and an energy absorption path. DCCBs can be grouped into mechanical switches with current injection and hybrid DCCBs. Mechanical switches with current injection use additional circuitry to inject a current into the arcing mechanical switch to create a current zero crossing [4, 7]. Hybrid DCCBs combine mechanical switches or disconnectors with power electronics to interrupt DC [5,6,8]. Many hybrid DCCBs such as ABB's concept shown in Fig. 1b feature proactive commutation. Proactive commutation means that the DCCB internally starts its interruption sequence before the DCCB actually receives a trip signal. Proactive commutation may compensate for fault detection delays and provide fast back-up protection in case of DCCB failure in an HVDC grid. If the DCCB does not receive a trip signal, proactive commutation is aborted and the DCCB changes to normal operation again. A current limiting inductor may be connected in series with the DCCB to limit the rate of rise of the fault current. The fault current would have a triangular shape independent of the



(a) General structure of DCCB

(b) ABB hybrid DCCB

Fig. 1: Illustration of DCCB concepts

DCCB concept in case of a DC line fault in a system with a large current limiting inductor, a stiff direct voltage source, and successful insertion of the metal-oxide varistor (MOV) [9].

In conventional DCCB test circuits, a pre-charged capacitor bank is discharged through an inductor into the DCCB to yield an approximately triangular fault current shape. In [6], a second pre-charged capacitor bank with an additional large inductor is discharged prior to the other capacitor bank to provide a current with low oscillation frequency mimicking a steady-state current. In [10], the use of short-circuit generators to provide the fault current is explained. If a low-voltage capacitor is used to provide the fault current, an additional charging circuit with higher voltage may be necessary for DCCBs with pre-charged capacitors [7]. In [11], a free-wheeling diode is placed in parallel to the low-voltage capacitor bank to protect the polarized capacitors from voltage reversal.

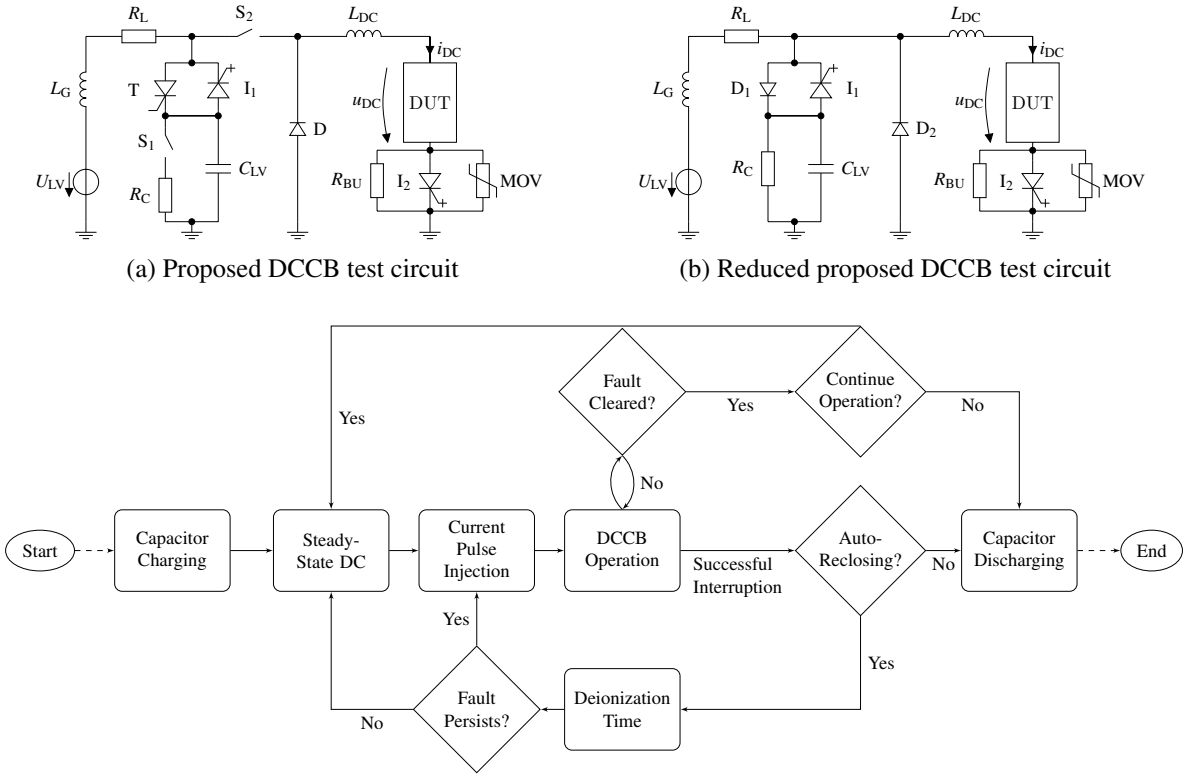
However, the fault current in a realistic HVDC system will never be perfectly triangular. Travelling waves have a strong influence on the fault current shape [12]. Furthermore, if a relatively small current limiting inductor is used as in conventional VSC-HVDC point-to-point links, the fault current shape is not triangular anymore at all as shown in [2]. The dimensioning and fault behavior of the VSC and its time of blocking, fault type, fault distance, transmission line characteristics, and the strength of the connected AC grids influence the fault current. The above-mentioned test circuits allow to evaluate the operation of a DCCB, but elaborate test circuits have to be used to give a more realistic picture. The operation modes auto-reclosing and proactive tripping have not been presented in tests yet. Four interesting test circuits have been described in [13–16]. In [13], a double pulse test circuit for semiconductor switches has been described where the low-voltage and high-voltage side are separated similar to a Weil-Dobke test circuit for AC circuit breakers. In [14], three parallel buck converters are used each with a pre-charged capacitor and a variable inductor. By controlling the buck converters, it is possible to generate complex fault current shapes. In [15], a test circuit is proposed where the capacitor bank for the fault current is charged from a rectified three-phase alternating voltage. This makes it possible to recharge the capacitor bank fast after an interruption sequence which allows testing of auto-reclosing. In [16], a controller for a flexible current source is proposed that switches between PI and tolerance band control to allow for fast dynamics.

In this paper, a DCCB test circuit for testing of down-scaled laboratory prototype DCCBs is proposed. The test circuit resolves several limitations of common test circuits by including a DC source. In addition to faults, the proposed DCCB test circuit allows to replicate load current interruption, temporary faults, and auto-reclosing. The paper is structured as follows: In Section *Concept*, the proposed DCCB test circuit is explained. In Section *Experimental Setup*, the planned experimental setup and a down-scaled mock-up test circuit are described. In Section *Results & Discussion*, experimental results from the down-scaled mock-up with a hybrid DCCB are shown. In Section *Conclusion*, all findings are summarized.

Concept

The schematic diagram of the DCCB test circuit is shown in Fig. 2a. In Fig. 2c, the flowchart of the corresponding test sequences is depicted.

In the state *Capacitor Charging*, the capacitor C_{LV} is charged from the direct voltage source U_{LV} with stray inductance L_G by firing the thyristor T. The charging time is determined by C_{LV} and the load



(a) Proposed DCCB test circuit

(b) Reduced proposed DCCB test circuit

(c) Flowchart of operation sequence

Fig. 2: Illustration of proposed DCCB test circuits

resistor R_L. If C_{LV} is charged up to the desired voltage level set by U_{LV} and the thyristors have recovered, operation is continued. In the state *Steady-State DC*, the contactor S_2 is closed while the IGCT I_2 is in the on-state to short R_{BU} and MOV. The IGCT I_1 is in the off-state to prohibit current injection from C_{LV}. U_{LV} builds up a current i_{DC} through the device under test (DUT). R_L limits i_{DC}. This phase corresponds to the steady-state DC stress of the DUT.

To impose the fault current in the state *Current Pulse Injection*, C_{LV} is discharged into the DUT by switching on I_1. The DUT has its own independent control logic which can trip the DUT at a set current level in the state *DCCB Operation*. Two modes have been implemented for testing. Firstly, it is possible that i_{DC} increases until the DUT interrupts i_{DC} and the decision state *Auto-Reclosing?* is entered. Secondly, a temporary overcurrent mode equivalent to a fault with short duration has been implemented, where I_1 and I_2 are turned off before the tripping level of the DUT is reached if yes is entered in the decision state *Fault Cleared?*. The test currents decrease due to the voltage inserted by MOV. Diode D is needed to provide a free-wheeling path. Afterwards, normal steady-state operation is resumed and the state *Steady-State DC* is entered again. This allows to test whether the proactive commutation mode, if the DUT supports it, works. After both testing variants, the test sequence may be continued.

In case of successful current interruption, the DUT can be reclosed after a set time corresponding to the deionization time of an arc fault in the state *Deionization Time*. During this time, C_{LV} is recharged. In case that C_{LV} has been completely discharged, the minimal deionization time is determined by R_L and C_{LV}. In the decision state *Fault Persists?*, it is decided whether i_{DC} rises again or steady-state operation is resumed. In case of a persisting fault, the state *Current Pulse Injection* is entered again, I_1 is turned on, C_{LV} discharges into the DUT and the above-described sequence is repeated. As the heat dissipation in C_{LV}, due to its ESR, and R_L must be limited, reclosing attempts are limited (once in the KTH laboratory).

Apart from the depicted test circuits and described sequence, several features have to be implemented to guarantee safety. The contactor S_1 connects the resistor R_C to C_{LV} to discharge it after the test. The setup should be caged and grounding switches, an electric door lock, a warning lamp, and an emergency

Table I: Parameters of planned DCCB test circuit and down-scaled mock-up DCCB test circuit

Circuit	I_{DC}/A	I_F/A	U_{LV}/kV	U_{HV}/kV	L_{DC}/mH	C_{LV}/mF	R_C/kΩ	R_L/Ω	R_{BU}/Ω
Planned	150	1400	0.5	12	1.8	13	20	3.33	3.33
Mock-up	10	100	0.25	0.6	10.2	6.6	15.5	16.6	91.6

button should be used for safety. It has to be mentioned that I_2 and MOV are essentially a solid-state DCCB which apart from the temporary fault mode also provides an additional level of safety. If the maximum test current is surpassed, the back-up solid-state DCCB interrupts. The resistor R_{BU} has been added to ensure that U_{LV} appears across the DUT when it is non-conductive. Furthermore, R_{BU} can be used to test whether the DUT still manages to interrupt if its lower terminal is not at ground potential. It is possible to arrange the test circuit differently to reduce the component count while still maintaining the same functionality, see the example in Fig. 2b.

Experimental Setup

The planned experimental setup and the down-scaled mock-up that has been used in the experiments for this work are explained in this section. All parameters are summarized in Tab. I.

DC Source

A DC generator is used as direct voltage source. The field winding rated for 500 V and 150 A in continuous operation is connected to the test setup. The terminals of the winding are switched to the mains of the setup through the switchyard of the lab and thus the DC generator does not occupy any space in the setup. It is possible to regulate the output voltage of the DC generator via its excitation. During the test, the DC generator is never separated from the setup. This is not an issue as there is always a path for the DC generator current. Note that the rotational speed of an induction motor decreases with increased load. Thus, the voltage of the DC generator decreases as well if an induction motor is used. Hence, R_L must be tuned to get the desired constant DC.

Capacitor Bank

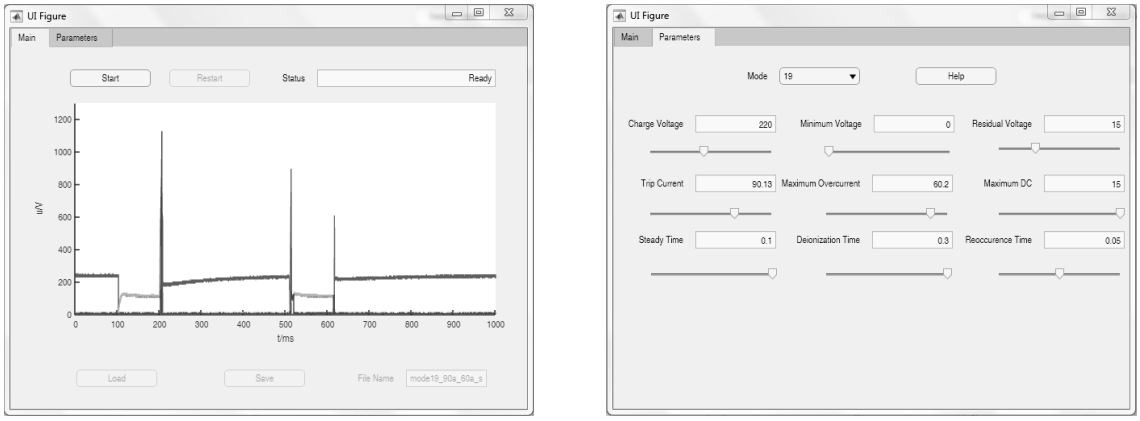
The main purpose of the capacitor bank is to provide the fault current, which is determined by C_{LV}, L_{DC}, U_{LV}, and the test control. As the voltage across the DCCB is determined by the MOV, the capacitor bank only has to store enough energy to supply the demanded fault current. Hence, it is convenient to use several low-voltage capacitors C_{LV} in parallel. For the setup, the KEMET ALS70 capacitor with 13 mF is going to be used. One capacitor is sufficient for the currently used peak current I_F. The size of C_{LV} cannot be increased above the chosen value, because the charging time would otherwise exceed reasonable deionization times. An additional diode in anti-parallel to the capacitor may be needed to protect polarized capacitors from negative voltages. The low-voltage thyristor T is connected to C_{LV} via R_L to charge up the capacitors at a low current. I_1 is used to discharge C_{LV} into the DUT. It is necessary that I_1 and I_2 can also turn off because of the temporary overcurrent mode. I_1 and I_2 should have a low on-state resistance to avoid current pulse damping.

DC Inductor & Resistors

A large in-house made air core inductor rated for 2 kA was inherited from a previous PhD project. The inductor is placed outdoors due to its size and connected to the setup via cables. Regarding resistors, it has to be mentioned that heat dissipation is limited as the total test sequence does not exceed 1 s.

DCCB

As DUT, any DCCB concept can be used. Only the DCCB control logic has to be adapted. It has to be mentioned, however, that the low-voltage rating of C_{LV} can be problematic if a DCCB with large on-state voltage is used, for instance a concept with a mechanical switch with a high arc voltage. The DCCB would in this case influence the test current before it inserts its MOV. The back-up DCCB can be rated for low-voltage as its task is only to decrease the test current in a reasonable time.



(a) Main control tab

(b) Parameter setting tab

Fig. 3: User interface for DCCB test circuit control

Measurements

One issue is that relatively large constant DC has to be measured. Thus, Rogowski coils cannot be used. Alternatives are shunts and hall-effect current sensors. Hall-effect current sensors are preferable as they also provide galvanic isolation. The voltage of the capacitor bank is monitored with a differential probe. In the down-scaled mock-up, the voltage across the DCCB was measured with a differential probe. However, in the planned test circuit the expected voltages are quite high and a high-voltage probe is suitable for this purpose. With high-voltage probes, the voltage is measured with respect to ground and the lower terminal of the DCCB shown in Fig. 2a is not on ground potential. There are several solutions to this problem. One option is to use two high voltage probes and measure at the upper and lower terminal of the DCCB and subtract the measured values. The disadvantage of this is that an additional oscilloscope input is necessary. Alternatively, the position of the DCCB and the back-up DCCB can be swapped so that the lower terminal of the DCCB is grounded. The disadvantage of this approach is that one cannot test interruption against potential, but one could test this separately.

Experiment Control

To control the experiment, the system-on-a-chip development board ZedBoard is used. The ZedBoard features an FPGA and a two-core processing system. The control logic runs on the FPGA. One core of the processing system is used to acquire and filter measurement values. FreeRTOS runs on the second core of the processing system and provides an interface to a computer. The whole test circuit has been simulated with Simulink Simscape. The control logic has been designed in Simulink as well using the Stateflow toolbox. The target hardware was configured using the Embedded Coder and the HDL coder toolbox. Before commissioning, the control logic was evaluated with an FPGA-in-the-loop simulation and eventually tested in the down-scaled mock-up test circuit. The ZedBoard and the oscilloscope are connected to the network via Ethernet which allows for galvanic isolation and remote setup control. The test parameters can be set in the user interface shown in Fig. 3. The user interface was setup using Matlab App Designer. The user interface also allows to show the measurement results and to save them to a text file for later data processing.

Down-Scaled Mock-Up

To test the control system, the test circuit with reduced component count shown in Fig. 2b has been built as down-scaled mock-up using components that are usually used for student labs on DC-DC converters in KTH's basic power electronics course. An overview of the setup is shown in Fig. 4. The DC generator is driven by an induction motor. IGBTs were used instead of IGCTs and D_1 was not needed due to the anti-parallel diode of the IGBT module. To fully test all modes of the test circuit, a hybrid DCCB as shown in Fig. 1b had to be used. However, no fast mechanical disconnector was available. The DCCB thus consisted of one IGBT in the main path and one IGBT in the commutation path. The IGBT in

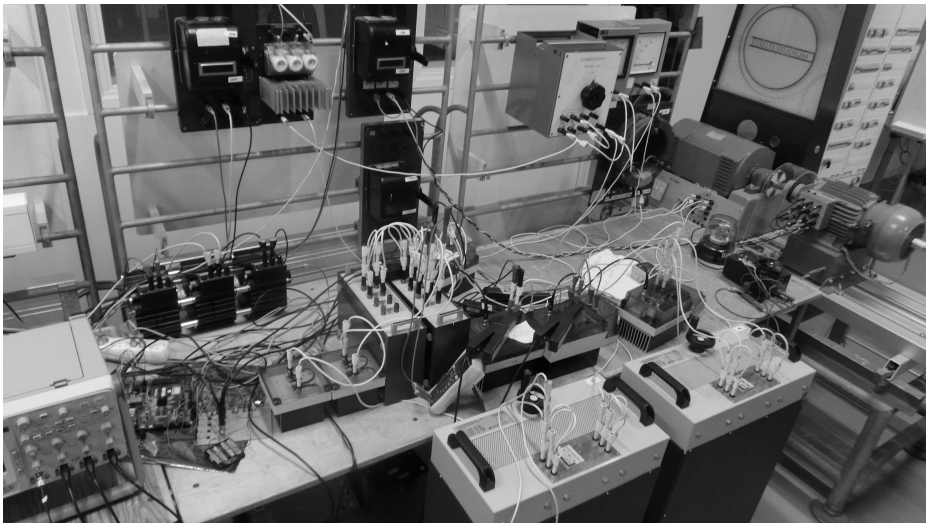
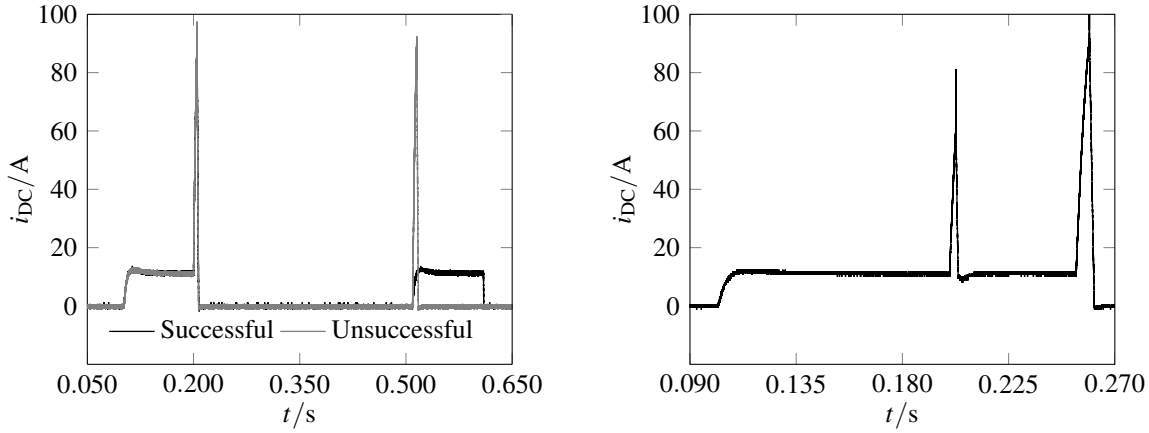


Fig. 4: Picture of down-scaled mock-up DCCB test circuit



(a) Test sequences with auto-reclosing attempt

(b) Test sequence with reappearing temporary fault

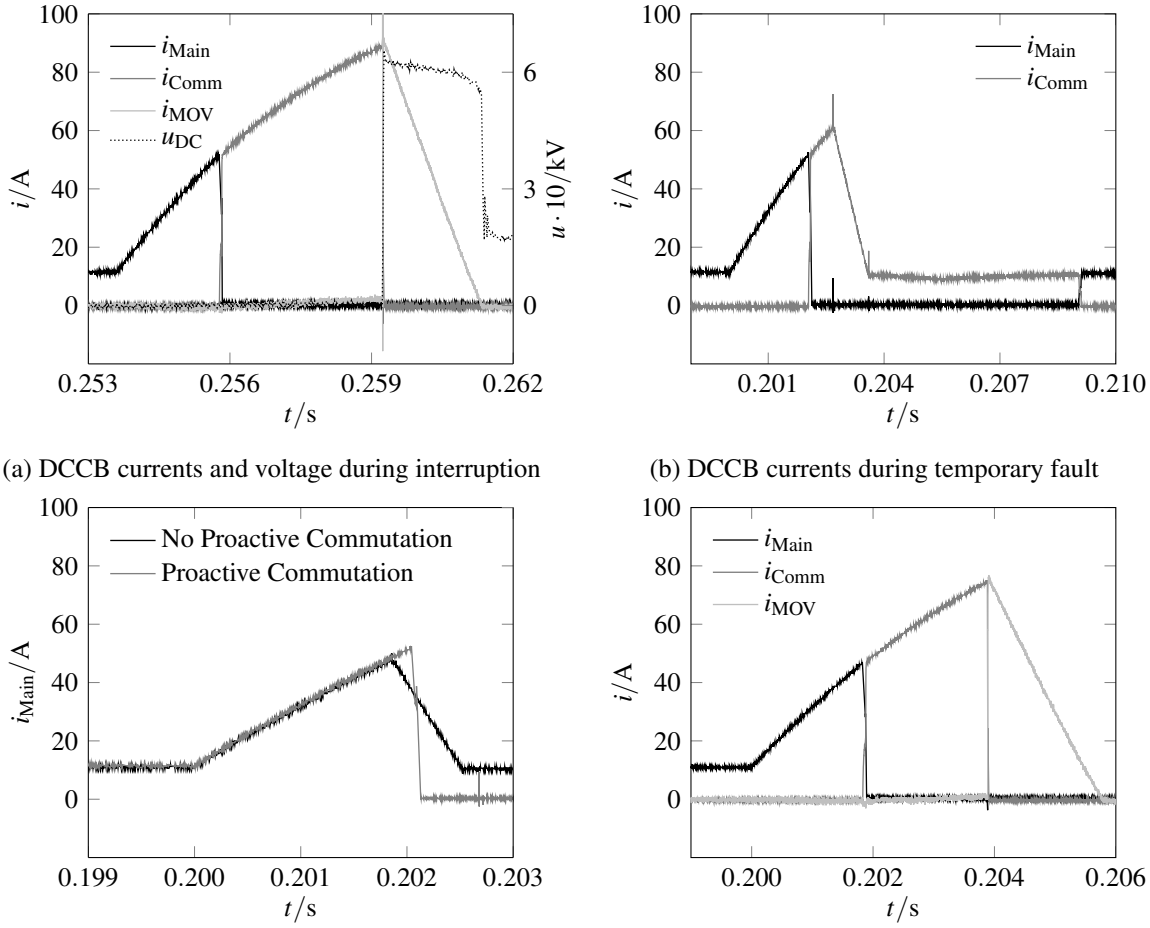
Fig. 5: Measurement results from mock-up DCCB test circuit with hybrid DCCB

the commutation path was controlled to emulate a mechanical disconnector that needs 2 ms to open by corresponding consideration in the control logic. A RCD snubber with a 822.9 Ω resistor and a 3.1 µF capacitor was connected in parallel to the DCCB. During the tests, severe EMI issues delayed the work. As recommendation, a good grounding layout should be used.

Results & Discussion

Measurement results from the down-scaled mock-up DCCB test circuit are depicted in Fig. 5 for selected test sequences. The proactive commutation threshold was set to 50 A. The snubber current is included in the i_{MOV} curves as the snubber is considered to be part of the energy absorption path. In Fig. 5a, the DCCB current is depicted for a test sequence, where firstly a constant DC is supplied and then a fault occurs. The DCCB interrupts and then recloses after a set deionization time of 300 ms. In one case, the fault is cleared and normal operation with constant DC is resumed. In the other case, the DCCB has to interrupt again as the fault had not cleared. In Fig. 5b, the DCCB current is depicted for a test sequence, where firstly a constant DC is supplied and then a temporary fault occurs that clears without tripping the DCCB. The fault reappears and the DCCB interrupts. The test circuit is capable of operating for any combination of constant DC, temporary fault, and fault with one capacitor bank recharging.

In Fig. 6a, the DCCB currents and voltage are depicted during an interruption process. The trip level was set to 90 A and due to proactive commutation the DCCB can directly interrupt. After the MOV absorbed



(a) DCCB currents and voltage during interruption

(b) DCCB currents during temporary fault

(c) Comparison of two temporary faults

(d) Trip below proactive commutation threshold

Fig. 6: Close-up of measurement results during temporary faults and faults

the energy from L_{DC}, a voltage oscillation is visible due to the recovery processes of the semiconductors and the inductor in the circuit. In Fig. 6b, the DCCB currents are depicted throughout and shortly after a temporary fault with a peak current of 60 A. Due to proactive commutation, the current is commutated from the main path to the commutation path. However, the semiconductors in the commutation path should not overheat. Therefore, the current is commutated back to the main path after no trip signal has been received within 5 ms after the fault. In Fig. 6c, the current in the main path of the hybrid DCCB is shown during two different temporary faults. The *Proactive Commutation* curve corresponds to the case already discussed for Fig. 6b. In the other case, the fault current does not surpass the proactive commutation threshold. Consequently, the current remains in the main path throughout the temporary fault. However, this also means that the semiconductors in the main path have to sustain the overcurrent for a longer time compared to the proactive commutation case. This has to be considered when dimensioning a hybrid DCCB. In Fig. 6d, the DCCB currents are depicted during a fault. The trip is already initiated at 45 A which is below the proactive commutation threshold. Thus, the disconnector would not have started to open and 2 ms pass until the DCCB is ready to interrupt. Compared to the fault shown in Fig. 6a, the peak fault current is higher than the current level at which the DCCB was tripped.

Conclusion

In this work, a test circuit suitable for testing down-scaled DCCBs has been described. In contrast to the previous state-of-the-art test circuits, the proposed test circuit allows constant DC stressing, auto-reclosing, and temporary fault testing. To achieve this, a DC generator is used as direct voltage source. The downside of the proposed test circuit is that the fault current is provided from a low-voltage source.

Thus, MOVs rated for high-voltage are not appropriately stressed and high on-state voltages of the DCCB would influence the fault current. If it is necessary to stress the DCCB with the rated voltage for a longer time, the test circuit has to be modified. This could potentially be achieved by splitting the test circuit in a low-voltage and high-voltage part, where additional energy is supplied to the MOV from the high-voltage side when it starts conducting. However, the proposed test circuit will mainly be used to evaluate DCCB concepts and is sufficient for this purpose. Experimental results from a down-scaled mock-up have highlighted the capabilities of the test circuit for a hybrid DCCB. The influence of the proactive commutation threshold and tripping instant was evaluated.

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