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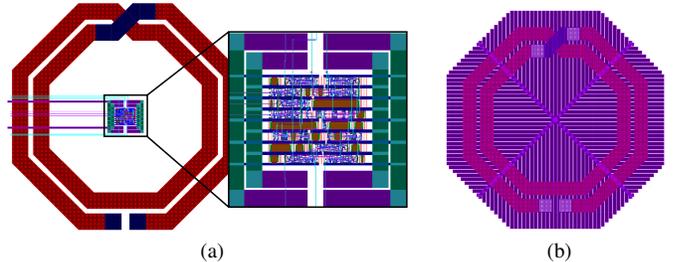
Fig. 1. (a) Top tier inductor with: n=2 turns, turn width w=20 μm, spacing between the turns s=6 μm and an output diameter D_{out}=280 μm. This topology results in a 1.3 nH inductance value. A 3-bit adder is placed on the bottom tier under the inductor. Its power ring is broken into two parts to suppress eddy currents. (b) Patterned Ground Shield (PGS)

I. INTRODUCTION

Monolithic 3-D (M3D) integration, along with its miniature-sized inter-layer vias, enables significant area savings and interconnect delay reduction for integrated circuits and systems [1]. As far as the applications of this technology are concerned, the research focus has been mainly with the area, performance and power gains of M3D digital systems [2]–[4]. Recently, applications of Monolithic 3-D (M3D) integration in radio frequency/analog mixed-signal (RF/AMS) circuits and systems have been proposed as well [5]. There, a frequency partition scheme was employed, in which the high-frequency blocks were placed in the top tier with low-parasitics SOI devices and the low-frequency ones in the bottom. MIM capacitors and high-frequency inductors were also implemented in the top tier, as the use of tungsten for the bottom tier's metals would increase the losses of these passive devices. Tungsten was considered for the bottom tier routing resources to ensure the latter's stability during the top tier processing, despite its high resistivity value compared to aluminum and copper. Furthermore, a top tier implementation for these passive devices increases their distance to the silicon surface, leading to reduced substrate-related losses. In [5] however, precious silicon area was sacrificed as no bottom tier blocks were placed underneath top tier-inductors. To fully exploit the advantages that M3D integration offers for area-efficient RF/AMS circuits, the potential of placing bottom tier digital blocks beneath top tier inductors, as shown in Fig. 1(a), must be investigated. Digital circuitry is routinely employed to improve the performance of RF/AMS systems. For instance, in [6], a technique was proposed to counter the impact of process mismatches, in addition to temperature and supply voltage

variations on the gain and linearity of active down-conversion mixers. This technique was based on digitally calibrating the mixer's biasing current and switching its loads.

In general, placing bottom tier digital blocks under top tier inductors could increase the capacitive loading of the former's wires, especially if a shield is employed. Furthermore, the rail-to-rail voltage excursions of digital signals could severely corrupt the performance of inductors. Lastly, the conventional power ring that surrounds digital blocks fails to suppress eddy currents induced by the inductor's magnetic field. In conventional 2-D processes, the limited space between the inductor and the digital block's wires would exacerbate these issues, prohibiting thus the placement of inductors over digital blocks. On the other hand, M3D integration technology could enable this placement through a design-technology co-optimization flow.

II. DESIGN-TECHNOLOGY CO-OPTIMIZATION

This co-optimization flow involves specifying the Back-End of Line (BEOL) features of the M3D process, deciding upon the insertion of a shield and its characteristics, as well as the modification/redesign of the digital block's power ring.

A. Process Description

The 20 nm FDSOI process from CEA-LETI, which is optimized for digital applications, is considered for the bottom tier (base process), with tungsten metal layers as in [7]. A 160 nm thick SiO_2 layer is deposited over the topmost metal of the base process and serves as the inter-layer dielectric

(ILD). On top of that, a 18 nm thick silicon layer is used for processing the top tier transistors. Since this work continues the exploration of [5], where high frequency blocks were placed on top, the BEOL of the base process cannot be reused in the top tier due to (a) the absence of a thick metal necessary for high performance inductors and (b) the small thickness of the metals and inter-metal dielectrics, which results in a small distance between the top-most metal and the silicon substrate and can cause extensive substrate losses for top-tier inductors. In this work, 5 aluminum metal layers, M1t-M5t, are considered in the top-tier, each 400 nm thick. The inter-metal distance is set to 400 nm and the average dielectric constant in the top tier is 3.1. One additional thick metal (4 μm thick) is reserved specifically for the inductors, M6t. The distance between M5t and M6t is set to 1 μm, to further increase the inductor-substrate distance.

B. Shield Implementation

To improve the electromagnetic isolation between the top tier inductor and the bottom tier's digital blocks (inter-tier isolation), the electric fields produced by the latter need to be terminated. The insertion of a patterned ground shield (PGS), as shown in Fig. 1(b), can help in this direction [8]. In this work, the width of the shield's metal fingers is set to 5 μm, whereas the spacing between them to 1 μm. The shield fingers are connected together through the two diagonals lines shown in Fig. 1(b). Eight ground connections are considered for the effective grounding of the shield, equally distributed along its perimeter. The PGS can be implemented either on the top or the bottom tier. A top tier implementation for the PGS is considered in this work to free-up routing resources in the bottom tier. The closer the shield is placed to the inductor, the lower the capacitance penalty on the bottom tier wires gets. Since tungsten is approximately 2.5 times more resistive than aluminum, the increase in the wire capacitance caused by the PGS needs to be minimized for a low penalty on the bottom tier's interconnect-delays. On the other hand, the closer the shield is placed to the inductor, the higher the drop in the inductor's quality factor gets, due to the increased capacitive coupling between the two.

To study this trade-off, the inductor topology of Fig. 1, designed in the described M3D process of section II-A, is employed. A 50 μm long horizontal wire, implemented on bottom tier's M3, is placed underneath the inductor, at its center and a top tier PGS is inserted between the wire and the inductor. Keysight's Momentum was employed to carry out the simulations. The wire's capacitance, Cap, is compared for various cases of the PGS layer, to analyze the impact of the shield on the loading of bottom tier wires. Furthermore, the inductor's maximum quality factor, Q_{max} and its self resonance frequency, f_{SR}, are also extracted to determine how the PGS layer affects the inductor's behavior. Ports P1 and P2 drive the inductor, whereas port P3 drives one end of the bottom tier wire (the left), while the other remains open. The simulated S-parameters are then converted to Y- and Z-parameters and the wire's capacitance, Cap, is calculated by
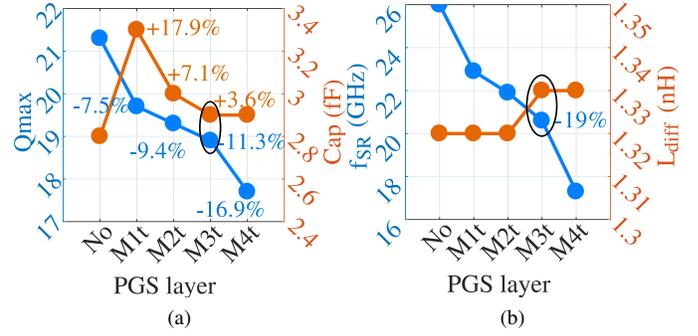

Fig. 2. (a) Q_{max} and wire capacitance, Cap, for various PGS layers (b) f_{SR} and L_{diff} for various PGS layers

(1). For the inductor, a differential excitation is assumed, so, its inductance and quality factor are calculated by (2)-(4).

$$Cap = \frac{1}{\omega}\Im(Y_{33}) \tag{1}$$

$$L_{diff} = \frac{1}{\omega}\Im(Z_{diff}) \tag{2}$$

$$Q_{diff} = \frac{\Im(Z_{diff})}{\Re(Z_{diff})} \tag{3}$$

$$Z_{diff} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \tag{4}$$

The results are plotted in Fig. 2(a-b). The inductance value remains almost constant ($\approx$1.3 nH) as the shield moves further from the substrate, changing by less than 0.8%. On the other hand, the shield layer appears to impact Q_{max}, f_{SR} and Cap remarkably. The results indicate that a M2t and M3t PGS lead to an optimal trade-off between Cap and Q_{max}. In this work, a M3t PGS is preferred to further minimize the penalty on the capacitance of the bottom tier's wires (+3.6% for the 50μm wire in this section), despite degrading the inductor's maximum quality factor and self-resonance frequency by 11.3% and 19% respectively.

C. Power Ring Design Considerations

The magnetic field from the inductor induces eddy (loop currents) on the closed loop that is formed by the digital block's power ring (PR). This in turn, causes an increase in the inductor's series resistance [8], and consequently a drop in its quality factor. To verify this, the topology shown in Fig. 3(a), along with a M3t PGS, is simulated. The inductor geometry is the same as the one from subsection II-B. As expected, the inductor's Q_{max} drops by approximately 20% compared to the case without a power ring, as it is shown in Fig. 3(c). To cancel this drop, the flow of eddy currents in the power ring needs to be mitigated. This can be achieved by breaking the power ring, along with the horizontal lines that feed the cell rows, as shown conceptually in Fig. 3(b) (case bPR). Naturally, the most optimal position for this breaking is along filler cells. The two parts of the power ring can
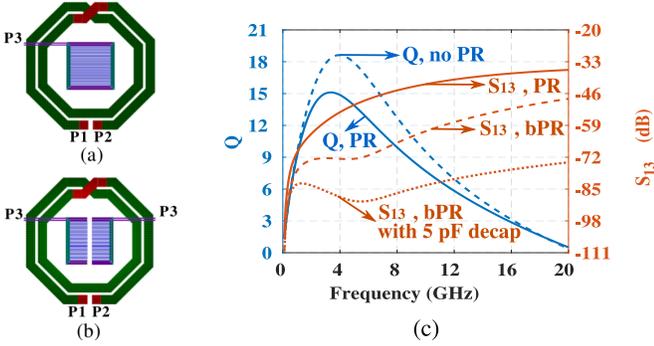
Fig. 3. (a) Top tier inductor over a conventional power ring in the bottom tier (b) Proposed Broken Power Ring (c) Comparison between the inductor's quality factor Q and the S_{13} parameter for cases (a) and (b)
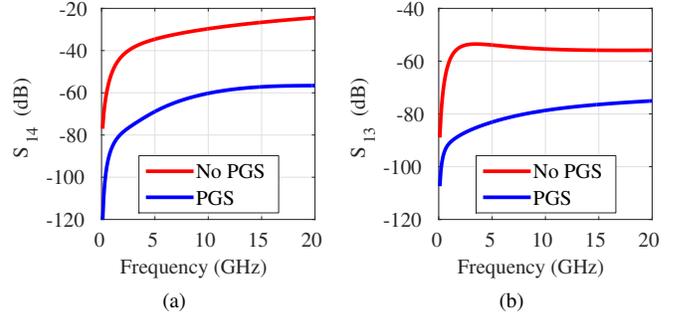

Fig. 4. (a) S_{14} with frequency (b) S_{13} with frequency

TABLE I
INDUCTANCE, QUALITY FACTOR AND CAPACITANCE OF THE CLOCK SIGNAL BEFORE AND AFTER THE STACKING

	L	Q_{max}	C_{clock}
with stacking	1.3 nH	18 (20.2)[*]	20.3 fF (20 fF)[*]
without stacking	1.3 nH	18.9 (21.3)[*]	20 fF

[*] The values inside the parenthesis refer to the case without PGS

be then reconnected manually, outside the inductor area. To quantify the electromagnetic isolation between the inductor and the power ring, the S_{13} parameter is used, with the ports connected as in Fig. 3(a-b). Assuming a perfect termination on port P3 (no reflected signal), then $S_{13} \simeq V1/V3$, so the S_{13} parameter approximates the crosstalk between the inductor and the bottom tier's power ring.

It appears that the breaking of the power ring results in an improvement of S_{13} as well. Further improvement of S_{13} ($\Delta S_{13} = 28$ dB at 10 GHz) is possible with the use of a decoupling capacitor (5 pF) between the supply rails, as also shown in Fig. 3(c).

III. DEMONSTRATION OF A 3-BIT ADDER, PLACED UNDER AN INDUCTOR

As a proof of concept, a 3-bit adder synthesized for a 1 GHz clock, has been placed under the top tier inductor of Fig. 1(a). The digital block makes use of four metal layers for its routing, which constitutes a significant portion of a 2-D process' BEOL. This demonstrates why such a placement is not favorable in a conventional process. The adder's power ring has been manually split in two parts and a 5 pF decoupling capacitor has been inserted between the supply rails. Two different scenarios are considered for the simulations: (a) with and (b) without a M3t PGS. Based on section's II-B results, where a M3t PGS increased the loading of a bottom tier wire by only 3.6%, the same synthesis script was employed for the adder, irrespective of the presence or not of a shield. The connections to the adder's I/O pins are assumed in the left-hand side of the inductor. To account for the worst case scenario, when all the I/O ports switch simultaneously and in the same direction, all the I/O signals are driven by port P4. The isolation between the inductor and the digital signals will be then quantified through the S_{14} parameter. S_{13} describes the isolation between the inductor and the power ring of the adder. The results are plotted in Fig. 4. Both, S_{13} and S_{14} remain below 60 dB when the PGS is included, for frequencies up to 10 GHz. The capacitive loading of the clock signal, C_{clock} and the inductor's Q_{max}, before and after stacking, are listed in Table I. It is worth noting that the M3t PGS increases the

loading of the clock-signal by only 1.5%. Furthermore, for low clock frequencies (< 0.5 GHz), the shield may not be needed in some applications, as the electromagnetic isolation is sufficiently high ($S_{13}, S_{14} < -60$ dB), even without it. This would also negate the drop in the inductor's Q_{max} that is posed by the shield.

IV. CONCLUSION

The potential of placing digital blocks in the bottom tier of a M3D process, under top tier inductors has been identified in this work. Inter-tier electromagnetic isolation in excess of 60 dB is possible through a combination of a PGS, a modified power ring and enough power-rails decoupling. M3D technology could potentially enable the co-existence of radio and digital blocks that share the same silicon area, opening thus opportunities for very compact integration.

REFERENCES

[1] P. Batude *et al.*, "3DVLSI with CoolCube process: An alternative path to scaling," in *Symp. VLSI Technol.*, Kyoto, 2015, pp. T48–T49.
[2] R. Boumchedda *et al.*, "High-Density 4T SRAM Bitcell in 14-nm 3-D CoolCube Technology Exploiting Assist Techniques," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 25, no. 8, pp. 2296–2306, 2017.
[3] J. Shi *et al.*, "On the Design of Ultra-High Density 14nm Finfet based Transistor-Level Monolithic 3D ICs," in *IEEE Comput. Soc. Annu. Symp. VLSI*, 2016.
[4] H. Sarhan *et al.*, "An Unbalanced Area Ratio Study for High Performance Monolithic 3D Integrated Circuits," in *VLSI (ISVLSI), IEEE Comput. Soc. Annu. Symp.* IEEE, 2015.
[5] P. Chaourani *et al.*, "Enabling Area Efficient RF ICs through Monolithic 3D Integration," in *Des. Autom. Test Eur. Conf. Exhib. -DATE*, 2017.
[6] S. Rodriguez *et al.*, "Digital calibration of gain and linearity in a CMOS RF mixer," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2008, pp. 1288–1291.
[7] F. Clermidy *et al.*, "Technology scaling: the CoolCube paradigm," in *SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. - S3S, IEEE*, 2015.
[8] C. P. Yue *et al.*, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, 1998.