Realization of a Planar Power Circuit With Silicon Carbide MOSFETs on Printed Circuit Board

Arash Edvin Risseh^{1*}, Hans-Peter Nee¹, Konstantin Kostov²

¹ School of Electrical Engineering, KTH Royal Institute of Technology, Stockholm, Sweden

² The Mads Clausen Institute, SDU Electrical Engineering, Sonderborg, Denmark

*E-mail: risseh@kth.se

Abstract—Silicon Carbide (SiC) MOSFETs offer excellent properties as switches in power converters. However, the package of the device is an issue that prevents utilizing the advantages of SiC, as for instance fast switching speed. The packages of currently available SiC devices are the same as those previously used for silicon devices with moderate electrical and thermal characteristics resulting in accelerated aging and reliability issues. Moreover, the parasitic inductance caused by the package, limits the switching time and operating frequency. By excluding the package, the parasitic inductances will be eliminated to a large extent. In this study, the procedure of manufacturing a half-bridge planar power module, using four SiC MOSFET bare dies and PCB, is described. According to simulations, the parasitic inductance L_{stray} of the structure is approximately 96 % lower than most commercial half-bridge modules. It is also shown that double-side cooling can be employed for the proposed module if substrates with low thermal resistance are employed.

Keywords—SiC MOSFET, planar power module, bare die, ultra-low parasitic inductance, double-sided cooling, PCB, DBC, high power density.

I. INTRODUCTION

When designing power converters one of the most important design choices is the choice of package of the power semiconductor devices. This choice affects several important aspects of the targeted power converter, i.e. the way of making the electrical contacts, the way of achieving thermal contact, the grade of sealing against moisture and pollution, maximum allowable temperature, power cycling, electrical parasitic elements of the package, and Kelvin Source/Emitter terminals to mention a few. Typically, any converter designed today would use either discrete packages of single chips or multichip power modules. Both types of packages come in various forms targeting different application areas. In several application areas there is a strong trend towards high power density and a high rate at which new generations of products are developed [1]–[3]. A good example of such an application area is power electronics for automotive applications [4]–[7]. Ever higher demands on compactness impose great challenges on both thermal design and high-speed switching. Additionally, such advanced designs are expected to be made at ever shorter development times. This calls for excellent thermal properties, minimum parasitic inductances, and a high degree of flexibility regarding the choice of main circuit and how many chips should be connected in parallel in each switch position. From a designers point-of-view an interesting option would be to combine double-side cooling with full freedom to choose the number of parallel-connected chips, and the gate drivers for

those chips would have to be as close as possible in order to enable the targeted switching speeds [8]–[13].

The basic building blocks in order to exploit the desired option of design would be bare dies (or extremely simple packages) of power semiconductor devices, simple isolated and very thin integrated gate drivers, and some kind of substrate facilitating electrical conduction, thermal conduction, and electric isolation. Unfortunately, good combinations of these building blocks are not available today. It is, nevertheless, interesting to explore some of the possibilities of the concept using existing technology because a successful combination would enable excellent thermal properties, excellent switching properties, rapid prototyping, efficient automated production, and use of high-volume low-cost power semiconductor devices and integrated gate drivers. Some investigations have been performed to demonstrate the concept of a planar module and possible packaging methods of semiconductor devices with focus on the thermal issues [14]–[17]. The goal of this paper is, however, to demonstrate an example of such a power circuit using silicon carbide (SiC) metal-oxide semiconductor field-effect transistor (MOSFET) bare dies (1.2 kV & 98 A) in combination with integrated gate drivers and standard printed circuit boards (PCBs) with focus on low parasitic inductance. As standard PCBs exhibit relatively poor thermal conduction, the thermal evaluation of this concept has been postponed to the future, and the evaluation of the circuit is performed by means of double-pulse tests with minimum heat generation. Nevertheless, double-side cooling would be possible with the chosen concept. The outline of the paper is as follows. In Section II the chosen concept is described in detail followed by a description of the different steps of the realization in Section III. Experimental results are presented in Section IV, and in Section V conclusions and discussions are given.

II. DESCRIPTION OF THE CONCEPT AND SIMULATION RESULTS

A model of a MOSFET is shown in Fig. 1. In this model the parasitic inductance and capacitance of the package as well as the external parasitic inductances from the circuit are shown. In order to reduce the total parasitic inductance of a MOSFET, the package of the device may be excluded and the bare die can be used. In that case, due to smaller distances between the pads of the die, also the external inductances will be reduced. In this study, a half-bridge with four bare dies from Wolfspeed (CPM2-1200-0025B) was designed. This SiC power MOSFET has a blocking voltage of 1200 V and manages 98 A. The layout of the die is shown in Fig. 3. The size of the die is 644

$\mu\text{m} \times 404 \mu\text{m} \times 180(\pm 40) \mu\text{m}$. The Gate and Source pads are located on the top side and the Drain pad is located on the backside. The clearance between the Gate and the Source pads is approximately $80 \mu\text{m}$.

Fig. 1. A model of a power MOSFET including the parasitic elements.

In order to design a power module a half-bridge with two SiC power MOSFETs, connected in parallel at the high- and low-side, was considered. The four bare dies could be directly connected to the PCB. However, due to the placement of the pads, two PCBs are required to create the necessary electrical connection between the Source and Drain pads at the low- and high-sides. Therefore, a module where the bare dies are sandwiched between two PCBs was designed. A sketch of the structure is shown in Fig. 2 where four bare dies are placed between two PCBs. The DC-link can be connected to one side of PCB 1 and the *phase node* is taken from the other side. The parasitic inductances and resistances of the design were extracted from ANSYS Q3D and are listed in Tables I and II and the corresponding parasitic inductances in the circuit can be seen in the schematic diagram in Fig. 4. The simulation was performed for regular FR4 with 2 mm thickness and $35 \mu\text{m}$ thick copper plate.

Fig. 2. Sketch of the planar power module with two SiC MOSFETs at high- and low-positions, respectively.

The simulated dimension of the structure was imported into a PCB-CAD software to design the real circuit. No changes were made on PCB 2 and the part on PCB 1 where the

Drain pads of the dies would be placed. The placement of the other components as the gate drivers, voltage sources, capacitor banks, DC-link capacitors and signal connectors could easily be decided and placed in the CAD software. The final layouts of PCB 1 and PCB 2 are shown in Figs. 6 and 7. Since the distance between Source and Gate pads is $80 \mu\text{m}$ the loop inductance will be extremely small. However, in order to create a larger clearance between the Gate and Source, only 4/5 of the lower side of the Gate pads were used for the connection. This would create $180 \mu\text{m}$ clearance between the Source and the Gate of the MOSFET.

Fig. 3. Layout and the size of the bare die and its pads. The thickness of the bare die is $180 \pm 40 \mu\text{m}$. The picture is used in the datasheet of the bare die, provided by manufacturer.

TABLE I. SIMULATION RESULTS SHOWS THE PARASITIC *inductance* OF PCB TRACES.

Parasitic Inductance [nH]	FET 1	FET 2	FET 3	FET 4
GATE	7.20	3.47	2.37	5.96
DRAIN	0.0862	0.0876	0.347	0.346
SOURCE	0.632	0.638	0.249	0.254

TABLE II. SIMULATION RESULTS SHOWS THE PARASITIC *resistances* OF PCB TRACES.

Parasitic Resistance [$\mu\Omega$]	FET 1	FET 2	FET 3	FET 4
GATE	8534	4323	3131	7344
DRAIN	58.51	59.14	132.3	132.6
SOURCE	216.5	217.1	122.4	124.2

In order to simplify the design and create similar parasitic Gate inductance on the high- and low-side, two separate gate drivers, also acting as an isolator, from ANALOG DEVICES (ADuM3221) were employed. This driver is a surface mount component with low profile (approx. 1.5 mm) and small distance between the leads. The drawback of this component is the low output current (4 A) and relatively low output

Fig. 4. Schematic diagram of the half-bridge configuration with two SiC MOSFETs in parallel at each position. The parasitic inductances in [nH] are included in the diagram.

voltage (18 V). An optimum gate driver for this case, however, would manage 24 V output voltage and >10 A in source and sink current, and act as an isolator simultaneously. The gate-drive circuits were placed on PCB 1 and the signals were transferred from PCB 1 to PCB 2, where the Gate and Source pads are connected, through connectors, see Fig. 5. The gate driver was supplied by isolated DC/DC converters with voltages between -3 to +15 V. The signals to the low- and high-position drivers were generated from a digital signal processor (DSP) and were transferred to the module by signal cables. PCB 1 was also prepared for two 100 μ F input capacitors (107TTA350M-350V).

Fig. 5. Structure of the planar power module. The Gate and Source voltages go via two connectors between PCB 1 and PCB 2.

Fig. 6. Actual layout of PCB 1 and the placement of the driving circuits, DC-link capacitors and the Drain pads of the MOSFETs.

Fig. 7. Actual layout of PCB 2 where the connection to Source and Gate pads are placed.

III. REALIZATION

Soldering of the bare dies on the PCBs has to be performed in two steps; first the dies (Drain-side) need to be soldered to PCB 1 and the second step is to solder PCB 2 to the bare dies (Source-side) and fix it on PCB 1, see Fig. 8. Therefore, two different solder pastes with different melting temperatures were used. SMD291SNL10T5-ND with a melting temperature of 218 $^{\circ}$ C was used to solder the Drain pads of the bare dies to PCB 1 and SMDLTLP15T4-ND with a melting temperature of 138 $^{\circ}$ C was used to solder PCB 2 to the Gate and Source pads, and to PCB 1.

The same amount of solder paste was placed on all Drain metallization and the bare dies were placed on PCB 2 and heated up with hot air according to the recommended temperature profile. The Drain pad is created of nickel and silver intermetallic alloys. Therefore, an ohmic connection is easily formed. However, the most sensitive part is the top side of the bare dies where the Source and Gate pads are placed and metallized by aluminum alloys and the clearance between the Source and Gate pads is 80 μ m. A number of trials showed that forming metallic connections to the pads was an extremely complex task due to the rapid creation of aluminum oxide on the surface of the pads. The best method found to be first reflowing the low-temperature solder paste on PCB 2, and then place PCB 2 over the bare dies and reflow it again. It was

necessary to employ a specially developed aluminum solder flux during the second reflow. The flux prevents the creation of aluminum oxide and will be activated at approx. 130 °C which is close to the melting temperature of SMDLTLP15T4-ND (138 °C). However, caution has to be taken if the entire processes needs to be repeated. The flux strips a thin layer of the aluminum from the pads each time it is activated. The connectors (Fig. 5) were first soldered to PCB 2 with the high-temperature solder paste and then, during the reflow process of PCB 2 to the bare dies, they were connected to PCB 1 by the low-temperature solder paste. Figure 9 shows the complete board where all components are soldered to the PCBs. It has to be mentioned that the only method to verify correct connections and functionality of the system is to perform an electrical double-pulse test because no visual inspection of the sandwiched structure is possible.

Fig. 8. Part of the manufactured PCBs. The Drain pads of the MOSFETs are soldered to PCB 1, and PCB 2 will be prepared to be soldered to the dies.

Fig. 9. Complete planar power module prepared for functionality test.

IV. VERIFICATION AND EXPERIMENTAL RESULTS

In order to verify correct connection of the pads, the functionality and proper switching, the module was configured for a double-pulse test. A high direct voltage source was

employed as a power supply. The input voltage and the current to the system were increased stepwise up to 400 V and 75 A. The inductor current could be increased by decreasing the inductance value. The inductor current was measured by a Rogowski current transducer and VDS and VGS of the upper SiC MOSFETs were studied on a high performance oscilloscope (MSO7104A-Agilent Technologies). The complete board, the components and the experimental setup can be seen in Fig. 10. The system response and the signals at 400 V input voltage and 75 A are presented in Fig. 11. The rise- and fall times of VDS of the high-side switches was measured to approximately 23 and 60 ns, respectively. The external gate resistance, R_g , was 10 Ω during this measurement. No oscillations in voltage during turn-on, and only one overshoot with an amplitude of 100 V during turn-off, were observed.

Fig. 10. The planar module and the experimental setup.

Fig. 11. Measurement results from double-pulse test. The green pulse shows the gate signal, the red one is the inductor current, the lilac shows the VDS of the upper switches and the yellow one shows the control signal from the controller (3.3 V).

V. CONCLUSION AND DISCUSSION

A planar power module with four SiC MOSFET bare dies was designed, manufactured and tested. The bare dies were soldered and directly attached on two PCBs. Since, the directly-attached bare dies have small dimensions the proposed structure can be manufactured with very short traces, creating low parasitic inductances. The planar module was exposed to a double-pulse test. Fast Switching speed was obtained and no significant oscillation in voltage and current could be observed at 400 V & 75 A. For the proposed module double-sided cooling on the Source- (PCB 2) and Drain-side (PCB 1) is possible. Fast switching and thereby low switching losses, together with double-side cooling enable either operation at lower temperature, with improved reliability, or operation at higher current with increased power density. Furthermore, the module can easily be custom-designed with freedom to choose the placement of other components on the board. Another advantage of the proposed module, from manufacturing point-of-view, is that the entire area of the pads is used for the electrical connections and all pad-to-substrate-connections can be created at once during a single reflow process. During the same reflow process additional components, such as gate-drive circuits, can be attached to the module. Since the gate-drive circuits, the module itself and other components are placed on the same board, the proposed module should probably have lower cost and higher power density than most commercial modules. This structure may be expanded with additional bare dies for higher current capability resulting in lower parasitic inductance as suggested in [18]. According to simulations the parasitic inductance between the Drain of the upper transistors to the Source of the low-side transistors of the current design is 0.653 nH which can be compared to 15-17 nH in commercial half-bridge modules.

It has also to be mentioned that further investigations on the proposed module is needed. In such investigation possibility of using substrates with low thermal resistance has to be studied. In addition, in order to easily attach the bare dies into the substrates, the pads have to be metalized not only by pure aluminum but by other intermetallic alloys combined with aluminum. The creation of aluminum oxide on the surface of the pads (made by pure aluminum) and also the short distances between the pads are the two most important issues to consider and need to be addressed for mass-manufacturing. Furthermore, in real applications the mismatch of the coefficient of thermal expansions of the bare dies, the soldering alloys as well as the substrates has to be thoroughly evaluated. In high-voltage applications, in order to achieve sufficient galvanic insulation between the two substrates, and to improve the mechanical properties a filler between PCB 1 and PCB 2 has to be employed.

REFERENCES

- [1] H. Hourdequin, L. Laudebat, M. L. Locatelli, and P. Bidan, "Design of packaging structures for high voltage power electronics devices: Electric field stress on insulation," in *IEEE International Conference on Dielectrics (ICD)*, vol. 2, Jul. 2016, pp. 999–1002.
- [2] Z. Chen, Y. Yao, W. Zhang, D. Boroyevich, K. Ngo, P. Mattavelli, and R. Burgos, "Development of a 1200 V, 120 A SiC MOSFET module for high-temperature and high-frequency applications," in *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, Oct. 2013, pp. 52–59.
- [3] S. Hazra, A. De, L. Cheng, J. Palmour, M. Schupbach, B. A. Hull, S. Allen, and S. Bhattacharya, "High switching performance of 1700-V, 50-A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.
- [4] A. Shimozuma, H. Hayashi, S. Higuchi, Y. Sakamoto, and S. Okada, "Packaging technology of power module for automotive applications," in *International Conference on Electronics Packaging (ICEP)*, Apr. 2017, pp. 117–121.
- [5] J. B. Casady, B. Hull, J. Zhang, D. Gajewski, G. Wang, S. Allen, J. Palmour, and K. Olejniczak, "First automotive reliability assessment and drive-train performance of large-area 900 V, 10 mohm SiC MOSFETs," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 2259–2262.
- [6] T. Bertelshofer, R. Horff, A. März, and M. M. Bakran, "Comparing 650 V and 900 V SiC MOSFETs for the application in an automotive inverter," in *18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sep. 2016, pp. 1–10.
- [7] A. E. Risseh, H. P. Nee, and C. Goupil, "Electrical power conditioning system for thermoelectric waste heat recovery in commercial vehicles," *IEEE Trans. Transp. Electrification*, vol. PP, no. 99, pp. 1 – 1, Jan. 2018.
- [8] M. Schulz, "Thermal management details and their influence on the aging of power semiconductors," in *16th European Conference on Power Electronics and Applications*, Aug. 2014, pp. 1–6.
- [9] K. Brinkfeldt, J. Ottosson, A. Otto, A. Mann, O. Zschieschang, S. Frankeser, and D. Andersson, "Thermal simulations and experimental verification of power modules designed for double sided cooling," in *IEEE 66th Electronic Components and Technology Conference (ECTC)*, May 2016, pp. 1415–1422.
- [10] S. Kicin, F. Traub, S. Hartmann, E. Bianda, C. Bernhard, S. Skibin, and F. Canales, "A new concept of a high-current power module allowing paralleling of many SiC devices assembled exploiting conventional packaging technologies," in *28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 2016, pp. 467–470.
- [11] M. Barrière, S. Azzopardi, R. Roder, I. Favre, E. Woïrgard, S. Bontemps, and F. L. Henaff, "Silver sintered double-sided cooling power package process for controlled Si power semiconductor devices with aluminum top-metallization," in *IEEE International Workshop on Integrated Power Packaging (IWIPP)*, May 2015, pp. 103–106.
- [12] A. Lemmon and R. Graves, "Parasitic extraction procedure for silicon carbide power modules," in *IEEE International Workshop on Integrated Power Packaging (IWIPP)*, May 2015, pp. 91–94.
- [13] Y. Xiao, H. Shah, T. P. Chow, and R. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 1, 2004, pp. 516–521.
- [14] Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 4907–4912.
- [15] D. Berry, L. Jiang, Y. Mei, S. Luo, K. Ngo, and G. Q. Lu, "Packaging of high-temperature planar power modules interconnected by low-temperature sintering of nanosilver paste," in *International Conference on Electronics Packaging (ICEP)*, Apr. 2014, pp. 549–554.
- [16] Z. Liang, F. Wang, and L. Tolbert, "Development of packaging technologies for advanced SiC power modules," in *IEEE Workshop on Wide Bandgap Power Devices and Applications*, Oct. 2014, pp. 42–47.
- [17] P. Ning, T. G. Lei, F. Wang, G. Q. Lu, K. D. T. Ngo, and K. Rajashekara, "A novel high-temperature planar package for SiC multichip phase-leg

power module,” *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2059–2067, Aug. 2010.

- [18] A. E. Risseh, H. P. Nee, and K. Kostov, “Fast switching planar power module with SiC MOSFETs and ultra-low parasitic inductance,” in *The 2018 International Power Electronics Conference -ECCE Asia-(IPEC-Niigata)*, May 2018.