<http://www.diva-portal.org>

Postprint

This is the accepted version of a paper published in *IEEE Microwave and Wireless Components Letters*. This paper has been peer-reviewed but does not include the final publisher proof-corrections or journal pagination.

Citation for the original published paper (version of record):

Shah, U., Liljeholm, J., Campion, J., Ebefors, T., Oberhammer, J. (2018)
Low Loss High Linearity RF Interposers Enabled by Through-Glass Vias
IEEE Microwave and Wireless Components Letters, 28(11): 960-962
<https://doi.org/10.1109/LMWC.2018.2869285>

Access to the published version may require subscription.

N.B. When citing this work, cite the original published paper.

Permanent link to this version:

<http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-238707>

Low Loss High Linearity RF Interposers Enabled by Through-Glass Vias

Umer Shah, *Member, IEEE*, Jessica Liljeholm, James Campion, *Student Member, IEEE*, Thorbjörn Ebefors, *Senior Member, IEEE*, and Joachim Oberhammer, *Senior Member, IEEE*

Abstract—This letter reports on a new low-loss and high linearity 3-D wafer-level interposer technology enabled by through glass vias (TGVs) with an inverted via configuration. The proposed TGV utilizes a tapered via sidewall profile to achieve a void-free conformal metal coverage with lower process time and fewer fabrication steps than a fully filled conventional TGV. Measurement results for a single 100 μm tall TGV show an insertion loss of 0.014 dB at 10 GHz and a DC resistance of 28 m Ω . Finally, this letter reports for the first time on nonlinearity measurements of TGVs. Single-tone measurements show that the third harmonic level for a coplanar waveguide (CPW) TGV test structure is only 2 dB higher than a reference CPW through line without TGVs, indicating an overall excellent linearity performance.

Index Terms—Through Glass Via (TGV), Micromachining, Heterogeneous Integration, Low Loss, High Linearity.

I. INTRODUCTION

INTERPOSERS with through-substrate vias are the key enabler for heterogeneous integrated System-in-Package (SiP) technologies. Such vias provide benefits in terms of system miniaturization, high-speed communication between chips, reduced power consumption, increased reliability by reducing the number of interconnects and cost reduction due to small form-factor [1]. Silicon substrates with through silicon vias (TSVs) are the most commonly used interposers. The coefficient of thermal expansion (CTE) of silicon interposers is well matched to silicon based integrated circuits (ICs) which effectively manages the warp for IC stacking. However, conventional TSVs suffer from substrate coupling, crosstalk and increased insertion loss at radio frequencies (RF) [2]. Numerous techniques have been employed for crosstalk mitigation and insertion loss reduction at the expense of process time and fabrication cost, including using high resistivity silicon substrate (HRSS), increasing thickness of the silicon dioxide liner and using modified TSV configurations such as air isolated TSV [2], coaxial TSV [3] and polymer clad, polymer embedded TSV. Another disadvantage is the nonlinearity of TSVs due to the formation of a metal-oxide-semiconductor (MOS) capacitor which, for large signals, varies with the voltage swing creating harmonics and other nonlinear effects [4].

The authors acknowledge the financial support by VINNOVA under grant no. 2014-05240 and ENIAC-JU Project Prominent under grant no. 324189.

Umer Shah, James Campion and Joachim Oberhammer are with the Department of Micro and Nanosystems, KTH Royal Institute of Technology, Stockholm SE-100 44, Sweden (e-mail: umers@kth.se).

Jessica Liljeholm and Thorbjörn Ebefors are with SILEX Microsystems AB, Järfälla, Sweden (e-mail: jessica.liljeholm@silex.se).

Thorbjörn Ebefors is now at SPINVERSE AB, Stockholm, Sweden (e-mail: thorbjorn.ebefors@spinverse.com).

Therefore, for high linearity and low insertion loss RF applications, glass is the preferred interposer material. Glass has excellent RF properties including a very high resistivity, low dielectric constant and a low loss tangent [5]. Moreover, glass offers panel-based manufacturability utilizing large panel sizes which reduces the overall cost [6]. Finally, the CTE of glass can be adjusted to achieve thermal compatibility with ICs as well as printed circuit boards which manages the warp for IC stacking [6].

For these reasons, there has been much recent development of TGVs, but few works report measured RF performance. TGVs based on localized glass reflow in silicon have been shown to achieve excellent RF performance but at the expense of fabrication complexity, time and cost [5]. Similarly, ultra-thin 3-D glass interposers with TGVs using panel-based fabrication process have achieved good RF results but require additional fabrication steps [6]. Recently, Corning Inc. has shown a TGV technology with high thermal reliability but require chemical mechanical polishing (CMP) and specialized thin wafer handling [7]. They reported on both fully filled and conformal vias but the insertion loss performance was reported only for the fully filled vias. None of the previous works report TGV linearity data which is important since glass is prone to electro-thermally induced passive intermodulation distortion (PIM) due to its low thermal conductivity [8].

In this letter, we report on a new low insertion loss, high linearity and a low cost TGV technology for wafer-level 3-D packages (WLP). The novel fabrication process reported here differs completely from previous work in literature since the blind conformally plated TGVs are revealed by thinning down the TGV substrate using wet chemical processing not requiring CMP. Additionally, the conformally plated blind TGVs are sealed using wafer level packaging through metal-to-metal bonding. Moreover, we show, for the first time, nonlinearity analysis of TGVs using single-tone harmonic measurements.

II. DESIGN AND FABRICATION

The TGV reported in this letter utilizes an inverted via configuration in a glass substrate formed using blind via holes with a tapered sidewall profile, ensuring low cost, void-free conformal metal coverage. The thermomechanical stress at the interface between the metal layer and the glass due to CTE mismatch is minimized when using a conformal metal layer instead of a fully filled via [9]. The use of blind vias ensures easier handling during processing. Additionally, the proposed TGV fabrication process allows for wafer-level packaging with

a hermetic capping glass lid wafer using thermo-compression bonding. Fig. 1 shows a comparison of the proposed TGV to the conventional TGV. The plating process time is substantially lower than for conventional TGVs where the through via hole needs to be filled completely. Electroplating contribute to almost 40% of the total via cost [10]. There is minimal difference in material cost for a fully filled and a conformal via and the benefit comes entirely from lower process time and fewer process steps. The insertion loss of the TGV due to variation in via pitch, diameter and height were simulated using CST Microwave Studio for two sets of TGVs with a 1 mm bottom RDL between them. The TGV pitch has marginal effect on the insertion loss when it is less than three times the TGV diameter. For a larger via pitch, larger via diameter is required to achieve a lower insertion loss. Fig. 2(a) shows that the insertion loss performance is largely similar for a 75 μm diameter fully filled straight and a conformally plated (7 μm thick gold layer) straight TGV. The conformally plated tapered TGV with the same via diameter and a 80° via angle achieves similar performance but reducing the via diameter while maintaining the same via angle increases the insertion loss. The insertion loss can be improved for smaller via diameters by adjusting the via angle to achieve a larger top via diameter. Fig. 2(b), shows that increasing the via height while maintaining the same via diameter and angle increases the insertion loss. This is due to the longer via length and smaller top via diameter. To improve the insertion loss for a larger via height, the TGV diameter has to be increased. Longer via leads to a larger via diameter which then requires a larger pitch to maintain substrate mechanical integrity.

The TGV WLP was fabricated in a commercial wafer foundry using a 150 mm alkaline earth boro-aluminosilicate Eagle glass substrate. The via holes were digitally processed achieving a tapered sidewall profile in a 500 μm thick glass wafer with a via diameter of 75 μm and an etch depth of 100 μm . The tapered sidewall profile ensures a conformal seed layer deposition by physical vapor deposition (PVD) followed by electroplating of a 7 μm thick gold layer [Fig. 3(a)]. The geometrical volume that needed to be filled was 2.3 times smaller than for a fully filled via. Assuming a uniform via plating rate, the electroplating time was reduced by 57% in comparison to a fully filled via which reduces the total via cost by 23%. Moreover, CMP was not required after electroplating neither for substrate thinning nor for removing the metal overburden. The via holes, redistribution layer (RDL) and bond frames were metallized in the same process step. Coplanar waveguide (CPW) test structures were patterned on a glass wafer plated with 5 μm gold redistribution layer which was bonded to the TGV wafer by thermo-compression bonding of gold [Fig. 3(b)], followed by backside thinning of the TGV wafer by wet chemical processing to open the top of the TGVs [Fig. 3(c)]. The CPW probing pads together with the routing interconnections were electroplated using a 7 μm thick gold layer across the top of the TGVs [Fig. 3(d)].

Fig. 4(a) show the top-view image of the TGV WLP. The cross-sectional SEM image of the TGVs is shown in Fig. 4(b).

Fig. 1. Schematic cross section of the through glass vias (TGVs): (a) conventional TGV; and (b) proposed inverted TGV with conformal metal plating.

Fig. 2. Design parameter study of the proposed TGV: (a) insertion loss variation with TGV diameter; and (b) insertion loss variation with TGV height.

Fig. 3. Fabrication process of the TGV WLP: (a) formation of the blind via holes followed by gold electroplating; (b) gold thermo-compression bonding of the glass lid wafer with patterned CPW lines and bond frames; (c) thinning and TGV reveal process; and (d) electroplating gold for probing pads.

Fig. 4. Images of the fabricated TGV WLP: (a) top-view microscope photograph; and (b) cross-sectional SEM image.

III. RF CHARACTERIZATION

The TGV test structure for RF measurements consisted of 50 Ω top RDL coplanar probe pads (line width = 100 μm and gap = 19 μm), two sets of TGVs and 50 Ω bottom CPW RDL (line width = 100 μm and gap = 33 μm) with variation in length from 700 μm to 2 mm. The probe pads were de-embedded from the s-parameter measurements using the technique outlined in [11]. Fig. 5 shows the measured de-embedded insertion and return loss for the combination of two TGVs and the bottom RDL. The insertion loss per unit length of the bottom RDL alone is calculated by measuring the TGV test structure with different lengths of the bottom RDL. The insertion loss of a single TGV was extracted by subtracting the insertion loss of the bottom RDL alone from

Fig. 5. Measured S-parameters of the TGV with de-embedded probe pads.

TABLE I
PERFORMANCE COMPARISON OF LOW LOSS TSVs AND TGVs

Technology and Ref. No.	Via Dia. [μm]	Via Height [μm]	Via Pitch [μm]	IL @ 10 GHz [dB]	Via loss characterization method
TSV [2]	13	330	100	0.3	single TSV
TSV [3]	70	150	—	0.044	single TSV
TGV [5]	40	100	80	0.05	2 TGVs+RDL
TGV [6]	15/30	30/100	27/60	0.02/—	single TGV
TGV [7]	80	400	160	0.1	2 TGVs+RDL
This work	75	100	170	0.014	single TGV

the measured data. The insertion loss of the bottom RDL alone at 10 GHz was 0.049 dB which resulted in a 0.014 dB insertion loss for a single TGV at 10 GHz. The measured DC resistance of a single via, including the RDL and the bond interfaces, was 28 mΩ. Table I summarizes the measured performance of the fabricated TGV in comparison to that of various published via technologies. The proposed TGV outperforms any previously reported TSVs and has similar or better performance in comparison to previously reported TGVs despite having partially filled vias. The pitch of 170 μm in this work results from the chosen TGV diameter, TGV length, the tapered sidewall profile which supports PVD of the metal seed layer, and the CPW dimensions used to measure the TGV properties. The TGV pitch can be reduced to 110 μm without modifying the other parameters but for reducing the TGV pitch further a smaller TGV diameter has to be chosen.

The linearity of the TGV was analyzed by measuring the power of the second and the third harmonics for the TGV test structure at a center frequency of 2.5 GHz. The measurements were performed for several input power levels ranging from 16.5 dBm to 36.5 dBm. Fig. 6(a) shows the test setup [12], where the isolators were well matched up to the frequency of the third harmonic, the low pass filter was used to suppress the harmonics of the signal generator and the notch filter was used to suppress the fundamental tone at the input of the spectrum analyzer. Fig. 6(b) shows the comparison of the harmonic power measurements for the TGV test structure and a through line of the same length without the TGVs. The second harmonic level for both the through line and the TGV test structure was the same while the third harmonic level for the TGV test structure was 2 dB higher in comparison with the through line. In comparison, the simulation results of the TSVs in [4] show a second harmonic level of -47 dBm for an input signal of 13 dBm indicating overall excellent linearity performance of the proposed TGVs.

Fig. 6. Harmonic measurement of the TGVs in comparison to a through line of the same length without TGVs: (a) test setup; and (b) measurements.

IV. CONCLUSION

In this letter, a fully functional TGV wafer-level 3-D package with a low cost fast fabrication process has been introduced. The proposed inverted via configuration with conformal metal coverage achieves a very low insertion loss of 0.014 dB at 10 GHz per TGV and a DC resistance of 28 mΩ for a daisy chain test structure. Moreover, the measured linearity of the CPW TGV test structure compared to a CPW through line showed no significant difference.

REFERENCES

- [1] S. J. Bleiker, A. C. Fischer *et al.*, "High-aspect-ratio through silicon vias for high-frequency application fabricated by magnetic assembly of gold-coated nickel wires," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 5, no. 1, pp. 21–27, Jan. 2015.
- [2] H. Oh, P. A. Thadesar *et al.*, "Low-loss air-isolated through-silicon vias for silicon interposers," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 3, pp. 168–170, Mar. 2016.
- [3] J.-M. Yook, D. Kim *et al.*, "Low-loss and high-isolation through silicon via technology for high performance RF applications," in *European Microw. Conf.*, Oct. 2014.
- [4] J. Cho, J. Kim *et al.*, "Nonlinear effects of TSV and harmonic generation," in *IEEE Electron. Compon. and Tech. Conf.*, Jun. 2012.
- [5] J.-Y. Lee, S.-W. Lee *et al.*, "Through-glass copper via using the glass reflow and seedless electroplating processes for wafer-level RF MEMS packaging," *J. Micromech. Microeng.*, vol. 23, no. 8, p. 085012, Jun. 2013.
- [6] V. Sukumaran, G. Kumar *et al.*, "Design, fabrication, and characterization of ultrathin 3-d glass interposers with through-package-vias at same pitch as TSVs in silicon," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 4, no. 5, pp. 786–795, May 2014.
- [7] A. B. Shorey and R. Lu, "Progress and application of through glass via (TGV) technology," in *Pan Pacific Microelect. Symp.*, Jan. 2016.
- [8] J. R. Wilkerson, P. G. Lam *et al.*, "Distributed passive intermodulation distortion on transmission lines," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 5, pp. 1190–1205, May 2011.
- [9] T. Ebefors, J. Fredlund *et al.*, "The development and evaluation of RF TSV for 3D IPD applications," in *IEEE Int. Conf. 3D System Integration*, Oct. 2013.
- [10] T. Hayashi, K. Kondo *et al.*, "High-speed through silicon via (TSV) filling using diallylamine additive," *IEEE Trans. Microw. Theory Tech.*, vol. 158, no. 12, pp. D715–D718, Nov. 2011.
- [11] H. Cho and D. E. Burk, "A three-step method for the de-embedding of high-frequency s-parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1371–1375, Jun. 1991.
- [12] C. D. Patel and G. M. Rebeiz, "A high-reliability high-linearity high-power RF MEMS metal-contact switch for DC40-GHz applications," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 10, pp. 3096–3112, Oct. 2012.