Implications of Capacitor Voltage Imbalance on the Operation of the Semi-Full-Bridge Submodule

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Parts of the paper have been presented at EPE'17 ECCE Europe (see end of introduction).

Abstract—Future meshed high-voltage direct current grids require modular multilevel converters with extended functionality. One of the most interesting new submodule topologies is the semi-full-bridge because it enables efficient handling of DC-side short circuits while having reduced power losses compared to an implementation with full-bridge submodules. However, the semi-full-bridge submodule requires the parallel connection of capacitors during normal operation which can cause a high redistribution current in case the voltages of the two submodule capacitors are not equal. The maximum voltage difference and resulting redistribution current have been studied analytically, by means of simulations and in a full-scale standalone submodule laboratory setup. The most critical parameter is the capacitance mismatch between the two capacitors. The experimental results from the full-scale prototype show that the redistribution current peaks at 500 A if the voltage difference is 10 V before paralleling and increases to 2500 A if the difference is 40 V. However, neglecting very unlikely cases, the maximum voltage difference predicted by simulations is not higher than 20–30 V for the considered case. Among other measures, a balancing controller is proposed which reduces the voltage difference safely if a certain maximum value is surpassed. The operating principle of the controller is described in detail and verified experimentally on a down-scaled submodule within a modular multilevel converter prototype. It can be concluded that excessively high redistribution currents can be prevented. Consequently, they are no obstacle for using the semi-full-bridge submodule in future HVDC converters.

Index Terms—AC-DC power conversion, HVDC converters, HVDC transmission, Power transmission, Fault tolerance, Power system faults.

I. INTRODUCTION

THERE is a clear trend towards extremely demanding new applications for power electronic converters like high-voltage direct current (HVDC) grids. Integrated HVDC multiterminal overlay grids may be appearing sooner than expected. The start of the rise of HVDC grids can be seen both in the developments in the German and Chinese networks [1].

Two of the most important components of such future HVDC supergrids are the power converters and DC circuit

breakers [2], [3]. Several new features have to be introduced in order to meet the demands that are imposed by networks of HVDC converters. Those new requirements as well as options for future advanced converters have been summarized in [4]. Reduced power loss is of paramount commercial importance. In addition, electronic failure management, small footprint, and lower semiconductor expenditure will play important roles. However, cost and performance have to be analyzed from a systems point of view in future HVDC grid applications.

During recent years viable candidate technologies for power converters and DC circuit breakers have been proposed. In the case of power converters, the preferred converter is the modular multilevel converter (MMC), first presented by Marquardt et al. [5]–[8], and in the case of DC circuit breakers various hybrid electronic/mechanical concepts have been reviewed in [9]–[11]. Both the converter and the DC circuit breaker are costly and voluminous to such an extent that the introduction of HVDC supergrids may be delayed unless more cost-effective and compact solutions are found. The cost of circuit breakers could be reduced by using power converters that are able to control the DC-side current in the event of a short circuit on the DC-side, because DC circuit breakers may not have to be installed in every single node if such converters are used [12].

Fast protection of the converters and associated equipment must be ensured throughout the whole network. Electronic DC-side current limitation and control by the converter itself, also referred to as *full-bridge functionality* [4], could be a particularly good alternative for meshed transmission systems with overhead lines where the probability of DC line faults is much higher due to lightning strikes or bad weather conditions. A variety of submodule topologies that fulfill this criterion are discussed in [13]. The full-bridge (FB) submodule belongs to this group. However, an MMC employing FB submodules utilizes twice the number of semiconductor switches in comparison to one with half-bridge (HB) submodules. This leads to high conduction losses which represents a severe drawback of the general use of FB submodules. The double-clamp submodules (DCS) [14], on the other hand, offers reduced losses but can only provide DC-side current blocking. It is not capable to control the fault current and, hence, cannot support the AC grid during DC short circuit faults.

In order to balance power loss, semiconductor cost and functionality, mixed cell MMC topologies with both HB and FB submodules have been proposed [15]–[17]. The combined use of these two basic cell types constitutes an improved

Manuscript sent April 3, 2018; revised August 21, 2018; accepted December 17, 2018.

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compromise, though particular attention has to be paid to enable successful voltage balancing at low values of the DC-side voltage. FB MMCs can also be utilized in hybrid configurations where they are combined with line-commutated converters (LCC). These concepts enable the operation of an LCC at leading power angles. A review of several possible topologies is presented in [18].

Regarding the physical volume of the MMC itself, it is found that a major contributor is the submodule capacitance [19]–[22]. The cell capacitors occupy more than half of the submodule volume. One alternative approach to realize submodules with a smaller capacitance is the concept of hybrid voltage source converter (VSC) topologies. Hybrid VSCs mix elements of the classic VSC and the MMC. They have been mainly proposed in order to reduce the converter footprint, which they achieve by requiring fewer submodules with a smaller capacitance. One of the most prominent representatives of this approach is the alternate arm converter (AAC) [23]. Different modes of operation have been presented in [24], [25]. Yet, the research and development phase of the AAC is still ongoing and no commercial application has been reported so far.

It can be noted that the search for new MMC submodule topologies remains important. The goal is to find topologies which enable efficient handling of DC-side short circuits, reduction of power loss, and lower submodule capacitance. The semi-full-bridge (SFB) submodule, presented in [26], is a very interesting topology from this point of view and was identified to be one of the most promising candidates for HVDC grid applications by leading research experts in the field [27]. Based on this, the authors of this paper conclude that the SFB submodule topology and its operation is a relevant topic and should be investigated in detail.

The SFB allows to insert negative voltages in the converter arms. It was shown that the ripple voltage across the submodule capacitor could be reduced by 59% compared to the case when only positive voltages were used [26]. The same negative voltages are also necessary in order to set up a voltage against the AC-side voltage in case of a DC-side short circuit. Moreover, the use of SFB instead of FB submodules reduces the number of components in an MMC, while still providing fault current limitation and bipolar voltage capability. Another interesting feature of this submodule topology is that the two submodule capacitors in the circuit can be connected either in series or in parallel when inserting positive voltages in the arm. In the latter case, the submodule capacitors can share the arm current such that the corresponding voltage deviation across the submodule capacitors is reduced by 50% during a conduction interval [26]. The parallel connection may, however, be problematic in case the two capacitor voltages are not equal. Due to the low impedance of the circuit, an initial voltage imbalance may give rise to excessive redistribution currents and depending on the damping of the circuit subsequent oscillations between the two capacitors may occur. A new HB topology was recently proposed which uses clamping diodes and buffer inductors to keep the submodule capacitor voltages balanced [28]. This topology forms the same balancing loop between two submodules as is the case of the SFB. However, this approach increases the complexity and cost

of the converter.

This paper presents a detailed study of the phenomenon of transient redistribution currents in the SFB and is structured as follows. In Section II, the basic switching operations of the SFB submodule are discussed with focus on the possible capacitor voltage imbalance and an analytical calculation of the redistribution current. A parameter study of the maximum difference in the capacitor voltages is presented in Section III. A balancing controller that limits the divergence of the capacitor voltages and thus the redistribution currents is proposed in Section IV. Two control methods are explained and theoretical analysis is provided in this part of the paper. In Section V, the simulation environment is described. Simulation results of the redistribution current are shown and verified against analytical calculations. Moreover, the new balancing controller is simulated and its impact on the submodule performance is analyzed. Finally, measurement data from two different experimental setups, a full-scale and down-scaled laboratory prototype of the SFB submodule, are presented in Section VI. Finally, a discussion is provided about various options on how a voltage imbalance between the two submodule capacitors can be handled without impairing the operation of the converter.

Note that part of this paper has been published in the Proceedings of the 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, 11-14 Sep., 2017 [29]. However, the parameter study of the maximum difference in the capacitor voltages has been considerably extended and twice as much measurement results are presented in this paper. Moreover, the proposed control mechanism to balance the capacitors, its analysis and experimental verification is entirely new.

II. SEMI-FULL-BRIDGE SUBMODULE

A. Operating Principles

The operation principles of the SFB and its energy fluctuation have been studied in [26]. The SFB can be considered as an extension of the DCS as presented in [14]. The main difference between the DCS and the SFB is that two diodes have been replaced by active switches which changes the function and operating principles of the submodule. A schematic diagram of the SFB is shown in Fig. 1, where i_{arm} denotes the arm current. The proposed SFB submodule contains two capacitors, C_1 and C_2 , which can be bypassed, connected in parallel, or in series. Thus, one SFB replaces two conventional submodules which are equipped with only one capacitor each. For evaluation purposes, the SFB submodule should therefore be compared to two series-connected HB or FB submodules.

Only two out of several possible switching states are relevant for this investigation. They are illustrated in Fig. 2. Switched-off devices are indicated with gray color. Using the parallel states of the SFB, i.e. controlling the submodule in such way that devices S_3 and S_5 are conducting in parallel, offers several benefits compared to the case of operating the bridge legs independently. Firstly, S_3 and S_5 must only be rated for half of the arm current. Thus, in terms of combined power rating of the semiconductors, the seven devices in the SFB correspond to six devices rated for the full arm current. Accordingly, the

Fig. 1: Schematic diagram of the proposed semi-full-bridge submodule.

Fig. 2: Switching states of the SFB submodule [29].

combined power rating of the devices in the SFB is 25% lower compared to a full-bridge submodule, and 50% higher compared to a half-bridge submodule. Secondly, advantages as regards the energy balancing at modulation indices above unity can be achieved. If the parallel states were not used, the operation of the SFB would in most aspects be equivalent to the combination of one half-bridge and one full-bridge submodule. However, such a mixed cell, or hybrid, configuration, is limited in its operating range due to the energy balancing between half-bridge and full-bridge submodules. As regards the SFB, the energy between the two capacitors can be easily balanced by utilizing the negative parallel state at any operating point up to modulation index $M = 3$.

B. Capacitor Voltage Imbalance

It can be assumed that the capacitance values of C_1 and C_2 differ slightly due to manufacturing tolerances. After some

time in operation the capacitance of film capacitors may also have decreased due to aging effects and their self-healing or clearing functionality. At the position of a local defect, a small part of the stored energy punctures the film and evaporates the thin metal layer. Hence, the local defect is disconnected similar to the function of a fuse [30]. Consequently, the two capacitors charge differently when they are inserted in series, although both are subjected to the same arm current. This results in different voltages across C_1 and C_2 which has been analytically derived in [26]. This voltage difference is balanced out when the switching state is changed from series- to parallel-connection of the capacitors. The equivalent circuit valid during the transient is illustrated in Fig. 3. The main elements of this circuit are the two capacitances C_1 and C_2 , the stray inductance L_σ , and the voltage drop due to the IGBT $V_{th,IGBT}$ and diode $V_{th,D}$. Moreover, the circuit contains several resistive elements, i.e. the ON-state resistances of IGBT and diode, the resistance of the busbar system as well as the equivalent series resistance (ESR) of the capacitors. The respective values of the full-scale prototype are listed in Table I. The values for IGBT, diode and busbars have been measured at 400A, while the ESR value is obtained from the datasheet [31].

TABLE I: Resistive elements in the circuit and prototype values.

Parameter	Symbol	Value
IGBT ON-state resistance	R_{IGBT}	3.75 m Ω
Diode ON-state resistance	R_D	2.6 m Ω
Busbar resistance	R_{bus}	1.5 m Ω
Capacitor ESR	ESR_C	< 0.15 m Ω

The resulting resistance can be expressed as

$$R_{res} = 2ESR_C + R_{IGBT} + R_D + R_{bus}. \quad (1)$$

All these elements together form a damped resonant circuit, whereby the damping may vary considerably depending on the circuit design as well as the choice of power semiconductors and capacitors. The redistribution current i_{rd} is superposed on the arm current during the capacitor voltage balancing process. However, the arm current is assumed to be zero in the following analytical study corresponding to the conditions of the performed experiments, see Section VI. Thus, the sum of both currents determines the current direction in S_3 and S_5 and, in consequence, whether IGBT or diode are conducting. Since it is possible to control the SFB in such a way that those devices are always conducting in parallel they could theoretically be rated only for half of the arm current [26].

C. Redistribution Current

In case of a voltage difference between the two capacitors in the SFB submodule there will be a current flowing when the capacitors are connected in parallel. This current redistributes charge from one capacitor to the other such that the two voltages become almost equal after a certain time. The

Fig. 3: Parasitic elements in the current path [29].

analytical calculation of the current is based on the equivalent circuit presented in Fig. 3. It is assumed that the capacitors have different capacitances C_1 and C_2 . Initially, the voltage V_{C2} is higher than the voltage V_{C1} such that shortly after time zero the redistribution current is flowing in the direction indicated in Fig. 3. The analysis of i_{rd} reveals that

$$i_{rd}(t) = \frac{\Delta V_C - V_{th,D} - V_{th,IGBT}}{\sqrt{L_\sigma \left(\frac{1}{C_1} + \frac{1}{C_2} \right) - \frac{R_{res}^2}{4}}} e^{-t/\tau} \sin(\omega t), \quad (2)$$

where ΔV_C is given by the voltage difference between the capacitors

$$\Delta V_C = V_{C2} - V_{C1}, \quad (3)$$

with τ referring to the time constant that is given by

$$\tau = \frac{2L_\sigma}{R_{res}} \quad (4)$$

and with ω describing the angular frequency that is given by

$$\omega = \sqrt{\frac{1}{L_\sigma} \frac{C_1 + C_2}{C_1 C_2} - \frac{1}{4} \left(\frac{R_{res}}{L_\sigma} \right)^2}. \quad (5)$$

The transients in the capacitor voltages can be described as follows

$$v_{C1}(t) = V_0 + \Delta V_C - \frac{\Delta V_C C_2}{C_1 + C_2} \left[1 - e^{-t/\tau} \left(\cos(\omega t) + \frac{1}{\tau \omega} \sin(\omega t) \right) \right] \quad (6)$$

$$v_{C2}(t) = V_0 + \frac{\Delta V_C C_1}{C_1 + C_2} \left[1 - e^{-t/\tau} \left(\cos(\omega t) + \frac{1}{\tau \omega} \sin(\omega t) \right) \right] \quad (7)$$

where V_0 is the nominal capacitor voltage.

It should be noted from (2) that the redistribution current is determined by the voltage difference ΔV_C and not by the absolute voltages V_{C1} and V_{C2} .

III. ANALYSIS OF THE MAXIMUM DIFFERENCE IN CAPACITOR VOLTAGES

An analytical study has been conducted in order to evaluate the influence of various MMC parameters on the maximum differences in the capacitor voltages $\Delta V_{C,max}$ for a realistic SFB submodule in an HVDC application. The impact of the following parameters has been studied: switching frequency, arm current i_{arm} , phase angle ϕ as well as capacitance C and its associated tolerances k . Phase-shifted carrier pulsewidth modulation (PSC-PWM) has been chosen to determine the required switching state of the SFB, i.e. whether it shall be inserted in series, parallel or bypassed. The state which generates negative terminal voltages is not part of this study since this state does not create any voltage imbalance among the two capacitors. Fig. 4 shows an example of a reference arm voltage v_{ref} , arm currents of different phase shifts, and PWM carriers during one fundamental cycle.

How the capacitor voltages would develop in this case is illustrated in Fig. 5. Since a capacitance tolerance of $k = \pm 10\%$ has been assumed in this example, the capacitor voltages diverge during their series connection, highlighted in gray, and are balanced out as soon as they are connected in parallel. It becomes clear that the longer the capacitors are connected in series the greater will be the resulting voltage difference, provided that the current is not changing direction during that time. Consequently, the voltage difference is inversely related to the carrier frequency. It can also be seen that the series connection of the capacitors coincides with low arm currents for active power transfer which reduces $\Delta V_{C,max}$. $\Delta V_{C,max}$ will be larger for increased load angles since the arm current is then higher during series connection.

Fig. 6 presents the results of a parameter study for $\Delta V_{C,max}$. A reference case has been assumed, where the peak arm current $\hat{I}_{arm} = 900A$, $\phi = 0^\circ$, $C = 4mF$ and $k = \pm 5\%$. A variation of the parameters ϕ , k , $\hat{I}_{arm}$, and C is presented in the

Fig. 4: Reference arm voltage and currents [29].

Fig. 5: Capacitor voltages during one fundamental cycle [29].

subplots as a function of the switching frequency. The other parameters are unchanged according to the reference case. The insets show a zoom to low switching frequencies as they are the most relevant for MMC applications.

All plots of Fig. 6 confirm the mentioned inverse relationship between $\Delta V_{C,\max}$ and the switching frequency. It is also shown that the spread in $\Delta V_{C,\max}$ is greatest for low switching frequencies and that it converges to a small value for high switching frequencies. Fig. 6a illustrates that the phase angle has a minor impact, in particular for small values of ϕ , whereas the capacitance tolerance k is critical concerning the amount of $\Delta V_{C,\max}$ as shown in Fig. 6b. However, the (dotted) case where the capacitance of one capacitor is 10% above its nominal value and the capacitance of the other capacitor is 10% below its nominal value is highly unlikely. It can instead be reasonably assumed that the capacitances of a batch of new capacitors have similar values which are probably slightly above their rated values. The influence of the arm current $\hat{I}_{\text{arm}}$ is shown in Fig. 6c. It can be seen that $\Delta V_{C,\max}$ increases with increased arm current. Finally, Fig. 6d illustrates the impact of the capacitance C on $\Delta V_{C,\max}$. It can be seen that the smaller the capacitance, the greater the difference between the two capacitor voltages.

Fig. 6 shows that, except for the extreme case of $k = \pm 10\%$, $\Delta V_{C,\max}$ is lower than 30V for switching frequencies greater than 100Hz and lower than 20V for switching frequencies greater than 150Hz. Immediately after parallelization of the capacitors, ΔV_C will translate into a certain peak value of the redistribution current. This peak value can be calculated with (2) provided that the circuit parameters are known, and should be kept within the safe operating area (SOA) of the employed semiconductor devices.

A mathematical expression for the voltage imbalance between the two capacitors ΔV_C has been recently presented in [32]. As discussed there, this voltage difference can be expressed as

(a) Phase angle ϕ

(b) Capacitance tolerance k

(c) Arm current $\hat{I}_{\text{arm}}$

(d) Capacitance C

Fig. 6: Parameter study of the maximum difference in the capacitor voltages.

$$\frac{\Delta V_C}{V_0} = \frac{T_Q 2(1 + m \frac{\sqrt{3}}{2})(1 + \delta)}{m \tau} \left(\frac{2k}{1 - k^2} \right). \quad (8)$$

Equation (8) takes the arm current, carrier frequency, phase angle, capacitance values, and capacitance tolerances into account. T_Q describes the charge transferred to the capacitors during the series-connected switching state which is expressed as coulombs per ampere alternating current. T_Q is a function of the modulation index, carrier frequency, and power angle and has to be pre-calculated numerically. According to (8), the voltage difference ΔV_C is proportional to the nominal submodule voltage V_0 and inversely proportional to the normalized energy storage τ .

IV. BALANCING CONTROLLER

In this section, two control methods for limiting the redistribution currents in the SFB submodule to an uncritical level are presented. In general, this can be achieved by balancing the capacitor voltages before their difference exceeds a certain threshold voltage. The proposed control methods allow such a voltage balancing, while preventing the parallel connection of the two capacitors. The fundamental principle of both control methods is that only one capacitor is inserted, allowing the arm current to either discharge the capacitor with higher voltage or charge the one with lower voltage.

The first method makes use of an inherent self-balancing mechanism of the SFB submodule and is described in Section IV-A. The advantage of this method is that the submodule changes automatically into the parallel state as soon as the balancing process is completed. It is, so to say, a passive method since the controller does not need to be actively deactivated. However, this method requires the arm current to be negative. Hence, it is particularly suitable for a converter operating in inverter mode, i.e. when the peak value of the arm voltage coincides with the negative peak value of the arm current. This operation mode corresponds to converter operation with active power transfer. In this case, the switching state when both capacitors are inserted in series and might diverge, that is close to the peak of the arm voltage, coincides with negative arm current values.

The second method, on the other hand, enables the capacitor voltage balancing also for positive arm currents. However, it requires an active change of switching states after the balancing has been accomplished. For that reason, this control method is called “active balancing control”. Further information is provided in Section IV-B.

The duration of the balancing process depends among other things on the magnitude of the current at the instant when this process is activated. Analytical calculations of the balancing time are derived in Section IV-C.

A. Self-Balancing Control

The self-balancing control method ensures to temporarily turn off S_4 during the series-connected switching state, provided that the arm current is negative. Thus, the arm current is redirected either through the diode of S_3 or S_5 depending

on which one is forward-biased by the capacitor voltage difference. Fig. 7 shows the equivalent circuit for the self-balancing mechanism.

Fig. 7: Equivalent circuit for self-balancing mechanism.

The two possible current paths, depending on which capacitor has a higher voltage, are illustrated in red colour in Fig. 8. Fig. 8a illustrates the case when the voltage of capacitor C_2 is greater than that of C_1 . The opposite situation is shown in Fig. 8b. Only one capacitor is inserted in either case. It should be noted that the capacitor with the higher voltage gets inserted by switching off S_4 and that this capacitor gets discharged due to the negative arm current. As soon as the voltages are equal, both diodes conduct and the switching state changes safely to the parallel state without redistribution current.

An illustration of the voltages and currents during the self-balancing mechanism is given in Fig. 9. In this case, the capacitance of C_1 has been chosen lower than the capacitance

(a) Current path for $V_{C1} < V_{C2}$. Discharge V_{C2} .

(b) Current path for $V_{C1} > V_{C2}$. Discharge V_{C1} .

Fig. 8: Current path during self-balancing control, $i_{arm} < 0$.

(a) Difference in capacitor voltages.

(b) Currents through the SFB submodule.

Fig. 9: Exemplary illustration of the self-balancing mechanism.

of C_2 , which means that during series connection C_1 discharges faster due to the negative arm current. Both capacitor voltages as well as their difference are shown in Fig. 9a. The currents flowing through the semiconductors of interest are shown in Fig. 9b. In this example, the controller is activated after 5 ms, when the voltage difference exceeds the defined threshold voltage. It can be seen that the current gets redirected from the IGBT of S_4 to the diode of S_3 , because S_4 is turned off. According to Fig. 8a, only C_2 is inserted, which discharges due to the negative arm current. It can be observed that when the controller is activated the difference in the capacitor voltages drops to zero. Simulation results and an analysis of the impact of the self-balancing control method on the harmonic performance of an SFB submodule is presented in Section V.

B. Active Balancing Control

This control method should be applied if the arm current is positive. In contrast to the self-balancing control method, the switching state has to be actively changed by switching either the left or right half-bridge of the SFB submodule. The active balancing method ensures to only insert the capacitor with lower voltage in order to charge it to the same level as the second capacitor, see Fig. 10. As soon as the two voltages are equal, the switching state of the submodule can be either changed back to series-connected or to parallel inserted state which would not cause a redistribution current since the voltages are balanced. As mentioned above, the duration of the balancing process can be calculated analytically and is derived in the following section.

In principle, it is possible to operate the SFB without using the positive and negative parallel states. The bridge legs of the submodule can be controlled separately. However, it should be noted that a path for the redistribution current might be created when inserting a single capacitor with negative polarity (via the switches that are in ON-state and the free-wheeling diodes). Without using the positive parallel state, there might be a voltage imbalance between the two capacitors when a transition from the bypass state to the negative state is required. Furthermore, the advantages of the parallel states, which are described in Section II-A, would be lost if the bridge legs operate independently without a parallel connection of the capacitors.

(a) Current path for $V_{C1} < V_{C2}$. Charge V_{C1} .

(b) Current path for $V_{C1} > V_{C2}$. Charge V_{C2} .

Fig. 10: Current path during active balancing control, $i_{arm} > 0$.

C. Balancing Time

The starting point for the calculation of the balancing time is the expression for the capacitor voltage v_C when subjected to the current i_{arm} , i.e.

$$v_C(t) = \frac{1}{C} \int i_{\text{arm}} dt + v_C(t_0), \quad (9)$$

where C is the capacitance and $v_C(t_0)$ is the initial voltage.

Using $i_{\text{arm}} = i_{\text{dc}} + \frac{\hat{i}_s}{2} \cos(\omega t - \varphi)$ yields

$$v_C(t) = \frac{1}{C} \int \left(i_{\text{dc}} + \frac{\hat{i}_s}{2} \cos(\omega t - \varphi) \right) dt + v_C(t_0), \quad (10)$$

where i_{dc} is a third of the dc-side current for the three-phase inverter case. The controller gets activated at time $t = t_0$ and the balancing process shall be finished at $t = t_{\text{end}}$. Solving the integral in (10) for these limits yields

$$C (v_C(t_{\text{end}}) - v_C(t_0)) = i_{\text{dc}} (t_{\text{end}} - t_0) + \frac{\hat{i}_s}{2\omega} (\sin(\omega t_{\text{end}} - \varphi) - \sin(\omega t_0 - \varphi)). \quad (11)$$

Equation (11) can be solved numerically for the balancing time, $t_{\text{bal}} = t_{\text{end}} - t_0$. An analytical expression can be found by applying the first-order Taylor polynomial of $\sin(\omega t - \varphi)$, which gives a linear approximation around the starting point $t = t_0$.

$$t_{\text{bal}} = \frac{C \Delta V_{C,\text{max}}}{i_{\text{dc}} + \frac{\hat{i}_s}{2} \cos(\omega t_0 - \varphi)}. \quad (12)$$

$\Delta V_{C,\text{max}}$ is the voltage difference before the balancing process starts which corresponds to the maximum allowed voltage difference. It can be observed that the denominator of (12) is the arm current value at the starting time of the controller. A more accurate expression for the balancing time can be found by applying the second-order Taylor polynomial for $\sin(\omega t - \varphi)$ around $t = t_0$. We obtain t_{bal} by solving the resulting quadratic equation. That is

$$t_{\text{bal}} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}, \quad (13)$$

with the coefficients a, b, c given by

$$a = \frac{\hat{i}_s}{4} \omega \sin(\omega t_0 - \varphi), \quad (14a)$$

$$b = - \left(i_{\text{dc}} + \frac{\hat{i}_s}{2} \cos(\omega t_0 - \varphi) \right), \quad (14b)$$

$$c = C \Delta V_{C,\text{max}}. \quad (14c)$$

V. SIMULATION RESULTS

A. Uncontrolled Balancing Process of the Capacitor Voltages

The characteristics of the redistribution current in the SFB submodule are validated by simulations in LTspice®. The equivalent circuit is shown in Fig. 11, where the current path and its direction are indicated in red color.

Fig. 11: Current path during the redistribution transient [29].

Ideal components are chosen and a voltage difference of 40V is assumed. A first assessment of the overall resistance R_{res} in the current path has been calculated based on measurements of the static characteristics of the semiconductor devices and copper busbars that are used in the experimental setup, see Section VI. The results show that the ON-state resistances of the IGBT modules, R_{IGBT} and R_{D} , follow the 125°C characteristic given in their datasheet [33], and thus have a significant contribution to the overall resistance, whereas the measured resistance of the busbar system R_{bus} is comparably small. The values used for R_{res} and the stray inductance L_{σ} have been obtained from a curve fit of the current measurement data in MATLAB based on (2). The fitted parameters for the simulation with LTspice® are listed in Table II together with other specifications of the simulated circuit.

TABLE II: Simulation parameters.

Parameter	Symbol	Value
Voltage difference	ΔV_C	40V
Submodule capacitance	C	4mF
Stray inductance	L_{σ}	230nH
Equivalent resistance	R_{res}	7.85mΩ
Simulation time step	Δt	1μs

Fig. 12 shows how the simulated redistribution current compares to the measurement. The inductance value of 230nH coincides with calculations that have been performed on the basis of measurements at a high-power IGBT module [34] and according to [35]. Moreover, the resulting resistance of 7.85mΩ shows a good agreement with the measured value.

From the measured current waveform shown in Fig. 12 it can be seen that the circuit is lower damped than critical. With the parameters given in Table II, the damping factor ζ can be calculated by

Fig. 12: Measurement data (blue) and simulation result (red) of the redistribution current [29].

$$\zeta = \frac{R_{\text{res}}}{2} \sqrt{\frac{C/2}{L_{\sigma}}} \quad (15)$$

In this case it occurs that $\zeta = 0.37$, which confirms that this is an underdamped system.

Fig. 13 illustrates the charge balancing process between the two capacitors. Their voltages converge after 0.3ms in the analytical calculation based on (2) but do not converge in the simulation. LTspice® takes the forward voltage drop of the semiconductor devices into account which is neglected in the analytical calculations. The oscillation stops as soon as the remaining voltage difference is less than the combined forward voltage drop over IGBT and diode.

B. MMC Test System and Balancing Controller

The functionality of the SFB as well as the proposed balancing controller are validated by simulating a three-phase MMC in the software PSCAD/EMTDC. The MMC is equipped with five SFB submodules per arm and is feeding a passive load. The parameters of the test case are summarized in Table III.

In the simulation, PSC-PWM is employed with four carriers to account for all available voltage levels. The internal arm-balancing control, including circulating-current and voltage control, is implemented based on [36]. Fig. 14 shows the intended effect of the balancing controller. It can be seen that the capacitor voltages are limited to a specified critical value $\Delta V_{C,\text{max}}$. The self-balancing mechanism is triggered whenever the voltage difference reaches the threshold level.

It is worth noting that the number of balancing actions should be minimized because only one voltage level is inserted for a short time instead of two and additional switching losses are introduced. A conservative analysis of the balancing

Fig. 13: Analytical calculation (solid) and simulation result (dashed) of the two capacitor voltages [29].

TABLE III: Parameters of simulation test case.

Parameter	Symbol	Value
Converter power	S	18MVA
DC-side voltage (pole-pole)	V_{dc}	30kV
Modulation index	M	0.9
Fundamental frequency	f_0	50Hz
Carrier frequency	f_c	80Hz
Submodules per arm	N_{sub}	5
Capacitors per arm	N_{cap}	10
Submodule capacitance	C	4mF
Passive load	R_{load}	11Ω
Simulation time step	Δt	1μs

control algorithm was conducted on submodule level. For this purpose, the capacitance values of the two capacitors in one converter submodule were changed by $\pm 10\%$ ($C_1 = 3.6\text{mF}$, $C_2 = 4.4\text{mF}$). Furthermore, in order to avoid averaging effects, only five fundamental cycles were analyzed because the switching pattern repeats after that time. The analysis includes an evaluation of the number of balancing switchings, the average switching frequency per device f_{avg} , and the maximum arm current prior a balancing action $|\hat{i}_{\text{arm,balance}}|$. These arm current values are of interest because the redistribution current superposes the normal load current and the IGBT modules have to withstand the sum of both. The results for various cases of maximum allowed capacitor voltage difference $\Delta V_{C,\text{max}}$ are presented in Table IV.

TABLE IV: Analysis of balancing controller ($T = 0.1\text{s}$, $k = \pm 10\%$).

$\Delta V_{C,\text{max}}$	10 V	20 V	30 V	40 V
No. balancing switchings	22	13	6	2
f_{avg} [Hz]	257	241	236	229
$ \hat{i}_{\text{arm,balance}} $ [A]	372	376	366	306

Fig. 14: Simulation results of the balancing controller for different levels of $\Delta V_{C,\max}$.

The number of control actions increase with a more stringent limit for the voltage difference. Accordingly, the average switching frequency is higher for these cases as well. Moreover, a fast Fourier transform (FFT) analysis of the terminal voltage of the respective SFB submodule was conducted, whereby the impact of the balancing controller on arm and converter level was not considered explicitly. The FFT analysis was not only conducted for the described capacitance difference of $\pm 10\%$, but also for the more realistic case of $\pm 5\%$. The results are plotted in Fig. 15 which illustrates the deviation of the voltage spectra for two different values of $\Delta V_{C,\max}$ from a reference spectrum without applied balancing control.

The magnitudes of the harmonic components differ considerably. A capacitance difference of $\pm 10\%$ results in a relatively large number of balancing actions as stated in Table IV because the voltage difference can be up to 60V, cf. Fig. 6b. It can be observed in Fig. 15a that the DC components and the fundamental components are reduced in this case. This effect is explained by the fact that less voltage is inserted than demanded by the voltage controller. Any deviations from the demanded voltage can be compensated in the modulator by increasing the reference value of the inserted arm voltage by a value corresponding to one capacitor voltage. A fast response from the modulator can be reasonably expected so that it is likely that the activated balancing control has only a negligible effect on the transient performance of the MMC. A compensation in the modulator was, however, not implemented in these simulations. Any remaining error in the DC component of the inserted voltage will eventually be taken care of by the circulating-current controller which adjusts the insertion indices of the arms [37]. An error in the fundamental component will be visible in the AC output voltage. The AC output current controller takes care of this error and also adjusts the insertion indices accordingly [36]. In addition, it can be seen in Fig. 15a that the second- and third-order harmonic components are increased due to the additional switching actions. The rest of the spectrum is randomly affected by the control mechanism,

(a) Capacitance difference of $\pm 10\%$ ($C_1 = 3.6\text{mF}$, $C_2 = 4.4\text{mF}$).

(b) Capacitance difference of $\pm 5\%$ ($C_1 = 3.8\text{mF}$, $C_2 = 4.2\text{mF}$).

Fig. 15: Deviation of voltage spectra with balancing controller from reference case without balancing controller.

whereas the largest deviations appear at subharmonics that constitute multiples of the carrier frequency and their related sidebands. It is an important finding of this analysis that the impact of the balancing controller is almost negligible if the capacitance difference is $\pm 5\%$, see Fig. 15b. The reason is that the amount of balancing switchings is very small. Fig. 6b shows that the difference in capacitor voltage is at most 30V for this case. By comparing the black and orange bars in Fig. 15 it can be further concluded that the discussed deviations of the harmonics are significantly reduced if the parameter $\Delta V_{C,\max}$ of the proposed balancing controller is increased. Due to the fact that the deviations in the FFT spectrum are very small for the case with a capacitance difference of $\pm 5\%$ and these deviations can be compensated for with the modulator it was chosen to not further elaborate on the FFT spectra of the alternating voltage.

The influence of the balancing controller on the output ac voltage and current waveforms has been analysed and is shown in Fig. 16. The simulation model has been modified in order to account for the realistic scenario of a capacitance mismatch in more than one submodule per arm. Two different cases have been simulated. In the first case, the five submodules per arm have $\pm 10\%$, $\pm 8\%$, $\pm 6\%$, $\pm 4\%$, $\pm 2\%$ difference, respectively, and in the second case they have $\pm 5\%$, $\pm 4\%$, $\pm 3\%$, $\pm 2\%$, $\pm 1\%$, respectively. The capacitor

Fig. 16: Influence of balancing controller on output ac voltage and current for $k = \pm 10, \dots, 2\%$ (dashed, orange) and $k = \pm 5, \dots, 1\%$ (dash-dotted, green).

voltage difference is strictly limited to $\Delta V_{C,\max} = 20V$ in both cases. The balancing actions triggered in the first case induce a slight deviation in the output waveforms, whereas there is no difference visible for the second case with lower capacitance difference.

The insertion indices of the five submodules, n_{1-5} , are adjusted by the implemented control scheme. They are shown in Fig. 17 for the reference case with equal capacitances, i.e. no controller activation, and for the case where the submodules have up to $\pm 10\%$ capacitance difference. It can be seen that the insertion indices are adjusted around the peak of the modulation reference, which is reasonable since the self-balancing control gets activated during the series-connection of the capacitors when the highest arm voltage is required. The insertion indices are generally increased to compensate for the lower than requested voltage that is inserted by some of the submodules in consequence of the control actions.

In summary, if there is a major mismatch between the capacitances of the two capacitors in one submodule ($k = \pm 10\%$), care should be taken that the voltage limit is not selected too stringent. It has been shown that the number of balancing actions and, hence, the deviation in the FFT spectrum can be significantly reduced by choosing a higher threshold voltage. However, a major mismatch between the capacitances might occur only after several years of operation and can be easily avoided with a capacitance monitoring scheme. The impact of the balancing controller on the output waveforms is small, even for a major capacitance mismatch in several submodules per arm and no compensation in the modulator. If the difference is $\pm 5\%$ or lower, the impact is negligible. Therefore, it can be concluded that the proposed balancing controller is a promising method to keep the capacitor voltage difference in the SFB below a defined limit. This means that the redistribution currents can be controlled to an uncritical level, which is also experimentally verified in Section VI-B.

Fig. 17: Insertion indices of arm submodules with equal capacitances (solid, black) and unequal capacitances (dashed, orange).

VI. EXPERIMENTAL RESULTS

A. Full-scale Submodule Prototype

The described phenomenon of transient redistribution currents due to a voltage imbalance between the two capacitors of the SFB has been investigated experimentally on a full-scale prototype. A drawing of the setup is shown in Fig. 18a and a photograph of the realized implementation is presented in Fig. 18b.

The SFB submodule has been equipped with five 3300V/1200A (MBN1200E33E) and two 3300V/800A (MBN800E33E) IGBT modules, both types manufactured by HITACHI. However, for the tests conducted for this publication only two of the lower rated IGBT modules are needed. The two capacitors, manufactured by VISHAY, have a rated direct voltage of 2650V and a nominal capacitance of 4mF with a tolerance of $\pm 5\%$ as stated in the datasheet [31].

Fig. 19 shows the results of the current and voltage measurement. An important finding is that the circuit is highly damped and the oscillations cease quickly. The peak of the current-spike scales with the amount of voltage difference between the two submodule capacitors and varies between 500A if $\Delta V_C = 10V$ and 2500A if $\Delta V_C = 40V$. The peak current values measured in the 30V and 40V experiment exceed the repetitive peak collector current rating of the used 3300V/800A IGBT module, which is 1600A according to the datasheet [33]. One should bear in mind that the IGBT modules have to withstand the sum of redistribution current and normal load current, whereas the load current is not included in the experiments. Thus, in order to calculate the total current through the devices S_3 and S_5 , the load current before paralleling the capacitors has to be added as an offset to the redistribution currents that are shown in Fig. 19a. The maximum load current that adds to the redistribution current has been quantified for the presented simulation case in Table IV of Section V.

(a) CAD drawing of the SFB submodule.

(b) Photograph of the laboratory prototype.

Fig. 18: Experimental setup of the full-scale prototype of the SFB submodule [29].

B. Down-Scaled Submodule Prototype

The proposed balancing control technique is implemented on a down-scaled MMC prototype with FB submodules to verify its functionality experimentally. It is worth remembering that the purpose of the balancing controller is the reduction of the redistribution current, while limiting the capacitor voltage difference is a means of achieving this. An SFB submodule is formed by reconnecting two FB submodules that have been customized with different capacitance values in order to cause voltage imbalance. The original switching signals generated for the two FB submodules are re-mapped in order to operate the SFB submodule properly. Finally, the balancing controller is implemented in the MMC control structure and tested. Before discussing the details of the SFB balancing controller experiments, the structure of the current MMC prototype is described briefly. The prototype used in the experiment employs a total of 30 FB submodules, i.e. five submodules per arm. The converter submodules are implemented on printed

(a) Redistribution currents.

(b) Capacitor voltages.

Fig. 19: Measurement results for various voltage differences ΔV_c between the two capacitors.

circuit boards (PCBs), which are inserted in the subracks and connected to a backplane, which provides the submodules with auxiliary power supply and control signals. The structure of the experimental setup together with a photograph is shown in Fig. 20.

The down-scaled MMC prototype has a rated power of 10 kW and its control system is based on Xilinx Zynq-7000 system-on-chip, which integrates a programmable logic with a processing system. The programmable logic performs low-

Fig. 20: Structure and photograph of the MMC prototype.

level control, i.e. modulation and communication with the submodules. The implemented modulation scheme is PSC-PWM, which ensures the balancing of the individual capacitor voltages within the arm [37]. The prototype is operated in inverter mode (dc-ac conversion) with a symmetrical three-phase resistive load. A detailed description of the down-scaled MMC prototype is presented in [38]. The experiment is designed as follows. The MMC prototype is adapted to this study by reconnecting two FB submodules to one SFB submodule, while operating the rest of the converter with FB submodules. The arm that contains the two reconnected FB submodules is illustrated in Fig. 21.

The schematic diagram of the SFB configuration as it is used in the experiments along with measurement points is shown in Fig. 22. The implemented PSC-PWM modulation scheme has been adapted for the SFB submodule. The PWM scheme provides switching signals to the four HB legs of the two FB submodules which are configured to one SFB, see Fig. 22. Those PWM signals are re-mapped in order to insert the corresponding output voltage according to

$$V_{SFB} = V_{FB1} + V_{FB2}. \quad (16)$$

Finally, the desired V_{SFB} is implemented ensuring that only viable switching states of the SFB submodule are used. The re-mapping algorithm is designed as described in Table V, where '0' stands for lower switch ON, '1' stands for higher switch ON, and 'X' stands for disabled bridge.

TABLE V: Signal re-mapping.

SFB output voltage V_{SFB}	FB ₁		FB ₂	
	HB ₁	HB ₂	HB ₁	HB ₂
$-V_C$	0	1	0	1
0	0	0	1	1
V_C	1	1	0	0
$2V_C$	1	0	X	0

(a) Schematic of reconnected phase arm.

(b) Description of power connectors (left) and photograph of reconnected phase arm (right).

Fig. 21: Configuration of one phase arm for the SFB balancing controller experiment.

Fig. 22: Schematic diagram of the SFB configuration. Points of voltage and current measurements are illustrated.

Furthermore, one of the FB submodules forming the SFB has been customized by removing three out of the ten electrolytic capacitors that are mounted on each PCB. In this way, a capacitance difference between the two capacitors of the SFB is achieved, which is a necessary precondition for a voltage imbalance between them. Fig. 23 shows a photograph of the customized PCB of FB₁ with three removed capacitors. Table VI lists important parameters for the SFB balancing controller experiment.

The carrier frequency is comparatively high, but it has not been feasible to change it without any major adjustments and adaptation efforts in the implemented MMC control structure. A high carrier frequency, respectively a high switching frequency, has implications on the duration of the switching

TABLE VI: MMC parameters - Balancing controller experiment.

Parameter	Symbol	Value
DC-side voltage (pole-pole)	V_{dc}	100 V
AC-side voltage amplitude	$\hat{v}_s$	49.5 V
Fundamental frequency	f_0	50 Hz
Arm inductance	L_{arm}	5.7 mH
Arm resistance	R_{arm}	0.55 Ω
Resistive load	R_{load}	7.35 Ω
Submodules per arm	N	5
Modulation index	M	0.99
Carrier frequency	f_c	763 Hz
FB capacitance	C	2.7 mF
SFB capacitance	C_1	1.9 mF
SFB capacitance	C_2	2.7 mF
Maximum capacitor voltage difference	$\Delta V_{C,max}$	0.2 V, 0.4 V

states and hence the maximum capacitor voltage difference as discussed in Section III. Simulations of the MMC prototype with the given parameter set in MATLAB/Simulink reveal that the maximum time of series connection is approximately 400 μ s and the maximum voltage difference is low (< 1 V) despite the relatively large difference in capacitance. In a real converter the relative capacitance difference would be much lower, but in the presented fast switching MMC prototype a higher difference for the capacitance is needed to create the investigated effect. Moreover, it could be observed in this experiment that due to the given modulation scheme, the voltage drifting phenomenon results from a cumulative drifting effect caused by the fast transition of parallel and series states, where the capacitor voltages diverge during the series state and converge during the parallel state. However, this does not imply any restrictions on the verification of the proposed control method, since its effectiveness can be observed in the measured redistribution currents, or in the low-pass filtered voltage difference, where the high-frequency switching operations are neglected. Since the MMC prototype operates in inverter mode, the self-balancing control method of the proposed balancing controller is applied, see Section IV-A. The control mechanism activates when three conditions are met: 1) the SFB operates in series-connected switching state; 2) the arm current is negative; 3) the capacitor voltage difference is higher than a specified threshold value, which is set to 0.2 V

Fig. 23: PCB with reduced capacitance. FB₁ of SFB submodule.

or 0.4 V. Experimental results for the relevant time interval when the switching states alternate between series and parallel insertion of the capacitors are presented in Fig. 24 for the case without control and for two different voltage thresholds. For the uncontrolled case shown in Fig. 24a, it can be observed that the current spikes coincide with a change to the parallel state. They are also more pronounced the higher the voltage difference and arm current magnitude are at the time of that change. Due to the fast transition between parallel and series states, the capacitor voltages do not converge after a single parallel state, but after several parallel states in a cumulative manner. This is why small dips are visible in the plot of the capacitor voltage difference. For the two cases applying the self-balancing control method, shown in Fig. 24b and Fig. 24c, a reduced capacitor voltage difference and lower redistribution current spikes can be observed. The spikes cannot be prevented entirely since the capacitor voltages do not balance completely. A reason for this is that the switching pattern forces the parallel state regularly (even if only for a small amount of time) so that condition 1) is not fulfilled anymore.

Fig. 25 shows the result of the redistribution current measured over a time period of 0.5 s. It can be seen that the controller significantly reduces the peak current, which verifies its functionality. The tops and bottoms of each box are the 25th and 75th percentiles of the measurement data, respectively. The line in the middle of each box is the median.

DISCUSSION

This section discusses how a voltage imbalance between the two submodule capacitors should be handled in case the submodule receives the control command to deliver one positive voltage level, i.e. the capacitors should be inserted in parallel. In the first, and probably simplest case, the voltage imbalance can be disregarded because the total current, i.e. half of the arm current plus the redistribution current, is less than the maximum allowable current. However, in case the predicted current is too high there are several possible options. The first option would be to include this case in the sorting algorithm. That is, if the voltage difference in one module exceeds a certain threshold this module is prioritized the next time one module should be bypassed. A second option could be to insert only one of the capacitors until the two capacitor voltages are equal and then connect the other one in parallel. As a third option, the proposed control mechanism can be applied to balance the capacitor voltages. It should be noted that with the second and third approach it has to be ensured that the maximum current is lower than the rated current of the devices S_3 and S_5 . Another option could be to refrain from inserting the submodule until the expected current is within the SOA. This could, however, put serious restrictions on the converter modulation, and must therefore be considered as a last option.

The analytical parameter study revealed that the voltage difference only becomes critical when a high value of capacitance tolerance ($k = \pm 10\%$) is assumed. It is, therefore, recommended to minimize a potential mismatch between the

Fig. 24: Measurements of internal submodule current and capacitor voltage difference, control signal, and switching state.

Fig. 25: Normalized peak redistribution current measured over a period of 0.5 s.

two capacitances of one submodule. Since the capacitance is usually measured and documented by the manufacturer, the capacitors could be grouped in pairs in order to minimize the difference from the very beginning. Moreover, an online monitoring system for the capacitances could be implemented. A potential difference between the two capacitors of one submodule, which might occur after several years of operation, would then be noticed by such a system. Consequently, the capacitor with higher capacitance can be given priority to be

inserted as the only capacitor. The resulting higher temperature accelerates ageing processes and thus reduces the capacitance [39]. As soon as the capacitances are back within a specific tolerance range, the capacitors are inserted in parallel again.

By ensuring that the two capacitors of a submodule have almost the same capacitance initially and by monitoring the capacitance over time along with the proposed balancing controller, the remaining additional current stress on the power semiconductor devices will be negligible. Consequently, the impact on the reliability of the power semiconductors can be disregarded. Therefore, a separate reliability analysis of this issue can be avoided.

CONCLUSION

The SFB is a promising submodule topology for future MMCs operating in meshed HVDC grids, yet it requires the parallel connection of capacitors during normal operation. This paralleling can cause high redistribution currents in case the capacitor voltages are not equal. The analytical parameter study of the maximum differences in the capacitor voltages shows that the switching frequency and capacitance tolerance are the most important parameters. The study indicates that the maximum voltage difference can be expected to be 20-30V for switching frequencies in the range of 100-150Hz. The quantification of the redistribution current as well as the identification of the circuit parameters of a realistic SFB implementation have been accomplished on a full-scale prototype. It could be demonstrated that the redistribution current peaks at critical levels if the voltage difference is greater than 20V

before paralleling. The circuit parameters can be used in the analytical expression such that peak value and frequency of the redistribution current can be determined from measurements of the capacitor voltage difference.

A new balancing controller is proposed to reduce the redistribution current. This control mechanism is verified by simulations of an MMC implemented with SFB submodules and experimentally on a down-scaled MMC prototype. The results demonstrate that the proposed controller is able to handle the voltage imbalance and limit the redistribution current without impairing the overall operation of the converter.

In summary, the impact of the capacitor voltage imbalance on the operation of the SFB submodule is identified and several options for an improved operation are presented. Based on this knowledge the submodule controller or the high-level control can decide on how to handle the voltage imbalance. It can be concluded that excessively high redistribution currents can be prevented by implementing proper control strategies and that those are therefore not an obstacle for using the SFB submodule in future HVDC converters.

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