Design of a Distributed Signal Processing Unit for Transmission Line Protection in a Centralized Substation Protection Architecture

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Abstract—Travelling-wave and time-domain-based protection functions provide significant response time improvements over conventional phasor-based protection functions in power systems. These types of protection functions require very high sampling rates in the order of several hundreds of kHz. This paper proposes a novel centralized substation protection architecture (CPC) based on distributed signal processing units (DSPU) that enables the deployment of these high sampling rate applications in digital substations utilizing an Ethernet-based process-level network. The design of the DSPU is elaborated, and its signal processing algorithms are discussed. Moreover, the performance of the DSPU is analysed through dynamic tests and verified through a numerical electromagnetic transient simulation.

Index Terms—Digital signal processing, Distributed processing, Edge computing, Power system protection, Power system transients, Substation protection, Systems architecture

Nomenclature

$x(t)$	Continuous-time function, $t \in \mathbb{R}$.
$x[n]$	Discrete-time quantized sequence, $n \in \mathbb{Z}$.
$x_{d_i}[n_{d_i}]$	Downsampled sequence by a factor d_i.
d_i	Downsampling factor at i^{th} decimation stage.
n_{d_i}	Sample index after i^{th} decimation stage.
F_N	Nyquist frequency of the signal $x(t)$.
f_{N,d_i}	Nyquist frequency of the signal $x_{d_i}[n_{d_i}]$.
F_S	Sampling frequency of ADC.
f_{s,d_i}	Digital sampling rate after i^{th} decimation stage.
M_i	Number of taps of the ith FIR lowpass filter.
$f_{p,i}$	Passband edge of the ith FIR lowpass filter.
$f_{st,i}$	Stopband edge of the ith FIR lowpass filter.
$\delta_{p,i} \, / \, \delta_{st,i}$	Ratio of passband to stopband error.
τ_i	Group delay of the ith FIR lowpass filter.
$e_{k,i}$	Magnitude error of kth harmonic at i^{th} FIR
$X_{d_i}^{nc}[m;k]$	Not-compensated k^{th} spectral component.
$X_{d_i}[m;k]$	Compensated spectral k^{th} component.
m	Indicates the latest sample of STFT window.
$f_{k,m}$	Estimated frequency of kth component.
$L_{H,m}$	Window length of discrete STFT.
$B_{H,m}$	Overlap of discrete STFT window.
P_H	Cycle time of harmonic module.
$t_{H,m}$	Timestamp of synchronised phasors.

I. Introduction

Digital signal processing (DSP) plays a vital role in power system protection for extracting different features of the voltage and current signals such as the fundamental phasor components, RMS values or the 2nd to 5th harmonic components. The importance of DSP in protection systems will increase due to power system phenomena such as increased magnitudes of harmonics and interharmonics [1], in particular subharmonics, as well as reduced system inertia and reduced short circuit ratio (SCR) [2]. These phenomena are mainly caused by an increasing number of inverter-connected generation and other non-linear loads. Travelling waves along transmission lines are fault induced signals and therefore provide a promising solution for protection systems in low SCR power systems. In [3] a transient based protection scheme is tested based on a sampling rate of 80 samples per cycle as suggested in IEC 61850-9-2LE. Nevertheless, higher sampling rates are required for travelling-wave based differential protection schemes. In [4] a sampling rate of $1\,\text{MHz}$ is proposed. These high sampling rates impose particular challenges for digital substations utilising an Ethernet-based process-level network and having a high degree of functional integration on a single platform consisting of computing hardware and execution environment. This type of architecture is referred to as centralized substation protection and control (CPC) as specified in [5] and is expected to foster new centralized functions such as dynamic state estimation-based protection schemes [6] at the substation level. Most of the proposed CPC architectures use merging units (MUs) to publish sampled values (SV) of the current and voltage signals on the process bus as in [7] and in [8], while the digital signal processing (DSP) algorithms and protection logic are executed on the centralized platform. This approach has two drawbacks. Firstly, publishing the signals with high sampling rates increases the communication burden significantly. Maximum latency and high bandwidth requirements decrease the size of process-level networks based on high-availability seamless redundancy (HSR) as indicated in [9]. Secondly, all the computationally expensive DSP algorithms,

such as finite impulse response (FIR) lowpass (LP) filter, short-time fourier transform (STFT), and discrete wavelet transform (DWT), are executed on the centralized platform, which leads to high computational requirements in order to execute the protection functions in real-time. In order to mitigate the first challenge of a high communication burden, [10] proposes to implement the travelling wave feature extraction, such as polarity and magnitude, on the MU and then publish the results on the process bus. The IEEE standard about *"Recommended Practice for Signal Treatment Applied to Smart Transducer"* indicates that signals will be entirely processed at the point of measurement in the future [11]. This recommendation is picked up by [12] and is applied to the application of power system protection in substations. The paper [12] proposes to integrate all the required DSP algorithms of the protection function in a dedicated device termed a distributed signal processing unit (DSPU), which publishes the results of the DSP algorithms on the process bus instead of raw samples. Thus the high communication burden as well as high computational burden of the centralized platform can be lowered and a scalable CPC architecture can be obtained.

A. Scope of the Paper

This paper builds on the CPC architecture proposed in [12] and modifies it in order to emphasise the importance of having a DSPU for each protection object such as transformer, transmission line or power system bus. Furthermore, this paper discusses the design of the different DSP algorithms required for transmission line protection.

B. Outline of the Paper

The reminder of this paper is structured as follows. In Sec. II the requirements for digital substations are stated and the novel CPC architecture is described. Then in Sec. III the design and structure of the transmission line DSPU and its DSP algorithms are elaborated. Furthermore, Sec. III discusses in detail the multirate filter bank and the discrete STFT utilised in the transmission line DSPU. In Sec. IV the functional performance of the multirate filter bank and discrete STFT is evaluated through different dynamic tests as well as through an electromagnetic transient (EMT) simulation. Lastly, Sec. V concludes the paper and proposes future work.

II. SUBSTATION AUTOMATION ARCHITECTURES

This section discusses the requirements that have been considered in this paper during the design of the DSPU. Then the novel CPC architecture based on DSPUs is described.

A. Requirements for Protection Systems in Substations

The two parts of IEC standards 61850-5 and 61869-9 comprise the communication requirements for protection functions and the requirements for digital interfaces of instrument transformers, respectively. Moreover, the IEEE standard 37.118 for Synchrophasor Measurements for Power Systems has been considered. Nonetheless, it should be mentioned that the main application of IEEE 37.118 is power system operation and

TABLE I
REQUIREMENTS FOR PROTECTION SYSTEMS IN SUBSTATIONS

Requirements	Value	Source
Transfer-time of SV	$3\,\mathrm{ms}$	IEC61850-5 [13]
Processing delay of SV	$2\,\mathrm{ms}$	IEC61869-9 [14]
Time synchronization accuracy	$1\,\mathrm{\mu s}$	IEC61850-5 [13]
Ratio error at $16.7\,\mathrm{Hz}$ or $20\,\mathrm{Hz}$	$10\,\%(0.92\,\mathrm{dB})$	IEC61869-6 [15]
Ratio error at 2nd to 5th harm.	$10\,\%(0.92\,\mathrm{dB})$	IEC61869-6 [15]
Inst. error from $50\,\mathrm{Hz}$ to $50\,\mathrm{kHz}$	$10\,\%(0.92\,\mathrm{dB})$	IEC61869-6 [15]
Instantaneous error at $500\,\mathrm{kHz}$	$30\,\%(3\,\mathrm{dB})$	IEC61869-6 [15]
Anti-aliasing filter attenuation	$\geq 20\,\mathrm{dB}$	IEC61869-6 [15]
Total vector error (TVE)	$1\,\%$	IEEE37.118 [16]

analysis and not power system protection in substations. Tab. I summarises the requirements that are of major concern for CPC architectures.

B. Proposed CPC Architecture based on DSPU

The proposed CPC architecture suggests to use a dedicated DSPU per protection object at the process level, which contains the DSP algorithms required by the corresponding protection functions, such as distance, differential or overcurrent protection based on phasor, time-domain or travelling-wave quantities. The protection object is defined by its respective protection zone with the current transformers (CTs) acting as boundaries [17]. This paper has modified the CPC architecture proposed in [12] and emphasises the importance of having a DSPU for each protection object such as transformer or power system bus. This modification is required, since some of the protection functions are partly based on the differential current samples instead of pre-processed phasor-domain quantities. The DSPU uses the three-phase secondary current and voltage signals as input and publishes the results of the DSP algorithms on an HSR closed-loop network at a synchronised publishing rate. Synchronisation is achieved through the precision time protocol (PTP) utilising the power utility profile and hardware timestamping to obtain an accuracy of below $1\,\mathrm{\mu s}$. Since the publishing rate is independent of the sampling rate, the communication load is reduced in case of high sampling rate protection applications. The DSP results are encoded using the common data classes (CDC) defined in IEC 61850-7-3 and are published by the Generic Object-Oriented Substation Event (GOOSE) application layer protocol configured with a fixed and synchronised publishing rate of $1\,\mathrm{ms}$, similar to [18] for wide-area networks (WAN). Furthermore, the entire protection function logic of the substation is integrated on a centralized platform, as shown in Fig. 1, and executed with a cycle time of $1\,\mathrm{ms}$ or slower. It can be seen from Fig. 1 that the proposed CPC architecture might lead to increased copper cabling in comparison to the MU approach. This is caused by the fact that the DSPU for transformer protection and system bus protection uses current and voltage signals from multiple bays, whereas the MU uses only measurements from its respective bay. Nevertheless, this drawback is expected to be overcome through the increased technical readiness and deployment of optical instrument transformers [19] and Rogowski Coils [20].
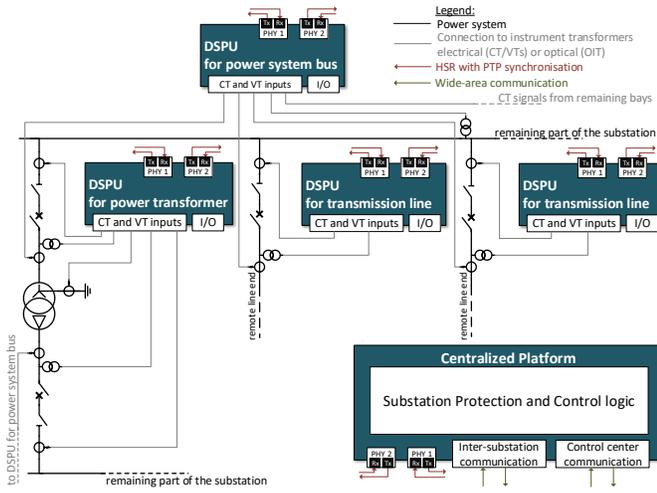
Fig. 1. Proposed CPC architecture based on DSPU

Fig. 2. Signal processing structure of the DSPU for transmission lines

III. DSPU FOR TRANSMISSION LINE PROTECTION

The following section describes the signal processing structure of the DSPU and then focuses on the multirate filter bank and the discrete STFT.

A. Signal Processing Structure of the DSPU

The different protection functions deployed in the power system can be clustered according to the required frequency spectrum of their input signals, namely phasor based, time-domain based and travelling-wave based. Most of the currently deployed protection functions are phasor based, which means that the fundamental component is of major importance as well as the 2nd to 5th harmonics for the detection of transformer inrush conditions and overexcitation situations, respectively. These quantities are provided by the *Harmonic module* as depicted in Fig. 2. Moreover, the time-domain protection functions are mostly concerned with the incremental quantities of the current and voltage signals that are obtained using the superposition principle. Furthermore, different time-domain functions utilise waveshape analysis to increase the security of phasor based protection functions. These quantities are provided by the *time-domain protection module* and *wave-shape analysis module* as shown in Fig. 2. The third group of protection function is travelling-wave based and analyses the electromagnetic waves of the power system transients in order to extract information about the polarity or amplitude as well as timing information. Thus the high frequency components of the voltage and current signals are of importance. These quantities are provided by the *travelling-wave protection module*. Lastly, the *Interharmonic module* is depicted in Fig. 2. Its main purpose is to provide information about the occurrence of interharmonics, such as subsynchronous resonances. The parameter P_{xx} underneath the modules indicates the cycle time of the corresponding module. It can be seen that the *Interhamonic module* publishes its DSP results every $1\,\text{s}$ whereas all the other modules report their results every $1\,\text{ms}$. The $1\,\text{second}$ cycle time of the *Interhamonic module* has been
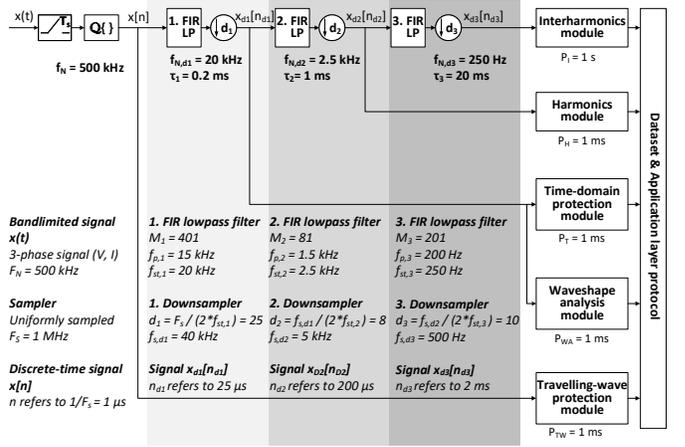
chosen in order to obtain a high frequency resolution of the results. Due to the different frequency spectrum requirements of the DSP algorithms, a multirate filter bank consisting of FIR LP filters is used to supply the signal inputs with the required frequency spectrum to the respective DSP modules as shown in Fig. 2. The input signals of the DSPU are the three-phase continuous functions $x(t)$ of secondary currents and voltages, which have been band-limited by analog anti-aliasing filters to the Nyquist frequency $F_N = 500\,\text{kHz}$. Thus the band-limited function $x(t)$ can be uniformly sampled with a sampling frequency $F_S = 1\,\text{MHz}$ and the discrete-time quantized signal $x[n]$ is obtained as shown in (1).

$$x[n] = Q\Big(x(nT_S)\Big) \tag{1}$$

Where the sampling period T_S is defined in (2) and $Q(x)$ represent the quantization process, which adds a quantisation error to the signal.

$$T_S = \frac{1}{F_S} = 1\,\mu\text{s} \tag{2}$$

B. Multirate Filter Bank

After the sampling and quantization processes the sequence is filtered by three cascaded causal FIR LP filter and down-samplers. Since the synchronization of samples and of measurements is of high importance in protection systems, FIR filters have been chosen over infinite impulse response (IIR) filters due to their linear phase response in the passband. Additionally, causal FIR filters are Bounded-Input-Bounded-Output (BIBO) stable, since the impulse response is absolutely summable. Equation (3) shows the discrete convolution in the form of a constant-coefficient-difference equation (CCDE) of the ith causal FIR filter and the succeeding downsampler.

TABLE II
DESIGN PARAMETERS FOR THE THREE FIR LP FILTERS

Design parameters	1st FIR LP	2nd FIR LP	3rd FIR LP
Number of taps M_i	401	81	201
Passband edge $f_{p,i}$	15 kHz	1.5 kHz	200 Hz
Stopband edge $f_{st,i}$	20 kHz	2.5 kHz	250 Hz
Weight $\delta_{p,i}$ / $\delta_{st,i}$	2/1	2/1	2/1

Fig. 3. Frequency response of the FIR lowpass filters

$$x_{d_i}[n_{d_i}] = \sum_{k=0}^{M_i-1} h_i[k]\, x_{d_{(i-1)}}[n_{d_i} d_i - k] \qquad (3)$$

$$= \sum_{k=0}^{M_i-1} b_{i,k}\, x_{d_{(i-1)}}[n_{d_i} d_i - k]\,,\ i \in \mathbb{N}^+$$

Where h_i is the impulse response of the ith FIR filter and with the kth coefficients corresponding to $h_i[k] = b_{i,k}$. The sequence before the first decimation stage is given by $x_{d_0}[n_{d_0}] = x[n]$.

In order to find the filter coefficients $b_{i,k}$ the Parks-McClellan algorithm has been used, which yields an equiripple magnitude response with linear phase and which minimizes the maximum error in the pass- and stopbands [21]. Tab. II contains the filter design parameters used as an input to the algorithm and Fig. 3 shows the frequency response of the three different FIR LP filters. The passband edge $f_{p,i}$ and stopband edge frequencies $f_{st,i}$ have been chosen under the consideration of the required Nyquist frequency f_{N,d_i} by each of the DSP modules. Then the number of taps has been selected considering the maximum error and processing delay requirements as well as the minimum attenuation requirements stated in Tab. I. It can be seen from Fig. 3 that there is a margin between the requirements and the filter performance that allows a further reduction of the high number of taps and thereby decreases the computational burden in terms of multiply-accumulate operations. The number of taps defines the group delay τ_i of the ith filter given in (4).

$$\tau_i = \frac{M_i - 1}{2}\frac{1}{f_{s,d_{(i-1)}}}\,,\ i \in \mathbb{N}^+, f_{s,d_0} = F_S \qquad (4)$$

Where the digital sampling rate f_{s,d_i} and the downsampling factor d_i are given in 5 and 6, respectively.

$$f_{s,d_i} = \frac{f_{s,d_{(i-1)}}}{d_i}\,,\ i \in \mathbb{N}^+, f_{s,d_0} = F_S \qquad (5)$$

$$d_i = \frac{f_{s,d_{(i-1)}}}{2 f_{st,i}}\,,\ i \in \mathbb{N}^+, f_{s,d_0} = F_S \qquad (6)$$

The downsampling factor d_i is conservatively chosen in (6) in order that the Nyquist frequency f_{N,d_i} equals the stopband edge frequency $f_{st,i}$. Evaluating (4) for the 1st, 2nd and 3rd FIR LP filter, the group delays of $200\,\mu s$, $1\,ms$ and $20\,ms$ are obtained, respectively. Adding the group delays of the 1st and 2nd multirate stage yields a total delay of $1.2\,ms$ that allows the *time-domain protection module*, *waveshape analysis module*
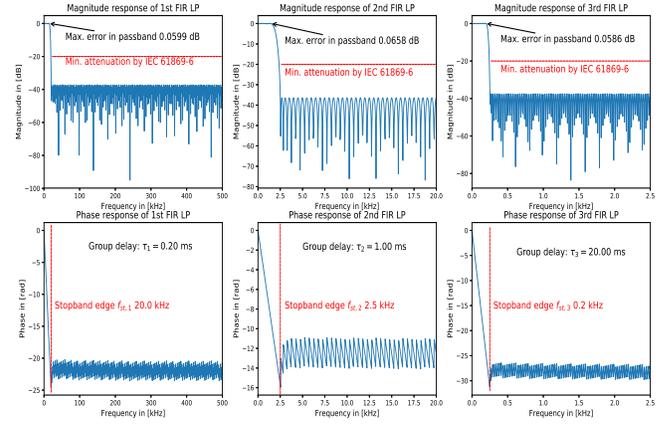
and *harmonic module* to process the input sequence faster than the maximum allowed processing delay requirement of $2\,ms$ for SV.

C. Harmonic Module

The purpose of the harmonic module is to obtain synchronised phasors of the harmonic components of interest for the transmission line protection. At its core the discrete STFT is applied on the sequence $x_{d_2}[n_{d_2}]$ for the specified digital frequency bins k and thereby the time-domain signal is converted to a frequency-domain signal by applying the basis vector $\psi_k = [1, e^{-j\frac{2\pi}{L_{H,m}}k}, \cdots, e^{-j\frac{2\pi}{L_{H,m}}(L_{H,m}-1)k}]^\top$. The integer signal $x_{d_2}[n_{d_2}]$ has been lowpassed filtered and downsampled as described in Sec. III-B. Since the STFT of real signals is symmetric in magnitude and all integer numbers are also real numbers, only the spectral components corresponding to positive frequencies are estimated and the magnitude is multiplied by 2, as shown in (8). The highest positive frequency after the 2nd decimation stage corresponds to the Nyquist frequency given in (7).

$$f_{N,d_2} = \frac{f_{s,d_2}}{2} \qquad (7)$$

Since the set of basis vectors $\{\psi_k\}$ is orthogonal and each element has norm $\sqrt{L_{H,m}}$, the results are normalised by the length of the STFT window $1/L_{H,m}$ in the analysis formula (8), which considers a rectangular window. Additionally, the estimated amplitude of the kth spectral component is divided by $\sqrt{2}$ in order to obtain the RMS value.

$$X_{d_2}^{nc}[m;k] = \frac{2}{\sqrt{2}L_{H,m}} \sum_{n_L=0}^{L_{H,m}-1} x_{d_2}[m-n_L] e^{-j\frac{2\pi(m-n_L)}{L_{H,m}}k} \quad (8)$$

$$k \in \left\{0, 1, \cdots, \left\lfloor \frac{L_{H,m}}{2} \right\rfloor \right\}$$

The index m indicates the latest sample of the sliding window as shown in (9a) and Δf_m corresponds to the frequency resolution of the discrete STFT calculated in (9b) at sample index m. The parameter $B_{H,0}$ in (9a) refers to the number

of samples of overlap of the sliding window at sample index $m = 0$.

$$m = \left\lfloor \frac{n_{d_2}}{L_{H,0} - B_{H,0}} \right\rfloor (L_{H,0} - B_{H,0}) \tag{9a}$$

$$\Delta f_m = \frac{f_{s,d_2}}{L_{H,m}} \tag{9b}$$

In transmission line protection the fundamental component $f_{1,m}$ of the voltage and current signals is of major concern and corresponds to the power system frequency. The estimated frequency $f_{1,m}$ is calculated later in (15). Nevertheless, in case of the DSPU for transformer protection the 2$^{\text{nd}}$ to 5$^{\text{th}}$ harmonics are of interest in order to detect inrush and overexcitation situations [12]. Since synchronised phasors are published by the harmonic module, it is important that the accumulated phase delays γ_{k,d_i} and the accumulated amplitude errors of the kth spectral component, introduced by the preceding FIR filters after the ith decimation stage, are properly compensated. The individual amplitude errors $e_{k,i}$ in p.u., introduced by the ith FIR filter, are obtained from the frequency response in Fig. 3. The accumulated phase delay γ_{k,d_i} is calculated in (10) and the amplitude compensation factor E_{k,d_i} is obtained by (11). If the group delay and amplitude error of the analog anti-aliasing filters are known, they should be included as well in (10) and (11), respectively.

$$\gamma_{k,d_i} = 2\pi f_{k,m} \sum_{j=1}^{i} \tau_j \tag{10}$$

$$E_{k,d_i} = \prod_{j=1}^{i} \frac{1}{1 - e_{k,j}} \tag{11}$$

Using γ_{k,d_i} and E_{k,d_i}, the estimate $X_{d_2}^{nc}[m;k]$ in (8) is compensated in (12).

$$X_{d_2}[m;k] = E_{k,d_i} \, X_{d_2}^{nc}[m;k] \, e^{j\gamma_{k,d_2}} \tag{12}$$

Then the phase and amplitude compensated spectral estimate $X_{d_2}[m;k]$ can be labelled by an appropriate time stamp of a point in time defined in (13).

$$t_{H,m} = \frac{m}{f_{s,d_2}} - \sum_{j=1}^{i} \tau_j \tag{13}$$

According to IEEE standard C37.118.1-2011 [16] the time tag is supposed to be placed in the middle of the observation window. Nonetheless, there is no standard for phasor quantities used by protection functions in substations, since these are traditionally part of the protection algorithm itself. From (13) it can be seen that the timestamp has been placed at the beginning of the observation window corresponding to the latest sample m. Since the fundamental power system frequency is not always stationary and varies around its nominal value of 50 or 60 Hz, respectively, the length of the observation window $L_{H,m}$ is decreased or increased if the frequency increases or decreases, respectively. Thereby the spectral leakage is

TABLE III
CONFIGURATION OF DSPU

$L_{H,0}$	$B_{H,0}$	P_H	f_{s,d_2}	$f_{1,0}$	Δf_0	F_S
100	95	1 ms	5 kHz	50 Hz	50 Hz	1 MHz

minimized. This is especially important for protection systems close to generator stations where the frequency can vary to a larger extend. The equation (14) shows the adjustment of the window length $L_{H,m}$ to the closest integer, as proposed in [22].

$$L_{H,m} = \left\lfloor \frac{f_{s,d_2}}{f_{1,m}} + 0.5 \right\rfloor \tag{14}$$

The power system frequency $f_{1,m}$ is estimated according to the equation in (15), as proposed in [23]. In this frequency estimation approach the angle θ of the positive sequence phasor is used. The constant cycle time of the harmonic module P_H is calculated in (16).

$$f_{1,m} = \frac{\theta[m] - \theta[m-1]}{2\pi \, P_H} \tag{15}$$

$$P_H = \frac{L_{H,0} - B_{H,0}}{f_{s,d_2}} \tag{16}$$

There are other methods to reduce the spectral leakage in case of off-nominal fundamental frequency, such as the adjustment of F_S of the ADC [24]. Nevertheless, this is not applicable in most CPC architecture, since all the ADCs are synchronised to an external absolute time reference. Minimizing spectral leakage can also be achieved through an enhanced interpolated-DFT [25]. Nonetheless, this approach has the disadvantage that a minimum window length of two fundamental periods has to be used and thus decreases the time location of the signal. Since the speed requirement in power system protection is of high importance, a one cycle observation window is desirable.

IV. SIMULATION AND RESULTS

In this section the performance of the discrete STFT is verified under step changes in phase and magnitude as well as during a frequency ramp test. Lastly, the harmonic module is tested by applying the 3-phase signal of a corresponding single-phase to ground fault. The processed signals are compensated according to their group delays τ_i in (4) and displayed according to their timestamp $t_{H,m}$ in (13). The DSPU has been configured according to the parameters in Tab. II and in Tab. III.

A. Results of Step Changes in Phase and Magnitude

Fig. 4 shows the step change in magnitude from 0.5 p.u. to 1 p.u., which is applied at time 0 s. It can be seen that the STFT requires one cycle to settle at the magnitude $|X_{d_2}[m,1]|$ of 1 p.u. of the fundamental component. During this dynamic phase the TVE increases to 50 %. Nevertheless, during steady-state the TVE remains below 1 % as required by [16]. Furthermore,
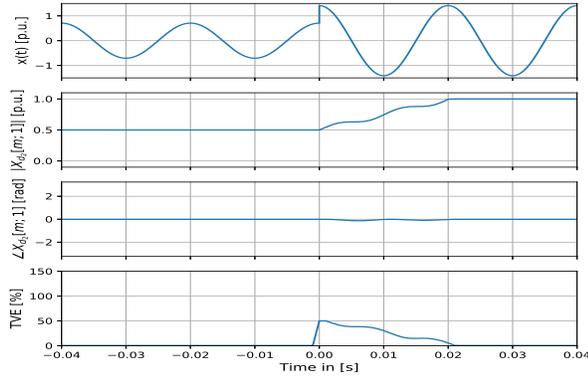
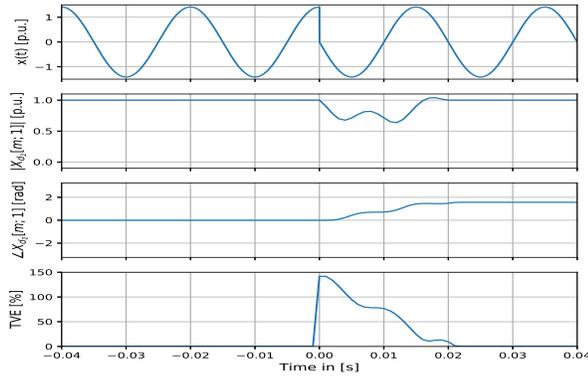Fig. 4. Performance under a step change in magnitude at time $0\,\mathrm{s}$

Fig. 5. Performance under a step change in phase at time $0\,\mathrm{s}$

Fig. 6. Performance during ramp of system frequency of 1 Hz/s
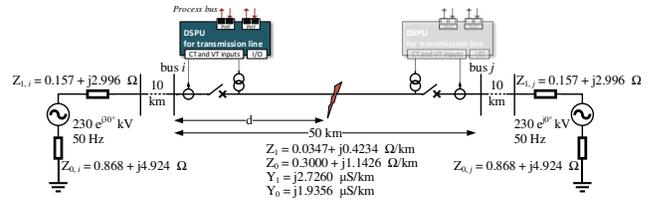
Fig. 7. Single line diagram of the tested three-phase 230 kV power system

it can be observed that the phase estimation is only marginal affected by the step change in magnitude.

Fig. 5 depicts the step change in phase from 0 to $\frac{\pi}{2}$ at time $0\,\mathrm{s}$. It can be seen that the estimate of the phase $\angle X_{d_2}[m,1]$ settles at $\frac{\pi}{2}$ after one period. The TVE increases above $100\,\%$ during the transient phase and then settles below the required $1\,\%$ during steady-state. It can also be seen that the estimate of the magnitude $|X_{d_2}[m,1]|$ of the fundamental component is shortly affected by the step change in phase.

B. Results of Frequency Ramp Test

The second test consists of a frequency ramp test as shown in Fig. 6. The frequency ramp rate of $1\,\frac{\mathrm{Hz}}{\mathrm{s}}$ is applied at time $0\,\mathrm{s}$ and plotted until time $2\,\mathrm{s}$. It can be seen that the estimated fundamental frequency $f_{1,m}$ is correctly estimated according to (15) and rises with the defined rate of $1\,\frac{\mathrm{Hz}}{\mathrm{s}}$. It can also be observed that the length of the observation window $L_{H,m}$ is adjusted to the closest integer value according to (14). Due to the adjustment of the length of the observation window, the estimate of the magnitude $|X_{d_2}[m,1]|$ and the phase $\angle X_{d_2}[m,1]$ of the fundamental component are kept stable.

C. Results of Numerical EMT Simulation

This test applies a secondary three phase current signal $i_{s,3\phi}(t)$ to the DSPU algorithms corresponding to a phase A
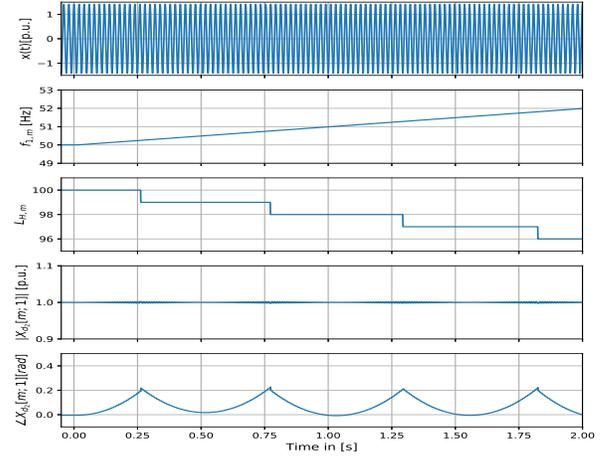
to ground fault. The current signal has been obtained by a numerical EMT simulation in PSCAD using the $230\,\mathrm{kV}$ power system model shown in Fig. 7. The fault is applied between bus i and bus j at a distance d of $10\,\mathrm{km}$ from bus i. The signal $i_{s,3\phi}(t)$ has been band-limited by a 2nd order Butterworth filter with a cutoff frequency of $400\,\mathrm{kHz}$ representing the analog anti-aliasing filter of the DSPU. This leads to an oversampled discrete-time quantized signal $x_{3\phi}[n]$ with $Fs = 1\,\mathrm{MHz}$ according to (1). The Fig. 8 shows the current signal and the results of the STFT in terms of magnitude and phase of the phase A current. The phase A to ground fault has been applied at time $0.3\,\mathrm{s}$ and the current is subject to a significant decaying DC offset. It can be seen that the magnitude of the fundamental component $|X_{d_2}|[m,1]$ of phase A reaches $4\,\mathrm{A}$ at $12\,\mathrm{ms}$ and stabilizes after $20\,\mathrm{ms}$. Moreover, the sharp edges of the magnitude estimates are caused by the frequent changes of the length of the observation window $L_{H,m}$ during the dynamic phase of the fault. At time $0.38\,\mathrm{s}$ the breaker opens at both line ends and the magnitude of the current settles to zero within one power system cycle. Once the magnitude settles below a configured threshold, the discrete STFT algorithm stops estimating the phasor components.

D. Discussion

The presented results show that the $1\,\mathrm{MHz}$-sampled signals are sufficiently filtered and downsampled in order to be used by the discrete STFT while still complying with the maximum error and minimum attenuation requirements in [15]. This filter
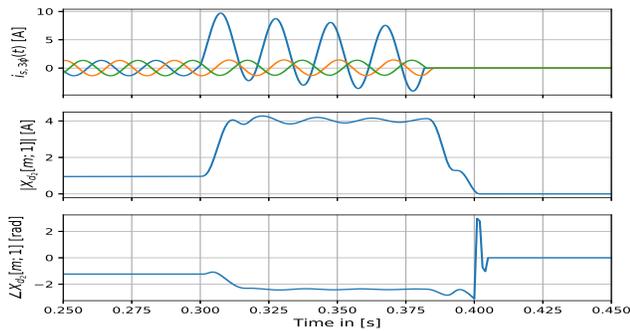
Fig. 8. Performance of STFT during a phase A to ground fault

performance is obtained by a relatively high number of taps M_i. Due to the existing margin between the requirements and the filter characteristics, it is expected that the number of taps M_i can be further reduced in the future. Additionally, it has been shown that the phase delay is properly compensated due to the linear phase characteristics of the passband of the FIR LP. Lastly, the results show that the TVE can be limited to below 1% during steady-state. Moreover, it can be deduced from the dynamic response of the discrete STFT that different implementations of the DSP algorithm, such as window length or window type, result in different dynamic responses. Therefore it is important in such a CPC architecture that the dynamic performance of the DSP algorithms for substation protection are specified similar to the IEEE standard C37.118 for synchrophasor measurements.

V. CONCLUSION

This paper has proposed a new CPC architecture based on DSPUs that enables the scalable integration of high sampling rate protection applications in digital substations. Furthermore, the design of the transmission line DSPU has been discussed and the structure of its DSP algorithm has been shown. In detail, the design of the multirate filter bank and the discrete STFT have been elaborated and their functional performance has been verified by analysing the behaviour under step changes and during off-nominal frequencies as well as by conducting numerical EMT simulation. As future work, the remaining DSP modules are developed and tested such as *travelling-wave protection module*, *time-domain protection module* or *interharmonics module*, and their corresponding IEC 61850 datasets need to be derived.

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