Circuit Design Techniques for Implantable Closed-Loop Neural Interfaces

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Tryck: Universitetsservice US AB
For my family
Abstract

Implantable neural interfaces are microelectronic systems, which have the potential to enable a wide range of applications, such as diagnosis and treatment of neurological disorders. These applications depend on neural interfaces to accurately record electrical activity from the surface of the brain, referred to as electrocorticography (ECoG), and provide controlled electrical stimulation as feedback. Since the electrical activity in the brain is caused by ionic currents in neurons, the bridge between living tissue and inorganic electronics is achieved via microelectrode arrays. The conversion of the ionic charge into freely moving electrons creates a built-in electrode potential that is several orders of magnitude larger than the ECoG signal, which increases the dynamic range, resolution and power consumption requirements of neural interfaces. Also, the small surface area of microelectrodes implies a high-impedance contact, which can attenuate the ECoG signal. Moreover, the applied electrical stimulation can also interfere with the recording and ultimately cause irreversible damages to the electrodes or change their impedance. This thesis is devoted to resolving the challenges of high-resolution recording and monitoring the electrode impedance in implantable neural interfaces.

The first part of this thesis investigates the state-of-the-art neural interfaces for ECoG and identifies their limitations. As a result of the investigation, a high-resolution ADC is proposed and implemented based on a ΔΣ modulator. In order to enhance performance, dynamic biasing and area-efficient switched-capacitor circuits were proposed. The ΔΣ modulator is combined with the analog front-end to provide a complete readout solution for high-resolution ECoG recording. The corresponding chip prototype was fabricated in a 180 nm CMOS process, and the measurement results showed a 14-ENOB over a 300 Hz bandwidth while dissipating 54 µW.

The second part of this thesis expands upon the well-known methods for impedance measurements and proposes an alternative digital method for monitoring the electrode-tissue interface impedance. The proposed method is based on the system identification technique from adaptive digital filtering, and it is compatible with existing circuitry for neural stimulation. The method is simple to implement and performs wide-band measurements. The system identification was first verified through behavioral simulations and then tested with a board-level prototype in order to validate the functionality under real conditions. The measurement results showed successful identification of the electrode-electrolyte and electrode-skin impedance magnitudes.

Keywords: Neural interface, ECoG, high-resolution, ADC, recording, delta-sigma modulator, system identification, impedance measurements.
Sammanfattning


Den första delen av avhandlingen undersöker demodernaste neurala gränssnitten för EKoG och identifierar deras begränsningar. Som en följd av undersökningen föreslås och implementeras en analog till digital omvandlare med hög upplösning baserat på en $\Delta \Sigma$ modulator. För att förbättra prestatända föreslår dynamisk förspänningsmodulator och yteffektiva omkopplade kondensatorkretsar. $\Delta \Sigma$ modulatorn kombineras med den analog front-end för att ge en komplett avläsningslösning för EKoG-registrering med hög upplösning. Motsvarande chipprototyp tillverkades i en 180 nm CMOS-process, och måtresultaten visade en 14-ENOB (effektivt antal bitar) över en 300 Hz-bandbredd med en 54 µW effektförbrukning.

Acknowledgment

The pursuit of a doctoral degree has been perhaps the most challenging adventure of my life. Luckily, I was surrounded by great people that shared some of the burden and gave me words of encouragement. I feel grateful for that, and I hope that the following words convey this feeling.

First and foremost, I want to acknowledge my main supervisor, Prof. Ana Rusu, for giving me the opportunity to do research in mixed-signal circuit design. This thesis work would not have been possible if it wasn’t for her demand for excellence, attention to detail and importance of sticking to deadlines. Looking back, I am humbled and grateful for the support, time, and patience she invested in my supervision. Also, I want to thank her for involving me in teaching activities, since it allowed me to experience the best part of academia. Lastly, I can say that I have grown as a person thanks to her professionalism and work ethics.

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<th>Description</th>
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<tbody>
<tr>
<td>ΔΣ</td>
<td>Delta-sigma</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to digital converter</td>
</tr>
<tr>
<td>AFE</td>
<td>Analog front-end</td>
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<tr>
<td>AP</td>
<td>Action potential</td>
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<tr>
<td>ASIC</td>
<td>Application specific integrated circuit</td>
</tr>
<tr>
<td>BCI</td>
<td>Brain computer interface</td>
</tr>
<tr>
<td>BP</td>
<td>Band-pass</td>
</tr>
<tr>
<td>BSP</td>
<td>Biosignal processor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
</tr>
<tr>
<td>CPU</td>
<td>Central processing unit</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to analog converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current</td>
</tr>
<tr>
<td>DDS</td>
<td>Direct digital synthesis</td>
</tr>
<tr>
<td>DEM</td>
<td>Dynamic element matching</td>
</tr>
<tr>
<td>DSL</td>
<td>Digital servo loop</td>
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<tr>
<td>DSP</td>
<td>Digital signal processing</td>
</tr>
<tr>
<td>ECoG</td>
<td>Electrocorticography</td>
</tr>
<tr>
<td>EEG</td>
<td>Electroencephalography</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
</tr>
<tr>
<td>ETI</td>
<td>Electrode tissue interface</td>
</tr>
<tr>
<td>ACRONYM</td>
<td>DEFINITION</td>
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<td>---------</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier transform</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of merit</td>
</tr>
<tr>
<td>FRA</td>
<td>Frequency response analyzer</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain bandwidth</td>
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<tr>
<td>HP</td>
<td>High-pass</td>
</tr>
<tr>
<td>IA</td>
<td>Instrumentation amplifier</td>
</tr>
<tr>
<td>IIR</td>
<td>Infinitive impulse response</td>
</tr>
<tr>
<td>LDO</td>
<td>Low dropout</td>
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<tr>
<td>LFP</td>
<td>Local field potential</td>
</tr>
<tr>
<td>LP</td>
<td>Low-pass</td>
</tr>
<tr>
<td>LS</td>
<td>Least square</td>
</tr>
<tr>
<td>MEA</td>
<td>Microelectrode array</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal insulator metal</td>
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<tr>
<td>NTF</td>
<td>Noise transfer function</td>
</tr>
<tr>
<td>OSR</td>
<td>Oversampling ratio</td>
</tr>
<tr>
<td>OTA</td>
<td>Operational transconductance amplifier</td>
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<tr>
<td>PCB</td>
<td>Printed circuit board</td>
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<tr>
<td>PMU</td>
<td>Power management unit</td>
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<tr>
<td>PSRR</td>
<td>Power supply rejection ration</td>
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<tr>
<td>PSD</td>
<td>Power spectral density</td>
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<tr>
<td>RFID</td>
<td>Radio frequency identification</td>
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<tr>
<td>RLS</td>
<td>Recursive least square</td>
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<tr>
<td>SAR</td>
<td>Successive approximation register</td>
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<tr>
<td>SNDR</td>
<td>Signal to noise and distortion ratio</td>
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<tr>
<td>SNR</td>
<td>Signal to noise ratio</td>
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<tr>
<td>SR</td>
<td>Slew-rate</td>
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<tr>
<td>SQNR</td>
<td>Signal to quantization noise ratio</td>
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<tr>
<td>STF</td>
<td>Signal transfer function</td>
</tr>
<tr>
<td>SUT</td>
<td>Sample under test</td>
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<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra wide band</td>
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<tr>
<td>VCO</td>
<td>Voltage controlled oscillator</td>
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List of Publications

List of appended papers


Summary of Appended Papers


  **Summary:** This paper presents a switched-capacitor implementation of a high-pass ΔΣ modulator. The proposed implementation is realized with dynamically biased inverter-based amplifiers enabled by the 4-bit quantizer. The DAC mismatch errors are mitigated by a custom tree structured dynamic element matching encoder. Simulation results demonstrate a peak SNDR of 96.4 dB and a SFDR of 101 dBc over a 300 Hz bandwidth. The total estimated power consumption of the delta-sigma modulator is 19.56 µW leading to a figure-of-merit of 0.6 pJ/conv.

  **Author’s contribution:** The main author proposed the high-pass ΔΣ topology for ECoG recording, designed and verified all analog/mixed-signal circuits, and wrote the manuscript draft.


  **Summary:** This paper presents a ΔΣ-based readout ASIC for closed-loop neural interfaces. The proposed ASIC can accurately record a peak input signal up to 240 mV over a 300 Hz bandwidth with an input referred noise of 5.23 µVrms, which amounts to 14-ENOB with a total power consumption of 54 µW. The proposed readout features a high-pass ΔΣ modulator with a tracking ADC and an embedded instrumentation amplifier. The design choices are supported with theoretical analysis, and the ASIC is validated by comprehensive electrical characterization across all packaged dies.

  **Author’s contribution:** The main author proposed the ASIC features, conducted the theoretical analysis, designed and verified all analog/mixed signal circuits, developed the custom evaluation board, performed the experimental characterization, and wrote the manuscript draft.
SUMMARY OF APPENDED PAPERS


Summary: This paper presents a switched-capacitor circuit with a combined functionality of an integrator and a voltage buffer. Also, the proposed circuit employs correlated double sampling technique to enable flicker noise canceling. The proposed circuit exploits the relationship between the effective noise bandwidth and noise floor density to aggressively reduce the size of the sampling capacitance with a negligible noise performance deterioration. The findings are supported with theoretical analysis and simulation results in a 0.18 µm CMOS process.

Author’s contribution: The main author proposed the integrator circuit, conducted the theoretical analysis, designed and verified all analog/mixed-signal circuits, and wrote the manuscript draft.


Summary: This paper presents an overview and discussion of the state-of-the-art impedance spectroscopy measurement methods. An alternative method based on adaptive IIR filtering and system identification technique is proposed to circumvent the challenges associated with the traditional sinusoidal generator. A well-known adaptive algorithm based on pseudo-linear regression and output-error formulation was used to tune the filter coefficients. The proposed method was validated through behavioral simulations.

Author’s contribution: The main author performed the literature review and proposed an all-digital approach, conducted behavioral simulations, and wrote the manuscript draft.


Summary: This paper presents the experimental results of a proof-of-concept impedance spectroscopy measurement method implemented with off-the-shelf components. In this work, the system identification is implemented in post-processing, which allows for design flexibility and optimization of the measurement setup. The electrical characterization and validation is performed using known RC component values and in real application conditions, such as in a saline solution and with skin impedance measurements.

Author’s contribution: The main author designed the proof-of-concept prototype, developed the custom evaluation board, performed the experimental characterization and validation, and wrote the manuscript draft.
Chapter 1

Introduction

The human brain is a power-efficient electrochemical system. It consists of approximately 22 billion neurons, interconnected intricately to achieve an astonishing computational performance while consuming approximately 14.6 W or 0.66 nW per neuron [1,2]. In comparison, a modern CPU has approximately 2 billion transistors and consumes around 65 W [3]. When it comes to sensorimotor processing, control, pattern recognition, and learning, the brain is more power-efficient than any state-of-the-art digital signal processor [1]. The computation is distributed among specialized regions in the brain, while the data is transferred via electrochemical reactions between the neuron's synaptic terminals [4]. The understanding of the brain electrical activity and its interface with electronics has been the driving force for a wide range of biomedical applications, such as diagnosis and treatment of neurological disorders [2,5–7]. For instance, brain-computer interfaces are used to restore speech in locked-in patients based on the recording of brain activity [8,9]. In severe cases of epilepsy, impaired areas of the brain are diagnosed by analyzing the recording of electrical activity before the surgery, to minimize the removal of healthy tissue [10,11]. Closed-loop neural interfaces, which employ both recording and stimulation, have been demonstrated as a viable treatment for sensing and suppressing symptoms of Parkinson’s disease [12,13], epileptic seizure control [14,15], and even controlled modulation of local neural activity [16,17].

The enabling technology for these applications are implantable neural interfaces. Initially, the brain activity had been recorded using bench-top acquisition kits and non-invasive electrodes on the scalp [18]. Although this approach is still used today, the advancements in electronics enabled form-factor miniaturization, radio communication, micro-machined electrode arrays, and low-power operation [19]. As a result, implantable neural interfaces are becoming a possibility, but challenging to implement due to various medical considerations, such as biocompatibility, size, weight, and heating [20]. In particular, high power-efficiency is an essential requirement for implantable devices due to heating limitations on the surrounding tissue and limited energy sources. Hence, there is a need for power-efficient solu-
tions at system and circuit level to support the development of implantable neural interfaces.

1.1 Background on Neural Interfaces

The research of neural electrical activity is a multidisciplinary problem, which requires expertise from various disciplines, such as neuroscience, chemistry, electronics, and signal processing. The electrical fields in the brain are caused by transmembrane ionic currents, which create electrical dipoles across the cell membrane [21]. Since the intracellular space is a conductive electrolyte, the electrical field propagates throughout the volume of the brain. The propagating field can stimulate the neighboring neurons, which either interfere constructively or destructively depending on the phase synchrony between the fields [22]. By placing electrodes in the vicinity of the field it is possible to measure its intensity and phase distribution, which is then used for further signal processing. However, the electrode-tissue interface generates an electrode offset (half-cell potential) in the order of hundred of millivolts, which is caused by the chemical reactions between the electrode material and ions in the tissue [23]. Moreover, this phenomenon is common in all types of neural recording techniques.

Depending on the location of the electrodes, the neural recording techniques are categorized as shown in Fig. 1.1. For instance, electroencephalography (EEG) is well-known due to its non-invasiveness and accessibility. In the EEG technique, Ag/AgCl electrodes are attached on the scalp, and the locations of the electrodes are standardized [24]. As shown in Fig. 1.1, the EEG signal has a small amplitude and frequency range due to its large separation from the aforementioned electrical field. Additionally, the quality of the contact impedance varies due to motion artifacts, which affects the fidelity of the recording [25]. Consequently, more invasive techniques were investigated by using implantable microelectrodes and external

![Figure 1.1: Electrode recording locations and the associated bio-potentials.](image-url)
recording interfaces. There are two common types of invasive microelectrodes, a platinum electrode array on a flexible substrate [11, 26] and a rigid silicon micro-needles with platinized tips [27]. The flexible electrode array is placed on top of the brain surface and is used for electrocorticography (ECoG), while the microneedles are injected in the volume of the brain to measure local field and action potentials (LFP and AP). As it can be seen in Fig. 1.1, larger signal amplitudes and bandwidths can be recorded with more invasive electrodes due to their proximity to the electrical activity. On the other hand, the tissue damage triggers an inflammation response, which makes long-term measurement a challenging prospect [20]. Therefore, among the invasive techniques, the ECoG technique provides the best trade-off between the signal amplitude and tissue damage.

The block diagram of a generic neural interface for both recording and stimulation is shown in Fig. 1.2. The neural interface typically consists of a microelectrode array (MEA), analog front-end (AFE), analog-to-digital converter (ADC), digital signal processor (DSP), communication module, power management unit (PMU) and neural stimulator. The number of electrodes in the flexible MEA usually varies between 16, 32, 64 [11,28–32], and it is commonly limited to a hundred due to a large number of interconnects between the array and the AFE [11,33]. Another aspect is that the number of electrodes impacts the area of the MEA, which also needs to be appropriate for the size of the specimen’s brain region. For instance, in human studies the area of the MEA should be sufficiently large, but also small enough for rat testing, e.g. 4x4 mm² [31]. The pitch of the electrodes is usually around 200-700 µm [31,33–35], since using smaller dimensions may not improve the spatiotemporal resolution as the two channels become indistinguishable from one another [33]. Each pair of electrodes requires a dedicated readout architecture for signal conditioning, which makes the design of multichannel neural interfaces particularly challenging as the power and area consumption scales up with the number of channels. The readout architecture consists of an AFE, which provides amplification and filtering, and an ADC for quantization. A common area reduction technique in multichannel applications is to use a single ADC at N times higher sampling rate and time-multiplexing to facilitate N channels with dedicated

Figure 1.2: Block diagram of a neural interface.
AFEs [36]. The overall power consumption per channel of this readout configuration increases because the AFE has less time to settle to the required resolution accuracy, which means higher amplifier gain-bandwidth requirements or even a dedicated ADC driver. More importantly, the crosstalk between a large number of channels can affect the signal fidelity [37]. An alternative approach is to have a dedicated readout architecture per channel, which is becoming more popular since it enables the future development of active electrodes [11]. In this way, the neural signal can be quantized at the electrode site and then transmitted to an off-chip processing unit, which allows for a better recording fidelity. The on-chip DSP is usually used for data modulation in combination with the communication module to reduce on-chip signal processing and, in turn, power consumption. However, the potential application of on-chip DSP for signal feature extraction is also being investigated [38–40]. After the recorded data is transmitted and processed externally, the communication module receives the instructions for neural stimulation, which can be used to treat symptoms of a neurological disorder [41]. The stimulation waveform is often a three-level pulse, which delivers either a voltage or current (charge) at the electrode site [42,43]. In practice, the same electrode cannot be used for concurrent recording and stimulation due to a temporary electrochemical disturbance at the electrode-tissue interface [11]. In order to provide power to all these blocks, continuous energy harvesting is required by the PMU [44]. Often the communication module is used to supply power to the PMU via inductive coupling, although alternative energy sources, such as vibration, thermal, and biochemical are also investigated [45]. Even though there are working solutions for all these blocks, there are still many biomedical considerations to overcome to reach fully implantable neural interfaces in human studies.

State-of-the-art solutions for ECoG neural interfaces are constricted to implantable MEA, while the neural interface is mounted externally on a rigid printed circuit board (PCB) [31]. In part, the reason for this is the integration incompatibility between two distinct technologies, the flexible electrode array manufacturing and semiconductor processing. For instance, in the case of a neural interface for AP recording, this issue is partly resolved since the silicon microneedles allow for the integration of the active circuitry at the electrode site [46–48]. A potential solution could be to integrate capacitive electrodes in the top-metal layer of a neural interface [11], though at the cost of increased susceptibility to motion artefacts, and common-mode noise due to the high electrode-tissue impedance. Provided that the packaging issue is resolved, a higher channel integration can be achieved. Therefore, there is a demand for readout architectures, which push the limits in power-efficiency.

1.2 Motivation

A conventional readout architecture for ECoG neural interfaces is shown in Fig.1.3a. The key challenges for a low power solution are the signal conditioning of both the
1.2. MOTIVATION

The issue of the electrode half-cell potential is usually mitigated using offset-rejection techniques [49], which are based on analogue high-pass filtering. The direct result of this filtering is the reduction of ECoG dynamic range from 80 dB to around 20 dB [50]. The reduction of the input signal dynamic range positively impacts the power consumption of the readout architecture and it also enables the amplification of the filtered ECoG signal by several orders of magnitude, which is provided via the instrumentation and programmable gain amplifier. Therefore, a quantization noise limited ADC can be used, which provides medium resolution and has low power consumption. However, analog filtering is prone to process variations [32], which is a significant drawback since most of the ECoG signal power is in the low-frequency spectrum, which coincides with the filter cut-off frequency. During multichannel recording, the cut-off frequency variations result in different distortions in the ECoG spectrum, which complicates the decryption of neural signals. Also, the input impedance of a neural recording system is impacted by the implementation of analog filtering techniques, which decreases the rejection of common-mode disturbances [51]. Constrained by these challenges, mixed-signal techniques have been used to enhance the conventional approach. For instance, a digital-to-analog converter and a digital
filter can be used in a feedback configuration to control the cut-off high-pass frequency [31, 49]. Apart from the digitally assisted feedback, the gain stages in the readout architecture remain unaffected. Hence, the line between the conventional analog and mixed-signal design is becoming more blurred. However, the conventional approach is no longer suitable in neural interfaces that employ stimulation functionality due to artifact generation inside the recording bandwidth [52]. These artifacts can saturate the conventional readout architectures due to high gain. As a result, recent works are focusing on using a high-resolution ADC for closed-loop neural interfaces [52, 53], which is a term used to designate that both the recording and stimulation functionality is integrated in a neural interface.

A readout based on a high-resolution ADC, which is shown in Fig. 1.3b, could provide a high dynamic range and allow for the aforementioned filtering issue to be solved in the digital domain, granted that the power consumption remains competitive with the conventional approach. Generally, a high-resolution ADC is limited by the thermal noise (given that the linearity is not an issue). Consequently, the power consumption has to be quadrupled to improve its resolution by a single bit. Therefore, the preconception was that an ADC with more than 80 dB of dynamic range would be a power-inefficient solution for neural interfaces. The Schreier figure-of-merit (FOMs) is a commonly used metric for characterizing the power-efficiency of high-resolution ADCs [54]. It can be used to fairly compare different architectures and circuit solutions based on the reported signal-to-noise-plus-distortion (SNDR) ratio, Nyquist bandwidth, and power consumption. The latest survey results for low Nyquist frequencies are shown in Fig. 1.4 [55]. This survey shows that there are power-efficient ADC implementations optimized for the 2 kHz signal.
bandwidth, but there is still a gap in the frequency range of low-frequency brain activity (0-300 Hz). Therefore, there is an unexplored opportunity to investigate the power-efficiency of a high-resolution ADC solution tailored for ECoG recording. However, a stand-alone ADC is not sufficient to interface directly with the MEA because the neural electrical activity cannot source/sink the necessary current (or charge) to drive the ADC input. The impedance of electrode-tissue interface (ETI) also depends on the electrode size and material, and it is unlikely to match between the recording channels due to different metabolic conditions. Moreover, the stimulation waveforms can also temporarily affect the ETI, which prevents the use of the same electrode for recording until the electrochemical equilibrium is reestablished. Placing a voltage buffer at the input of the ADC, as shown in Fig. 1.3b, could provide the necessary decoupling from the ETI, but its design requirements would be too demanding to implement due to the high dynamic range. For these reasons, a power-efficient and high-resolution readout for direct coupling to the electrodes, as illustrated in Fig. 1.3c, as well as monitoring the ETI impedance for ensuring high fidelity ECoG recording, are essential.

1.3 Research Objectives

The primary goal of this thesis is to investigate the potential of a high-resolution ADC tailored for ECoG recording at both system and circuit level. In particular, the focus is on \( \Delta \Sigma \) ADC based topologies, which can enable direct coupling to the electrodes. The secondary goal is to investigate architecture solutions for ETI impedance measurements, which can be easily combined with stimulation waveforms, which are used in closed-loop neural interfaces. The following objectives are established to fulfill these goals:

- **Objective 1:** Investigate the application requirements and state-of-the-art solutions for neural recording interfaces and identify a possible solution.
- **Objective 2:** Explore and propose a power-efficient high-resolution ADC topology tailored for ECoG recording, which is competitive with the commonly used approaches.
- **Objective 3:** Develop a complete readout architecture based on the chosen high-resolution ADC topology.
- **Objective 4:** Suggest circuit techniques for minimising the power and area consumption in the readout architecture.
- **Objective 5:** Explore the state-of-the-art systems for bioimpedance measurements and propose a low-complexity solution suitable for neural interfaces.
1.4 Research Contributions

The contributions of these research objectives are listed as follows:

- **Contribution 1 [Paper I]**: A multi-bit high-pass $\Delta\Sigma$ modulator, which can directly convert a chopper modulated signal to the digital domain with high power-efficiency, is proposed. Based on behavioral simulations, minimum requirements have been determined considering the design consideration. The high-pass $\Delta\Sigma$ modulator is implemented using switched-capacitor circuits, which employ inverter-based amplifiers and dynamic biasing. Also, a tree-structured dynamic element matching technique is developed in Verilog, synthesized and verified via simulations. Based on transistor level simulation results with random process and device mismatches, the implemented technique successfully mitigates the 4-bit DAC nonlinearity.

- **Contribution 2 [Paper II]**: A $\Delta\Sigma$ based readout ASIC implementation for ECoG recording systems is analyzed, implemented and experimentally verified. The novelties in the architecture include an embedded instrumentation amplifier inside a $\Delta\Sigma$ modulator loop, and a tracking algorithm to reduce the number of comparators needed in the multi-bit quantizer.

- **Contribution 3 [Paper III]**: An area-efficient switched-capacitor integrator circuit with flicker noise cancellation is proposed and designed. The integrator circuit exploits the thermal noise limit to reduce the capacitor area consumption substantially without significant performance deterioration. Additionally, the proposed circuit includes internal voltage buffering, which can potentially reduce the complexity of the $\Delta\Sigma$ based readout architecture and by doing so decrease the overall power and area consumption.

- **Contribution 4 [Papers IV and V]**: The most well-known impedance measurement methods are reviewed, and an alternative method for impedance spectroscopy is proposed based on adaptive digital filtering. The method was first validated in behavioral simulations, and afterward experimentally verified with a board-level prototype. The proposed measurement method is suitable for monitoring ETI impedance using a three-level excitation waveform, which is commonly found in neural stimulator circuits.

1.5 Thesis Organization

This thesis work is organized into five chapters in the following manner:

- **Chapter 1** has presented the background information for this thesis work. Also, the motivation behind for the thesis work is presented, as well as the objectives and contributions.
1.5. THESIS ORGANIZATION

- **Chapter 2** presents an overview of state-of-the-art neural interfaces. Different approaches based on recently published works are compared and discussed in-depth. Predictions about the developments of readout architectures for neural recording are given and a performance survey is conducted.

- **Chapter 3** is devoted to the high-pass $\Delta\Sigma$ modulator, its similarities and differences compared to the conventional low-pass and band-pass $\Delta\Sigma$ modulators. Also, the power-aware methodology for determining the modulator’s requirements is described. Technical details about the $\Delta\Sigma$-based readout ASIC implementation and measurement setup are discussed in-depth. Potential enhancement of the proposed readout based on the proposed area-efficient switched-capacitor design is investigated.

- **Chapter 4** provides an introduction to the challenges associated with the electrode-tissue interface in neural stimulation and recording. The importance of impedance measurements for implantable neural interfaces is explained, and a method based on the $\Delta\Sigma$ readout is proposed. Lastly, an alternative approach based on the system identification technique is described, which utilizes a wide-band pulse waveform for excitation.

- **Chapter 5** provides concluding statements for the conducted thesis work, describes the development process and suggests possible research directions for further improvements.
Chapter 2

ECoG Neural Interfaces: An Overview

The first observations of ECoG signals in exposed animal brains were reported by Richard Caton in 1875 [56, 57]. The neural recording interface of that period was a Kelvin mirror galvanometer, which had a limited bandwidth of around 6 Hz [58]. Half a century later, in 1929, a psychiatrist by the name of Hans Berger used scalp electrodes and an improved galvanometer to record the first human EEG signal [57]. The intent was to use EEG recordings as a tool to diagnose mental health disorders, which did not catch on until the early 1940s when EEG was used for diagnosing epilepsy. In severe cases, where medication was not providing a sufficient elevation of symptoms, the only option was a surgical removal of the affected neural tissue. In this procedure, the application of EEG/ECoG techniques prior to tissue removal became a golden standard [11]. The specialized operating rooms were equipped with a 6-channel ECoG recording interface, which was modular so that each amplifier could be easily replaced in case of a failure [59]. The silver-chloride electrodes had to undergo a special treatment prior to recording, which involved several electrochemical baths followed by steam sterilization. Hence, the operation protocol consisted of planing out the craniotomy with the help of the EEG technique, followed by a precise isolation via the ECoG technique of the exposed cortex by scanning a 10x10 cm² area [59]. In some cases, when the seizures did not spontaneously occur, electrical stimulation was applied to induce them, which can even be considered as the pioneering steps in neural stimulation. Although the amplitude and bandwidth of neural signals increases with the level of invasiveness, the electrical activity still represents the rhythmic behavior of a group of neurons but with a different ensemble size, also referred to as spatial resolution. Therefore, similar readout architectures can be found across different recording techniques (EEG, ECoG, LFP). However, the focus of this chapter will be primarily on the readout architectures targeting ECoG signals since the design choices, and specifications, are strongly influenced by the input signal properties.
CHAPTER 2. ECOG NEURAL INTERFACES: AN OVERVIEW

Figure 2.1: System architectures used for ECoG recording interfaces can be categorized as a) partially- and b) fully-implantable.

2.1 System Architectures

Over the last two decades, ECoG recording interfaces have improved tremendously thanks to the advancements in application specific integrated circuits (ASICs), but fully-implantable human neural interfaces remain elusive due to long-term implantation challenges. In terms of their system architecture, they can be categorized as shown in Fig. 2.1. The two architectures are labeled as partially- and fully-implantable, while the categorization is based on the integration of electronics with the electrodes [60]. The main appeal of the partially-implantable approach is that the implantation procedure for flexible microelectrode arrays is mature, well-understood, and approved for clinical use in both animal and human studies. Additionally, these studies tend to be relatively short in duration so longevity of microelectrodes or the reliability of the electronics is not a key issue. Thus, biomedical considerations are addressed beforehand, which allows the focus to be moved to the data processing [61], optimal electrode placement [62] and the development of readout architectures, which will be covered later in-detail. On the other hand, the fully-implantable approach is comparatively more challenging not just in terms of circuit design but also in terms of bio-compatibility, hermetic encapsulation, physical mass, and reliability. A fully-implantable system substitutes cables with wireless telemetry, which minimizes the risk of brain infection. A short interconnect between the electrodes and the readout circuitry reduces the inter-channel crosstalk and the susceptibility to interferes. Also, motion artifacts are reduced due to lack of cables, though motion artifacts are not completely eliminated due to the brain movement in the skull. Lastly, this type of system architecture is particularly useful for studies on animals, which can freely roam around their habitats [63]. Neither of these systems would not be possible without custom ASICs, which gradually introduced the necessary advancements, such as high channel density, integration of wireless telemetry, packaging solutions, and neural stimulation.
2.1. SYSTEM ARCHITECTURES

### 2.1.1 Approaches to multi-channel ECoG recording

The first ASIC for ECoG recording was reported in [64]. The custom ASIC was reconfigurable, and could facilitate either EEG, ECoG, LFP or AP recording. The readout employed 16-channels, where each channel consisted of a front-end amplifier and a dedicated ADC as shown in Fig. 2.2, an approach later coined as single-channel recording or biopotential ADC [53]. The electrodes were capacitively coupled using large on-chip capacitors to a front-end amplifier with moderate gain (40 dB) while the quantization was performed by a first-order continuous-time incremental ∆Σ ADC (10-bit). The front-end amplifier employed a simple and power-efficient fully-differential topology with capacitive feedback and pseudo-resistors (MOS transistor in sub-threshold) for band-pass filtering, which was popularized by Harisson et al for AP recording [65]. The experimental results included the in-vivo tests on an anesthetized rat using 1 MΩ tungsten micro-needle electrodes, as well as EEG recording with gel electrodes on human subjects. An improved continuous-time ∆Σ ADC based readout was reported in [53], and it omitted a dedicated front-end amplifier by combining it with the integrator while the offset compensation was achieved with passive high-pass filters.

Around the time of the above mentioned first ASIC, the research endeavors in the circuit design community had divided among the LFP/AP and EEG recording [66–68]. One reason could be that the LFP/AP recording utilized the full range of an in-vivo experiment since rat studies relied on using micro-needle electrodes, which, in turn, provided access to high-frequency neural activity. On the other hand, human ECoG clinical studies were rare and occurred under very special conditions, such as prior to a brain surgery (epilepsy treatment) [6,69]. Considering that ECoG ASICs were initially driven primarily by the application in brain-computer interfaces (BCIs) [38], the lack of popularity can be attributed to the overlap with the EEG based BCIs. Contrary to the ECoG based BCIs, the popularity of ASICs for EEG recording can be attributed to the practicality of testing BCIs and to the...
The next advancement in the development of ECoG recording can be attributed to the CINESIC32 readout architecture [29]. The CINESIC32 featured 32-channels with a time-multiplexing scheme in which 8-channels were quantized by a single ADC with an 8x higher sampling frequency as shown in Fig.2.3. Gradually, the multiplexing approach became synonymous with multi-channel recording term. Similarly to [64], CINESIC32 employed a capacitively coupled front-end amplifier, in addition to an intermediate amplifier, a biquad filter (with unity-gain) and a SAR ADC (typically 10-12-bit). However, the AC-coupling capacitors were placed off-chip, externally, to allow for a higher channel count on the die. The additional amplification (>60 dB) in the signal path provided a low in-band noise performance \(0.7 \mu V_{\text{rms}}\) over \(0.5-300\) Hz, which enabled the use of ultra-low power SAR ADC topology. This type of readout architecture was coined as conventional in the introduction chapter, because it was ubiquitous for many years across all types of neural signal modalities until the closed-loop neural interfaces became more widespread. In fact, a similarly cascaded architecture but with an on-chip 16-bit ADC was used in commercial Intan2000 chips for extracellular neural recording several years later [71]. The popularity of the multiplexing approach originates from the potential to optimize the power and area product by designing a Nyquist ADC with a higher sampling rate to accommodate several channels [36]. Also, a more popular variation of the readout uses a buffer instead of the biquad filter by increasing the ADC oversampling rate [37]. Competitive results have been also achieved with an incremental \(\Delta \Sigma\) ADC, which can be used to accommodate multiplexed channels as long as the internal integrator states and decimator are reset before subsequent recording [72,73]. Although multiplexing is an efficient technique to reduce the area, it also introduces issues with inter-channel crosstalk. Alternatively, the active circuitry can be buried underneath on-chip MIM capacitors, without a negative impact on the performance [53, 74].
2.1.2 Enabling Fully-Implantable ECoG Recording

The first proof-of-concept fully-implantable ECoG neural interface was demonstrated via the WIMAGINE system [30], which is an expansion of the CINESIC32. The system followed the biomedical guidelines set out in [6], and it introduced wireless telemetry and energy harvesting using commercial off-the-shelf modules. Compared to [29], the work in [30] included the electrode array merged at the bottom side of the PCB and antennas for telemetry and inductive coupling, while the entire implant was packaged in a hermetic housing made of titanium. A scaled down version in a cylindric package including the electrodes (25mm x 2mm) was implanted in nonhuman primates for 26 weeks, after which the implant was surgically removed and histological examinations were performed to analyze the suitability of long-term implantation. The preliminary results showed that there were no adverse effects on the brain matter due to implantation. The main bottleneck of the WIMAGINE system was the low data rate due to power constraints. Moreover, the thermal conductivity of the implant dissipated the heat, such that the tissue temperature increased only by 1°C on the titanium side and 0.3°C on the electrode array (bottom) side while dissipating 350 mW, which includes the power of inductive coupling. As a result, the reported power (heat) density was approximately 22 mW/cm², which is about 4x below the safety limit recommended in [75]. As a result, the up-link data rate was peaked at 450 kbps (kilo-bits-per-second), which could facilitate 12-bit sampling at 600 Sps over 64 channels, within a 2 m range.

Even though the data rate of a neural interface is modest compared to a modern broadband network, the up-link of a raw neural recording can be costly in terms of an energy budget for an implantable device. As a result, development of neural interfaces focused on signal feature extraction [38,76,77] and data compression [78–81] to reduce the amount of raw information that needs to be transmitted. For instance, in [38], an on-chip multi-band energy extractor was reported, which employed analog techniques to measure the spectral changes in frequency sub-bands, which are most often used in BCI applications. Similarly, a substantial power reduction can be achieved by extracting the ECoG signal features in the digital domain prior to transmission [76]. Additionally, a near lossless compressive sensing with a compression ratio of 8x was demonstrated in [79]. Despite the efficacy of these techniques, they may not be suitable in emerging applications when the correlation between the ECoG signal and the phenomena under study may not be known a-priori. Similarly, a more power-efficient solution could be achieved simply by trading-off the noise performance in the front-end amplifier by the amount that would be degraded in the compression. Alternatively, a simpler solution can be achieved by exploring different data transmission modulation schemes, such as ultra-wideband radio (UWB) [32,82], amplitude/frequency shift-keying [11,30,32]. For instance, a micro-ECoG implant with on-chip backscattering communication module was reported for the first time in [31]. It featured a 1 Mbps up-link while the transmitter consumed about 1% of the total power consumption, but the backscattering link functioned with no bit-errors up to a distance of 1 cm.
Apart from the shorter telemetry range, the micro-ECoG implant substantially improved upon the overall performance of the WIMATE system, which allowed for further expansion of the recording capacity to 64-channels by not relying on large AC-coupling capacitors to implement high-pass filtering. Instead, the readout was DC-coupled, as shown in Fig. 2.4, via a chopping mixer in front of $C_{in}$. The pseudo-resistors are used only to provide biasing and do not affect the high-pass filtering. More importantly, a digitally-assisted servo loop was utilized for the first time in ECoG recording to compensate the electrode offset. Resulting in approximately an order of magnitude lower area consumption per channel compared to state-of-the-art. Moreover, a voltage controlled oscillator (VCO)-based ADC was employed to fully exploit the advantages of technology scaling in 65 nm CMOS process, which further improved the miniaturization of the readout architecture. Although the VCO ADC was implemented with 13-bit resolution, due to VCO non-linearity and the lack of on-chip compensation, the achieved effective-number-of-bits was approximately 8-bit. Alternatively, a multiplying SAR ADC designed for 8-bits was used in [32], which featured inter-channel gain equalization while maintaining a competitive area per channel. To maintain a high recording fidelity while employing a digital servo loop, a high-resolution DAC is required, such as a $\Delta\Sigma$ DAC [31] or a current-steering DAC [32]. Apart from the electronics miniaturization, the $\mu$ECoG implant featured a custom 4x4 mm$^2$ electrode array composed of a bio-compatible material (Parylene-C). The flexible array was bonded to the rigid PCB surface, which proved to be a formidable challenge. However, the authors concluded that the bonding process could be potentially adapted directly to die-to-flexible-substrate to further reduce the implant form-factor.
The next approach in miniaturization was the integration of the electrode array and antenna on the same die as the active circuitry in the ENIAC chip [11]. The electrodes were implemented in the top metal layer, and the antenna was placed around the circumference of a 3x3 mm\(^2\) area. However, due to the bio-incompatibility of the semiconductor materials, the chip needed to be completely encapsulated in TiO\(_2\)/ZrO\(_2\) as shown in Fig. 2.5a. Hence, the electrodes were AC-coupled with the tissue through the encapsulation layer, which had a high relative dielectric constant to ensure high capacitive coupling (1 nF). An alternative post-CMOS processing for on-chip electrodes was shown in [83], in which the passivation layer was exposed to achieve a DC-coupling between the top metal layer and the neural tissue while the bio-compatibility was ensured by platinizing the exposed aluminum, as shown in Fig. 2.5b. A potential packaging solution, which is inspired by the aforementioned approaches, could be to utilize flip-chip bonding, as shown in Fig. 2.5c. The advantage of this approach would be the compatibility with both the semiconductor and the electrode processing, while the encapsulation and bio-compatibility could be assured with flexible polymers. In this way, the electrode geometry can be adjusted to the specimen’s brain without constraining the die size, while the rigid silicon substrate can be buffered from the soft neural tissue resulting in improved longevity of the implant. However, one of the issues with this proposed packaging approach is that polymer materials do not provide a sufficient level of encapsulation compared to titanium [84]. Nevertheless, this approach illustrates one research direction for neural interfaces, in which the focus is given to solving the integration challenges of hybrid technologies.
2.1.4 Integration of Neural Stimulation

In parallel with the development of ASICs for neural recording, the neural stimulation circuits (neurostimulators), such as the aforementioned ENIAC system, emerged as a promising solution for treating neurological disorders in cases when medication and/or surgical treatment was ineffective [7, 85, 86]. For instance, a neurological disorder, such as an epileptic seizure, if detected in a timely manner, can be inhibited with electrical stimulation before exhibiting the symptoms [14]. This type of feedback configuration is coined as a closed-loop neural interface, and it has the potential to be superior in terms of efficacy and power consumption than an open-loop configuration [85]. However, due to limited resources on-chip, the integration of a low-latency decision making DSP with high sensitivity and specificity is a key challenge for closed-loop neural interfaces [86]. Consequently, a high-channel neural interface usually employs an off-chip DSP due to computational demands at the cost of increased latency. Additionally, stimulation circuits require a high-voltage CMOS process, e.g. thicker gate-oxide transistors, due to the high-impedance of the electrode-tissue interface. These relatively high-swing stimulation waveforms (e.g. hundreds of millivolts) can couple to the recording electrode via crosstalk, tissue conduction or substrate coupling and saturate the analog front-end [53], which, in turn, increases the latency by the duration of the recovery (settling) time. A workaround solution is to reset the pseudo-resistors [15], but at the cost of deteriorating the high-pass cut-off corner and introducing ripples in the continuous-time operation. Alternatively, an artifact cancellation technique based on adaptive digital filters can be used to estimate the electrode-tissue impedance and reduce the stimulation artifacts [87, 88]. However, the technique requires high-resolution recording prior to digital cancellation. Therefore, there is an increasing interest for high-resolution readout architectures, which can preform neural recording during stimulation [7, 89]. In addition, apart from the deep-brain and extracellular stimulation [90, 91], which employ micro-needle electrodes, a closed-loop neural stimulator is typically interfaced with the brain using a flexible electrode array. This is motivated by the seizure detection algorithms, which process the synchronous activity from a region of neurons [85]. Thus, neurostimulators are reinforcing the research importance of ECoG neural interfaces with a medium number of channels (≈ 16) to enable on-chip DSP, while at the same time changing the readout architecture to withstand the large in-band interferes. In fact, the amplifier topology with pseudo-resistor is slowly being phased-out due to its limited linearity performance and offset voltage induced by leakage [52]. Instead, duty-cycled resistors [52, 92] and the previously mentioned digitally-assisted DC servo-loop are becoming preferred solutions. The appeal of duty-cycled resistor is that it can be used as a substitute for a pseudo-transistor though at the cost of an additional 1 MΩ polysilicon resistor. Comparatively, digitally-assisted readout architectures do not require large time constants on-chip, and can better utilize the advantages of technology scaling.
2.2 Future Perspectives and Summary

The ongoing development of ECoG neural interfaces can be attributed to the importance of treating neurological disorders. For instance, the socioeconomic impact of brain research has been identified and supported by the European Commission through funding programs, such as Horizon 2020 [94]. As a result, the research on closed-loop ECoG interfaces is becoming more popular in recent years [95]. Their rapid technological development is also raising questions about ethical considerations and their consequences in the future on the society [96]. For instance, apart from the medical benefits, it is possible to imagine that this technology could bring upon brain augmentation in healthy individuals. Thus, it will be important to form a consensus about these ethical issues moving forward, but perhaps a more prompt and practical issue is the lack of specification standardization.

Table 2.1: Performance summary of the state-of-the-art neural interfaces.

|-----------|-----------|--------------|-----------|------------|-------------|------------|-------------|-------------|------------|----------|--------------|-------------|---------|---------|-------------|-----------|----------|---------|--------------|-----------|----------------|------------|--------|---------------|
The summary of the discussed ECoG neural interfaces is presented in Table 2.1. It highlights the most notable performance metrics from the perspective of main building blocks, such as the readout architecture, DSP, wireless communication and power transfer. For instance, the ASICs have been often implemented in a 0.18 $\mu$m CMOS process mainly for the benefit of analog circuits, e.g. AFE. The reported power consumption varies depending on the system complexity, and it continuously reduces over time by using emerging power-efficient approaches. Additionally, the channel density has aggregated at 64-channels for ECoG, though the aforementioned advancements with on-chip electrodes may indicate a distributed sensor network approach in the future. Although, it is difficult to estimate an optimal number of electrodes, the works shown in Table. 2.1 with on-chip DSP, indicate that a low (8) to medium (16) number of active channels can be sufficient. This depends on the current integration capabilities for a fully-implantable system. Moreover, closed-loop neural interfaces require high effective-number-of-bits (ENOB) due to the aforementioned stimulation artifacts, which imposes a large bit-size logic operation that can further tax the computational on-chip resources.

The shift from the analog dominant signal conditioning to digital feature extraction is pushing the development toward smaller technology nodes. Consequently, the VCO-based readout architecture with DSL is becoming particularly popular in a smaller technology node, e.g. 65 nm. However, due to the non-linear behavior of a VCO ADC, a digital on-chip compensation is required. Admittedly, this doesn’t violate the affinity toward technology scaling of the topology, but the consumed die area diminishes the area advantage [52]. Similarly, a SAR ADC can be considered as a scalable ADC topology, but the DAC mismatches make it impractical to achieve an ENOB of more than 10-bit. Even in the case of 1-bit incremental $\Delta \Sigma$ ADCs [72,73], the ENOB performance is comparable with that of the compensated VCOs. On the other hand, an even higher ENOB has been demonstrated with multi-bit $\Delta \Sigma$ ADC [86,92], which can enable artifact tolerant neural interfaces.

Despite the application of high-resolution ADCs in ECoG neural interfaces, the readout architectures still require a dedicated AFE to provide low-noise amplification, low THD, and high CMRR/PSRR, as it can be seen in Table 2.1. Typically, the AFE input referred noise ranges from 1 to 5 $\mu$V$_{rms}$. Such low levels of noise are usually needed in EEG applications due to low signal amplitudes. However, the root-mean-square of a white noise source is the same as its standard deviation ($\sigma$). This implies that the noise amplitude can reach values as high as $6\sigma$. Apart from the low-noise performance, the AFE provides usually a voltage gain between 30-60 dB, which considerably relaxes the noise requirements on the remaining blocks in the readout. As a result, the neural signal is amplified to the ADC full-scale voltage, which introduces nonlinearities that are reported using the total-harmonic distortion (THD) parameter. Although noise and linearity are equally important for recording fidelity, the THD is generally a byproduct of the AFE loop-gain rather than the primary design constraint. Commonly reported values of THD are between 0.1% to 1%, which, independently of the ADC, limits the readout to approximately an ENOB of 8- to 5-bit, respectively. Lastly, the power supply and common mode
rejection ratios (PSRR/CMRR) are important parameters for rejecting the disturbances, which are picked up by the electrodes or power rails. For instance, in EEG recording, a CMRR in the order of 100 dB is needed to reject the 50/60 Hz signal from the power grid, though smaller value around 70 dB can be tolerated in a fully-implantable ECoG recording. On the other hand, in a partially-implantable approach, the shielding effects of the human skull are lost and the long electrode interconnects are prone to picking up interferes and motion artifacts, which implies a CMRR requirement similar to non-invasive EEG recording. Based on the results for PSRR in Table 2.1, a value of at least 70 dB should be sufficient for rejecting the noise picked up from the harvested wireless power.

The power demands of a closed-loop neural interface require an abundant energy source that can facilitate long-term operation of the aforementioned building blocks. For instance, these demands can be facilitated via wireless power transfer. The frequency of electromagnetic coupling determines the antenna form-factor and tissue absorption rates. Based on the works in Table 2.1 and the safety limits for power emission of electromagnetic fields in the human body in [97], a good trade-off is achieved in the range of 200 MHz to 300 MHz. At these frequencies, the antenna length is still small enough (e.g. a few millimeters) that it can be folded around the electrode array [11,31]. Ideally, the same antenna is reused for both power transfer and wireless telemetry, which reduces the form-factor of the overall systems but at the same time constricts the transmission to the coupling frequency. Typical power emission levels from the energy source are up to hundred milliwatts, from which only 1-2 mW are harvested by the neural interface. Assuming that the future development focuses on 8-16-channel readout architectures, the power budget per channel distribution will be around 125 µW. Considering the overall system complexity and the demand for high-resolution recording, the efficient utilization of this limited resource will be paramount.

In this chapter, relevant advancements in ECoG neural interfaces have been presented. The primary focus of this chapter was placed on the readout architecture development though other aspects, such as wireless telemetry and packaging, have been discussed. The advent of neural stimulation and on-chip feature extraction has created a demand for high-resolution DC-coupled neural recording. However, the limited power availability is still a bottleneck for a complete system integration. In the following chapter, the focus will be placed on investigating and proposing power-efficient solution to achieve a high-resolution and DC-coupled readout architecture.
Chapter 3

$\Delta \Sigma$-based Architecture for ECoG Recording

The previous chapter has provided a general overview of ECoG neural interfaces, the challenges of fully-implantable integrated ECoG interfaces, and identified the need for high-resolution recording in closed-loop neural stimulators. The existing solutions have demonstrated 12-ENOB by employing complex digital linearization techniques in ADC topologies with medium resolution. The achieved ENOB may not be enough in some neural stimulation applications [98], which is motivating the development of ECoG based neural interfaces toward $\Delta \Sigma$-based readouts. The circuit specification of a high-resolution ADC can be established based on the performance summary from the previous chapter, specifically, the AFE input referred noise of around 5 $\mu V_{rms}$ over a 300 Hz bandwidth. In most neural stimulation scenarios, the differential artifacts can exhibit up to 200-mV$_{pp}$, while common-mode artifacts can be up to 700-mV$_{pp}$ [98]. Hence, an input signal swing of up to 480-mV$_{pp}$ can be considered large enough to cover most cases. The larger the ratio between the input signal and noise, the higher the dynamic range and consequently the ENOB. However, each additional bit leads to quadrupling of the ADC’s power consumption. In comparison, the ADC bandwidth linearly increases the power consumption to maintain the same power-efficiency (e.g. figure-of-merit from Chapter 1). Therefore, it is important to investigate the power requirements of a high-resolution ADC for the specifications mentioned above. The $\Delta \Sigma$-ADC is the most well-known solution for high-resolution applications with low to medium signal bandwidths [54,99,100]. Also, a $\Delta \Sigma$-ADC provides a lot of design flexibility concerning its order, oversampling and quantizer resolution, which has to be considered when determining the minimum power consumption for the constraints above [101]. Since the total received wireless power amounts to about 125 $\mu W$ per channel, the power allocation is competitive between the wireless communication, on-chip DSP, and the readout. Therefore, the readout has to target power consumption of around 40 $\mu W$ assuming an equal power budget distribution. At the
same time, a ΔΣ-ADC requires an AFE to interface with the electrodes without deteriorating the recording fidelity. Dividing the design challenge between the AFE and ADC is a good starting point, but ultimately it is essential to have an efficient power utilization across the complete readout architecture.

In this chapter, the high-pass ΔΣ topology from [Paper I] will be elaborated in detail and supported with a power-aware loop-filter design methodology. After that, the proposed ΔΣ-based readout ASIC implementation will be expanded and complemented with a detailed description of the measurement setup. Lastly, a potential enhancement will be shown based on the proposed circuit technique from [Paper II].

3.1 High-pass Delta-Sigma Modulator

A ΔΣ-ADC, also referred to as ΣΔ-ADC, employs several techniques, such as oversampling, noise-shaping, and decimation, in order to achieve a high-resolution conversion. Oversampling is performed thanks to a much higher sampling frequency relative to the Nyquist bandwidth. Noise-shaping is achieved by employing negative-feedback around the quantizer, as shown in Fig. 3.1. Decimation refers to digital filtering, which removes the out-of-band noise, and reduces the sample rate. As it can be seen in Fig. 3.1, a ΔΣ-ADC consists of a ΔΣ modulator and a decimator. The ΔΣ modulator is a combination of analog and mixed-signal circuits. The loop-filter is the core analog block of a ΔΣ modulator. Depending on the loop-filter type, the ΔΣ modulator can be categorized as follows:

- Low-pass (LP) ΔΣ modulator
- Band-pass (BP) ΔΣ modulator
- High-pass (HP) ΔΣ modulator

Out of the three architectures, the LPΔΣ modulator is the most well-known. The low-pass prefix corresponds to the frequency response of the signal transfer function (STF), which is approximately unity at DC. On the other hand, in a BPΔΣ modulator, the STF is unity around $f_s/4$ while in the case of the HPΔΣ modulator, the STF is unity at $f_s/2$, where $f_s$ is the sampling frequency. Although
3.1. HIGH-PASS DELTA-SIGMA MODULATOR

Figure 3.2: a) Frequency response of the LP/BP/HP STF; b) the power spectral density of the ECoG signal before and after applying the chopping technique.

the ECoG frequency range coincides with the low-pass STF, the LP$\Delta\Sigma$ modulator may not be the most power-efficient solution when considering that the ECoG signal is usually up-converted in frequency to mitigate the impact of flicker noise as shown in Fig. 3.2. A BP$\Delta\Sigma$ or an HP$\Delta\Sigma$ modulator can provide potentially more efficient utilisation of the oversampling technique compared to a conventional LP$\Delta\Sigma$ modulator for a narrow-band input signal that is offset by a carrier frequency. Moreover, between the two modulators, it is more advantageous to employ an HP$\Delta\Sigma$ modulator since its loop-filter is constructed using high-pass filters, which are simpler circuits compared to resonators in the BP$\Delta\Sigma$ modulator.

To understand this circuit complexity, it is necessary to briefly explain the differences in the noise-transfer-functions (NTFs) between these modulators. For instance, the discrete-time NTF of a first-order LP$\Delta\Sigma$ modulator is equal to:

\[
\text{NTF}_{\text{LP}}(z) = \frac{z - 1}{z}. \tag{3.1}
\]

where \(z = e^{-2\pi f_{\text{in}}/f_s}\), and \(f_{\text{in}}\) is the input signal frequency. The NTF\(_{\text{LP}}(z)\) has one zero at \(z = 1\), which corresponds to a zero at DC, and a pole at the origin as shown in Fig. 3.3. The NTF\(_{\text{LP}}(z)\) has a high-pass characteristic, which can be confusing to relate with the LP$\Delta\Sigma$ modulator, but the naming convention is related to the STF. For a dynamic input signal, the quantization noise can be approximated as a white noise source, which is then shaped by a high-pass characteristic. Nevertheless, the total integrated quantization noise remains unaffected by the high-pass filtering. Hence, the term noise-shaping refers to the change in power spectral density of the quantization noise. In order to achieve high-resolution performance, all of the out-of-band noise has to be removed in the digital domain by the decimator without affecting the low-frequency input signal.

Having NTF\(_{\text{LP}}(z)\), the NTF\(_{\text{HP}}(z)\) of a BP$\Delta\Sigma$ modulator can be found by sub-
substituting \( z \) with \(-z^2\) in (3.1), which equals to:

\[
\text{NTF}_{\text{HP}}(z) = \frac{z^2 + 1}{z^2} = \frac{(z + i)(z - i)}{z^2}.
\]

Compared to (3.1), the expression in (3.2) is a second-order transfer function but the degree of noise shaping is the same as that of the NTF\(_{\text{LP}}(z)\). Even though there are two zeros at \( z = \pm i \), they are split apart in the complex plane (see Fig. 3.3b). Hence, even when the signal is at the chopping frequency \( f_{\text{chop}} = \frac{f_s}{4} \), the quantization noise is attenuated by a single zero. Thus, a disadvantage of a BP\(\Delta\Sigma\) modulator is that it requires two integrators (a resonator) to achieve the same order of noise-shaping. As a result, the corresponding circuit implementation requires double the amount of amplifiers, which makes the BP\(\Delta\Sigma\) modulator comparatively a power hungry solution.

Finally, the NTF of a HP\(\Delta\Sigma\) modulator can be found by substituting \( z \) with \(-z\) in (3.1), which equals to:

\[
\text{NTF}_{\text{HP}}(z) = \frac{z + 1}{z}.
\]

As it can be seen from (3.3) and Fig. 3.3c, the NTF\(_{\text{HP}}(z)\) is a single-order transfer function with a zero at \( f_s/2 \), and a pole at origin, which provides a low-pass frequency response. Moreover, the NTF\(_{\text{HP}}(z)\) is symmetric to the frequency response of the NTF\(_{\text{LP}}(z)\) with respect to the \( f_s/4 \) point. Therefore, the two functions are similar mathematically and provide the same order of noise-shaping. Also, an equivalent HP\(\Delta\Sigma\) modulator requires the same number of amplifiers, and can reuse the same loop-filter architectures developed for a LP\(\Delta\Sigma\) modulator with minor modification. In conclusion, the HP\(\Delta\Sigma\) modulator combines the benefits of the other two modulators, which makes it a promising power-efficient solution for converting a chopper modulated ECoG signal with a chopping frequency of \( f_{\text{chop}} = \frac{f_s}{2} \).

### 3.1.1 Design Considerations

An HP\(\Delta\Sigma\) modulator has three design variables to achieve a desired resolution: the loop-filter order, oversampling ratio and the quantizer resolution. Depending
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Figure 3.4: A second-order loop-filter implemented with a) feedforward and b) feedback topology.

3.1.1.1 Loop-filter Order

The loop-filter provides in-band attenuation of the quantization noise due to its gain and the negative feedback around the quantizer. The loop-filter is generally implemented as a cascade of simpler building blocks, which provide the necessary gain and determine the order. Even though high-order loop-filters compromise the stability of a \( \Delta \Sigma \) modulators, they are particularly beneficial in applications where oversampling is impractical due to the high-frequency content of the input signal. In comparison, a single-order loop-filter is unconditionally stable, but it is prone to generating pattern noise (limit cycles) which violates the assumption that the quantization noise has a uniform power spectral density.

As shown in Fig. 3.4, a higher order loop-filter can be constructed using either a feedforward or feedback topology. Feedforward topology has more relaxed output swing requirements for the amplifiers that implement the loop-filter than the feedback topology, which makes the feedforward topology more popular in low-power applications [99]. From the circuit implementation aspect, the feedforward topology requires an additional analog adder for summing the forward paths while the feedback topology requires additional DACs. More importantly, the STF of the feedforward topology tends to exhibit peaking in the frequency response, which

on the chosen set of variables, the overall power consumption can vary due to different circuit implementation requirements.
may amplify unwanted interference. A simple workaround for this issue is to feedforward the input signal directly to the adder, which ensures a unity-STF across the whole Nyquist frequency range regardless of the loop-filter.

An HPΔΣ modulator with a unity-STF relaxes the amplifiers’ linearity requirements because they do not have to process the full amplitude of the input signal, but rather just the quantization noise. Furthermore, the feedforward topology implies that the first amplifier has the most stringent circuit requirements since the gain of the other amplifiers attenuates the non-idealities of subsequent amplifiers. Hence, the power consumption of the loop-filter will be primarily determined by the circuit specifications of the first amplifier. Since the application requirements limit the amplifier’s thermal noise, ideally the slew-rate and gain requirements should be fulfilled without expending additional power.

Based on these considerations and the analysis results presented in [Paper I], a second-order loop-filter with a feedforward topology and unity-STF was chosen. As a result, simple single-stage amplifiers were sufficient to meet the modulator requirements.

### 3.1.1.2 Oversampling Ratio

The oversampling ratio (OSR) determines the sampling frequency for a defined input signal bandwidth, which impacts the power spectral density of the quantization and thermal noise after sampling. However, the two noise sources are affected differently with the OSR. For instance, the signal-to-quantization-noise-ratio (SQNR) improves by approximately 9 dB in a first-order and by 15 dB in a second-order loop-filter by doubling the OSR. On the other hand, the signal-to-noise-ratio (SNR) improves by 3 dB by doubling the OSR since there are no benefits of noise-shaping regarding thermal noise. The trade-off with increasing the OSR is that for a defined capacitive load, the HPΔΣ modulator requires amplifiers with a larger slew-rate and gain-bandwidth product (shorter settling-time). Although increasing the OSR improves SNR, the upper OSR limit is indirectly imposed by the power-efficiency of transistors in the weak inversion region. Since the transistor transconductance changes linearly with the biasing current in weak inversion, the power consumption of the loop-filter will scale linearly with the sampling frequency and the OSR.

The HPΔΣ modulator shown in [Paper I] uses an OSR of 256, which is an over-design concerning SQNR (≈110 dB based on behavioural simulation without process and device mismatch). On the other hand, regarding SNR (≈98 dB), the chosen OSR is a trade-off between the size of the sampling capacitors (thermal noise) and sampling frequency (power dissipation).

### 3.1.1.3 Quantizer Resolution

The quantizer is often a single-bit ADC implemented as a comparator for simplicity, which also implies an inherently linear 1-bit DAC. As a result, the power of the quantization error is $e^2_q = V_{FS}^2/12$, where $V_{FS}$ is the DAC full-scale voltage. Gen-
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Generally, \( V_{FS} \) can be a significant fraction of the analog supply voltage, which imposes challenging amplifier slew-rate requirement under a low-power budget. On the other hand, a multi-bit quantizer can avoid this issue by decreasing the quantization error power by orders of magnitude (e.g. \( e_{qs}^2 = \frac{1}{2} \frac{V_{FS}^2}{12} \) for a 4-bit quantizer). However, a multi-bit quantizer implies a multi-bit DAC, which is inherently nonlinear due to variations in the quantization levels and resolution is generally limited to 4-6-bits. Even with proper layout techniques, the ENOB of a DAC peaks at 10-bits due to process and devices variations on the die. To circumvent these limitations, digital linearization techniques, such as dynamic element matching (DEM), are applied to boost the DAC linearity.

The tree-structured DEM encoder shown in [Paper I] consists of combination logic and shift registers, which makes its power consumption negligible when considering the power reduction benefits of using a 4-bit quantizer.

3.1.2 High-pass Filter Design Methodology

This subsection describes in more detail the design methodology of the HPΔΣ modulator shown in [Paper I], which adheres to the considerations regarding the loop-filter, oversampling and quantizer resolution. The core building block of the presented HPΔΣ modulator is a switched-capacitor high-pass filter, which is labeled as \( H_1(z) \) in Fig. 3.4a. As shown in [Paper I], the total input referred noise of the employed high-pass filter is strongly influenced by the product of the sampling capacitance, \( C_{s1} \), and OSR, and the coefficient of the first high-pass filter, \( b_1 \). At the same time, the OTA’s equivalent transconductance, \( G_m \), is a function of the gain-bandwidth (GBW) product and the equivalent loading capacitance, \( C_{eq,int1} \), both of which are a function of OSR, \( C_{s1} \), and \( b_1 \). Moreover, the GBW and \( C_{eq,int1} \) dependencies with respect to \( b_1 \) are given by (3.4) and (3.5):

\[
\text{GBW} = \frac{1 + b_1}{2\pi \tau},
\]

where \( \tau \) is the required settling time, which is obtained from behavioral simulations.

\[
C_{eq,int1} \approx C_{s1}(1 + 0.05 \cdot (1 + b_1^{-1})) + 0.21 C_{s1} \cdot (1 + b_1^{-1}).
\]

The product of \( C_{eq,int1} \) and GBW directly impacts the OTA transistor’s biasing current, \( I_{BIAS} \), in the signal path. Both the slew-rate (SR), and GBW, increase with \( b_1 \), but, at different rates as it can be seen in Fig. 3.5. Consequently, a crossing point occurs, after which, a higher \( I_{BIAS} \) current is required to maintain the SR than the GBW specification for the amplifier topology in [Paper I]. Thanks to the 4-bit quantizer, the required \( I_{BIAS} \) for the SR is less than the value necessary for the GBW as long as \( b_1 < 0.7 \). On the other hand, a higher value of \( b_1 \) is better for noise performance. In [Papers I and II], \( b_1 \) is set to 0.6 as a trade-off between minimum \( I_{BIAS} \) (for \( b_1 = 0.5 \)) and noise performance.

Apart from the settling-time constraints on \( G_m \), the open-loop gain, \( A_{dc} \), of the OTA can also affect the power consumption. Since a switched-capacitor, \( C_{eq,int1} \),
can be approximated as an equivalent resistor \((f_s C_{eq,int})^{-1}\), where \(f_s\) is the sampling frequency, the open-loop gain of the OTA may be affected by the equivalent switching-capacitive load in the following manner:

\[
A_{dc} \approx \frac{G_m}{f_s C_{eq,int}}
\]

(3.6)

Ideally, \(G_m\) should be sufficient to meet the amplifier DC gain, \(A_{dc}\), requirement without further increasing \(I_{BIAS}\). The length of the transistors in the signal path is set to approximately 1 µm to minimize the reduction of \(A_{dc}\). Additionally, as it can be seen in [Paper I], there is a sufficient margin in SQNR to tolerate a reduction in \(A_{dc}\) due to a finite equivalent output resistance.

The loop-filter has been implemented with single-stage OTAs, and it consumes approximately half of the total modulator power. Considering the constrictions placed on the OTAs, the minimum \(I_{BIAS}\) is chosen. However, the loading conditions in the high-pass filter change depending on the clock phase. In particular, during the sampling phase, \(C_s1\) is disconnected from the amplifier, which intuitively indicates that the capacitive loading will reduce. The analysis given in [Paper I] concluded that the equivalent load decreases by a factor of three. Therefore, by dynamically adjusting \(I_{BIAS}\) to the corresponding clock phase, the loop-filter power consumption can be reduced by approximately 23%.

### 3.2 ASIC Implementation

The promising power-efficiency achieved by the proposed HPΔΣ modulator paved the way toward the ΔΣ-based readout ASIC presented in [Paper II]. The two significant improvements were the integration of a high dynamic range instrumentation amplifier (IA) and a low power tracking ADC shown in Fig. 3.6. Compared
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Figure 3.6: Block diagram of the ∆Σ-based readout ASIC architecture.

to [Paper I], $C_{s1}$ is reduced by half in [Paper II], and the input amplitude is reduced from 300 mV to 240 mV due to the IA linearity limitations.

The primary design challenge in the IA was the linear buffering of the up-converted (chopped) input signal at 76.8 kHz while driving a 6.6 pF load. Based on the results in [Paper I], the peak signal-to-noise-and-distortion-ratio (SNDR) of the proposed HPΔΣ modulator (with process and device mismatches) is around 95 dB, which had to be matched by the THD of the IA. Half of the power was relocated from the loop-filter to the IA by employing a smaller $C_{s1}$, and thus smaller $I_{BIAS}$, to achieve the targeted linearity. Moreover, due to the limited voltage headroom in the IA, it was not possible to process 480 mVpp while maintaining the THD specification. Therefore, the IA was embedded in the ∆Σ-loop, as illustrated in Fig. 3.6), to take advantage of the low-swing voltage environment provided by the 4-bit quantization.

The low IA output swing is achieved thanks to the integration of a current-steering DAC. The DAC from Fig. 3.6 was made part of the IA’s biasing network without adding additional transistors. Each unit element of the current-steering DAC had to be implemented using a cascoded current source so that the output resistance does not limit the linearity. The following formula from [102] was used to estimate the required output resistance:

$$R_u > R_{in} \cdot 2^{(2 \cdot ENOB - 2)}$$

where $R_u$ is the shunting resistance of each unit element, and $R_{in}$ is the equivalent input resistance looking into the source of the first stage. Additionally, the dimensions of a unit element had to be sufficiently large to maintain a 1% standard deviation so that the DEM encoder could suppress the DAC distortion. Monte Carlo simulations indicated that due to identical biasing conditions each unit-element was exhibiting correlated mismatches. These simulations lead to better than expected linearity of the DAC, even without DEM, due to the limitations of the transistor models and simulation tools. However, when replicating the standard deviation in a Verilog-AMS model of the DAC, the THD was much larger because each element
had a different seed for the random function. Apart from reducing the process and device variation effects, the transistors dimensions, in particular, the W/L aspect ratio, also impact the noise performance. For instance, the required transistor area can be achieved by increasing the width of the unit element at the cost of increasing its current noise. The W/L ratio was chosen so that the transconductance is approximately 80% of its value in weak inversion region, \( g_{m,\text{max}} \), for the same biasing current, which represents a trade-off between noise and mismatches. Decreasing the W/L ratio further leads to larger overdrive voltage, which can force the unit elements to the ohmic region of operation due to limited voltage headroom. Moreover, transistors with a small W/L ratio are difficult to layout since they have to be broken in length and connected in a cascode, which complicates the routing scheme. The 80% of \( g_{m,\text{max}} \) proposed approach leads to transistors that can be fragmented into several smaller transistors. For instance, ten unit-elements and the diode-connected reference were divided into 110 smaller transistors and patterned as shown in Fig. 3.7. The transistors were placed in a common-centroid, such that each multiple of a unit-element occurs once in a row and a column. In this way, the mismatch error was spatially distributed between the elements to avoid any inter-element correlation, which was a necessary consideration for the DEM technique. Moreover, to reduce any systematic error due to a voltage drop across wiring, the source connection was tapered to account for the varying current densities. On the other hand, the cascode had to boost the shunting resistance of a current source to \( R_u \) in (3.7) while maximizing the voltage headroom for the input signal swing. The dimensions of the cascode were limited by the parasitic capacitance introduced at the source of the first stage due to IA stability consider-
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Figure 3.8: Half-circuit schematics of the a) first, b) second, and c) third iteration of the IA signal path.

As a result, each unit element is implemented with a dedicated cascode to save headroom. The $I_{\text{unit}} = 850$ nA element value is a trade-off between noise and power, which directly implies that $R_1$ value, and consequently $R_2$, are fixed for a desired DAC full-scale ($10I_{\text{unit}}R_1$).

After addressing the DAC implementation issues, the second obstacle was determining an optimal signal path for the IA. The conventional three opamp topology was eliminated early on due to a large number of amplifiers and resistors [103]. Instead, a more power-efficient and simpler current feedback IA topology was investigated [70]. All the design iterations are shown in Fig. 3.8. The first iteration consists of a PMOS and an NMOS common-source stage with source degeneration as shown in Fig. 3.8a. The issue with this approach was that the output common-mode level was too low for the tail current source of the second stage. The second iteration employed a source-follower to introduce a degree of freedom in setting up the output common-mode level and an additional current-mirror stage. The problem with this iteration was the additional biasing current, $I_{DS4}$, in the mirroring stage, which was required to convert the current back into output voltage, $V_{out}$. The biasing current of $M_1$, and therefore $M_3$, is dictated by the noise specifications. Since the $(W_4/W_3)$ ratio is equal to unity, this implies that $I_{DS4} = I_{DS3} = I_{DS1}$. Therefore, the second signal path consumes significantly more power than the first one. Additionally, it is also more non-linear due to the limited loop-gain of a current mirror. The third iteration revises the initial signal path with a folded-cascode to increase the output common-mode level at the cost of additional noise. The biasing current of $M_2$ in Fig. 3.8c can be less than $M_1$ to save power, provided that the equivalent resistance looking into the source of $M_2$ is low enough so that the pole at node $V_X$ does not affect stability. Lastly, the third iteration is the most efficient at utilizing the biasing of the unit elements from the current-steering DAC, which is connected at node $V_{DAC}$ to boost the transconductance of $M_3$. The main benefit of this topology is that the two stages mutually boost their loop-gains beyond that.
of a single common-source stage thanks to the current feedback. In this way, a high loop-gain and therefore linearity can be achieved in a power-efficient manner.

The final signal path has four internal nodes, which introduce four poles. The impact of poles at nodes $V_X$ and $V_{DAC}$ has been already mentioned. The $V_Y$ node is a high impedance node, so the corresponding pole can be made dominant with additional capacitance. Unfortunately, this implies that some of the IA’s loop-gain has to be traded off for stability. Since the output load, $C_{s1}$, is defined by the thermal noise limit in the first high-pass filter, a series resistor $R_3$ is added to $C_{s1}$ to introduce a left half plane zero. In this way, a phase margin of 70° can be achieved without modifying $C_{s1}$. The addition of $R_3$ also improves the total integrated noise across $C_{s1}$ by reducing the effective noise bandwidth.

The addition of the IA to the $\Delta\Sigma$-loop provided a buffered output of the quantization error, which is generally not accessible in a $\Delta\Sigma$ modulator. Hence, it was possible to track the smaller magnitude of the quantization error at the cost of a minor hardware overhead. The analysis given in [Paper II] indicated that four comparators were sufficient to substitute the operation of a 4-bit flash ADC. The cost was additional digital logic to maintain the tracking operation at the chopping rate. The Verilog code for the tracking ADC was integrated into the DEM encoder to take advantage of the standardized digital design flow. A custom triggering scheme was required to enable the operation of the tracking ADC. As it can be seen in Fig. 3.9, the first triggering pulse, $CLK_1$ is generated when all of the comparator outputs, $Q_{<3:0>}$, reach their corresponding asymptotic values. The subsequent pulses, $CLK_2$ and $CLK_3$, are then delayed using inverters with long-channel transistors, which are loaded with MOS-capacitors as shown in Fig. 3.9. In this way, the delay cells can be placed-and-routed alongside standard digital logic.

Another critical detail toward enabling the tracking ADC was the matching of $R_2$ in the IA (see Fig. 3.6) to the resistor ladder in the flash ADC. Since $R_2I_{\text{unit}}$ defines the decision levels in the DAC, $R_2$ needs to match with the resistor ladder to replicate the functionality of a 4-bit flash ADC. Hence, the same layout is used in both resistors to improve matching. As it can be seen in Fig. 3.10, the voltage reference (VREF sub-block) is placed nearby the IA, such that resistors are in proximity to each other, with the same alignment and orientation. Unfortunately, this implies that the reference voltage has to be routed back to the comparators. As a result, wire cross-coupling and n-well isolation were employed to attenuate
inter-block interference and substrate noise. Also, the feed-forward paths for the IA, HPF1 and HPF2 in Fig. 3.10 were routed similarly.

In addition to fulfilling the matching considerations in the tracking ADC, a well-thought-of floorplan can reduce the time spent on top-level routing and cross-talk between noise sensitive building blocks. The critical aspects of a floorplan are the knowledge about the area, interconnection and functionality of the sub-blocks. The area of the sub-blocks can be estimated by comparing the dimensions of transistors and passive devices at the schematic level. Also, by planning out the arrangements of input/output ports in the sub-blocks, the number of wire crossings due to inter-block routing can be reduced. In the case of the biasing network, wire crossings are unavoidable due to its connectivity with all the sub-blocks, as shown by the highlighted area in Fig. 3.10, so shielding was used to reduce crosstalk.

The sub-blocks separation was made larger than four times the epitaxial layer of the wafer to reduce the impact of substrate noise [104]. This rule-of-thumb is applicable in advanced CMOS processes, where the substrate can be treated as a single electrical node due to the high substrate doping, which is needed to prevent the latch-up effect. The employed 180 nm high-voltage CMOS process has an epitaxial layer of about 7 µm so the sub-block separation should be at least 28 µm to reduce the impact of substrate noise. Increasing the separation further does not provide a substantial benefit. Similarly, the analog and digital power supplies were isolated so as not to deteriorate noise performance due to the mixed-signal functionality of the ΔΣ-based readout. The supply voltage isolation is achieved by employing power rail cuts (open-circuit) in the I/O ring while maintaining a continuous ground due to ESD requirements. In this way, it is also possible to create a dedicated supply for the I/O digital pads, which makes it easier to measure the average power consumption of the proposed readout.
3.3 Measurement Setup and Experimental Results

The primary performance metric of the $\Delta\Sigma$-based readout is the signal-to-noise-and-distortion ratio (SNDR), which is extracted from the readout’s output power spectral density for an in-band tone at the input. A block diagram of the measurement setup is shown in Fig. 3.11. The principal instrument in the setup is the Keysight U8903B Performance Audio Analyzer, which has two channels for signal generation and two for spectral analysis. When it is used as a generator, the U8903B operates as an 18-bit DAC with a sample-rate of 192 kHz. According to its datasheet, the signal generator has up to 17.65-ENOB for a $1 \text{Vrms}$ sine-wave at 1 kHz. Considering that the proposed readout achieves around 14-ENOB for an approximately six times smaller input $\text{rms}$ value, $170 \text{mVrms}$, the employed generator is sufficiently linear for benchmarking the prototype performance. However, the generator requires a common-mode level adjustment before it can be connected to the readout. Therefore, a common-mode level shifter was implemented on the evaluation board with an off-the-shelf amplifier (AD8475).

An XLR cable was used to connect the U8903B generator with the AD8475 using the Neutrik NC3FAV2-0 connector. The XLR is a shielded cable, which carries the wires for the fully-differential and common-mode signals, and is commonly used in audio applications. During the measurements, the XLR cable provided a better signal fidelity (e.g. fewer spurs) at higher frequencies compared to a pair of coaxial
3.3. MEASUREMENT SETUP AND EXPERIMENTAL RESULTS

Figure 3.12: Custom evaluation board for the ASIC electrical characterization.

cables. Similarly, an additional XLR cable was used to connect the low-pass filtered output of the AD8475 (using the Neutrik NC3MAV2-0) to the spectrum analyzer channel of the U8903B. This integrated functionality proved to be particularly useful when optimizing the RC values in the low-pass filter to reduce the amount of noise-aliasing without degrading the linearity of the AD8475.

The digital logic analyzer (TLA 621) saves the 4-bit output stream from the proposed readout. A sample of the stream is captured at the rising clock edge until the memory of the logic analyzer is filled up, which amounts to an array of 524289-points. This extensive array is then sliced into eight arrays of 65536-points to average the power spectral density. Even with the smaller data array, the frequency resolution of the FFT is 2.34375 Hz, which amounts to 128 FFT bins in the 300 Hz bandwidth. Hanning type-2 window function was used before the FFT, which still leaves 120 in-band bins (after removing the 3-bins for the DC offset and 5-bins for the test-tone) to accurately estimate the total integrated noise.

The clock jitter was estimated roughly by measuring the clock period over 2000 samples with a digital oscilloscope Keysight MSO-X 3024A. Based on the results, the standard deviation for a period was around 110 ps, which was low enough not to break the timing violations for the on-chip digital logic.

3.3.1 Evaluation Board

As it can be seen in Fig. 3.12, a custom 4-layer FR4 board with 0.8 mm thickness was designed considering the grounding and routing techniques for precise mixed-
signal systems [105–107]. The primary consideration at board-level is to group the discrete components, such that the inter-component routing is confined in an island. The reference (ground) potential is established at the intersection between islands, which is placed underneath the chip. In this way, the ground return path should ideally be contained within each island, which will reduce the interference between blocks. The isolation can be further improved by adding slits in the ground provided that the routing is avoided above the slits. The first (top) and forth (bottom) layer were used for the signal routing. The second layer was entirely dedicated to the ground plane to reduce the inductance in the return path, while the third layer was used for power routing. The dimensions of the evaluation board are 13.2 x 11.7 cm² mostly due to the large footprints of the cable connectors.

3.3.2 Low Distortion Signal Generator

The experimental results shown in [Paper II] are based on the measured SNDR values for a variety of input test-tones with different amplitudes and frequencies. Hence, the SNDR of the signal generator is critical for the electrical characterization. The fully-differential test-tone is first verified by inspecting the power spectral density (PSD) at the input of the chip with the spectrum analyzer. As it can be seen in Fig. 3.13, there are no harmonic distortions above the noise floor. The spectrum analyzer reports an SNDR (or SINAD) of 91.07 dB over a 96 kHz bandwidth for the filtered output of the AD8475 with a cut-off frequency of approximately 400 kHz. After checking the SNDR of the test-tone, the amplitude was set to 520 mV_{rms} and

![Image](image-url)

Figure 3.13: Measured PSD of the common-mode level shifter output and the results of the spectral analysis.
3.3. MEASUREMENT SETUP AND EXPERIMENTAL RESULTS

3.3.3 Dynamic Range and Linearity Measurements

The measurement plots of SNDR/SNR dependence with amplitude for sample no.1 are shown in Fig. 3.14a. Depending on the sample, the SNDR can peak at varying amplitudes due to process and device variations. Measurement were performed across ten packaged ASICs, and all the samples functioned properly and have similar behavior. After determining the maximum input amplitude corresponding to the peak SNDR for each sample, the measurements were repeated with the DEM encoder. In this way, the DAC unit elements were no longer randomized by the tree-structured DEM technique. The PSD with the DEM encoder enabled/disabled for sample no.1 is shown in Fig. 3.14b. Apart from demonstrating the necessity and efficacy of the DEM encoder, this benchmark also reveals the matching accuracy of the employed CMOS process. The results in [Paper II] show that the 11-level current-steering DAC is linear up to approximately 11-bits when accounting for all the harmonic distortion (including the spurs above the 300 Hz bandwidth line).

3.3.4 Frequency Sweep of the SNDR/SNR

In the frequency sweep measurements, the test-tone frequencies correspond to a particular FFT bin to avoid spectral leakage (e.g. coherent sampling). In practice, some of the signal power still leaks, for example when the generator and clock source are not phase locked. The chosen Hann2 windowing function has a signal
bin size of 5 (± 2 bins from the centre bin), which is why the DC component
spreads to two additional bins and should not be mistaken with flicker noise. The
chosen frequencies, 37.5 Hz, 57.5 Hz, 75 Hz, and 93.75 Hz for the power spectral
density in Fig. 3.15a correspond to the following FFT bin numbers: 16, 24, 32, and
40, respectively. The measured SNDR/SNR shown in Fig. 3.15b are plotted up to
93.75 Hz since higher frequencies would produce harmonic distortions beyond the
integration bandwidth, which would not be included in the SNDR calculations. On
the other hand, lower frequencies were not tested due to generator limitations and
limited memory depth of the logic analyzer. These results indicate that the ASIC
performance is approximately constant over the signal bandwidth.

3.3.5 PSRR/CMRR Measurements

The PSRR measurements were performed by bypassing the LDOs 1-5 (see Fig. 3.11)
and supplying the 1.8 V directly from the single-ended output of the signal generator.
In this way, the mixed-signal operation of the readout was validated since both
the analog and digital domains were supplied via a single voltage source. Fortu-
nately, the U8903B has a low output impedance of 100 \( \Omega \). Note that the differential
input of the NC3FAV2-0 was shorted to ground with the 49.9 \( \Omega \) resistors. The
generator amplitude was increased up to 128.3 mV\(_{\text{rms}}\), which made it possible to
distinguish the in-band tone from the noise floor as shown in Fig. 3.16. The chosen
test-tone approximates the 50 Hz interference from the power grid and corresponds
to the 24\(^{\text{th}}\) FFT bin.

For measuring the CMRR, the AC \( 128.3 \text{ mV}_{\text{rms}} \) and DC (0.6 V) common-mode
signals were supplied by the signal generator via a coaxial cable to the VOCD input
of the AD8475, which controls the common-mode level of its differential outputs.
The CMRR measurements were performed under two conditions: with and without
electrode mismatch. For instance, \( \Delta R_{\text{electrode}} = 50 \, \text{k}\Omega \) was added in series to \( V_{\text{in}} \),
input to replicate a large electrode mismatch as shown in Fig. 3.17. As a result,
3.3. MEASUREMENT SETUP AND EXPERIMENTAL RESULTS

Figure 3.16: Measured PSD with test-tone at 128.27 mV_{rms} and 56.25 Hz in the supply rail for sample no.1.

\[ \Delta R_{electrode} \] forms a voltage divider with the finite input impedance of the IA, \( Z_{in} \), which can be extracted in the following way:

\[ Z_{in} \approx \frac{\Delta R_{electrode}}{\Delta V_{in}} V_{CM,AC}, \quad (3.8) \]

where \( \Delta V_{in} \) is the magnitude of the in-band tone measured from the output PSD, and \( V_{CM,AC} \) is the amplitude of the common-mode AC signal.

The results of the test-bench with electrode mismatch are shown in Fig. 3.18. The ASIC’s input impedance extracted from these measurement results is approximately 94 M\( \Omega \), which is sufficiently high for neural recording. On the other hand, the results without electrode mismatch in Fig. 3.19 show a CMRR of approximately 98 dB for the IA, due to the applied layout matching and chopping techniques.
Figure 3.18: Measured PSD for sample no.1 with the common-mode test-tone at 128.27 mV$_{\text{rms}}$ and 56.25 Hz and electrode mismatch.

Figure 3.19: Measured PSD for sample no.1 with the common-mode test-tone with 128.3 mV$_{\text{rms}}$ and 56.25 Hz.

3.3.6 Input-referred Noise/Offset Voltage Measurements

The loop-filter reconfiguration between the high-pass (HP) and low-pass (LP) operation has been implemented to validate the advantage of a high-pass $\Delta\Sigma$ modulator regarding flicker noise and offset suppression. This was achieved by using an enable signal to do the following: 1) disable the chopping clocks; 2) change the polarity of the feedforward path from the first high-pass filter; 3) reconfigure the sign detection logic. Although the sign detection logic was functioning correctly in the HP operation, during the LP operation it was limited to a specific condition due to an error in the reconfiguration. Specifically, the low-pass $\Delta\Sigma$ modulator operated
correctly as long as the input signal did not change polarity. Consequently, both types of measurements were performed under the same conditions with a 58.5 mV differential DC offset, which was sourced from the signal generator via AD8475 in Fig. 3.11. The value of the external offset was chosen to be around the first DAC quantization level to maintain the signal polarity. In order to measure the internal readout offset, the inputs to the IA were disconnected from the AD8475, and the on-chip input common-mode feedback amplifier provided the biasing voltage. The measurement results of the offset voltage in the readout across ten samples are given in Fig. 3.21, which demonstrate the efficacy of the chopping and layout techniques.
3.4 Enhancement for the proposed $\Delta\Sigma$-based readout

The measurement results for the ASIC in [Paper II] showed competitive performance in most of the metrics when compared to the state-of-the-art, but the area consumption could still be improved. This section describes a potential enhancement for the proposed readout by expanding upon the area-efficient switched-capacitor integrator presented in [Paper III]. A significant reduction in sampling capacitance, and therefore area, can be achieved by utilizing the proposed circuit as the building block of the $\Delta\Sigma$-based readout.

In order to exploit the circuit technique from [Paper III], it is necessary first to modify the $\Delta\Sigma$-based readout as it is illustrated in Fig. 3.22. First, the building blocks of the loop-filter have to be transformed from high-pass filters to integrators, which will change the loop-filter topology accordingly, as shown in Fig. 3.22a. The original loop-filter coefficients are carried over from [Paper I]. Since the proposed integrator can have a non-delaying transfer function, it can not be easily substituted in the loop-filter. A workaround solution is found by replacing the second delaying integrator and the feedforward path from the output of the first integrator with an equivalent non-delaying integrator shown in Fig. 3.22b. The integrator transfer function from [Paper III], $H_1(z)$, given by

$$H_1(z) \approx \frac{1 + \frac{C_1^* + C_{p2}}{C_2(1+A_0)} - \left(1 - \frac{C_1^*}{C_2}\right) z^{-1}}{\left(1 + \frac{C_1^* + C_{p2}}{C_2(1+A_0)}\right) \left(1 + \frac{C_{p2}}{C_2}\right) - z^{-1}}.$$  \hspace{1cm} (3.9)

can be approximated by the delaying integrator in Fig. 3.22b for the following conditions: i) $C_1^*/C_2 = 0.6$; ii) the parasitic capacitance, $C_{p2}$, is neglected; iii) the amplifier DC gain $A_0 \gg 1$.

The proposed integrator employs correlated double sampling instead of chopping to mitigate the impact of flicker noise. These noise canceling properties are observed for the non-delaying integrator topology. Since the noise performance is critical for the first building block in the $\Delta\Sigma$-loop filter, the two integrators are swapped around node $V_1$ as shown in Fig. 3.22c. This modification can be implemented without affecting the NTF since the multiplication between discrete transfer functions is commutative. The $0.6z^{-1}/(1 - z^{-1})$ block can also be implemented with the delaying topology of the proposed integrator. On the other hand, an additional DAC is necessary for the tracking ADC because the IA, which was providing the buffered quantization error, was removed. Alternatively, the 4-bit flash ADC can be used instead, but the delaying integrator will have to be implemented with a more complex amplifier topology to facilitate the full swing of the input signal. Concerning the power consumption, the tracking ADC approach demonstrates a 60% power reduction (due to negligible logic power consumption) compared to the 4-bit flash ADC, which amounts to $3\mu W$ of reduction based on the results in [Paper I]. Moreover, the additional switched-capacitor DAC, which is needed to enable the tracking operation, can be implemented with a smaller unit.
3.4. ENHANCEMENT FOR THE PROPOSED ΔΣ-BASED READOUT

The capacitance then in the feedback DAC. Therefore, it should not have a significant impact on the overall power consumption but it would require a different layout. Also, the input feedforward path can be buffered directly by the proposed integrator, which would substantially reduce the design complexity of the enhanced readout and potentially reduce the total power consumption by more than 50%. Thus, the modified low-pass ΔΣ-based readout still has a high-input impedance, which would allow it to be DC-coupled to the microelectrode array. However, a more in-depth analysis of the circuit implementation challenges is needed in future research work.

![Diagram](image)

Figure 3.22: a) Modified ΔΣ-based readout with a low-pass loop-filter. b) The equivalent representation of the second integrator and feedforward path from $V_i$ in the loop-filter. c) The enhanced readout with the reorganized loop-filter.
3.5 Summary

In this chapter, different topologies of $\Delta\Sigma$ modulators have been explained, and the high-pass topology was employed due to its advantage of converting a chopper modulated signal in a power-efficient manner. The circuit implementation challenges of a high-pass $\Delta\Sigma$ modulator have been discussed within the context of the loop-filter order, oversampling and quantizer resolution. The choice of the charge transfer coefficient in the switched-capacitor high-pass filters was motivated based on the minimum biasing current needed to fulfill the gain-bandwidth and slew-rate requirements. After that, the circuit design challenges and details of the ASIC implementation were provided. For instance, embedding the instrumentation amplifier in the $\Delta\Sigma$-loop and the utilization of the tracking ADC were motivated based on tackling the challenges of achieving a high-linearity performance. In order to measure the performance metrics, a custom evaluation board and corresponding measurement setup have been developed. Lastly, an enhanced $\Delta\Sigma$-based readout architecture was proposed based on an area-efficient integrator.
Chapter 4

Impedance Measurement Method for Neural Interfaces

Implantable neural interfaces depend on the electrode-tissue interface to reliably transduce the ion charge into freely moving electrons throughout the implantation period. The transduction mechanism depends on the type of chemical reactions, which can be capacitive, Faradaic or a combination of both. For instance, noble metals, such as platinum or iridium, are the preferred electrode material since they exhibit a combination of both mechanisms [108]. For the capacitive reactions, the applied electric field induces ion separation and dipole alignment in the electrolyte (e.g. cerebral fluid), but due to the small charge per area capacity at the double-layer interface, the charge injection levels are low. On the other hand, Faradaic reactions create or consume chemical species, which are either oxidized or reduced. Consequently, Faradaic reactions introduce chemical species in the tissue environment, but they have an abundance of charge for stimulation.

Regardless of the type of reaction, the electrical stimulation temporarily depolarizes the membranes of nearby neurons to elicit a functional response (e.g. preventing an epileptic seizure). Consequently, stimulating electrodes cannot be used at the same time for neural recording due to the induced depolarization of neurons within the effective range of the electrode. Generally, the stimulation waveform is a series of biphasic current pulses, which can simply control the amount of injected charge via the pulse duration and magnitude. The primary constraint imposed on the stimulation waveform is to maintain a charge-balance between the pulses. If this consideration is violated, then an irreversible reaction can occur at the electrode-tissue interface, which can decrease the electrode efficacy or cause tissue damage [109]. Apart from the charge-balance constraints, the stimulation waveform also has to stay within the charge limits per pulse to prevent irreversible degradation, such as electrode dissolution or delamination [108].
Considering the issues mentioned above, the electrode characterization is conducted under controlled laboratory conditions outside living organism (referred to as in-vitro) and tested for reversibility of chemical reactions, charge injection limitations, and impedance [110]. However, long-term studies in living organism (referred to as in-vivo) exhibit dynamically changing conditions throughout the implantation period due to biological responses [111,112]. For instance, the electrode-tissue impedance increases in the post-implantation period until the swelling and the trauma subsides [113]. Additionally, the foreign-body-response of the immune system can create an organic film around the implant, which effectively decouples (“rejects”) the neural interface and increases the electrode-tissue impedance [84,114]. Moreover, a variation in the impedance of the electrode-tissue interface (ETI) can be caused by a change in tissue morphology or by the electrode degradation [115]. As a result, to achieve a power efficient solution despite the high voltage compliance ±10 V the system should be adaptable to the variations in ETI impedance [116]. Therefore, a simple impedance analyzer could be beneficial for monitoring the condition of the electrode-tissue interface or for adjusting the stimulation parameters in implantable (e.g. in-vivo) conditions.

4.1 ∆Σ-based Impedance Analyzer

The most popular method for measuring impedance is based on applying a sinusoidal excitation waveform to a sample-under-test \( Z_{SUT} \) while measuring the change in the magnitude and phase of the response signal in relation to the excitation waveform. This measurement approach is referred to as the frequency response analyzer (FRA) in [Paper IV]. In brief, the FRA method is implemented using I/Q demodulation scheme, in which the response waveform is supplied to two parallel paths where it mixes with the local oscillators. The two oscillators have a 90° phase shift in order to produce in-phase and quadrature mixing components, which are referred to as I- and Q-components, respectively. The result of each down-conversion is a DC component after low-pass filtering. The DC components represent the magnitudes of the real and imaginary part of \( Z_{SUT} \).

In principle, the I/Q demodulation scheme can also be performed using two quadrature ∆Σ ADCs [117–119], since the mixing operation can be replicated with the sampling operation. The block diagram of a similar method is shown in Fig. 4.1. It consists of the sinusoidal excitation waveform generator, the \( Z_{SUT} \), and two ∆Σ-based readouts. In order to perform I/Q demodulation with the proposed method, the excitation waveform frequency, \( f_{EXC} \), has to be set to \( f_s/2 \) carrier frequency and the up-conversion mixers in the ∆Σ-based readouts (see Fig.2 in [Paper II]) have to be disabled. In this way, the resulting response waveform, \( V_{SUT} \), is directly converted by the HP∆Σ modulator at the carrier frequency.

The in-phase component, \( D_{out,I} \), is acquired (with the bottom readout in Fig. 4.1) by phase-locking the sampling clock (CLK) to the excitation waveform, while the quadrature component, \( D_{out,Q} \), is acquired by triggering the top readout to the
**4.1. \( \Delta \Sigma \)-BASED IMPEDANCE ANALYZER**

![Diagram of \( \Delta \Sigma \)-based impedance analyzer](image)

Figure 4.1: Fully differential \( \Delta \Sigma \)-based impedance analyzer with an example of the I/Q demodulation principle on an excitation and response waveforms.

complementary clock signal (CLK). This time-interleaving sampling effectively achieves the necessary 90° degree phase shift for I/Q demodulation, but only at the \( fs/2 \) carrier frequency. Therefore, wide-band impedance measurements are acquired by sweeping the sampling and excitation frequency point-by-point, while maintaining the relation between them. The upper frequency range is limited by the IA settling-time, but, in principle, there is no lower limit for reducing the sampling frequency in a switched-capacitor loop-filter. The magnitude and phase angle of \( Z_{SUT} \) impedance are calculated from \( D_{out,I} \) and \( D_{out,Q} \) as shown in Fig. 4.1.

Compared to a \( \Delta \Sigma \)-based readout for ECoG recording, a \( \Delta \Sigma \)-based impedance analyzer is more sensitive to clock jitter. The impact of this non-ideality is illustrated for both applications in Fig. 4.2. In the case of neural recording, a slowly changing ECoG signal is up-converted with a square wave above the flicker noise corner, which produces a waveform with quick transitions. In the \( \Delta \Sigma \)-based readout, sampling and chopping clocks are synchronized to assure that the sampling instance occurs before the transition of the chopping clock. As a result, the sampling noise due to clock jitter (after decimation) can be calculated as:

\[
\bar{v}_{n1,\text{jitter}} = \frac{1}{\text{OSR}} \left[ \frac{\Delta V_{in}}{\Delta t} \right]_{\text{max}} \cdot \delta t \approx \frac{1}{\text{OSR}} V_{in,pp} \cdot \pi f_{in} \cdot \delta t, \tag{4.1}
\]

where \( V_{in,pp} \) is the peak-to-peak value and \( f_{in} \) is the frequency of a sinusoidal input signal, while \( \delta t \) is the \( \text{rms} \) value of the clock jitter. Since the sampling noise
CHAPTER 4. IMPEDANCE MEASUREMENT METHOD FOR NEURAL INTERFACES

Figure 4.2: Impact of the clock jitter on a chopper-modulated ($\Delta V_1$) and sinusoidal ($\Delta V_2$) waveforms.

has a white spectrum, the OSR can improve noise performance. In the case of a $\Delta\Sigma$-based impedance analyzer, the response signal, $V_{\text{SUT}}$, has an unknown phase delay introduced by the SUT impedance. The peak-to-peak value is assumed to be the same for simplicity. Consequently, the sampling noise is now a function of the excitation frequency and is calculated as:

$$\bar{v}_{n2,\text{jitter}} \approx \frac{1}{\text{OSR}} V_{\text{in,pp}} \cdot \pi f_s/2 \cdot \delta t,$$

(4.2)

where $f_s$ is the sampling rate. Since the power of the ECoG signal is contained up to 300 Hz and the impedance is generally measured over a wide frequency range (e.g. from 1 kHz to 100 kHz), $f_{in}$ is assumed to be substantially smaller than $f_s/2$. For example, by substituting the measured parameters of the $\Delta\Sigma$-based readout ASIC: $V_{\text{in,pp}} = 480 \text{ mV}_{\text{pp}}$, OSR = 256, $f_{in} = 300 \text{ Hz}$, $f_s = 153.6 \text{ kHz}$, $\delta t = 110 \text{ ps}$ in (4.1), $\bar{v}_{n1,\text{jitter}} = 0.05 \mu V_{\text{rms}}$ is obtained compared to a $\bar{v}_{n2,\text{jitter}} = 11.8 \mu V_{\text{rms}}$ when using (4.2). This result implies that the SNDR of the $\Delta\Sigma$-based readout will be degraded by 8 dB, which implies that the ENOB will be limited to 13-bits.

The remaining challenge for enabling a $\Delta\Sigma$-based impedance analyzer is the implementation of a high-voltage compliance sinusoidal generator for neural stimulation. In order to facilitate the necessary reconfiguration in terms of frequency and amplitude, such a generator can be implemented with direct digital synthesis (DDS) as shown in Fig. 4.1. Moreover, the resolution and linearity of the DAC impact the spectral purity of the sinusoidal waveform (e.g. THD), which has to be circumvented by using linearization techniques (e.g. DEM encoder). Even though a sinusoidal generator satisfies the net charge balance, it is difficult to justify its
4.2 An All-Digital Approach for Impedance Measurements

In order to enable the impedance characterization of the ETI, the measurement method should be compatible with currently used excitation waveforms for neural stimulation. Ideally, the ETI impedance should be measured while the closed-loop neural stimulation is performed so as not to disrupt the healthy brain activity with additional charge injection. A simple biphasic current pulse waveform shown in Fig. 4.3 is predominately used for neural stimulation because it can be implemented with complementary current sources and switches [120]. However, this type of excitation waveform is not compatible with well-known impedance measurement methods reviewed in [Paper IV]. Instead, an all-digital alternative based on system identification approach was proposed, which is expanded upon in this subsection.

4.2.1 System Identification

System identification refers to the configuration in which the output of an unknown process (or SUT referred to in [Papers IV and V]) is compared with the output of the adaptive filter for the same input. The block diagram of the system identification is illustrated for two different configurations in Fig. 4.3, which are referred to as the equation-error and the output-error [121]. The advantage of the equation-error formulation is that it can use linear regression algorithm to tune the filter coefficients, since it separates the IIR filter into two FIR filters as shown in Fig. 4.3, but it is prone to bias estimation and has to copy the denominator coefficients. On the other hand, the output-error formulation is used to directly tune a single IIR filter, which is then compared to the desired response, but the filter coefficients depend on previous input values and during identification a pseudo linear approximation has to be made. In [Papers IV and V], output-error configuration is used since it matches closer to the measurement setup conditions.

The adaptive filter can be implemented in the analog or digital domain, but the later can exploit the computational power of the digital signal processor used in closed-loop neural interfaces. In the case of a digital IIR filter, the output-error is based on the following recursive equation

\[ y(n) = \sum_{m=1}^{N-1} a_m(n)y(n-m) + \sum_{m=0}^{M-1} b_m(n)u(n-m), \]  

(4.3)

where \( m \) represents the previous samples, \( a_m(n) \) and \( b_m(n) \) are the time-varying tunable coefficients, while \( u(n) \) and \( y(n) \) correspond to the samples of excitation and the filter output waveforms, respectively. The equation in (4.3) can be expressed
Figure 4.3: a) The equation-error and b) the output-error formulation in system identification applications.

using a delay-operator, $q$, in the following way:

$$ y(n) = \frac{B(n, q)}{1 - A(n, q)} u(n), $$

(4.4)

where

$$ A(n, q) = \sum_{m=1}^{N-1} a_m(n) q^{-m} \quad \text{and} \quad B(n, q) = \sum_{m=0}^{M-1} b_m(n) q^{-m} $$

(4.5)

Alternatively, (4.3) can be represented as the product of the coefficient vector, $\theta$, 

...
and the regression matrix $X$ (defined in [Paper IV]), which is equal to

$$y = X \cdot \theta,$$

where $\theta = [b_1(n) \ldots b_m(n) \ a_1(n) \ldots a_m(n)]^T$. The expression in (4.4) is useful to interpret Fig. 4.3, while the expression in (4.6) is useful during the adaptive algorithm programming. Because the delayed filter outputs formulated in $X$ depends on previous coefficient values, $y(n)$ is considered a nonlinear function of $\theta$. Consequently, the output-error, $e(n) = d(n) - y(n)$, is also a nonlinear function of $\theta$, which causes multiple local minima in the mean-square-output-error. To avoid this issue, the number of poles and zeros of the adaptive filter should be greater or equal to the order of the SUT transfer function; additionally, the excitation waveform has to be a white-noise source, and the order of the adaptive filter numerator exceeds that of the SUT denominator [121].

The filter coefficients are estimated by the adaptive algorithm, which gradually reduces the mean-square-output-error (the cost function $I(\theta)$ in [Paper IV]) until it is approximately the same as the measured noise. The adaptive algorithm achieves this by calculating the gradient of the cost function concerning the filter coefficients. If the algorithm is implemented using the alternative recursive least square (RLS) method (online), as in [Paper IV], then the coefficients are updated along the negative gradient of the cost function in each clock cycle, as illustrated in Fig. 4.4. An in-depth explanation of the algorithm is given in [122]. This approach is useful for implementing the system identification in a behavioral simulator in order to model the measurement non-idealities, observe the internal waveforms and the algorithm convergence over time. Moreover, the code shown in Fig. 4.4 can be adapted to a hardware description language, which can be executed in real-time on a digital signal processor. The advantage of this approach is low-latency, which is an essential aspect of control systems. For instance, a closed-loop neural interface with an on-chip DSP could potentially benefit from the recursive approach by adjusting the neural stimulation parameters (e.g. pulse duration or amplitude) in real-time.

The adaptive algorithm can be implemented using the least square (LS) method shown in [Paper V]. In this case, the coefficients are estimated in post-processing (offline) after the measurement results have been collected. Compared to the RLS, the LS method requires inversion of the Hessian matrix $(X^T X)^{-1}$, which is a computationally demanding task [123]. Hence, the offline method is more suited for off-chip DSP. Moreover, the RLS approach avoids this issue by applying a matrix inversion lemma shown in [122] to calculate $S_p$ in Fig. 4.4. In this way, the algorithm complexity reduces from $O(M^3)$ to $O(M^2)$ [121], where $M$ is the number of filter coefficients. The offline approach is suited for the exploration of the system identification technique as a potential measurement method for the ETI impedance.
4.2.2 Limitations of the Proposed Measurement Method

System identification provides a simple hardware solution for impedance measurements over a wide bandwidth. The experimental results in [Paper V] demonstrated that the main limitation of this measurement technique is the estimation of the ETI phase response. The most likely explanation for a poor phase response estimation is the complexity of the ETI model equations [124]. An equivalent model of the ETI impedance is shown in Fig. 4.5a, where the capacitive and Faradic reactions are modeled with a constant-phase angle impedance $Z_{CPA}$ and charge-transfer resistance $R_{CT}$, respectively. Apart from these primary components, the model also includes the reversible electrode offset (half-cell) potential $E_{rev}$, which is measured relative to the hydrogen electrode, and the Warburg impedance, $Z_W$, which represents the diffusion of ions into the electrode material.
4.2. AN ALL-DIGITAL APPROACH FOR IMPEDANCE MEASUREMENTS

Figure 4.5: a) Equivalent model of the electrode-tissue interface. b) Illustration of the double-layer capacitance across an electrode with an arbitrary ion polarization.

The non-linear V/I behavior of $R_{CT}$, which is described by the Butler-Volmer equation [124], is used to model the DC signal through the ETI. For small signal voltage swing (over-potential) across $R_{CT}$, the charge-transfer has linear behavior. In implantable electrodes, the neural signal should reach the readout without attenuation so a small $R_{CT}$ value would be desirable, though it doesn’t help with its non-linearity. Noble metals are preferred as the electrode material since they have a symmetrical current-voltage relationship [125], and are less chemically active, which provides a high $R_{CT}$ and implicitly better linearity via double-layer charging [126]. Fortunately, their overall impedance can be reduced by increasing the electrode surface roughness and therefore the capacitive coupling of the double-layer [126].

The $Z_{CPA}$ is defined as

$$Z_{CPA} = \frac{1}{(j\omega C_{dl})^\beta} \quad (4.7)$$

where $C_{dl}$ is the double-layer capacitance illustrated in Fig. 4.5b, and $\beta$ is an empirical constant. The $C_{dl}$ component models the charge accumulation at the ETI, which also causes the built-in electrode offset [103]. A constant phase angle can occur in parallel RC network (e.g. $\theta = R_{CT}C_{dl}\omega = \tan(\beta\pi/2)$), when the $R_{CT}$ and $C_{dl}$ are frequency dependent as $f^{-\beta}$ [127]. Although these aspects are essential for
understanding the electrochemistry of electrodes, impedance magnitude measurements can be sufficient for characterizing the quality of the recording, adjusting the stimulation parameters, and for tracking the electrode and tissue conditions during the implantation period.

4.3 Summary

The bridge between the living brain tissue and inorganic silicon electronics may appear deceptively simple, but at its core is a complicated biomedical engineering challenge. The two domains are bridged together with a microelectrode array, which acts as an electrochemical sensor or transducer for the charged ions. The direct contact of the microelectrodes with the brain surface introduces many challenges, such as tissue damage due to a difference in material rigidity, immune response due to packaging bio-compatibility, and toxicity of chemical byproducts at the interface. Although the advancements in electrode fabrication tackle these challenges, there is a lack of knowledge on the long-term in-vivo electrode behavior and its impact on the neural interface performance. ETI impedance appears to be a good status indicator of the considerations mentioned above. However, impedance measurements are currently not common functionality in state-of-the-art neural interfaces due to the hardware complexity associated with the FRA approach and the limited power budget.

In this chapter, two impedance measurement methods were introduced. First is a high-resolution approach based on the conventional FRA method while the second is a low-complexity hardware implementation that is compatible with conventional neural interface circuits. The FRA based approach employs two slightly modified ΔΣ-based readouts to conduct the so-called I/Q demodulation. Hence, the same ECoG recording readout can be reused as a high-resolution impedance analyzer with minor performance degradation, which is cost-effective in terms of die area and power consumption. The main bottleneck of this approach is the sinusoidal generator, which is more power and area demanding than a simple biphasic pulse generator. As a result, an alternative measurement method based on the system identification technique was proposed, which relies on the biphasic pulse generator. Therefore, the system identification is fully compatible with the existing neural stimulators and the medium resolution ADCs used in conventional readout architectures. Also, it allows for flexibility in signal processing, which can be tailored to the capabilities of the next-generation neural interfaces.
Closed-loop neural interfaces are close to becoming fully-implantable medical devices thanks to the technological advancements, such as wireless telemetry, large scale integration, and battery-less operation. Their development is motivated and influenced by the promising results achieved with brain controlled interfaces and the treatment of neurological disorders. These applications are enabled by the capacity for both recording and stimulation of the brain’s electrical activity, which is a feature of the emerging closed-loop neural interfaces. However, the introduction of artificial electrical pulses in the brain for neural stimulation has added new design challenges to the research field. In terms of neural recording, a larger ENOB is required to avoid the readout saturation in the presence of stimulation artifacts. In terms of neural stimulation, an impedance measurement method will be needed to monitor the condition of the microelectrode array and adjust the stimulation parameters accordingly. This thesis work has proposed circuit design techniques for tackling the challenges of high-resolution neural recording and electrode-tissue impedance measurements. The following concluding statements are formulated based on the experience that was acquired throughout the conducted research work.

Firstly, the development of the readout architecture was devoted to the ECoG recording. The motivation for this choice was supported by the fact that closed-loop neural interfaces rely on the processing of ECoG recording to elicit functional neural stimulation. An overview of ECoG-specific readout architectures was presented and key advancements were highlighted. Several development directions were observed, which include: i) the shift toward a dedicated ADC per channel; ii) the replacement of passive high-pass filters with digitally-assisted offset removal techniques; and iii) the need for higher ENOB. Additionally, a comprehensive performance survey was conducted to establish the circuit specifications, and to estimate the available power budget for the readout, considering all the functionalities in a closed-loop neural interface. These observations lead the development toward a readout architecture based on a high-resolution ADC per channel.
Secondly, a brief description of various $\Delta\Sigma$ modulator topologies was given. The high-pass $\Delta\Sigma$ modulator was concluded to be the most promising solution due to its capability to convert an amplitude modulated signal in a power-efficient manner. The selection of the loop-filter order, oversampling ratio, and quantizer resolution was scrutinized from the circuit implementation perspective. As a result, a power-efficient high-pass $\Delta\Sigma$ modulator was achieved by applying various design techniques in a switched-capacitor implementation. In terms of performance metrics, a peak SNDR of 96.4 dB over a 300 Hz bandwidth was achieved while consuming 19.56 $\mu$W. The corresponding Schreier figure-of-merit is approximately 168.26 dB, which is competitive with recently published high-resolution ADCs for low-frequency applications.

The high-pass $\Delta\Sigma$ modulator was employed in the $\Delta\Sigma$-based readout, which embeds the analog front-end. The complete readout was fabricated in a 0.18 $\mu$m CMOS process. The architecture improvements and added circuits were the result of fixing the main shortcomings in the previous design, which were the high-impedance interface to electrodes and quantizer power dissipation. The measurement results showed that the $\Delta\Sigma$-based readout architecture achieves 14-ENOB, which was among the highest reported ENOB at the time of publication. The proposed readout consumes in total 54 $\mu$W out of which approximately 60% is dissipated in the instrumentation amplifier and current-steering DAC. Although the power consumption overshoots the estimated budget per channel by 35%, the figure-of-merit for the readout architecture (AFE+ADC) was 155.5 dB, which was among the best reported. Hence, the chip prototype successfully demonstrated the potential of high-resolution $\Delta\Sigma$-based readout for ECoG recording.

Apart from the power budget issue, the die area utilization by the switched-capacitor circuits could be improved further. An in-depth explanation of the IA’s impact on the $\Delta\Sigma$-loop stability and noise performance has been performed and possible enhancements have been identified. The proposed technique exploited the thermal noise limit by introducing a degree of freedom in setting up the noise floor density independently of the effective noise bandwidth. The technique was demonstrated on an integrator circuit, which satisfied the requirements for the high-pass $\Delta\Sigma$ modulator. Instead of using chopping to reduce the contribution of flicker noise, correlated double sampling was employed since it did not require additional switches. The general procedure for the proposed technique was presented in this thesis. Theoretically, by using this technique the enhanced $\Delta\Sigma$-based readout would benefit from up to 75% reduced MIM capacitor area, and from up to 24 $\mu$W less power consumption. However, the enhanced readout was not verified in simulations since it required a substantial design overhaul and it was left as a potential future work. Additionally, a second iteration of the chip layout could greatly improve the overall area-efficiency since minimum DRC rules were avoided for the benefit of reducing the physical mask design time.

Thirdly, the electrode-tissue interface was introduced, and the importance of impedance measurements in neural interfaces was stated. By reviewing well-known measurement methods, it was envisaged that the $\Delta\Sigma$-based readout can be eas-
ily reused to enable high-resolution impedance measurements. The inspiration for the ΔΣ-based impedance analyzer came from the fact that high-pass ΔΣ modulators were initially developed for direct-conversion radio receivers. However, the performance of the high-pass ΔΣ modulator was sensitive to clock jitter since the intermediate frequency (IF) was equal to half of the sampling frequency. Moreover, in the case of a low-IF high-pass ΔΣ-based receiver, the image rejection filter requires high selectivity due to the proximity of the intermediate and sampling frequency. Based on the noise calculations and measurement results performed on the ΔΣ-based readout ASIC, it was concluded that the ΔΣ-based impedance analyzer would have 13-ENOB. The high performance is maintained despite the above mentioned jitter sensitivity due to a relatively low clock frequency compared to radio applications. However, the proposed measurement method was not pursued because it implied the need for a low-distortion sinusoidal generator. Additionally, it was difficult to motivate the use of a sinusoidal excitation waveform since there was no clear indication that it would provide an advantage over the more popular biphasic pulse for in-vivo conditions. As a result, the system identification technique was proposed since it was compatible with the biphasic pulse waveform.

The system identification technique was initially proven through behavioral simulations, which demonstrated that further experimental validation is required. Hence, a proof-of-concept prototype was implemented using off-the-shelf components to validate the method in real application conditions. The PCB prototype was implemented considering the limitations of commercial components, which implied a suboptimal circuit solution in terms of performance (power, settling-time, CMRR) so the focus was placed on validating the measurement method. One of the main issues was the placement of the sample-under-test in the feedback network of the ADC driver. This solution enabled a simple way to provide current excitation via the virtual ground, but at the cost of significantly reduced frequency range. Nevertheless, this conclusion also indicated that the first parasitic pole should be approximately at the same frequency as the ADC sampling rate. The second issue was the period of the pseudo-random noise sequence, which was limited to 255 clock cycles even with an increased register length. Additionally, due to a roll-off at low frequencies in the power spectral density of the excitation waveform, the measurement setup is currently limited to $[f_s/20, f_s/2]$ frequency bands, where $f_s$ is the ADC clock frequency. Lastly, more research is needed to investigate the equivalent discrete-time model of the electrode-tissue interface for a better phase estimation.

The work in this thesis has successfully completed the research objectives defined in section 1.3. Though more research and medical collaboration is necessary to enable fully-implantable neural interfaces, the appended research papers demonstrate the potential of power-efficient high-resolution readouts and a simple impedance measurement method for implantable closed-loop neural interfaces.
Bibliography


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