High-Temperature Radio Circuits in Silicon Carbide Bipolar Technology

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To my parents
Abstract

High-temperature electronics find many niche applications in downhole drilling, aviation, automotive and future exploration of inner planets like Venus and Mercury. Past studies have shown the potential of silicon carbide (SiC) electronics for catering these extreme temperature applications. In particular, analog, digital and mixed-signal integrated circuits, based on in-house SiC bipolar technology, have been shown to operate successfully for temperatures as high as 500 °C. This thesis aims at exploring the potential of in-house SiC bipolar technology for realizing high-temperature radio frequency (RF) circuits.

To that end, the in-house SiC bipolar junction transistors (BJTs) are first characterized up to 300 °C for RF figures of merit like unity current gain bandwidth and unity power gain bandwidth. The measurement results showed the feasibility of the current batch of SiC BJTs for developing RF circuits operating at low-end of very high frequency (VHF) band. Thereafter, three fundamental blocks of a high-temperature radio receiver, i.e. an intermediate-frequency amplifier, an oscillator and a down-conversion mixer were implemented. Firstly, an intermediate-frequency amplifier has been designed and measurement results demonstrated operation up to 251 °C. The proposed amplifier achieved a gain, input, and output matching of 16 dB, -7.5 dB and -11.2 dB, respectively, at 54.6 MHz and 251 °C. Next, 500 °C operation of an active down-conversion mixer has been exhibited. Measurements have shown that the conversion gain of the proposed mixer is 4.7 dB at 500 °C. Lastly, a negative resistance oscillator has been designed and tested successfully up to 400 °C. It has been shown that at 400 °C, the proposed oscillator delivers an output power of 8.4 dBm into a 50 Ω load.

In addition to SiC BJTs, the aforementioned circuits also employed spiral inductors implemented on PCBs, commercially available ceramic capacitors and thick-film resistors. Therefore, this thesis presents the evaluation of passives to assess their feasibility for high temperature operation. This work also identifies and addresses several challenges associated with the development flow of high-temperature RF circuits.

Keywords: 4H-SiC, active down-conversion mixer, BJT, EM simulations, silicon carbide, high-temperature, IF amplifier, LTCC, negative resistance oscillator, passives, RF circuits.
Sammanfattning

Högtemperatelektronik har många specialiserade tillämpningar inom borfhål-, flyg-, och fordonsindustrin, och för framtida utforskningstilldrag till de inre planeterna Venus och Merkurius. Tidigare studier har visat att halvledarteknik i kiselkarbid (SiC) kan användas i dessa extrema tillämpningar. KTHs egenutvecklade kiselkarbid-bipolärtransistorteknik har tidigare använts för analoga, digitala och blandade signaler, och demonstrerat funktionallitet ända upp till 500 °C. Målet med denna avhandling är att undersöka den egenutvecklade kiselkarbid-bipolärtransistorteknikens möjligheter för att kunna realisera högtemperatur-radiokretsar.

Först karakteriserades de egenutvecklade kisekarbid-bipolärtransistorerna upp till 300 °C för att erhålla radiofrekvens (RF) godhetstal såsom ström- förstärkningsbandbredd och effektförstärkningsbandbredd. Mätresultaten visade att processflödesversionen av kiselkarbid-bipolärtransistorer kunde användas för RF-kretsar i den nedre delen av metervågsfrekvensbandet (VHF). Därefter implementerades tre fundamentala block för ett högtemperatur radiosottagarsystem: en mellanfrekvensförstärkare, en oscillator och en mixer för frekvens-nedblandning. Till att börja med så designades och karakteriserades en mellanfrekvensförstärkare upp till 251 °C. Förstärkaren uppnåde en förstärkning, ingångs- och utgångsanpassningsdämpning på 16 dB, -7.5 dB och 11.2 dB, respektive, med en frekvens på 54.6 MHz vid 251 °C. Därefter demonstrerades en aktiv mixer för frekvensnedblandning som fungerar vid 500 °C. Måtresultat indikerar att mixerns omvandlingsförstärkning är 4.7 dB vid 500 °C. Slutligen designades en negativresistansoscillator och testades upp till 400 °C. Oscillatorn har en uteffekt på 8.4 dBm med 50 °C last vid 400 °C.

Utöver kiselkarbid-bipolärtransistorerna så använde de redan nämnda kretssarna sig av spiralinluktantans på kretskortet, kommersiellt tillgängliga keramikkondensatorer och tjockfilmsmotstånd. Därmed presenterar denna avhandling även en genomgång av passiva komponenter med avseende på deras lämplighet inom högtemperaturställämpningar. Detta verk identifierar och bemöter flera utmaningar med utvecklingsflödet för högtemperatur radiokretsar.

Nykkelord: 4H-SiC, aktiv mixer för frekvensnedblandning, bipolärtransistor, EM simulerings- och kiselkarbid, högtemperatur, medelfrekvensförstärkare, LTCC, negativresistansoscillator, passiva komponenter, radiokretsar.


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<th>Definition</th>
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<tbody>
<tr>
<td>ADS</td>
<td>Advanced design system</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar junction transistor</td>
</tr>
<tr>
<td>BPF</td>
<td>Bandpass filter</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer aided design</td>
</tr>
<tr>
<td>CB</td>
<td>Common-base</td>
</tr>
<tr>
<td>CC</td>
<td>Common-collector</td>
</tr>
<tr>
<td>CE</td>
<td>Common-emitter</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
</tr>
<tr>
<td>ENIG</td>
<td>Electroless nickel immersion gold</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency shift keying</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium nitride</td>
</tr>
<tr>
<td>GSG</td>
<td>Ground/signal/ground</td>
</tr>
<tr>
<td>HEMT</td>
<td>High electron mobility transistor</td>
</tr>
<tr>
<td>HT</td>
<td>High-Temperature</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate frequency</td>
</tr>
<tr>
<td>IO</td>
<td>Input/output</td>
</tr>
<tr>
<td>JFET</td>
<td>Junction field effect transistor</td>
</tr>
<tr>
<td>LNA</td>
<td>Low noise amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local oscillator</td>
</tr>
<tr>
<td>LPF</td>
<td>Lowpass filter</td>
</tr>
<tr>
<td>LTCC</td>
<td>Low temperature co-fired ceramic</td>
</tr>
<tr>
<td>MAG</td>
<td>Maximum available gain</td>
</tr>
<tr>
<td>MCU</td>
<td>Microcontroller unit</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal semiconductor field effect transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
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<tr>
<td>NRO</td>
<td>Negative resistance oscillator</td>
</tr>
<tr>
<td>PA</td>
<td>Power amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature amplitude modulation</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature phase shift keying</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
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<tr>
<td>---------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RFC</td>
<td>Radio frequency choke</td>
</tr>
<tr>
<td>RT</td>
<td>Room temperature</td>
</tr>
<tr>
<td>S</td>
<td>Scattering</td>
</tr>
<tr>
<td>SGP</td>
<td>Spice Gummel Poon</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon carbide</td>
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<tr>
<td>SMA</td>
<td>SunMiniature version A</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon-on-insulator</td>
</tr>
<tr>
<td>SOLT</td>
<td>Short-open-load-through</td>
</tr>
<tr>
<td>SRF</td>
<td>Self-resonant frequency</td>
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<tr>
<td>VCO</td>
<td>Voltage controlled oscillator</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable gain amplifier</td>
</tr>
<tr>
<td>VHF</td>
<td>Very high frequency</td>
</tr>
<tr>
<td>VNA</td>
<td>Vector network analyzer</td>
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List of Publications

Appended Papers


Related Publications Not Included in This Thesis


Summary of Appended Papers


  **Summary**: This paper presents a two-stage small signal intermediate frequency amplifier for high-temperature communication systems. The proposed amplifier is implemented using in-house silicon carbide bipolar technology. Measurements show that the proposed amplifier can operate from room temperature up to 251 °C. At a center frequency of 54.6 MHz, the amplifier has a gain of 22 dB at room temperature which decreases gradually to 16 dB at 251 °C. Throughout the measured temperature range, it achieves an input and output return loss of less than -7 dB and -11 dB, respectively. The amplifier has a 1-dB output compression point of about 1.4 dBm, which remains fairly constant with temperature. Each amplifier stage is biased with a collector current of 10 mA and a base-collector voltage of 3 V. Under the aforementioned biasing, the maximum power dissipation of the amplifier is 221 mW.

  **Author’s contribution**: The author performed 100% circuit design and simulations, 100% layout and characterization, and wrote 80% of the manuscript.


  **Summary**: This paper presents an active down-conversion mixer for high-temperature communication receivers. The mixer is based on an in-house developed 4H-SiC BJT and down-converts a narrow-band RF input signal centered around 59 MHz to an intermediate frequency of 500 kHz. Measurements show that the mixer operates from room temperature up to 500 °C. The conversion gain is 15 dB at 25 °C, which decreases to 4.7 dB at 500 °C. The input 1-dB compression point is 1 dBm at 25 °C and -2.5 dBm at 500 °C. The mixer is biased with a collector current of 10 mA from a 20 V supply.
and has a maximum DC power consumption of 204 mW. High-temperature reliability evaluation of the mixer shows a conversion gain degradation of 1.4 dB after 3-hours of continuous operation at 500 °C.

**Author’s contribution:** The author performed 100% circuit design and simulation, 100% layout and characterization, and wrote 95% of the manuscript.


  **Summary:** Radio frequency oscillator design typically requires large-signal, high-frequency simulation models for the transistors. The development of such models is generally difficult and time consuming due to a large number of measurements needed for parameter extraction. The situation is further aggravated as the parameter extraction process has to be repeated at multiple temperature points in order to design a wide-temperature range oscillator. To circumvent this modeling effort, an alternative small-signal, S-parameter based design method can be employed directly without going into complex parameter extraction and model fitting process. This method is demonstrated through the design and prototyping of a 58 MHz high-temperature oscillator, based on an in-house 4H-SiC BJT. The BJT at elevated temperature (up to 300 °C) was accessed by on-wafer probing and connected by RF-cables to the rest of circuit passives, which were kept at room temperature.

  **Author’s contribution:** The author performed 100% circuit design and simulation, 100% layout and characterization, and wrote 100% of the manuscript.


  **Summary:** This paper presents a 59.5 MHz negative resistance oscillator for high-temperature operation. The oscillator employs an in-house 4H-SiC BJT, integrated with the required circuit passives on a low-temperature cofired ceramic substrate. Measurements show that the oscillator operates from room temperature up to 400 °C. The oscillator delivers an output power of 11.2 dBm into a 50 Ω load at 25 °C, which decreases to 8.4 dBm at 400 °C. The oscillation frequency varies by 3.3% in the entire temperature range. The oscillator is biased with a collector current of 35 mA from a 12 V supply and has a maximum DC power consumption of 431 mW.

  **Author’s contribution:** The author performed 100% circuit design and simulation, 100% layout and characterization, and wrote 95% of the manuscript.
Chapter 1

Introduction

Electronics has transformed our lives significantly during the last few decades. With applications ranging from communication, healthcare, transportation to defense and security, electronic circuits and systems are ubiquitous. Silicon (Si) has generally remained the semiconductor of choice for electronics industry due to its low cost, very large-scale integration capabilities, and relatively simple processing and this situation is predicted to persist for many more years to come. However, there are niche applications in industries like spacecraft, oil and gas drilling, aviation and automotive that require high-temperature (HT) electronics, capable of operating beyond the commercial (85 °C) and military specifications (125 °C) of silicon-based-electronics [1–5].

1.1 Applications of High-Temperature Electronics

Planetary exploration of Venus is probably the most exciting application that can benefit from HT electronics. Venus and Earth are inner planets with approximately the same size and density. Though both these planets started as "twins", the evolution of their climates took very different trajectories. Past studies show that Venus is surrounded with thick clouds of carbon dioxide, which prevents any solar flux reaching its surface from escaping [6]. Due to this "greenhouse runaway" effect, Venus gradually became the hottest planet of the solar system with an average surface temperature of around 465 °C [7]. How and when the climate of Venus took such a drastic turn? Did Venus ever have oceans, and if so, for how long? How volcanically active it has been over the last billion years? These are some unanswered scientific questions that Venus exploration missions seek to address [8, 9]. The answers to these important questions will not only improve our understanding of the evolution of terrestrial planets but will also provide an insight into the possible future of Earth. However, any surface probes or landers for long-term exploration missions to Venus would require temperature-hardened electronics to operate reliably under harsh Venusian temperatures.
In downhole oil/gas drilling and geothermal applications, the electronic systems are required to monitor the drilling tools as well as gather data related to the state of the reservoir, such as its temperature, pressure and geometry [10]. The downhole temperature rises by up to 9 °C per 100 m of drilling depth [11] and the peak oil/gas downhole temperatures are currently around 210 °C [12,13]. Although the conventional electronics are still being employed by oil/gas drilling industry, they require thermally insulated or actively cooled chambers [14]. These cooling techniques are generally costly and have a large footprint. Furthermore, the oil/gas industry is seeking even deeper reservoirs with ambient temperatures approaching 300 °C [15] whereas the cooling solutions are currently limited to 250 °C [16]. The geothermal energy reserves exist even deeper with temperatures as high as 600 °C [1]. For these reasons, HT electronics capable of operating reliably without any cooling is greatly desired in the downhole oil/gas and geothermal industry.

The automotive industry represents the largest potential user of HT electronics. In order to improve the performance, efficiency and reliability of automobiles, the automotive industry is rapidly replacing the mechanical and hydraulic based control systems with their electronic counterparts. However, as the number of electronic systems are increasing, it is no longer feasible to locate them at one centralized location with benign temperature requirements. The present trend demands a more distributed approach, with sensors and control electronics residing closer to the heat sources. The typical temperature requirements for such electronics can range between 150 °C for engine compartments and on-wheel sensors to 850 °C for exhaust pipes [2,3].

Aviation is another area that would benefit from HT electronics. For instance, the health of an aircraft engine can be monitored effectively by in-situ monitoring of parameters like temperature, pressure and composition of emission gases. This data can then be analyzed to indicate if the engine is in need of maintenance. Such an engine monitoring system requires electronics for data conditioning and transmission, capable of surviving up to 600 °C [4].

The applications of HT electronics and the required ambient temperatures are summarized in Table. 1.1. The silicon-on-insulator (SOI) technology can provide electronic systems operating only up to 300 °C [1,17,18]. Therefore, alternative semiconductor technologies are required to extend the operating temperature even further.

1.2 Wide-Bandgap Semiconductors

The electrical properties of semiconductors can be modified by the intentional addition of impurity elements called dopants. In addition to dopants, a certain amount of thermally generated carriers (also known as intrinsic carriers) are also present inside the semiconductors. The concentration of these thermally generated carriers \(n_i\) depends on the energy-bandgap of the semiconductor \(E_G\) and temperature
1.2. WIDE-BANDGAP SEMICONDUCTORS

Table 1.1: An overview of high-temperature applications and temperature requirements [1–4].

<table>
<thead>
<tr>
<th>High-Temperature Application</th>
<th>Ambient Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deep-well drilling telemetry</td>
<td></td>
</tr>
<tr>
<td>Oil and gas</td>
<td>300 °C</td>
</tr>
<tr>
<td>Geothermal</td>
<td>600 °C</td>
</tr>
<tr>
<td>Automotive</td>
<td></td>
</tr>
<tr>
<td>Engine compartment and on-wheel sensors</td>
<td>150 °C</td>
</tr>
<tr>
<td>Electronic suspension and brakes</td>
<td>250 °C</td>
</tr>
<tr>
<td>On-cylinder and exhaust pipe</td>
<td>850 °C</td>
</tr>
<tr>
<td>Turbine Engine</td>
<td></td>
</tr>
<tr>
<td>Electric actuation</td>
<td>150 °C - 600 °C</td>
</tr>
<tr>
<td>Sensor, telemetry and control</td>
<td>300 °C - 600 °C</td>
</tr>
<tr>
<td>Spacecraft</td>
<td></td>
</tr>
<tr>
<td>Venus and Mercury exploration</td>
<td>550 °C</td>
</tr>
<tr>
<td>Engine monitoring system</td>
<td>600 °C</td>
</tr>
<tr>
<td>Industrial</td>
<td></td>
</tr>
<tr>
<td>High-power processing</td>
<td>300 °C - 600 °C</td>
</tr>
</tbody>
</table>

\[
n_i = \sqrt{N_C N_V} e^{-E_G/2kT} \tag{1.1}
\]

where \(N_C\) and \(N_V\) are the effective electron and hole density of states, respectively and \(k\) is the Boltzmann constant. Although both \(N_C\) and \(N_V\) are temperature dependent, \(n_i\) in (1.1) is fundamentally governed by the exponential term. At sufficiently high temperatures, \(n_i\) approaches the dopant concentration and subsequently affects the functionality of the semiconductor device. Equation (1.1) also suggests that at a given temperature, \(n_i\) decreases exponentially with the energy-bandgap. Therefore, by employing semiconductors with wide energy bandgaps, the generation of thermally generated carriers can be suppressed. Two such wide-bandgap semiconductors are silicon carbide and gallium nitride (GaN) with \(E_G\) of 3.2 eV and 3.4 eV, respectively. For comparison purposes, assume a reference threshold of \(n_i = 1 \cdot 10^{14} \, \text{cm}^{-3}\) for a semiconductor device to operate properly. Fig. 1.1 shows that \(n_i\) in Si would reach \(1 \cdot 10^{14} \, \text{cm}^{-3}\) at 200 °C whereas \(n_i\) in SiC and GaN would reach the same value at temperatures approaching 800 °C. Moreover, SiC and GaN based devices also provide better performance than Si in terms of leakage currents. To elaborate this, consider the leakage current (\(I_L\)) in a
CHAPTER 1. INTRODUCTION

Figure 1.1: Intrinsic carrier concentration versus temperature for different semiconductor technologies.

reverse-biased $P^+N$ junction:

$$I_L \approx -qA n_i \left[ \frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right]$$ (1.2)

where $A$ is the area of the junction, $N_D$ is the n-type doping concentration, $W$ is the width of depletion region, $D_P$ is the hole diffusion constant and $\tau$ is the effective minority carrier lifetime. Ignoring the second term in (1.2), $I_L$ shows a square dependence on $n_i$, which is orders of magnitude smaller in SiC and GaN than Si. Thus, it can be inferred that both SiC and GaN are superior to Si, even at temperatures where Si can still be used. Nevertheless, due to very large-scale integration capability, low cost and a very evolved fabrication process, bulk-silicon and SOI technologies will continue to remain the workhorse of semiconductor industry for applications up to $300$ °C. For applications beyond that temperature, wide-bandgap materials like GaN and SiC become indispensable.

High-temperature operation of many GaN and SiC devices and integrated circuits (ICs) have been reported in the literature. In [20], $600$ °C operation of an $\text{Al}_2\text{O}_3/\text{AlGaN/GaN}$ metal-insulator-semiconductor, high electron mobility transistor (HEMT) technology has been reported. Although these HEMTs operate up to $600$ °C, they exhibit instability in threshold voltage beyond $300$ °C. In [21], stable performance of a GaN BJT at $300$ °C and GaN metal semiconductor field effect transistor (MESFET) at $400$ °C has been shown. For SiC, several HT ICs have been demonstrated. In [22–29], analog and digital ICs, based on SiC junction field effect transistor (JFET) technology, have been shown to work reliably up to or over $400$ °C. More recently, NASA reported SiC JFET based ICs operating at
an extreme temperature of 800 °C [30]. The HT operation of analog and digital ICs based on SiC metal oxide semiconductor field effect transistor (MOSFET) and complementary metal oxide semiconductor (CMOS) technologies have been reported in [31–43]. The operating temperatures of these ICs range from 200 °C in [43] to 540 °C in [39]. In [44–46], digital and mixed-signal ICs based on SiC MESFET technology have been shown to work up to 300 °C. High-temperature analog and digital ICs, based on KTH’s in-house SiC bipolar technology, have been shown to operate up to 500 °C in [47–53] and 600 °C in [54]. In addition to the aforementioned digital and analog circuits, several SiC and GaN based HT RF circuits have also been demonstrated. In [55–60], RF blocks of a downhole communication transceiver, employing GaN HEMTs, have been shown to operate up to 230 °C. In [61], high-frequency performance of SiC MESFETs have been demonstrated from 25 °C up to 250 °C. SiC MESFET have extensively been used for developing HT RF circuits, especially oscillators in [62–69]. The operating temperature of these oscillators range from 200 °C in [62] to 470 °C in [67]. SiC JFETs have also been used to demonstrate HT RF circuits and systems working up to 300 °C in [70,71] and 450 °C in [72,73]. The aforementioned review suggests that both SiC and GaN are excellent candidates for the development of HT sensor systems.

1.3 Motivation

The block diagram of a typical sensor system is illustrated in Fig. 1.2. It comprises transducers, an analog front-end, a microcontroller unit (MCU), a memory buffer and a supply to power up the electronics. A transceiver is also required to transmit the data out of HT ambiance for further investigation as well as to control and configure the sensor system. These communication requirements motivate the development of a HT transceiver, capable of residing at the same HT ambiance as the remaining sensor system. This thesis focuses on the development of RF circuits for receiver part of the HT communication system (highlighted in gray).
A receiver comprises RF circuits like oscillators, amplifiers, mixers, etc. In this thesis, the implementation of these RF circuits using the in-house 4H-SiC bipolar technology is presented. The same technology was used previously to demonstrate HT sensors [74–77], front-end electronics [47,48,50–53], power supplies [49,78–80] and different microcontroller blocks [54,81,82] as part of a HT sensor system. This research is a next step towards utilizing the in-house SiC bipolar technology as a unified platform to develop all electronics for HT sensors, including its communication system.

1.4 Research objectives

The main goal of this thesis is to demonstrate proof-of-concept, HT RF circuits based on the in-house SiC bipolar technology. In particular, it involves the following three objectives:

- **Objective 1**: Investigate the potential of in-house SiC bipolar technology for developing RF circuits.

- **Objective 2**: Identify the challenges associated with the design, prototyping and characterization of HT RF circuits and propose solutions.

- **Objective 3**: Design, prototype and characterize RF circuits for HT radio receiver.

1.5 Research contributions

The author’s contribution to the aforementioned objectives are summarized as follows:

- **Contribution 1**: An intermediate frequency (IF) amplifier is designed, prototyped and characterized up to 251 °C. The amplifier is prototyped on a Rogers-4003C printed circuit board (PCB) and consists of two cascaded SiC BJTs in common-emitter configuration. The matching is performed using four L-section networks employing HT capacitors and spiral inductors. At a center frequency of 54.6 MHz, the amplifier has a gain of 22 dB at room temperature (RT), which decreases gradually to 16 dB at 251 °C. Throughout the measured temperature range, it achieves an input and output return loss of less than -7 dB and -11 dB, respectively. The maximum power dissipation of the amplifier is 221 mW. [Paper I]

- **Contribution 2**: An active down-conversion mixer is designed, prototyped and characterized up to 500 °C. The mixer is prototyped on a low temperature co-fired ceramic (LTCC) board and employ an in-house SiC BJT, commercial HT capacitors, resistors and an on-board spiral inductor. The measured conversion
gain of the mixer decreases from 15 dB at RT to 4.7 dB at 500 °C. The input 1-dB compression point is 1 dBm at 25 °C and -2.5 dBm at 500 °C. The mixer consumes a DC power of 204 mW. An RF interfacing solution to enable HT characterization of RF circuits is also proposed and employed successfully up to 500 °C. [Paper II]

- **Contribution 3**: A design approach based on small-signal, scattering (S) parameters is validated through demonstration of a SiC-BJT based 58 MHz negative-resistance oscillator (NRO) from RT up to 300 °C. However, during this validation, only the active device was heated while the remaining circuit was kept at room-temperature. [Paper III]

- **Contribution 4**: A 59.5 MHz NRO is designed, prototyped and characterized up to 400 °C. The NRO design is based on the methodology described in [Paper III], however in contrast to [Paper III], the entire circuit and not just the BJT is exposed to HT. Measurement were made on the NRO utilizing the RF interfacing solution proposed in [Paper II] and the results show that the NRO delivers an output power of 11.2 dBm and 8.4 dBm at 25 °C and 400 °C, respectively. The frequency of the oscillator varies by 3.3% in the measured temperature range and its maximum DC power consumption is 431 mW. [Paper IV]

This thesis is part of a collaboration project on the development of HT electronics. The SiC-BJT devices were fabricated by a fellow PhD student at KTH whereas the LTCC boards were manufactured by our collaborating partners at the University of Arkansas. The author was involved in the S-parameter measurements of the fabricated devices. The author also proposed, implemented and measured all RF circuits and designed all test-boards.

1.6 Thesis organization

This thesis is organized into six chapters as follows:

- **Chapter 1** introduces this thesis work. In addition, it provides the motivation, describes the objectives and presents the author’s contribution and the outline.

- **Chapter 2** starts by providing a background of different receiver architectures followed by a survey of HT RF circuits based on various GaN and SiC device technologies. Thereafter, based on high-frequency characterization of in-house SiC BJTs, the selection of RF-band is motivated. The challenges associated with the design, prototyping and characterization of HT RF circuits are highlighted in the end.

- **Chapter 3** reports the design, implementation and characterization of the IF amplifier. The issues pertaining to the device selection and amplifier topology are presented. This is followed by a discussion on the design of matching networks,
electromagnetic (EM) simulations of the spiral inductors and the entire IF amplifier at various temperatures and the selection of HT PCB and capacitors. Finally, the measurement results of the IF amplifier are presented and discussed.

- **Chapter 4** discusses the design, implementation and measurement of two active down-conversion mixer prototypes. The first prototype is mounted on a FR-4 PCB and characterized at RT for functional verification of the mixer whereas the second prototypes is mounted on the LTCC and is characterized up to 500 °C. The chapter also covers the description of an RF interface, proposed for measurements up to 500 °C with the infrastructure currently available at KTH labs.

- **Chapter 5** reports the comparison between different oscillator design methodologies based on small signal S-parameters. Furthermore, it also presents the design, implementation and characterization of three NRO prototypes realized in this work.

- **Chapter 6** concludes the thesis and suggests future research directions.
In this chapter, various receiver architectures are discussed and circuits that constitute a radio receiver are introduced. An overview of the state-of-art high-temperature RF circuits based on SiC and GaN device technologies and the potential and limitations of in-house SiC bipolar technology for developing HT RF circuits are described in detail. Various challenges associated with the complete development cycle of HT RF circuits are also identified.

2.1 Receiver Architectures

Fig. 2.1 shows the block diagram of a typical homodyne receiver. The front-end bandpass filter (BPF) is tuned to the RF frequency \( f_{RF} \) to allow the RF signal to pass while rejecting or attenuating the out-of-band interferes. The low noise amplifier (LNA) amplifies the filtered signal without adding considerable in-band

![Homodyne receiver diagram](image)

Figure 2.1: Homodyne receiver.
CHAPTER 2. HIGH-TEMPERATURE RADIO RECEIVER: BACKGROUND AND CHALLENGES

Figure 2.2: Spectrum of mixing operation in homodyne receiver with symmetric RF input.

Figure 2.3: Spectrum of mixing operation in homodyne receiver with asymmetric RF input.

noise. The noise performance of LNA is critical as the receiver noise factor ($F_{RX}$) is primarily determined by the noise factor of the LNA ($F_{LNA}$), considering that it has sufficiently high gain ($G_{LNA}$), as shown by the following equation:

$$F_{RX} = F_{LNA} + \frac{F_{SS} - 1}{G_{LNA}}$$  \hspace{1cm} (2.1)

where $F_{SS}$ is the noise factor of the subsequent stages following the LNA. The mixer multiplies the amplified RF signal with the local oscillator (LO) signal at a frequency ($f_{LO}$)$=f_{RF}$ to perform the following frequency translation:

$$f_{LO} \pm f_{RF}$$  \hspace{1cm} (2.2)

The desired down-converted signal at $f_{LO} - f_{RF}$ (centered at DC), is subsequently filtered from the up-converted term $f_{LO} + f_{RF}$ and other mixing spurs by using a low pass filter (LPF). The mixing and filtering operations are illustrated in Fig. 2.2.

Even though the homodyne receiver topology in Fig. 2.1 is relatively simple, its application is limited to signals with symmetrical spectrum around $f_{RF}$ (top-left spectrum in Fig. 2.2), e.g. amplitude modulated signals. However, the commonly used modulation schemes like FSK, QPSK and QAM have asymmetric spectrum around $f_{RF}$. The down-conversion of such signals to DC corrupts the output signal spectrum as illustrated in Fig. 2.3. This issue can be circumvented by creating an in-phase ($I$) and a quadrature phase ($Q$) version of the down-converted signal using the homodyne receiver topology in Fig. 2.4. Though exhibiting identical
2.1. RECEIVER ARCHITECTURES

Figure 2.4: Homodyne receiver with IQ demodulator.

spectrum, \( I \) and \( Q \) are separated by a phase difference of \( 90^\circ \) and together can reconstruct the original information. Additionally, \( I \) and \( Q \) can also be exploited to demodulate the amplitude, phase and frequency modulated signals, by using the following relationships:

\[
A = \sqrt{I^2 + Q^2} \quad (2.3)
\]

\[
\phi = \tan^{-1} \left( \frac{Q}{I} \right) \quad (2.4)
\]

\[
f = \frac{\partial \phi}{\partial t} \quad (2.5)
\]

where \( A \), \( \phi \) and \( f \) are the amplitude, phase and frequency of the demodulated signal, respectively.

The homodyne receivers suffer from two issues pertaining to the LO leakage through the parasitic capacitances as shown in Fig. 2.5. Firstly, part of leaked signal from the LO is amplified by the LNA and mixes with itself (LO self-mixing) and produces large DC offsets. These DC offsets can potentially saturate the baseband

Figure 2.5: Leakage of LO signal through the parasitic capacitances.
12

CHAPTER 2. HIGH-TEMPERATURE RADIO RECEIVER: BACKGROUND AND CHALLENGES

Figure 2.6: Heterodyne receiver.

circuits following the LPF. Secondly, a fraction of leaked LO signal is also radiated by the antenna, creating interference in nearby receivers operating in the same band.

The former issue can be resolved by AC coupling (high-pass filtering) the output of the LPF to the subsequent baseband stage. The latter issue is more cumbersome to address as the BPF is unable to suppress the leaked LO signal, which falls inside the RF-band for homodyne receivers. The foregoing discussion suggests that if an LO frequency different than the RF frequency is utilized, the transmission of any leaked LO signal to the antenna is suppressed by the BPF of both the emitting as well as victim receiver. This concept is utilized in the heterodyne receiver topology shown in Fig. 2.6. The first local oscillator (LO₁), at a frequency \( f_{LO₁} \), is used to down-convert the incoming RF signal to an IF frequency \( f_{IF₁} = f_{LO₁} - f_{RF} \). Since \( f_{LO₁} \neq f_{RF} \), any leaked signal from LO₁ is attenuated by the BPF before it can reach the antenna. The down-converted signal at \( f_{IF₁} \) is then amplified by the IF amplifier, which additionally filters out mixing spurs via its bandpass input matching network. The amplification and filtering is preferred at IF frequencies since the gain of amplifying transistors increases and the quality factor requirement for filters decreases with the decrease in frequency, respectively. Following the IF amplifier, the heterodyne topology is similar to Fig. 2.4. However, depending on the final IF frequency \( f_{IF₂} \), the heterodyne receivers are either categorized as zero-IF or low-IF receivers.

In the zero-IF receivers, \( f_{IF₂} = f_{LO₂} - f_{IF₁} = 0 \), which implies that zero-IF heterodyne receivers also suffer from the DC offset issue experienced by their homodyne counterparts. Consequently, a DC block capacitor \( (C_{C}) \) is required to couple the LPF to the baseband stage. To avoid intersymbol interference, \( C_{C} \) should be large enough to prevent considerable loss of signal spectrum near DC, as shown in Fig. 2.7(a). In the low-IF heterodyne receivers, \( f_{IF₂} \) is centered at a low frequency as shown in Fig. 2.7(b). The low-IF heterodyne receiver offers two advantages over its zero-IF counterpart. Firstly, the required value of \( C_{C} \) (consequently, the cutoff-frequency of high pass filter) becomes less stringent. Secondly, the contribution of in-band flicker noise is also reduced as it can be seen by comparing the area of shaded gray regions in Fig. 2.7(a) and Fig. 2.7(b).
2.2 A Survey of High-Temperature RF Circuits

The last section outlined the common radio receiver architectures as well as their pros and cons. This section presents an overview of previously reported HT RF circuits and systems.

Many high-temperature RF circuits based on different SiC and GaN device technologies have been reported over the last few years. These circuits range from oscillators, amplifiers, mixers to subsystems like HT sensors and RF modulators. A group at Virginia Tech has demonstrated building blocks of a HT, low-IF heterodyne transceiver in [55–60]. The transceiver is designed for a RF-band between 230.5 MHz to 285.5 MHz and an ambient temperature of 230 °C. The reported building blocks include an LNA [55], a class-A power amplifier (PA) [56], an IF variable gain amplifier (VGA) [57], a voltage controlled oscillator (VCO) [58] and an active [59] as well as a passive mixer [60]. The commercial 0.25 µm GaN HEMTs by Qorvo are employed as active devices in all these circuits. High-temperature operation of GaN HEMT based RF circuits has been demonstrated by a few other groups as well. For example, 150 °C operation of a 2 GHz, class-E PA based on a discrete GaN power transistor has been presented in [83]. The PA maintained an output power of 4 W and a gain of more than 10 dB for 1500 hours at 150 °C. Similarly, GaN HEMTs on Si substrate have been used to prototype a 58 MHz lamb-wave oscillator in [84]. The oscillator is shown to work up to 250 °C while maintaining an output power of more than 11 dBm.

SiC MESFETs have been used extensively for developing HT RF circuits, especially oscillators [62–69]. The initial works on HT MESFET based oscillators include a 453 MHz cross-coupled differential oscillator working up to 125 °C into a 50 Ω load [64], a 1 GHz Clapp oscillator working up to 200 °C [62] and a 27 MHz Colpitts oscillator designed for pressure sensing applications and operating up to 400 °C [63]. The oscillator design in [62] is later integrated with an on-board slot antenna and the final circuit is shown to work up to 270 °C [65]. The 200 °C and 250 °C operation of a 720 MHz and 940 MHz Clapp oscillator, respectively, is presented in [66]. The 470 °C operation of 30 MHz and 90 MHz Clapp oscillators have been demonstrated in [67]. The oscillators in [67] cease to oscillate above 470 °C due to the excessive leakage currents through the Schottky gate junction of

![Figure 2.7: Output spectrum of heterodyne receiver with (a) zero-IF and (b) low-IF.](image)
CHAPTER 2. HIGH-TEMPERATURE RADIO RECEIVER: BACKGROUND
AND CHALLENGES

the MESFETs. Clapp oscillators, in conjunction with capacitive pressure sensors located in their resonators, have been used to develop 300 °C [68] and 400 °C [69] pressure sensors.

Silicon carbide JFETs have been employed to develop HT RF modulators and sensors in [70–73]. In [70], the output amplitude of a 19 MHz Colpitts oscillator is modulated by varying the gate-voltage of a SiC JFET load connected at the output. The amplitude modulator is shown to work up to 280 °C, although with a non-negligible temperature drift in the resonance frequency and the output voltage. The same group also reported a 300 °C, SiC JFET based frequency modulator in which a SiC varactor is placed in the LC-tank of the oscillator [71]. In [72,73], SiC JFET based temperature and pressure sensors for HT applications have been reported. These sensor systems include transducers, baseband circuits as well as RF transmitters operating at a center frequency of 70 MHz. The aforementioned sensors have been shown to operate up to 450 °C.

2.3 In-House SiC Bipolar Technology

SiC is an excellent semiconductor material for realizing high-temperature electronics. In contrast to Si, which has only one crystal structure, SiC exists in over two hundred different crystal structures or polytypes [85]. These polytypes differ from each other based on the stacking order of a double layer of carbon and silicon atoms. Fig. 2.8 shows the three most common SiC polytypes: 3C-SiC, 4H-SiC and 6H-SiC, where the digits correspond to the number of double layers before the pattern repeats. The electrical proprieties of these three SiC polytypes are compared with Si in Table. 2.1. It can be seen that in addition to offering wider bandgaps as compared to Si, SiC polytypes provide around ten times larger critical electric fields.

![Figure 2.8: Stacking sequence of double layers of the three most common SiC polytypes.](image-url)
2.3. IN-HOUSE SIC BIPOLAR TECHNOLOGY

Table 2.1: Electrical properties of Si and SiC polytypes. aPerpendicular and bparallel to c-axis, where c-axis is normal to the Si-C bilayer plane.

<table>
<thead>
<tr>
<th>Property</th>
<th>Units</th>
<th>SI</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap</td>
<td>eV</td>
<td>1.12</td>
<td>2.4</td>
<td>3.0</td>
<td>3.2</td>
</tr>
<tr>
<td>Critical electric field</td>
<td>MV/cm</td>
<td>0.25</td>
<td>2.0</td>
<td>2.5</td>
<td>2.2</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>W/(cm·K)</td>
<td>1.5</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Saturated electron velocity</td>
<td>cm²/(V·s)</td>
<td>1.0</td>
<td>2.5</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Electron mobility</td>
<td>cm²/(V·s)</td>
<td>1350</td>
<td>1000</td>
<td>500¹/100²</td>
<td>950⁵/1150⁶</td>
</tr>
<tr>
<td>Hole mobility</td>
<td>cm²/(V·s)</td>
<td>480</td>
<td>40</td>
<td>80</td>
<td>120</td>
</tr>
<tr>
<td>Relative permittivity</td>
<td></td>
<td>11.9</td>
<td>9.7</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

...and more than three times better thermal conductivities than Si. The large critical electrical field offered by SiC is exploited widely to develop power devices capable of blocking large reverse voltages. Additionally, large thermal conductivity of SiC assists in better heat transfer from the device to the ambiance. Amongst the three SiC polytypes presented in Table 2.1, 4H-SiC is generally preferred over 3C-SiC and 6H-SiC due to its relatively wider bandgap and higher carrier mobilities.

The SiC group at KTH has over two decades of research and development experience in 4H-SiC bipolar technology [81,82,86,87]. The extensive research and process maturity has led to the development in 4H-SiC BJT based HT analog and mixed signal ICs discussed in Section 1.3, with the future outlook on the realization of large-scale integrated circuits like CPUs. As with the general evolution of new technologies, the development of in-house RF devices is lagging behind its low frequency counterparts. However, the device scaling in the current batch of in-house 4H-SiC BJTs has resulted in an appreciable RF performance improvement as compared to the previous batches as it will be shown in the next subsection.

2.3.1 RF Transistor’s Figures of Merit

The RF transistors are generally benchmarked by two important parameters i.e. the unity current gain bandwidth (\(f_T\)) and unity power gain bandwidth (\(f_{MAX}\)). The \(f_T\) of a BJT is given by:

\[
\frac{1}{2\pi f_T} \approx \frac{(C_{j, BE} + C_{j, BC})}{g_m} + \frac{C_{d, BE}}{g_m}
\]

(2.6)

\[
= \frac{(C_{j, BE} + C_{j, BC})}{g_m} + \left( \frac{t_B^2}{2D_n} + \frac{t_B}{v_{sat}} \right)
\]

(2.7)

where \(C_{j, BE}\) and \(C_{j, BC}\) are the base-emitter and base-collector junction capacitances, \(C_{d, BE}\) is the base-emitter diffusion capacitance, \(g_m\) is the transconductance,
\( v_{\text{sat}} \) is the saturation velocity and, \( t_B \) and \( D_n \) are the thickness and the minority carrier diffusion constant in the quasi-neutral base region, respectively. For sufficiently large values of \( g_m \), \( f_T \) approaches a maximum value, described by the base-transit time in (2.7). The base transit time is typically dominated by the first term, therefore the maximum \( f_T \) of a BJT device technology becomes:

\[
f_T \approx \frac{1}{2\pi} \cdot \frac{2D_n}{t_B^2} \propto \frac{1}{t_B^2}
\]  

Equation (2.8) suggests that \( f_T \) of a bipolar technology can be improved by scaling the thickness of the base region. However, the decrease in \( t_B \) results in an increase in base resistance \( (r_B) \) which, in turn, degrades \( f_{\text{MAX}} \) of the device as shown by the following equation:

\[
f_{\text{MAX}} = \sqrt{\frac{f_T}{8\pi r_BC_{j,BC}}} 
\]  

Therefore, the increase in base-sheet resistance due to the scaling of \( t_B \) is typically compensated by an increase in the doping concentration of the base region.

Previously, \( f_T \) of a 70 \( \mu \)m \( \times \) 24 \( \mu \)m in-house SiC BJT with a base thickness of 0.3 \( \mu \)m and doping concentration of \( 1.4 \cdot 10^{18} \text{ cm}^{-3} \) \cite{Paper_I} was extracted at RT and 150\( ^\circ \)C. The peak \( f_T \) was around 500 MHz and 580 MHz at RT and 150\( ^\circ \)C, respectively. Similarly, \( f_{\text{MAX}} \) was also extracted at 150 \( ^\circ \)C, with a peak value of around 270 MHz. In order to improve the \( f_T \) and \( f_{\text{MAX}} \) of the in-house SiC BJTs, a new batch of devices were fabricated with base thickness scaled down to 0.2 \( \mu \)m whereas doping concentration was increased slightly to \( 1.5 \cdot 10^{18} \text{ cm}^{-3} \). Fig. 2.9(a) and Fig. 2.9(b) shows the chip-layout and photograph of the aforementioned devices, respectively. At the center of the chip, sixteen SiC BJT devices with different dimensions and emitter finger count are connected to RF pads for RF characterization. The last row of the chip contains four de-embedding structures \cite{Paper_I} to remove the parasitics of pads from the measured RF data. The periphery of the chip contains the same SiC BJTs as the centered ones but connected to 80 \( \mu \)m \( \times \) 80 \( \mu \)m DC pads for bond-wiring purposes.

The S-parameters of a 2-fingered, 40 \( \mu \)m \( \times \) 10 \( \mu \)m fabricated device were measured from RT up to 300 \( ^\circ \)C and were used to extract \( f_T \) and \( f_{\text{MAX}} \). The extracted values of \( f_T \) and \( f_{\text{MAX}} \) are shown in (Fig. 4, \cite{Paper_I}). It can be seen that the peak value of \( f_T \), at RT and 300 \( ^\circ \)C, is around 2.9 GHz and 1.7 GHz, respectively, which is a considerable improvement as compared to the previous batch. Similarly, an increase in peak \( f_{\text{MAX}} \) was also observed with RT and 300 \( ^\circ \)C values of \( f_{\text{MAX}} \) improving to around 393 MHz and 304 MHz, respectively. The relatively low values of \( f_{\text{MAX}} \) as compared to \( f_T \) are attributed to high base resistance of SiC bipolar technology \cite{Paper_I}.
2.3. IN-HOUSE SiC BIPOLAR TECHNOLOGY

2.3.2 Proposed Circuits for Radio Receiver

As mentioned in Section 1.4, the aim of this thesis is the development of proof-of-concept, 4H-SiC BJT-based RF circuits for a HT radio receiver. Since a radio receiver is composed of several RF circuits, it is imperative to investigate which of those circuits are practically realizable with the current batch of devices. To this end, the feasibility of a heterodyne receiver topology with low-IF is studied as a test case. The preference of selected receiver topology is motivated by the advantages it offers over other receiver architectures as discussed in Section 2.1.

Fig. 2.10 shows a low-IF heterodyne receiver. The selection of RF-band of the receiver depends on the amplification capability of the fabricated SiC BJTs at high-frequencies. The maximum available gain ($MAG$) provided by a two-fingered, $40 \mu m \times 10 \mu m$ SiC BJT as a function of frequency is shown in Fig. 2.11. The $MAG$ is relatively reasonable (>10 dB) at 25 °C and 300 °C for frequencies up to 500 kHz.
CHAPTER 2. HIGH-TEMPERATURE RADIO RECEIVER: BACKGROUND AND CHALLENGES

Figure 2.11: Maximum available gain of the SiC BJT at $I_C = 10$ mA.

59 MHz. However, the antenna dimensions at these RF frequencies can be quite large. The situation is further exacerbated by the fact that the minimum noise figure of the SiC BJT is around 20 dB (Fig. 6, [Paper I]), much larger than the state-of-art HT GaN HEMT based LNA reported in [55]. Both these factors suggest that the current batch of SiC BJTs are not suitable for developing the RF receiver front-end and further device optimization is required to increase the high-frequency gain of SiC BJTs to allow smaller antenna dimensions and also to improve their noise performance. Nevertheless, the fabricated SiC BJTs can still be employed for developing RF circuits following the RF receiver front-end (gray region in Fig. 2.10) as motivated below.

As the input signal gets amplified and down-converted by the RF receiver front-end (based on a future generation of SiC BJTs with possibly better high-frequency gain and noise performance), the noise contribution of IF amplifier will be attenuated considerably (eqn. 2.1). Moreover, the current batch of SiC BJTs provide reasonable gain at frequencies up to 59 MHz as shown in Fig. 2.11. The two preceding arguments motivated the design of 59 MHz IF amplifier based on the "noisy" fabricated devices [Paper I]. The tuned IF amplifier is followed by a second mixer which down-converts the output of IF amplifier to a non-zero intermediate frequency. As the second mixer stage typically drives baseband amplifiers, the low-IF should be selected such that it remains within the bandwidth of these amplifiers. Previously published HT baseband amplifiers have demonstrated a bandwidth of around 500 kHz [48,51]. Therefore, a low-IF of 500 kHz was selected and an active mixer was designed to provide a 59 MHz to 500 kHz down-conversion [Paper II]. Lastly, a 59.5 MHz local oscillator was designed to allow the aforementioned frequency translation by the mixer [Paper IV].

This work in relation with other state-of-art HT RF circuits based on different wide-bandgap semiconductor device technologies is summarized in Table 2.2.
Table 2.2: An overview of state-of-art high-temperature RF circuits.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Circuit</th>
<th>Max. Temp. [°C]</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN HEMT</td>
<td>Low noise amplifier</td>
<td>230</td>
<td>[55]</td>
</tr>
<tr>
<td></td>
<td>Power amplifier</td>
<td>230</td>
<td>[56]</td>
</tr>
<tr>
<td></td>
<td>IF variable gain amplifier</td>
<td>230</td>
<td>[57]</td>
</tr>
<tr>
<td></td>
<td>Voltage controlled oscillator</td>
<td>230</td>
<td>[58]</td>
</tr>
<tr>
<td></td>
<td>Mixers</td>
<td>250</td>
<td>[59,60]</td>
</tr>
<tr>
<td>SiC MESFET</td>
<td>Oscillator</td>
<td>470</td>
<td>[67]</td>
</tr>
<tr>
<td></td>
<td>Pressure sensor</td>
<td>400</td>
<td>[69]</td>
</tr>
<tr>
<td>SiC JFET</td>
<td>RF modulators</td>
<td>300</td>
<td>[71]</td>
</tr>
<tr>
<td></td>
<td>Temperature sensor</td>
<td>450</td>
<td>[72]</td>
</tr>
<tr>
<td></td>
<td>Pressure sensor</td>
<td>450</td>
<td>[73]</td>
</tr>
<tr>
<td>SiC BJT</td>
<td>IF amplifier</td>
<td>251</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Oscillator</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mixer</td>
<td>500</td>
<td></td>
</tr>
</tbody>
</table>

### 2.4 RF Circuit Development at High-Temperatures

The development of HT RF circuits has challenges at each step of the development process, i.e. design, prototyping and characterization. In this section, these challenges are identified while the proposed solutions are presented in later chapters.

#### 2.4.1 Design Challenges

The availability of accurate device models for the active devices is invaluable during the design phase of circuit development. Such device models are used in conjunction with computer aided design (CAD) tools to design, simulate and analyze the circuits for their functionality and performance. Spice Gummel Poon (SGP) [89] is a BJT device model that has been used extensively by our group (specifically, its DC version) to design a number of HT SiC BJT analog and mixed-signal circuits. However, the development of SGP model is complex and time-consuming due to a large number of measurements needed for its parameter extraction process. The situation is further aggravated for high-frequency device modeling as the parameter extraction process (which now requires AC parameters as well) has to be repeated at multiple temperature points in order to design wide-temperature range circuits. To circumvent this modeling effort, design methodologies based on small-signal S-parameters were employed for developing the RF circuits in this work.
2.4.2 Prototyping Challenges

Hybrid circuit technology has predominately been used for prototyping HT RF circuits [55–60, 62–73]. This is in contrast to the reported HT digital and analog circuits which are almost exclusively based on on-chip integrated circuits with occasional off-chip passive components. One possible reason for the absence of SiC-based extreme temperature RF ICs in the reported literature is the unavailability of a repeatable IC fabrication process and the corresponding high-frequency, high-temperature device models. Impedance matching, which is a key aspect of RF circuit design, requires a-priori knowledge about the input and output impedance of active devices used to design RF ICs. As the high-temperature SiC device technologies are still going through a continuous research phase, impedances of one batch of device may differ considerably from the next batch under the same operating conditions. These process variations can potentially result in a considerable RF IC performance degradation due to mismatch losses.

The hybrid RF circuit technology is based on discrete active devices, mounted with the required circuit passives on HT PCB boards. Therefore, in addition to the HT capability of active devices, the performance of PCBs and reliability of passives also becomes crucial at high temperatures. Table 2.3 lists PCB boards that have been used previously for prototyping HT RF circuits. These substrates generally remain stable with very little change in their dielectric constant with temperature [57, 59, 90]. In regard to passives, a few vendors offer HT capacitors, inductors and resistors for space and military applications. For example, Compex offer capacitors rated up to 120 °C and IPDiA, Murata and Presidio Components Inc. provide HT capacitors with temperature rating of 250 °C. Coilcraft and Vishay offer 240 °C air core inductors and 250 °C thick-film resistors, respectively. The temperature ratings of these commercially available passives fall short of the stringent demands imposed on them by some of the HT applications in Table. 1.1. Nevertheless, a few of these commercial passives have been used with success at temperatures beyond their specified ratings [68, 90]. Though, a similar approach has been utilized in this work as well, the intrinsic reliability associated with utilizing passives beyond their

Table 2.3: High-temperature PCBs.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>( \epsilon_r )</th>
<th>CTE (ppm/°C)</th>
<th>Temp. [°C]</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO 3010</td>
<td>11.2</td>
<td>16</td>
<td>230</td>
<td>[57]</td>
</tr>
<tr>
<td>RO 4003C</td>
<td>3.55</td>
<td>46</td>
<td>250</td>
<td>[59]</td>
</tr>
<tr>
<td>Aluminum nitride</td>
<td>9</td>
<td>4.02</td>
<td>280</td>
<td>[70]</td>
</tr>
<tr>
<td>Aluminum oxide</td>
<td>9.8</td>
<td>6.82</td>
<td>470</td>
<td>[67]</td>
</tr>
<tr>
<td>LTCC</td>
<td>7.1</td>
<td>4.4</td>
<td>450</td>
<td>[72, 73]</td>
</tr>
</tbody>
</table>

1Presidio Components Inc. has recently started offering 500 °C capacitors
rated temperatures necessitates further research and development.

2.4.3 Measurement Challenges

The characterization of hybrid RF circuits require a coplanar (or microstrip) to coaxial interface between the input/output ports of the circuit and the measuring instrument. Two commonly used RF interfaces include SubMiniature version A (SMA) connectors and RF probes. The HT operation of the SMA connectors is limited by their temperature rating to about 200 °C. However, in [59, 60], SMA connectors have been shown to operate up to 250 °C. In [91], NASA has demonstrated a measurement setup capable of characterizing RF circuits above 500 °C. The measurement setup is based on a thermal chuck for heating the PCB and above the thermal chuck, two RF probe fixtures are installed to hold the customized ground/signal/ground (GSG) RF probes. At KTH, there is a similar RF measurement setup but it does not allow measurements beyond 300 °C due to the heating limitation of the thermal chuck. Another thermal chuck at KTH can go as high as 600 °C, but it lacks the necessary fixtures to hold the RF probes. Therefore, based on the existing infrastructure at KTH, a HT RF measurements setup has been proposed and shown to work up to 500 °C [Paper II]. The details of the proposed measurement setup are provided in Chapter 4.
Chapter 3

Intermediate-Frequency Amplifier

The amplifier design at RF and microwave frequencies fundamentally involve implementation of appropriate matching networks around the active device. These matching networks are designed to exploit the transistor properties for meeting certain noise, output power, gain and bandwidth specifications. For instance, noise figure of a transistor can be minimized by providing optimal reflection coefficient at the input port, output power can be maximized by load-line match at the output port and gain can be maximized by conjugately matching both the input and output ports of the transistor to the source and load impedances, respectively.

In this chapter, the design of a 59 MHz HT IF amplifier, based on the fabricated SiC BJTs, is discussed in detail. The design goal is to maximize the gain provided by the SiC BJTs by employing tuned matching networks. The chapter begins with a brief introduction to the fundamentals of amplifier design. In particular, the design equations required for simultaneous conjugate matching and stability analysis are provided. A discussion on the selection of BJT size and amplifier topology is presented thereafter. This is followed by a complete description of IF amplifier circuit design, simulations, analysis and prototyping. The measurement results are provided at the end.

3.1 Amplifier Design Fundamentals

The block diagram of a single stage, tuned amplifier is shown in Fig. 3.1. $Z_S$ and $Z_L$ represent the source and load impedances (typically 50 Ω), respectively. $\Gamma_S$ and $\Gamma_L$ are the reflection coefficients looking into the input and output matching networks whereas $\Gamma_{IN}$ and $\Gamma_{OUT}$ are the reflection coefficients looking into the input and output ports of the transistor, respectively. The power gain ($G_T$) of the amplifier is defined as the ratio between the power delivered to the load and the power available from the source. The expressions for $G_T$ in terms of $\Gamma_S$, $\Gamma_L$ and
CHAPTER 3. INTERMEDIATE-FREQUENCY AMPLIFIER

Figure 3.1: Block diagram of a tuned amplifier.

S-parameters of the transistor are given as [92]:

\[
G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{3.1}
\]

\[
= \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT}\Gamma_L|^2} \tag{3.2}
\]

where

\[
\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{3.3}
\]

\[
\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{3.4}
\]

In order to maximize \(G_T\), the matching networks are designed to transform \(Z_S\) and \(Z_L\) to satisfy the following conditions for simultaneous conjugate matching:

\[
\Gamma_S = \Gamma_{IN}^\ast \tag{3.5}
\]

and

\[
\Gamma_L = \Gamma_{OUT}^\ast \tag{3.6}
\]

Solving (3.3) to (3.6) give the values of \(\Gamma_S\) and \(\Gamma_L\) required for designing the input and output conjugate matching networks, respectively. Terming these as \(\Gamma_{MS}\) and \(\Gamma_{ML}\), we get:

\[
\Gamma_{MS} = \frac{B_1 \pm \sqrt{B_1^2 - 4C_1^2}}{2C_1} \tag{3.7}
\]

\[
\Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4C_2^2}}{2C_2} \tag{3.8}
\]

where

\[
B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{3.9}
\]

\[
B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{3.10}
\]
3.2. DEVICE AND TOPOLOGY SELECTION

\[ C_1 = S_{11} - \Delta S^*_2 \] \tag{3.11} \\
\[ C_2 = S_{22} - \Delta S^*_1 \] \tag{3.12} \\
and \\
\[ \Delta = S_{11}S_{22} - S_{12}S_{21} \] \tag{3.13}

Another important consideration while designing an amplifier is to keep it stable. An amplifier is unconditionally stable if \(|\Gamma_{IN}| < 1\) and \(|\Gamma_{OUT}| < 1\) for all passive source and load impedances, i.e. \(|\Gamma_S| < 1\) and \(|\Gamma_L| < 1\). A convenient way to express the necessary and sufficient conditions for unconditional stability are:

\[ K > 1 \quad \text{and} \quad |\Delta| < 1 \] \tag{3.14}

where

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \] \tag{3.15}

An unconditionally stable amplifier will not oscillate for any combination of source and load impedances. Furthermore, for an unconditionally stable transistor, the expressions for \(\Gamma_{MS}\) and \(\Gamma_{ML}\) in (3.7) and (3.8) with minus signs are meaningful and are subsequently used for designing the matching networks.

3.2 Device and Topology Selection

As mentioned in Section 2.3.1, the fabricated chips contain sixteen different SiC BJTs, with varying emitter lengths and number of emitter fingers. In particular, each chip contains BJTs with four emitter lengths i.e. 40 \(\mu\)m, 50 \(\mu\)m, 60 \(\mu\)m and 70 \(\mu\)m with 1, 2, 4 and 6 emitter fingers for each of the aforementioned length. The width of emitter fingers in all the devices was kept at 10 \(\mu\)m. The fundamental reason behind adding different transistor sizes was to analyze the effect of emitter scaling on the device performance as well as the development of scaled device models in future research projects. In this work, RF circuits have been designed using only two of the sixteen device variants, i.e. BJTs with emitter finger dimensions of 40 \(\mu\)m \(\times\) 10 \(\mu\)m and emitter finger count of 2 and 4. Accordingly, these two devices were compared for their feasibility as amplifying stages in the IF amplifier, for three BJT configurations, i.e. common-base (CB), common-emitter (CE) and common-collector (CC).

Fig. 3.2(a), Fig. 3.2(b) and Fig. 3.2(c) show the MAG of the 2-fingered BJT at 25 °C and 300 °C in CB, CE and CC configuration, respectively. The BJT is biased at a collector current \((I_C)\) of 10 mA since increasing \(I_C\) beyond that resulted in only marginal improvement in power gain (Fig. 5, [Paper I]). In CB configuration, the power gain of the BJT is around 2 dB at 59 MHz, a value too small for practical applications. The fundamental reason behind this small power
gain is that the device is operating as a current-buffer in CB configuration which "nullifies" the major contributor of the power gain in the SiC BJT, i.e. its current gain. A comparison between the power gain of CE and CC configuration shows that at 59 MHz and 25 °C, the aforementioned topologies offer almost similar gain. However at 300 °C, the CE configuration offers about 1.5 dB more power gain than the CC configuration. This suggests that CE topology is a better candidate for implementing the IF amplifier, especially at elevated temperature, as compared to its CC counterpart.

The maximum available gain of the 4-fingered BJT at 25 °C and 300 °C in CB, CE and CC configuration is shown in Fig. 3.3(a), Fig. 3.3(b) and Fig. 3.3(c), respectively. To keep the analysis comparable with the 2-fingered BJT, the biasing current density of 4-fingered BJT was kept the same as the 2-fingered BJT. This
3.3 Circuit Design, Simulation Results and Prototyping

3.3.1 Circuit Design and Schematic Simulations

The S-parameters of the transistor are required to design the input and output matching networks for simultaneous conjugate matching. Accordingly, S-parameters of a 2-fingered, 40 $\mu$m x 10 $\mu$m on-wafer SiC BJT were measured with the Agilent’s vector network analyzer (E8361A) using GGB Industries’s high temperature RF probes (40A-GSG-150-DP-HT). The calibration up to the tips of the probes was performed at 25 °C using short-open-load-through (SOLT) standards on a CS-5 calibration substrate. Following the calibration, S-parameter measurements of the transistor were made at various temperature points between 25 °C to 300 °C. The measured S-parameters of the transistor were then de-embedded from the RF pads using an open, on-wafer de-embedding structure. The de-embedding process involves [88,93]:

1. Converting the measured S-parameters of the transistor ([S]_M) and the open-structure ([S]_O) to corresponding Y-parameters

Figure 3.4: Block diagram of the proposed two stage IF amplifier.
• \([S]_M \rightarrow [Y]_M\) and \([S]_O \rightarrow [Y]_O\)

2. Subtracting the Y-parameters of the open-structure from the Y-parameters of the transistor
   • \([Y] = [Y]_M - [Y]_O\)

3. Converting the resultant Y-parameters from step-2 back to the S-parameters
   • \([Y] \rightarrow [S]\)

The de-embedded S-parameters of the BJT at 25 °C, 100 °C, 200 °C and 300 °C are shown in Fig. 3.5. The same de-embedding procedure was performed for all S-parameter measurements in this work but the process will not be restated for the sake of brevity. The de-embedded S-parameters in Fig. 3.5 were used to design both stages of the IF amplifier. The utilization of same set of S-parameters for both transistors imply identical input and output matching networks for both transistors.

Figure 3.5: De-embedded S-parameters of a 2-fingered, 40 \(\mu\)m \(\times\) 10 \(\mu\)m SiC BJT in CE configuration biased at \(I_C = 10\) mA.
amplifying stages in Fig. 3.4. This was done primarily because each fabricated chip had only one RF pad-connected BJT of same dimensions (and finger count). On the other hand, each chip contained two BJTs of same dimensions (and finger count) connected to the DC pads (peripheral devices in Fig. 2.9). Fig. 3.6(a) and Fig. 3.6(b) shows the RF pad-connected and the DC pad-connected 2-fingered, 40 \( \mu m \times 10 \mu m \) SiC BJTs, respectively. The actual amplifier was implemented using the two DC pad-connected BJTs, which though were physically different from the RF-pad connected BJT (whose S-parameters are shown in Fig. 3.5), but were dimensionally identical and located on the same chip as well. It was assumed that due to the close proximity of the BJTs used for designing and implementing the amplifier, their S-parameter dispersion would be negligible. The same procedure was repeated for almost all the circuits presented in this work. The only exception is the first oscillator prototype presented in Section 5.2, where the same transistor was used for designing and implementing the circuit.

Note that the S-parameters of SiC BJT in Fig. 3.5 are different at different temperatures. This temperature dependence of S-parameters poses a fundamental question while designing matching networks of wide temperature range RF circuits. That is, S-parameters of which temperature point should be employed for designing the matching networks? A few possible choices are the minimum or maximum temperatures in the temperature range of interest or the average temperature between the two extremes. For instance, in the GaN HEMT based PA [56] and IF amplifier [57], the matching networks were designed using the S-parameters of the HEMTs at 230 °C, the maximum temperature targeted by the aforementioned amplifiers. For the amplifier design, S-parameters at 100 °C were selected as a somewhat arbitrary starting point. The optimization and tuning of the matching networks (if required) can be considered during EM simulations of the IF amplifier, as it will be discussed shortly.

The first step in the amplifier design is usually the evaluation of the active device for stability. Using (3.13) and (3.15), the \( K \) factor and \( |\Delta| \) of the SiC BJT were calculated at 25 °C, 100 °C, 200 °C and 300 °C as shown in Fig. 3.7. It can be seen that the SiC BJT fulfills the criteria for unconditional stability given
in (3.14) at all the measured temperatures and throughout the frequency range. This implies that the amplifier does not require a network for stabilizing the active device. Following the stability analysis, equations (3.7) to (3.13), in conjunction with the S-parameters of SiC BJT at 100 °C, were used to find $\Gamma_{MS}$ and $\Gamma_{ML}$. The calculated values of $\Gamma_{MS}$ and $\Gamma_{ML}$ are:

\[
\Gamma_{MS} = 0.983 \angle 2.06^\circ \quad \text{and} \quad \Gamma_{ML} = 0.703 \angle 30.13^\circ
\]  

(3.16)

Since the IF center frequency is relatively small for utilizing transmission lines based matching, only the lumped capacitors and inductors based matching networks were considered. An L-section matching network topology was selected for transforming the 50 $\Omega$ impedance to the desired reflection coefficients in (3.16). The L-section matching networks are simple to design and require only two reactive components. However, the bandwidth of an L-section is solely a function of load and source resistances across the L-section [94]. Therefore, for applications where high frequency selectivity or wideband matching networks are required, an L-section network may have to be replaced by a $\pi$, $T$ or a multi-section L network. Since the proposed IF amplifier is not designed to fulfill any bandwidth constraints, the L-section matching was chosen as it reduces the number of passive components and circuit complexity.

The input and output matching networks were designed using the Smith Chart Utility of Keysight’s (formerly Agilent) Advanced Design System (ADS). Fig. 3.8(a) and Fig. 3.8(b) show the input and output matching networks of the SiC BJT in CE configuration. The matching networks were designed using lumped inductors and standard valued capacitors. The networks in Fig. 3.8(a) and Fig. 3.8(b) are not the only L-sections that can perform the desired matching. Fig. 3.9(a) and Fig. 3.9(b) show two alternate L-sections that can also accomplish the required matching. However, in this work, the L-sections in Fig. 3.8 were preferred over the ones in Fig. 3.9 for a couple of reasons. Firstly, the inductors required in Fig. 3.8...
3.3. CIRCUIT DESIGN, SIMULATION RESULTS AND PROTOTYPING

Figure 3.8: (a) Input and (b) output matching of the BJT in CE configuration.

are smaller in size as compared to their corresponding counterparts in Fig. 3.9. The small inductors present compact footprint and also facilitate in satisfying the condition generally imposed on matching network inductors (i.e. their self-resonant frequency (SRF) should be sufficiently large as compared to the design frequency). Secondly, the L-sections in Fig. 3.8 can also act as biasing networks, i.e. the series capacitors can act as DC blocks whereas the shunt inductors can be employed as RF choke (RFC) inductors for DC feeding. The utilization of matching network

Figure 3.9: Alternate (a) input and (b) output matching of the BJT in CE configuration.
for biasing eliminates the need for additional large RFC inductors and DC block capacitors, thereby greatly simplifying the circuit implementation. The complete circuit diagram of the proposed IF amplifier is shown in (Fig. 7, [Paper I]).

The schematic level simulations of the complete IF amplifier were carried out in ADS. The quality factor of the inductors ($Q_L$) and capacitors ($Q_C$) were assumed to be 50 and 100, respectively. The selected values of $Q_L$ and $Q_C$ were based on the results in [62] and some preliminary EM simulations on inductors. Fig. 3.10(a), Fig. 3.10(b) and Fig. 3.10(c) shows the simulated $S_{11}$, $S_{22}$ and $S_{21}$ of the IF amplifier at 100 °C, respectively. It can be seen that at 59 MHz, the amplifier demonstrates an excellent input and output matching of -65 dB and -27 dB, respectively. The simulated $S_{21}$ of the amplifier at 59 MHz is 22 dB, which is about 2 dB smaller than the ideal MAG of two SiC BJTs in CE configuration. This result is fairly reasonable and can be expected for matching networks implemented using lossy passive components.

### 3.3.2 Post-Layout EM Simulations

At the beginning of this research project, the setup for measuring RF circuits beyond 300 °C was not established and therefore the IF amplifier was developed targeting the maximum temperature limit of 300 °C. Therefore, a Rogers-4003C PCB was selected for implementing the IF amplifier since its glass transition temperature is 150 °C.
3.3. CIRCUIT DESIGN, SIMULATION RESULTS AND PROTOTYPING

Figure 3.12: Simulated effective inductance of the (a) input and (b) output matching network inductors versus frequency.

Temperature is in excess of 280 °C. The PCB employed 35 µm copper metalization with electroless nickel/immersion gold (ENIG) surface finish. Fig. 3.11 shows the PCB stack used for EM simulations and prototyping. \textit{cond}, \textit{cond2} and \textit{hole} represent the top metalization, bottom metalization and the via layers, respectively. An additional substrate was added under \textit{cond2} to electrically isolate it from the metallic thermal chuck used for HT characterization.

First, the spiral inductors were designed for the matching networks using the EM simulator of ADS. The spacing between the inductor coils and the width of the coils were kept at 0.3 mm for both input and output matching network inductors. In order to decrease the area footprint, the input matching network (=1050 nH) was realized by stacking two spiral inductors, one on \textit{cond} and the other on \textit{cond2}, of the PCB. The total inductance \((L_T)\) of a stacked inductor is a sum of individual single layer spirals and their mutual inductance:

\[ L_T = L_1 + L_2 + M_{12} \]  \hspace{1cm} (3.17)

where \(L_1, L_2\) and \(M_{12}\) are the individual single layer spiral inductances and the mutual inductance between the two spirals, respectively. For the output matching network inductor (=202 nH), a single spiral inductor on \textit{cond} was used while the crossover was done in \textit{cond2}.

To analyze the effect of temperature on the inductance and \(Q_L\), resistivity of the metalization layers \((\rho)\) was varied according to the following relationship:

\[ \rho = \rho_c(1 + \alpha \Delta T) \]  \hspace{1cm} (3.18)

where \(\rho_c=1.724 \mu\Omega \cdot \text{cm}, \alpha=0.00393/°\text{C} \) (for annealed copper [95]) and \(\Delta T\) is the temperature difference from RT. Fig. 3.12(a) and Fig. 3.12(b) show the simulated effective inductance \((L_E)\) of the input and output matching network inductors as
CHAPTER 3. INTERMEDIATE-FREQUENCY AMPLIFIER

(a)

Figure 3.13: Simulated quality factor of the (a) input and (b) output matching network inductors versus frequency.

The $L_E$ was calculated from the simulated Y-parameters of the inductors using the equation:

$$ L_E = \frac{\text{Im}\left(\frac{1}{Y_{11}}\right)}{\omega} \quad (3.19) $$

where $\omega$ is the frequency in radians. It can be seen from Fig. 3.12(a) and Fig. 3.12(b) that the input and output matching network inductors have an $L_E$ of about 1050 nH and 202 nH, respectively at 59 MHz. Furthermore, $L_E$ for both inductors remain virtually unchanged with temperature (only 0.5% variation). A similar observation about temperature variation of gold spiral inductors on alumina substrate was made in [96]. The simulated $Q_L$ of both the input and output matching network inductors are shown in Fig. 3.13(a) and Fig. 3.13(b), respectively. The $Q_L$ was calculated from the simulated Y-parameters of the inductors using the equation:

$$ Q_L = \frac{\omega L_E}{\text{Re}\left(\frac{1}{Y_{11}}\right)} \quad (3.20) $$

One can see that the $Q_L$ decreases with temperature. This decrease in $Q_L$ is a consequence of increase in metalization resistivity with temperature. Finally, layout of the complete amplifier, employing the aforementioned inductors, was designed and simulations were performed at 25 °C, 100 °C, 200 °C and 300 °C. Fig. 3.14 shows the S-parameters of IF amplifier from the EM simulations. $Q_C$ of 100 was assumed for the simulations. At a frequency of 59 MHz, the worst case input and output matching occurs at 25 °C, with $S_{11} \approx -13$ dB (5% reflected power) and $S_{22} \approx -22$ dB (0.6% reflected power). The EM simulated $S_{21}$ of the amplifier at 59 MHz is 22 dB at RT which gradually drops to about 19 dB at 300 °C. The simulation
results indicate that the amplifier performance is fairly reasonable throughout the temperature range and consequently no optimization was considered.

3.3.3 Prototyping and Measurement Setup

The amplifier prototype is shown in Fig. 3.15. The PCB contains the IF amplifier circuit as well as the test structures for characterizing the inductors. The input and output coplanar-to-coax interface to the IF amplifier was provided through RF probes, therefore the PCB also contains the GSG input/output (IO) pads for landing those probes. On the bottom metalization, one can see the ground plane, the bottom spiral of the stacked input matching network inductors and the crossovers for the output matching network inductors. The complete IF amplifier, which includes the HT capacitors as well as the SiC BJTs bond-wired to the PCB, is shown
For HT characterization of the amplifier, the PCB was placed on a thermal chuck as shown in Fig. 3.16(a). The biasing was provided through five DC needles held by the DCM-210 positioners. The HT RF probes supported by two 180° apart RF fixtures from Cascade Microtech were used to connect the VNA ports to the GSG IO pads of the amplifier. Fig. 3.16(b) shows the dummy PCB which was added under the PCB containing the circuit to electrically isolate the latter from the thermal chuck. The amplifier was characterized at chuck temperatures of 25 °C, 100 °C and then in 50 °C steps up to the final temperature of 300 °C. At each value of the aforementioned chuck temperature, the equilibrium temperature at the top of the PCB was monitored with an IR thermometer and reported in [Paper I].

3.4 Measurement Results

The measurement results of the proposed IF amplifier are fully presented in [Paper I]. The measurements showed that the center frequency of the IF amplifier is shifted down to around 54.6 MHz as compared to the design value of 59 MHz. This frequency deviation can be attributed to the measured effective inductance of the input and output matching inductors being larger than their simulated counterparts (Fig. 13(a), [Paper I]), the tolerances in the matching capacitors, and the parameter variation of SiC BJTs used for implementing the amplifier as compared to the ones used for simulations (as discussed in Section 3.3.1). Although around the center frequency, both $S_{11}$ and $S_{22}$ degrade with temperature, the amplifier still maintains a reasonable match ($S_{11} < -7$ dB and $S_{22} < -11$ dB) at 54.6 MHz, throughout the entire temperature range. The maximum measured gain of the amplifier degraded from 22 dB to 16 dB as the chuck temperature was increased from 25 °C to 300 °C. The output 1-dB compression point of the IF amplifier remained fairly constant around 1.4 dBm with temperature. The amplifier consumes a DC
power of 221 mW. The measured performance of the IF amplifier demonstrates the feasibility of SiC BJTs for developing HT gain blocks for communication receivers.
Chapter 4

Active Down-Conversion Mixer

Mixers are critical building blocks of a communication system, where they are used for frequency translation in conjunction with the oscillators. In this chapter, the design, simulation and measurements of two SiC BJT-based active down-conversion mixers are presented. The first mixer is prototyped for RT operation and laid the foundation for the development of 500 °C mixer, presented in [Paper II]. Both mixers were designed for RF ($f_{RF}$), LO ($f_{LO}$) and IF frequencies ($f_{IF}$) of 59 MHz, 59.5 MHz and 500 kHz, respectively, in accordance with the specification in Section 2.3.2. A detailed description of the measurement setup which allowed RF characterization of the proposed mixers is also presented.

4.1 Mixer Design Fundamentals

In its simplest form, a mixer can be realized with a switching transistor. If the LO signal is controlling the switching activity and the RF signal is applied to the input of the switch, then the output is effectively the multiplication of RF input by a square wave, toggling between 0 and 1. This multiplication leads to the desired IF term (as well as some 'mixing spurs'). However, the switching mixer belongs to passive class of mixers which do not provide any gain. In fact, the conversion loss of a switching mixer is $1/\pi \approx -10 \text{ dB}$ [97].

Active mixers, on the other hand, not only mix the RF and LO signals but also provide conversion gain (CG). Fig. 4.1 shows a single-ended, active mixer topology. Although the circuit in Fig. 4.1 employs bipolar transistors, the analysis remains valid for other transistors as well. The transistor $M_1$ acts a transconductance amplifier, converting the RF input voltage to current. The transistor $M_2$ operates as a switch and toggles the current reaching collector resistor ($R_C$) on and off. The conversion gain of the mixer in Fig. 4.1, for a large LO swing is given by [97]:

$$CG = \frac{1}{\pi} gm_1 R_C$$

(4.1)
where $gm_1$ is the transconductance of transistor $M_1$. Therefore, by controlling $gm_1$ and $R_C$, arbitrarily large CG can be obtained (practical values are limited by the power budget, supply voltage etc.).

Note that the mixer topology in Fig. 4.1 employs two separate BJTs (and matching networks) for the RF and LO signals. A relatively simpler active mixer topology, employing only a single transistor, is shown in Fig. 4.2 [98]. Both the LO and RF signals are applied to the base of same BJT whereas the IF output is tapped from the collector. Ignoring the DC signals and higher order terms, the collector current of BJT in Fig. 4.2 is given as [98]:

$$I_C = ... + \frac{1}{2}BV_{RF}V_{LO}\{\cos[2\pi(f_{LO}-f_{RF})t] + \cos[2\pi(f_{LO}+f_{RF})t]\} + ... \quad (4.2)$$

where $V_{RF}$ and $V_{LO}$ are the portion of RF and LO voltages reaching the base of BJT from the respective ports whereas $B$ is the second derivative of collector
current with respect to base voltage. The desired IF output voltage is simply the down-converted component in (4.2) times $R_C$. Since the mixer topology in Fig. 4.2 requires a single transistor (and matching network) as compared to the two in Fig. 4.1, it is relatively simple to implement. For this reason, both SiC-BJT mixers in this work are implemented using the mixer topology in Fig. 4.2.

4.2 First Prototype: Evaluation of Mixer Performance at RT

The mixing of RF and LO signals is related to the large-signal behavior of non-linear devices (term $B$ in (4.2)). Therefore, large-signal models of nonlinear devices are invaluable for designing mixer circuits for a particular CG, port isolation, noise performance, etc. Due to the unavailability of such models for SiC BJTs, a workaround based on the following two steps was adopted. In the first step, a mixer circuit was designed only for RT operation using the small-signal S-parameters of a SiC BJT [98]. The performance of the designed circuit was evaluated at RT by prototyping it on an FR-4 PCB. In the second step, a second mixer was designed in a way similar to the first but prototyped on an LTCC board to allow for HT measurements.

In the rest of this section, design, prototyping and characterization of the first prototype are discussed. The measurement setup which enabled characterization of RF circuits without employing RF probes is also presented.

4.2.1 Circuit Design and Simulation Results

The proposed mixer, based on the topology shown in Fig. 4.2, was designed using the RT S-parameters of a 2-fingered, 40 $\mu$m $\times$ 10 $\mu$m SiC BJT in CE configuration. The LO signal was coupled to the transistor via a coupling capacitor ($C_{LO}$). The value of $C_{LO}$ should be small enough to prevent considerable RF signal leakage to the LO port. The coupling of RF signal to the LO port is quantified by the return loss, which is given as [98]:

$$\text{Return Loss} = -20 \log |\Gamma_{LO}|_{f_{RF}}$$

where $\Gamma_{LO}|_{f_{RF}}$ is the value of $\Gamma_{LO}$ at $f_{RF}$. The return loss at $f_{RF}$ as a function of $C_{LO}$ is shown in Fig. 4.3. Note that the return loss is $\approx0$ dB around 1 pF and increases with $C_{LO}$. A $C_{LO}$ of 7 pF was selected which gives a return loss of 0.28 dB at $f_{RF}$. A 0.28 dB return loss implies that only about 6% of the incoming RF power is leaked to the LO port. However, as $f_{RF}$ is very close to $f_{LO}$, a large part of LO signal also gets attenuated by $C_{LO}$. This attenuation is quantified by the insertion loss, which is given as [98]:

$$\text{Insertion Loss} = -10 \log \left(1 - |\Gamma_{LO}|^2_{f_{LO}}\right)$$
where $\Gamma_{LO}|_{f_{LO}}$ is the value of $\Gamma_{LO}$ at $f_{LO}$. The insertion loss at $f_{LO}$ as a function of $C_{LO}$ is also shown in Fig. 4.3. For $C_{LO}=7$ pF, the insertion loss is 11.93 dB, which means the LO power reaching the transistor is 11.93 dB less than the power provided by the LO source. This seemingly high power loss is still tolerable since the power provided by the LO source can be adjusted.

Following the selection of $C_{LO}$, the modified input impedance $Z_{IN}$, which is equal to the transistor’s input impedance in parallel with the series combination of $C_{LO}$ and 50 Ω LO port, is conjugately matched to the RF port. The matching was provided by a high-pass, L-section matching network (similar to the one shown in Fig. 3.8(a)). The matching network was designed in the Smith Chart Utility of ADS and constitutes a 9.6 pF series capacitor ($C_{RF}$) and a 427 nH shunt inductor ($L_{RF}$). The schematic level simulations were performed after the matching and the resultant $\Gamma_{RF}$ is shown in Fig. 4.4. It can be seen that the matching network provides $\Gamma_{RF} = -30$ dB at $f_{RF} = 59$ MHz.
4.2 FIRST PROTOTYPE: EVALUATION OF MIXER PERFORMANCE AT RT

Figure 4.5: (a) Real and (b) imaginary components of $Z_{\text{OUT}}$ and $Z_{\text{EQ}}$.

The collector of the SiC BJT was connected to the supply voltage via $R_C = 1 \text{ k}\Omega$ resistor. The value of $R_C$ can be increased to improve the CG but at the cost of higher power consumption. Thereafter, a filtering network was designed to provide RF-IF and LO-IF isolation as follows. First, $Z_{\text{OUT}}$ was estimated using the two-port Z-parameters:

$$Z_{\text{OUT}} = Z_{22} - \frac{Z_{12}Z_{21}}{Z_{11} + Z_S} \quad (4.5)$$

where $Z_S = 50 \Omega$ is the source impedance at the input port. The real and imaginary parts of $Z_{\text{OUT}}$ at $f_{\text{RF}}$ and $f_{\text{LO}}$ are shown in Fig. 4.5(a) and Fig. 4.5(b), respectively. $Z_{\text{OUT}}$ at $f_{\text{RF}}$ (and to a good degree at $f_{\text{LO}}$ as well) can be represented by an equivalent RC network ($Z_{\text{EQ}}$), constituting of a 116.66 $\Omega$ resistor ($R_{\text{EQ}}$) and a 31.6 pF capacitor ($C_{\text{EQ}}$). The equivalence can be seen by comparing the real and imaginary components of $Z_{\text{OUT}}$ and $Z_{\text{EQ}}$ in Fig. 4.5(a) and Fig. 4.5(b), respectively. This equivalent network is connected to a filtering network as shown in Fig. 4.6(a). The simulated transfer function ($\text{OUT}/\text{IN}$) of the circuit in Fig. 4.6(a) is shown in Fig. 4.6(b). The plot in Fig. 4.6(b) indicates that the $\text{OUT}$ at both $f_{\text{RF}}$ and $f_{\text{LO}}$ is smaller than the $\text{IN}$ signal by around 39 dB, a fairly good attenuation factor.

Following the schematic level design, the layout and EM simulations of the mixer were performed in ADS. Fig. 4.7 shows the FR-4 PCB stack with 35 $\mu$m copper metalizations ($\rho_v = 1.724 \, \mu\Omega \cdot \text{cm}$) used for the EM simulations. Similar to Fig. 3.11, cond, cond2 and hole represent the top metalization, bottom metalization and the via layers, respectively. A dummy substrate was added under cond2 to electrically isolate cond2 from the chuck. The pcvia1 represents the vias in the dummy substrate. This layer was added since the proposed measurement setup, that will be described shortly, requires via openings in the dummy PCB. The bond layer was used to simulate the effects of the chuck.

The $L_{\text{RF}}$ was realized with a stacked spiral inductor on cond and cond2 layers. The stripe width and spacing of spirals were kept at 0.3 mm. The effective induc-
CHAPTER 4. ACTIVE DOWN-CONVERSION MIXER

Figure 4.6: (a) Equivalent output impedance of mixer attached to a filtering network. (b) transfer function of (a).

Figure 4.7: PCB stack used for EM simulations of the first mixer prototype.

Figure 4.8: Simulated (a) effective inductance and (b) quality factor of \( L_{RF} \).

tance and quality factor of the inductor were calculated using (3.19) and (3.20) and are shown in Fig. 4.8(a) and Fig. 4.8(b), respectively. The effective inductance and quality factor of the inductor at \( f_{RF} \) is 430 nH (close to the desired value of 427 nH) and 60, respectively.

The EM simulated \( \Gamma_{RF} \) of the complete mixer circuit is shown in Fig. 4.9. The \( C_{RF} \) was changed from a non-standard value of 9.6 pF to a standard value of 9 pF. Due to the change in \( C_{RF} \) and the effects of layout, the minimum value of \( \Gamma_{RF} \)
4.2 FIRST PROTOTYPE: EVALUATION OF MIXER PERFORMANCE AT RT

4.2.1 First Prototype Design

Figure 4.9: EM simulation of RF port matching at RT.

Figure 4.10: (a) Mixer circuit. (b) Prototype.

shifted to 59.5 MHz instead of 59 MHz, however $\Gamma_{RF}$ is still -20 dB (1% reflected power) at $f_{RF}$. Therefore, no further modifications were made in the final circuit. The final mixer circuit is shown in Fig. 4.10(a) where $C_{B1}=C_{B2}=10 \text{ nF}$ are the bypass capacitors and $C_{B3}=10 \text{ nF}$ is the DC block capacitor.

4.2.2 Prototyping, Measurement Setup and Results

The prototype of the mixer circuit is shown in Fig. 4.10(b). A jumper was added to tap the IF output of the mixer after filtering. The illustration in Fig. 4.11 represents the measurement setup which allows RF interfacing without employing GSG probes. The top PCB ("PCB with circuit") contains the mixer circuit (i.e. the PCB shown in Fig. 4.10(b)). The top PCB is screwed on another PCB ("Dummy PCB"), which effectively extend the LO and RF ports beyond the thermal chuck boundary. A thin alumina-sheet is placed under the "Dummy PCB" to prevent
short-circuiting. The extended ports were screwed to SMA connectors using 1-cm long copper wires. The fundamental idea behind using the aforementioned setup is that the extension of RF and LO ports of the mixer beyond the chuck boundary, supplemented by the additional 1-cm long copper wires, would result in a thermal gradient between the chuck and the SMA connectors. This thermal gradient can potentially allow the SMA connectors to work without significant performance degradation even when the temperature of chuck is as high as 500 °C. Obviously, the performance degradation of SMA connectors with temperature can not be measured in the first prototype as FR-4 PCB melts at such extreme temperatures. However, one can still determine the amount of power the proposed interface reflects due to mismatch. Accordingly, the reflection-coefficient of coax-to-microstrip interface to a 50 Ω termination was measured using the setup shown in Fig. 4.12(a). The measured $S_{11}$ is plotted in Fig. 4.12(b) and shows that the return loss is less than -20 dB (1% reflected power) both at $f_{RF}$ and $f_{LO}$. This indicates the suitability of the proposed RF interface in the frequency band of interest.

The complete measurement setup is shown in Fig. 4.13(a). The mixer was biased with SCS-4200 using probing needles. Rohde & Schwarz signal generator (SMIQ-06B) was used to provide the LO signal whereas the RF signal was provided with the Agilent waveform generator (33250A). The IF output voltage was measured.
4.3 Second Prototype: High-Temperature Variant of First Prototype

Based on the encouraging results from the first mixer, a second mixer prototype was developed on an LTCC board for HT operation. LTCC was selected as a substrate material due to its high-temperature dielectric material and multilayer capability. The latter property not only facilitates the development of spiral inductors but also proves useful in electrically isolating the circuit from the thermal chuck, as will be shown shortly.

4.3.1 Circuit Design and Simulation Results

The design of HT mixer prototype follows the same flow as the first prototype. A \( C_{LO} = 6 \) pF was first selected to couple the LO port to the base of SiC BJT. The chosen value of \( C_{LO} \) is slightly smaller than the value of 7 pF used in the first prototype. This decision was forced because 7 pF HT capacitor was not available at the time of selection. Nevertheless, \( C_{LO} = 6 \) pF offers a return loss of 0.21 dB at \( f_{RF} \) and an insertion loss of 13.2 dB at \( f_{LO} \). Both these values are fairly close to the corresponding values in the previous design. Afterwards, \( Z_{IN} \) was conjugately matched to the 50 \( \Omega \) RF port via a high-pass, L-section matching network (similar to the...
CHAPTER 4. ACTIVE DOWN-CONVERSION MIXER

Figure 4.14: (a) Schematic simulation of RF port matching at RT. (b) Transfer function of the mixer output connected to a filtering network.

Figure 4.15: PCB stack used for EM simulations of the second mixer prototype.

one shown in Fig. 3.8(a)). The matching network constitutes a series $C_{RF}=11.8$ pF capacitor and a shunt $L_{RF}=335$ nH inductor. The schematic level simulations were performed after the matching and the resultant $\Gamma_{RF}$ at RT is shown in Fig. 4.14(a). It can be seen that the matching network provides $\Gamma_{RF} = -32$ dB at $f_{RF} = 59$ MHz.

The collector of the SiC BJT was connected to the supply voltage via $R_{C}=1$ kΩ resistor. Based on the design principle discussed for the first prototype, a filtering network was designed to provide RF-IF and LO-IF isolation. $Z_{OUT}$ was estimated using (4.5) and was represented in terms of an equivalent RC network constituting of $R_{EQ}=74.95$ Ω and $C_{EQ}=31.1$ pF. This equivalent network was then connected to a filtering network which is similar to the network in Fig. 4.6(a) but without $R_1$ and $C_1$. The filtering network was simplified to keep the count of passive components small. The simulated transfer function of the cascade of RC equivalent network followed by the filtering network is shown in Fig. 4.14(b). It can be seen that at both $f_{RF}$ and $f_{LO}$, the $IN$ signal undergoes an attenuation of around -20 dB.

The layout and EM simulations of the mixer circuit were performed in ADS. Fig. 4.15 shows the LTCC stack with 15 μm gold metalization (LL505 metal system [99]) used for the EM simulations. The naming and purpose of each layer has already been described in Section 4.2.1. The $L_{RF}$ was realized with a stacked spiral inductor on cond and cond2 layers. The stripe width and spacing of spirals were kept at 0.6 mm and 0.3 mm, respectively. The effective inductance and quality
factor of the inductor were calculated using (3.19) and (3.20) and are shown in Fig. 4.16(a) and Fig. 4.16(b), respectively. The effective inductance and quality factor of the inductor at $f_{RF}$ is around 330 nH (close to the desired value of 335 nH) and 25, respectively. Note that the peak value of quality factor of inductor in the second prototype (Fig. 4.16(b)) is smaller than the corresponding value for the first prototype (Fig. 4.8(b)). This is a consequence of more than four times higher resistivity for LL505 metalization system in the second prototype as compared to the copper metalization in the first prototype. The issue of increased resistivity was partially counteracted by doubling the inductor stripe width in the second prototype as compared to the first prototype.

To analyze the effect of temperature on $\Gamma_{RF}$, EM simulations were performed by varying $\rho$ of the gold metalization according to (3.18). A $\rho_{G}=7.5 \mu\Omega\cdot\text{cm}$ (from the datasheet of LL505 metalization) and $\alpha=0.0034/\degree\text{C}$ [96] were used for the simulations. The $C_{RF}$ was changed from 11.8 pF to 10.7 pF since it provided better post-layout $\Gamma_{RF}$ matching. Fig. 4.17 shows the EM-simulated $\Gamma_{RF}$ at various temperatures. Though one can observe small drifts in the frequency of minimum $\Gamma_{RF}$ with temperature, $\Gamma_{RF}$ remains less than -19 dB ($\approx 1.3\%$ reflected power) at $f_{RF}$.
for all simulated temperatures. This completes the mixer design and the final circuit is shown in (Fig. 2, [Paper II]).

4.3.2 Measurement Setup, Prototyping and Results

The illustration in Fig. 4.18 represents the measurement setup. This measurement setup is similar to Fig. 4.11 but with one difference. The screws to join "PCB with circuit" and "dummy PCB" as well as alumina sheet are not required. This is a direct consequence of multilayer capability of LTCC board which allows the circuit and dummy PCB to be implemented as a single PCB. To evaluate the potential degradation of SMA connectors (described in the last section) at HT, they were screwed to the LTCC board which was then heated to 500 °C. This was followed by monitoring the jacket temperature of SMA connectors using an IF thermometer, which remained less than 200 °C. After two hours, the LTCC was cooled back to RT and the SMA connectors were again used to measure $S_{11}$ of the setup in Fig. 4.12(a). The measured $S_{11}$ for one of the SMA connector before and after heating is shown in in Fig. 4.19. One can see negligible variation in the measured results which implies that the SMA connector was not degraded during the HT operation.

Figure 4.18: Proposed measurement setup for HT characterization of RF circuits.

Figure 4.19: Measured reflection coefficient of a 50 Ω load before and after heating the SMA-connector-copper wire interface.
4.3. SECOND PROTOTYPE: HIGH-TEMPERATURE VARIANT OF FIRST PROTOTYPE

The performance and reliability of HT resistors and capacitors were also evaluated. Fig. 4.20(a) and Fig. 4.20(b) show the percentage change in the resistance of a 1 kΩ Vishay resistor, a 10 nF (largest value used) and a 4.7 pF (smallest value used) Presidio Components Inc. capacitors, respectively, versus temperature. The resistance and capacitance variation remained within +3.5% and -2%, respectively, as compared to their values at 25 °C. Moreover, negligible parameter variation with time, even after several hours of continuous operation at 500 °C was observed.

Following this initial testing, the SiC BJT chip and passive components were mounted on the LTCC board and the final prototype is shown in Fig. 3(a), [Paper II]. The characterization and measurement results of the mixer from RT up to 500 °C are fully presented in [Paper II]. CG as a function of $P_{LO}$ for a $P_{RF}$ of -16 dBm is shown in Fig. 4(a), [Paper II]. CG increases linearly with $P_{LO}$ up to the onset of saturation at about 15 dBm. This result is fairly similar to the one obtained from the first prototype. Furthermore, the measurement results over a wide temperature range showed that the CG decreases with temperature, e.g., for $P_{LO}$=15 dBm, CG drops from 15 dB at RT to 4.7 dB at 500 °C. This can be seen in Fig. 4.20(a) and Fig. 4.20(b), which show the transient IF output voltage (in blue), and the corresponding spectrum (in green) at RT and 500 °C, respectively, for $P_{RF}$=-7 dBm and $P_{LO}$=15 dBm. The spectrum amplitude in the bottom right of the plots shows that the component of IF output at $f_{RF}$ is -4.9 dBV$_{rms}$ and -15.3 dBV$_{rms}$, corresponding to a CG of 15.1 dB and 4.71 dB at RT and 500 °C, respectively. The spectrum also shows the RF and LO signal leakage in the IF output. The RF-IF and LO-IF isolations never degraded by more than 24 dB and 28 dB, respectively, at all measured temperatures.

To evaluate the linearity of the mixer, $P_{RF}$ was swept from -16 dBm to the onset of gain compression while $P_{LO}$ was kept constant at 15 dBm. The corresponding CG as a function of $P_{RF}$ is shown in Fig. 5(b), [Paper II]. The input 1-dB compression point increases from 1 dBm at RT to 8.8 dBm at 400 °C. However,
at 500 °C, the 1-dB compression point decreases to -2.5 dBm. Lastly, during the reliability evaluation of the mixer at 500 °C, a decrease in CG was observed with time. In particular, the CG dropped by 1.4 dB after 3-hours of continuous operation. This performance deterioration is believed to be caused by the increase in access and contact resistance of SiC BJT due to the degradation of aluminum metalization.
Chapter 5

Negative Resistance Oscillator

Oscillators are one of the main circuits of electronic systems. They are used in consumer electronics, test equipment as well as in communication systems. In this chapter, the design, simulation and measurement results of three SiC BJT based oscillators are discussed in detail. The first two oscillator prototypes served as a foundation for the development of the third oscillator, which was measured successfully up to 400 °C. The chapter initially describes different oscillator design methodologies and motivates the selection of the methodology used in this work. This is followed by a detailed presentation of the design, simulation and measurement results of all three oscillators.

5.1 Oscillator Design Fundamentals

Oscillators, especially the self-limiting ones, for which the output amplitude is limited by the gain saturation, are inherently nonlinear. Consequently, design methodologies based on large-signal S-parameters [100] and/or nonlinear device models [101] are preferred for designing these oscillators. The large-signal S-parameter measurements of the active device requires nonlinear vector network analyzers, a very expensive instrument which was unavailable at KTH during the course of this work. The development of large-signal active device models, on the other hand, is also difficult and time consuming due to a large number of measurements needed for parameter extraction. The situation is exacerbated further as the parameter extraction process for the active device has to be repeated at multiple temperature points, if that device is employed to design a wide-temperature range oscillator. To circumvent both these issues, oscillator design methodologies based on small signal S-parameters can be utilized [102,103]. Accordingly, two small-signal S-parameters based techniques for oscillator design, namely the open-loop [102] and the two-port negative resistance method [103] were investigated and compared.

The open-loop method is based on a cascade of an amplifier and a resonator as shown in Fig. 5.1. The resonator controls the operating frequency of the oscillator
CHAPTER 5. NEGATIVE RESISTANCE OSCILLATOR

Figure 5.1: Open-loop amplifier-resonator cascade with output coupling.

whereas the amplifier stage provides energy to compensate for the losses of the resonator. The oscillator is formed by connecting the input and output ports of the amplifier-resonator cascade and the load is coupled to a suitable node, e.g., at the output of the amplifier. The necessary start-up conditions for the oscillator are given by the open-loop Bode response of the amplifier-resonator cascade \[102\]:

1. The gain \((S_{21})\) of the amplifier-resonator cascade must be greater than 0 dB at the frequency of phase zero crossing \((\phi_0)\).

2. The phase of slope at \(\phi_0\) must be negative and if there are multiple \(\phi_0\), the quantity with a negative slope must exceed the quantity with a positive slope.

In order to design the amplifier-resonator cascade for meeting the start-up conditions, the input and output ports of the cascade are required to be connected to the reference impedance of the simulator (e.g. 50 \(\Omega\) for ADS). However, if the reference impedance of the simulator is not matched to both the input \((Z_{IN})\) and output impedances \((Z_{OUT})\) of the cascade, the closed-loop conditions would not comply with the simulated open-loop conditions. This leads to a mismatch error in the gain margin given by \[102\]:

\[
\text{Mismatch Error} = 20 \log \frac{1}{1 - S_{11}S_{22}} \quad (5.1)
\]

Equation (5.1) shows that the mismatch error decreases for small values of \(S_{11}\) and \(S_{22}\). This implies that for correct prediction of the loop-gain, the input and output impedance of the cascade should have a reasonable match with a common reference impedance. The matching can be performed by employing the resonator as part of the matching network, e.g. the capacitive tap resonator of a Colpitts oscillator. However, when such matching proves difficult, the following relationship could be used to accurately determine the true complex gain \((G)\) of a self-terminated
5.1. OSCILLATOR DESIGN FUNDAMENTALS

Figure 5.2: Two-port negative resistance oscillator.

cascade [104]:

\[
G = \frac{S_{21} - S_{12}}{1 - S_{11}S_{22} + S_{21}S_{12} - 2S_{12}}
\]  

(5.2)

The second small-signal S-parameters based oscillator design methodology is the so-called two-port negative resistance method. The block diagram of a two-port NRO is shown in Fig. 5.2. The transistor in Fig. 5.2 is characterized by its S-parameters whereas \( Z_T \) and \( Z_L \) represent the terminating and load impedances, respectively. The basic procedure for designing an NRO is as follows [103]:

1. Use a potentially unstable transistor at the desired frequency of oscillation \((f_0)\).
   If the transistor is unconditionally stable at \( f_0 \), add proper feedback to make it potentially unstable.

2. Design the terminating network to make \(|\Gamma_{IN}| > 1\) or equivalently \( \text{Re}\{Z_{IN}\} < 0 \).

3. Design the load network so \( \text{Im}\{Z_{IN}\} \) resonates at \( f_0 \) as well as to couple the NRO to the load.

It is imperative to mention that in Fig. 5.2, Port 1 of the transistor is connected to the terminating network and Port 2 to the load network. However, this does not have to be always the case and the relative positions of these networks can be exchanged without any loss in generality. The necessary start-up conditions for the NRO are given by [103]:

\[
|\Gamma_{IN}(f_0)\ \Gamma_{L}(f_0)| > 1
\]  

(5.3)

and

\[
\angle\Gamma_{IN}(f_0)\ \Gamma_{L}(f_0) = 0
\]  

(5.4)
or equivalently,

\[ |\text{Re}\{Z_{IN}(f_o)\}| > \text{Re}\{Z_L\} \]  

(5.5)

and

\[ \text{Im}\{Z_{IN}(f_o)\} = - \text{Im}\{Z_L(f_o)\} \]  

(5.6)

A subtle difference between the open-loop and two-port negative resistance method lies in the role of the active device [102]. In the open-loop method, the amplifying transistor in the cascade has to be stable otherwise it may lead to spurious oscillations at a frequency other than the frequency of phase zero crossing. On the other hand, in the two-port negative resistance method, the transistor is intentionally made unstable and the instability is controlled to occur at the desired frequency. Though both methods are quite useful for designing RF oscillators, two-port negative resistance method is relatively simple and straightforward as it does not impose any matching requirements, typically required for the open-loop method. Therefore, in this work, the two-port negative resistance method was chosen for designing SiC BJT based oscillators.

5.2 First Prototype: Validation of Two-Port Negative Resistance Method

The two-port negative resistance method for oscillator design is based on small-signal S-parameters of the active device, therefore it can not predict large-signal performance parameters of the oscillator, e.g. output power, harmonic content, phase noise, etc. In order to evaluate the oscillator for aforementioned performance parameters and to validate the two-port negative resistance method, an NRO based on a 2-fingered, 40 $\mu$m $\times$ 10 $\mu$m SiC BJT was designed, prototyped and measured [Paper III]. This first oscillator prototype was designed for an oscillation frequency of 58 MHz rather than 59.5 MHz, as proposed in Section 2.3.2. The difference is related to the fact that the first oscillator prototype is one of the earlier circuit realized in this work and was designed (to validate the method) prior to devising the specifications in Section 2.3.2. The later two oscillator prototypes were designed for an oscillation frequency of 59.5 MHz, in accordance with the specifications in Section 2.3.2.

5.2.1 Circuit Design and Simulation Results

In the first oscillator prototype, the on-wafer SiC BJT was not diced and bond-wired to the PCB, instead its base-emitter (B-E) and collector-emitter (C-E) ports were extended using two 0.5 m coaxial cables in conjunction with the RF probes (Fig. 2, [Paper III]). The shifted BJT ports, now with coaxial interface, were then directly connected to a PCB (containing all the remaining components of the NRO)
5.2. FIRST PROTOTYPE: VALIDATION OF TWO-PORT NEGATIVE RESISTANCE METHOD

through SMA connectors (Fig. 5, [Paper III]). The shifting of BJT ports made the connectivity between on-wafer SiC BJT and PCB possible and expedited the validation process as no dicing and bond-wiring steps were required.

The S-parameters of the embedded-BJT (cascade of cables and BJT) were used to design the NRO. The terminating and load networks of NRO were connected to B-E and C-E ports, respectively. The primary reason behind using C-E port to connect the load network was that the C-E port can deliver more output power as compared to its B-E counterpart. The NRO was designed using the measured S-parameters of BJT at 300 °C, the maximum temperature of the RF probes based measurement setup. However, in this first prototype, only the BJT was kept at elevated temperatures during measurements while the remaining circuit components were at RT (Fig. 5, [Paper III]). The circuit design of NRO based on the two-port negative resistance method is now presented as follows.

All the fabricated SiC BJTs were unconditionally stable ($K > 1$ and $|\Delta| < 1$) at all measured frequencies, biasing points and temperatures. Therefore, as a first step, the embedded-BJT was made potentially unstable by employing a suitable feedback. A simple way to analyze the effects of the feedback component on the stability of the active device is to calculate its effect on the $\mu'$ factor, which is given by [103]:

$$\mu' = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} \tag{5.7}$$

The $\mu'$ factor represents the stability of a two-port network in terms of a single condition, i.e. if $\mu' > 1$, the two port is unconditionally stable and potentially unstable otherwise. Fig. 5.3(a) and Fig. 5.3(b) show $\mu'$ of the embedded-BJT as a function of inductive and capacitive feedback at 58 MHz, respectively. It can be seen that an inductance of around 140 nH makes the embedded-BJT potentially more

![Figure 5.3: Simulated $\mu'$ of the embedded-BJT at 58 MHz versus the (a) inductive and (b) capacitive feedback.](image-url)
unstable since it decreases $\mu'$ to 0.65. Similarly, a capacitance of 37 pF decreases $\mu'$ to its minimum value of around 0.985, however this decrease is less pronounced as compared to the one provided by inductive feedback. The implications of the type of feedback and the value of $\mu'$ on the NRO design becomes more evident by drawing the $|\Gamma_{IN}| = 1$ circle in the $\Gamma_T$ plane. The center and radius of the $|\Gamma_{IN}| = 1$ circle is given by [103]:

\[
\text{radius} = \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \quad (5.8)
\]

\[
\text{center} = \frac{(S_{11} - \Delta S_{22}^*)}{|S_{11}|^2 - |\Delta|^2} \quad (5.9)
\]

Fig. 5.4(a) and Fig. 5.4(b) show $|\Gamma_{IN}| = 1$ circles in $\Gamma_T$ plane for a 120 nH feedback inductor (120 nH was used instead of 140 nH since it was readily available) and a 37 pF feedback capacitor, respectively. The $|\Gamma_{IN}| = 1$ circle represents the boundary between the stable region (where $|\Gamma_{IN}| < 1$) and the unstable region (where $|\Gamma_{IN}| > 1$) in the $\Gamma_T$ plane. The two regions can be distinguished as follows. For $\Gamma_T = 0$, $\Gamma_{IN}$ becomes equal to $S_{22}$ in Fig. 5.2. This implies that the center of Smith Chart ($\Gamma_T = 0$) represents a stable region when $|S_{22}| < 1$ and an unstable region when $|S_{22}| > 1$. Since $|S_{22}| < 1$ in both cases, the center of Smith Chart represent the stable regions and consequently the shaded areas mark the unstable regions. That is, any $Z_T$ in the shaded region of Smith Chart would make $|\Gamma_{IN}| > 1$. Two observations can be made from Fig. 5.4(a) and Fig. 5.4(b). Firstly, a bigger set of terminating impedances (shaded regions) can generate $|\Gamma_{IN}| > 1$ when the feedback is inductive as compared to when the feedback is capacitance.

![Figure 5.4](image-url)

**Figure 5.4:** $|\Gamma_{IN}| = 1$ circles in the $\Gamma_T$ plane for (a) 120 nH feedback inductor and (b) 37 pF feedback capacitor. Corresponding $S_{22}$ of the embedded-BJT is also shown.
This is related to value of $\mu'$ being smaller for inductive feedback as compared to the capacitive feedback since $\mu'$ is essentially the distance from the center of Smith Chart to the closest point on $|\Gamma_{IN}| = 1$ circle. Secondly, the unstable region in Fig. 5.4(b) occupies only the inductive impedances. This implies that an inductor is essential for realizing the terminating network of NRO when the feedback is capacitive. This is not desired since (i) inductors are more lossy and occupy bigger footprint as compared to capacitors, (ii) it would require an additional capacitor as a DC block to prevent grounding the base of BJT. On the other hand, when the feedback is inductive, both inductive as well as capacitive terminating impedances can be employed to make $|\Gamma_{IN}| > 1$. The foregoing discussion motivated the selection of 120 nH inductor in the feedback of NRO in [Paper III].

Once the feedback inductor ($L_F$) was selected, the next step was to choose an appropriate terminating network. Only purely capacitive reactances (green line in Fig. 5.4(a)) were considered. As mentioned before, any capacitive reactance in the unstable region would give $|\Gamma_{IN}| > 1$ or equivalently $\text{Re}\{Z_{IN}\} < 0$. However, the NRO was designed to directly drive $\text{Re}\{Z_L\} = 50 \, \Omega$ load and consequently the start-up condition in (5.5) requires a terminating network that would produce $\text{Re}\{Z_{IN}\} < -50 \, \Omega$. Fig. 5.5(a) shows $\text{Re}\{Z_{IN}\}$ as a function of terminating network capacitor ($C_T$). The black line represents the threshold under which $\text{Re}\{Z_{IN}\}$ is less than -50 $\Omega$. It can be seen that any value of $C_T$ between 10 pF and 34 pF would result in $\text{Re}\{Z_{IN}\} < -50 \, \Omega$. The minimum value of $\text{Re}\{Z_{IN}\}$ is -978 $\Omega$ which occurs at 31 pF. However, such extreme values for $\text{Re}\{Z_{IN}\}$ are not recommended as they may cause spurious oscillations in the oscillator or produce large harmonic content [103]. Therefore, a $C_T$ of 18 pF was selected which gives a moderate $\text{Re}\{Z_{IN}\}$ of $-115 \, \Omega$ at 58 MHz. Fig. 5.5(b) shows $\text{Im}\{Z_{IN}\}$ as a function of $C_T$.

Figure 5.5: (a) Real and (b) imaginary components of $Z_{IN}$ at 58 MHz as a function of terminating network capacitor.
For a $C_T$ of 18 pF, $\text{Im}\{Z_{IN}\}$ has an inductive reactance of around 85 Ω, which was resonated at 58 MHz by employing a load network capacitor ($C_L$) of 33 pF ($\approx$ 83 Ω @ 58 MHz) to fulfill (5.6).

Since the NRO was designed using S-parameters of the BJT at 300 °C, it was important to investigate if the designed circuit fulfills the start-up conditions at other temperatures as well. This was verified conveniently by using the OscTest component in ADS, which essentially calculates the product of $\Gamma_{IN}\Gamma_L$. The phase zero crossing and magnitude of $\Gamma_{IN}\Gamma_L$ at phase zero crossing can be compared against (5.3) and (5.4) to evaluate the start-up conditions for the oscillator at various temperatures. Fig. 5.6(a) shows the phase of $\Gamma_{IN}\Gamma_L$ as a function of frequency. Note that the frequency at which the phase crosses zero degrees is around the design frequency of 58 MHz and remains virtually unaffected by temperature (<1% variation). Fig. 5.6(b) shows $|\Gamma_{IN}\Gamma_L|$ at various temperatures. Though the maximum value of $|\Gamma_{IN}\Gamma_L|$ occurs at around 53 MHz, the value of $|\Gamma_{IN}\Gamma_L|$ at frequencies of phase zero crossings is still greater than one at all temperatures. This suggests that the start-up conditions in (5.3) and (5.4) are fulfilled at all simulated temperatures between 25 °C to 300 °C. Lastly, note that at 58 MHz, $|\Gamma_{IN}\Gamma_L|$ is smaller at 25 °C as compared to the remaining three temperature points. An implication of this observation will be discussed shortly.

### 5.2.2 Prototyping, Measurement Setup and Results

The NRO was realized using commercial, off-the-shelf inductors and capacitors. A 1.6 mm thick FR-4 PCB was used to mount $L_F$, $C_T$ and $C_L$ as well as the DC block capacitor in the feedback path and two RF chokes for biasing. Three SMA connectors were soldered to the PCB, two of which were used to connect the
5.3. SECOND PROTOTYPE: IMPROVING THE OUTPUT POWER OF OSCILLATOR

extended B-E and C-E ports of the BJT to the PCB while the remaining one was used to connect the output of the NRO to a 50 Ω spectrum analyzer. The complete NRO prototype can be seen in (Fig. 4, [Paper III]). The NRO was characterized from 25 °C to 300 °C by varying the temperature of the thermal chuck on which the SiC BJT was placed. During measurements, the PCB was kept at RT, as can be seen in (Fig. 5, [Paper III]).

The measurement results of the proposed NRO are fully presented in [Paper III]. In particular, the measured output power, fundamental frequency of oscillation and phase noise of the NRO as a function of chuck temperature are shown in (Table 1, [Paper III]). The maximum value of output power is 8.8 dBm and occurs at 300 °C, the temperature used for designing the NRO. As the chuck temperature was lowered from 300 °C to 100 °C, a marginal degradation of 0.7 dB in the output power was observed. However, the degradation of output power was more pronounced when temperature was decreased further to 25 °C. At 25 °C, the output power reached its minimum value of 5.9 dBm. This trend displays a relatively good correlation between $|\Gamma_{IN}\Gamma_L|$ plotted in Fig. 5.6(b) and the output power of the oscillator. Moreover, the measured fundamental frequency of oscillation and its variation with temperature is also in excellent agreement with the simulated results presented in the last section. Finally, the NRO exhibited good noise performance throughout the measured temperature range, with an average 100 kHz offset phase noise of around -103 dBc/Hz. Though only the SiC BJT was exposed to elevated temperatures in the work presented in [Paper III], it nevertheless demonstrated the potential of two-port negative resistance method for developing HT oscillators and laid the foundation for remaining two NRO prototypes that will be presented in subsequent sections.

5.3 Second Prototype: Improving the Output Power of Oscillator

The mixers developed in this work require an LO power of around 15 dBm to maximize their conversion gain, as shown in Fig. 4.13(b) and (Fig. 4(a), [Paper II]). However, the maximum output power provided by the first NRO prototype was 8.8 dBm. Therefore, a second NRO was designed to address this output power discrepancy. The second prototype was developed for an oscillation frequency of 59.5 MHz and was different from the first prototype in three aspects: (i) the entire circuit, including the active device, was mounted on the PCB, (ii) the commercial off-the-shelf inductors were replaced by spiral inductors implemented on PCB and, (iii) the prototype was developed to conform with the HT measurement setup discussed in Section 4.3.2.

The output power provided by an oscillator can be enhanced by cascading it with an amplifier as shown in Fig. 5.7. In addition to providing more output power, the oscillator-amplifier cascade also reduces the effect of load variation on the oscillation frequency [105]. The realization of oscillator-amplifier cascade, however,
requires additional active device as well as passive components, thereby leading to a relatively complicated implementation. A relatively simple solution to achieve more output power is to use a larger oscillator transistor [105]. Therefore, the second NRO was designed using a 4-fingered, $40 \mu m \times 10 \mu m$ SiC BJT instead of the 2-fingered BJT used in the development of first prototype. The second NRO prototype was developed only for RT operation to evaluate the improvement in oscillator’s output power due to device scaling. Accordingly, the S-parameters of SiC BJT at $25^\circ C$ were used to design the NRO.

5.3.1 Circuit Design and Simulation Results

Similar to the previous design, the feedback in second NRO was provided by an inductor. Fig. 5.8 shows $\mu'$ as a function of feedback inductance at 59.5 MHz. $L_F=350$ nH was selected since it minimizes $\mu'$. As mentioned earlier, both $L_F$ and RFCs in the second NRO were implemented on PCB. The parasitics of these inductors influence the selection of the terminating network. Therefore, instead of directly using schematic simulations for the selection of $C_T$, EM simulations were used first to design both $L_F$ and RFCs. These EM defined inductors were then used to find an appropriate terminating capacitor in schematic level simulations, as will be discussed shortly.

![Figure 5.8: $\mu'$ of the BJT at 59.5 MHz versus the inductive feedback.](image-url)
5.3. SECOND PROTOTYPE: IMPROVING THE OUTPUT POWER OF OSCILLATOR

Figure 5.9: PCB stack used for EM simulations and prototyping of the second NRO.

Figure 5.10: (a) Effective inductance of $L_F$ and (b) magnitude of RF choke impedance as a function of frequency.

Fig. 5.9 shows the FR-4 PCB stack with 35 $\mu$m copper metalizations used for designing the spiral inductors. The naming and purpose of each layer has already been described in Section 4.2.1. The feedback inductor was realized with a spiral inductor on $\text{cond}$ layer whereas the crossover was done in $\text{cond}2$. The stripe width and spacing of spirals were kept at 0.6 mm and 0.3 mm, respectively. The effective inductance ($L_E$) of the feedback inductor was calculated from the simulated Y-parameters using:

$$L_E = \frac{-\text{Im}\left(\frac{1}{Y_{12}}\right)}{\omega}$$

(5.10)

where $\omega$ is the frequency in radians. As shown in Fig. 5.10(a), the equivalent inductance of the feedback inductor at 59.5 MHz is 349 nH, very close to the desired value. Similar to $L_F$, the RF chokes were implemented using spiral inductors on $\text{cond}$ layer with both stripe width and spacing of 0.3 mm. The magnitude of RFC
CHAPTER 5. NEGATIVE RESISTANCE OSCILLATOR

impedance as a function of frequency is shown in Fig. 5.10(b). As the RFC was designed to have a parallel self-resonance frequency close to the oscillation frequency of NRO, the RFC offers maximum impedance around 59.5 MHz.

Once both $L_F$ and RFCs were designed, a sweep of $C_T$ was performed to find an appropriate value for the terminating network capacitor. Fig. 5.11(a) shows $\text{Re}\{Z_{IN}\}$ as a function of $C_T$ at 59.5 MHz. The area under the black line represents $\text{Re}\{Z_{IN}\}$ that would fulfill the start-up condition in (5.5) to drive a 50 $\Omega$ load. A $C_T=31.7$ pF was selected (realized using two standard capacitor values of 27 pF and 4.7 pF) which provides $\text{Re}\{Z_{IN}\}=-190$ $\Omega$. Fig. 5.11(b) shows $\text{Im}\{Z_{IN}\}$ as a function of $C_T$. For $C_T=31.7$ pF, $\text{Im}\{Z_{IN}\}$ has an inductive reactance of around 96 $\Omega$, which was resonated at 59.5 MHz by employing $C_L=27$ pF ($\approx 99$ $\Omega$ @ 59.5 MHz) to fulfill (5.6).

5.3.2 Prototyping, Measurement Setup and Results

The chip containing the SiC BJT was diced and glued to the FR-4 PCB. The SiC BJT was then bond-wired to the PCB and the remaining circuit components were soldered. Fig. 5.12(a) shows the complete prototype of the second NRO whereas the measurement setup is shown in Fig. 5.12(b).

The output power of the NRO as a function of biasing collector current is shown in Fig. 5.13(a). During measurements, the supply voltage was kept at 12 V. It can be seen that the output power of the NRO increases with collector current up to 40 mA where it reaches its maximum value of 16.8 dBm. The output power begins to decrease as collector current is increased beyond 40 mA. The measured oscillation frequency lies within 0.7% of the desired oscillation frequency of 59.5 MHz at all values of collector current. In Fig. 5.13(b), the output spectrum of the oscillator at
5.3. SECOND PROTOTYPE: IMPROVING THE OUTPUT POWER OF OSCILLATOR

35 mA indicates that by employing the larger device, i.e. the 4-fingered SiC BJT, the NRO can surpass the output power goal of $\geq 15 \text{ dBm}$, at least at RT.

![Second NRO prototype](image1)

![Measurement setup](image2)

Figure 5.12: (a) Second NRO prototype. (b) Measurement setup.

![Output power and oscillation frequency](image3)

![Measured spectrum](image4)

Figure 5.13: (a) Output power and oscillation frequency of NRO versus biasing current. (b) Measured spectrum of the NRO at RT for a biasing current of 35 mA.
5.4 Third Prototype: High-Temperature Variant of Second Prototype

The third and last NRO, similar to the second NRO, was based on a 4-fingered, \(40 \mu m \times 10 \mu m\) SiC BJT. However, to enable HT characterization, it was prototyped on a HT LTCC board rather than an FR-4 PCB.

5.4.1 Circuit Design and Simulation Results

The design flow for the third NRO is similar to the one employed for designing the second NRO. Accordingly, the value of the feedback inductor was first selected to make the 4-fingered BJT potentially unstable at 59.5 MHz. Fig. 5.14 shows \(\mu'\) factor of the SiC BJT as a function of feedback inductor. Based on the \(\mu'\) plot in Fig. 5.14, \(L_F=350\) nH was selected as a feedback component since it minimizes \(\mu'\) at 59.5 MHz.

Following the selection of feedback inductor, the next step was to design spiral inductors for implementing both \(L_F\) and RF chokes. Fig. 5.15 shows the LTCC stack with 15 \(\mu\)m gold metalization (LL505 metal system [99]) used for designing

![Figure 5.14: \(\mu'\) of the BJT at 59.5 MHz versus the inductive feedback.](image)

![Figure 5.15: PCB stack used for EM simulations and prototyping of the third NRO.](image)
5.4. THIRD PROTOTYPE: HIGH-TEMPERATURE VARIANT OF SECOND PROTOTYPE

the aforementioned inductors using EM simulations. The naming and purpose of each layer has already been described in Section 4.2.1. The feedback spiral inductor was realized on cond layer whereas the crossover was done in cond2. The stripe width and spacing of spirals were kept at 0.6 mm and 0.3 mm, respectively. The effective inductance of the feedback inductor was calculated from the simulated Y-parameters using (5.10) and is shown in Fig. 5.16(a). The value of the effective inductance at 59.5 MHz is 355 nH, which is very close to the intended value of 350 nH. The RF chokes were implemented using spiral inductors with both stripe width and spacing of 0.3 mm. Fig. 5.16(b) shows that the magnitude of RFC impedance peaks very close to 59.5 MHz, which is the oscillation frequency for the NRO. A comparison between Fig. 5.16(b) and Fig. 5.10(b) indicate that the maximum value of impedance in the former case is smaller as compared to the latter case. This is related to the fact that the resistance of gold metalization in third NRO prototype is larger than the resistance of copper metalization in the second NRO prototype (compare $\rho$ and metalization thickness in Section 4.2.1 and Section 4.3.1). This leads to a lower quality factor and consequently smaller maximum impedance for the gold-based RFC at its parallel self-resonance frequency.

Once both $L_F$ and RFCs were designed, a swept of $C_T$ was performed to find an appropriate value of the terminating network capacitor. Fig. 5.17(a) shows Re [$Z_{IN}$] as a function of $C_T$ at 59.5 MHz. The area under the black line represents Re [$Z_{IN}$] that would fulfill the start-up condition in (5.5) to drive a 50 $\Omega$ load. A $C_T=27$ pF was selected which provides Re [$Z_{IN}$]=-270 $\Omega$. Fig. 5.11(b) shows Im [$Z_{IN}$] as a function of $C_T$. For $C_T=27$ pF, Im [$Z_{IN}$] has an inductive reactance of around 175 $\Omega$, which was resonated by employing $C_L=15$ pF ($\approx 178$ $\Omega$ @ 59.5 MHz) to fulfill (5.6).

The designed NRO was simulated at temperatures up to 300 °C to evaluate
CHAPTER 5. NEGATIVE RESISTANCE OSCILLATOR

Figure 5.17: (a) Real and (b) imaginary components of $Z_{IN}$ at 59.5 MHz as a function of terminating network capacitor.

Figure 5.18: (a) Phase and (b) magnitude of $\Gamma_{IN}\Gamma_L$ as a function of frequency at various temperatures.

if it can fulfill the start-up conditions. The measured S-parameters of the SiC BJT in conjunction with the resistivity model for gold metalization in LTCC-9k7 system (refer to Section 4.3.1) were used for the simulations. Fig. 5.18(a) shows the simulated phase of $\Gamma_{IN}\Gamma_L$ as a function of frequency at various temperatures. The frequency at which the phase crosses zero degrees is within 1% of the design frequency. Fig. 5.18(b) shows the simulated magnitude of $\Gamma_{IN}\Gamma_L$. The value of $|\Gamma_{IN}\Gamma_L|$ at frequencies of phase zero crossings is greater than one at all temperatures. This suggests that the start-up conditions in (5.3) and (5.4) are fulfilled at
5.4. THIRD PROTOTYPE: HIGH-TEMPERATURE VARIANT OF SECOND PROTOTYPE

all simulated temperatures between 25 °C and 300 °C.

5.4.2 Prototyping, Measurement Setup and Results

The NRO was prototyped on a LTCC board and the complete prototype and measurement setup is shown in (Fig. 3, [Paper IV]). The measurement results of the proposed NRO are fully presented in [Paper IV]. In (Fig. 4, [Paper IV]), the oscillation frequency and output power of the NRO at RT is shown as a function of biasing collector current. The oscillation frequency varies by 0.5% across the whole range of collector current and is slightly smaller than the design frequency of 59.5 MHz. The output power of the oscillator initially increases with the biasing collector current but begins to saturate around 11 dBm as collector current approaches 35 mA. The oscillator output from RT up to 400 °C for a biasing current of 35 mA is shown in (Fig. 5, [Paper IV]). It can be seen that the oscillation frequency varies by 3.3% and the output power decreases by 2.8 dB as temperature is increased from 25 °C to 400 °C. Moreover, the harmonics remain 29 dB below the output power at the fundamental frequency whereas the phase noise was less than -95 dBc/Hz at a 100 kHz offset frequency throughout the measured temperature range. The circuit ceased to oscillate as the temperature was increased to 425 °C due to the failure of DC block capacitor in the feedback path. Such failures are an indication that further research is required to develop reliable HT passives, especially capacitors.

Finally, a comparison between the second and third NRO shows that the output power of latter is 11.2 dBm at RT, which is 4 dB smaller than the former for the same biasing current of 35 mA. This can be attributed to a relatively lossy metalization and/or due to the difference between the large-signal behavior of the SiC BJTs used in realizing the aforementioned NROs. For the third NRO, as the temperature is increased to 400 °C, the output power degrades further to 8.4 dBm. It can be inferred from (Fig. 4(a), [Paper II]) that the conversion gain of the mixer at 400 °C drops approximately to 0 dB for an LO power of 8.4 dBm. However, the degradation of LO power in the mixer circuit can be counteracted by reducing the insertion loss caused by the coupling capacitor, i.e. by employing a larger coupling capacitor. This can potentially lead to improvement in conversion gain of the mixer even when the output power provided by the LO is relatively small.
Chapter 6

Conclusions and Future Outlook

In this dissertation, the design, analysis, prototyping and characterization of proof-of-concept high-temperature RF circuits, based on in-house SiC npn BJTs have been presented. In particular, the development flow and measurement results of three high-temperature radio receiver blocks, i.e., an intermediate-frequency amplifier, an active down-conversion mixer and a negative resistance oscillator have been demonstrated.

Firstly, an intermediate-frequency amplifier has been implemented and tested successfully from 25 °C up to 251 °C. The amplifier employed a two-stage cascaded topology where each stage was composed of an in-house SiC BJT in a common-emitter configuration. At a center frequency of 54.6 MHz, the amplifier has a gain of 22 dB at room temperature which decreased gradually to 16 dB at 251 °C. Thereafter, a 59.5 MHz oscillator and an active mixer to down-convert a 59 MHz RF signal to a low-IF of 500 kHz, have been successfully tested at high temperatures. Both these nonlinear circuits were designed using methodologies based on small-signal S-parameters of the active devices. A consequence of employing linear techniques for designing nonlinear circuits is that large-signal performance parameters can not be determined. The issue was addressed by first prototyping the oscillator and mixer circuits for room-temperature operation using inexpensive FR-4 PCB boards and commercial off-the-shelf passives. Once their measured performance was deemed satisfactory at room-temperature, they were prototyped again for high-temperature operation using LTCC substrate and high-temperature passives. The high-temperature measurements have shown that the proposed oscillator is capable of delivering an output power of 8.4 dBm into a 50 Ω load up to 400 °C and the proposed mixer exhibits a conversion gain of 4.7 dB up to 500 °C.

The performance and reliability of passive components is also critical for the development of high-temperature RF circuits. Accordingly, thick-film Vishay resistors and Presidio Components Inc. capacitors have been characterized up to 500 °C to evaluate their feasibility for high-temperature applications. It has been shown that the resistance and capacitance values remained within +3.5% and -2%,
respectively, as compared to their 25 °C values. Moreover, high-temperature die-attach adhesive (Resbond 989F) and a conductive epoxy (PELCO® silver paste) for attaching passives to the PCB pads, have been identified and their stable operation up to 500 °C has been demonstrated. A measurement setup for characterizing RF circuits up to 500 °C has also been demonstrated.

Overall, the objectives of this thesis have been accomplished. However, more research is required for developing temperature-scalable, nonlinear device models for the SiC BJTs. The availability of such models would reduce the circuit development time, enable realization of more complex circuits like power amplifiers, phase-locked loops, frequency synthesizers etc., and facilitates the development of the entire communication system. The development cycle of high-temperature RF circuits would also benefit from the availability of a 500 °C (or higher) RF-probe based measurement setup. Such setup would enable S-parameters measurements of BJTs beyond the currently allowed limit of 300 °C, facilitate the characterization of inductors and capacitors as a function of temperature and extend the frequency range for characterization above the VHF-band, which is the limit of the proposed SMA connector-copper wire based coax-to-microstrip interface. Lastly, further research effort is required for improving the high-frequency capability of in-house SiC bipolar technology and the reliability of its metalization system at high temperatures.
Bibliography


