Integration of silicide nanowires as Schottky barrier source/drain in FinFETs

Doctoral Thesis
by
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Abstract

The steady and aggressive downscaling of the physical dimensions of the conventional metal-oxide-semiconductor field-effect-transistor (MOSFET) has been the main driving force for the IC industry and information technology over the past decades. As the device dimensions approach the fundamental limits, novel double/tri-gate device architecture such as FinFET is needed to guarantee the ultimate downscaling. Furthermore, Schottky barrier source/drain technology presents a promising solution to reducing the parasitic source/drain resistance in the FinFET. The ultimate goal of this thesis is to integrate Schottky barrier source/drain in FinFETs, with an emphasis on process development and integration towards competitive devices.

First, a robust sidewall transfer lithography (STL) technology is developed for mass fabrication of Si-nanowires in a controllable manner. A scalable self-aligned silicide (SALICIDE) process for Pt-silicides is also developed. Directly accessible and uniform NWs of Ni- and Pt-silicides are routinely fabricated by combining STL and SALICIDE. The silicide NWs are characterized by resistivity values comparable to those of their thin–film counterparts.

Second, a systematic experimental study is performed for dopant segregation (DS) at the PtSi/Si and NiSi/Si interfaces in order to modulate the effective SBHs needed for competitive FinFETs. Two complementary schemes SIDS (silicidation induced dopant segregation) and SADS (silicide as diffusion source) are compared, and both yield substantial SBH modifications for both polarities of Schottky diodes (i.e. $\phi_{bn}$ and $\phi_{bp}$).

Third, Schottky barrier source/drain MOSFETs are fabricated in UTB-SOI. With PtSi that is usually used as the Schottky barrier source/drain for $p$-channel SB-MOSFETs, DS with appropriate dopants leads to excellent performance for both types of SB-MOSFETs. However, a large variation in position of the PtSi/Si interface with reference to the gate edge (i.e., underlap) along the gate width is evidenced by TEM.

Finally, integration of PtSi NWs in FinFETs is carried out by combining the STL technology, the Pt-SALICIDE process and the DS technology, all developed during the course of this thesis work. The performance of the $p$-channel FinFETs is improved by DS with B, confirming the SB-FinFET concept despite device performance fluctuations mostly likely due to the presence of the PtSi-to-gate underlap.

Key words: CMOS technology, MOSFET, FinFET, Schottky diode, Schottky barrier source/drain, silicide, SALICIDE, SOI, multiple-gate, nanowire, sidewall transfer lithography.
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Appendix Papers

I. A novel, robust self-aligned process for platinum silicide nanowires

II. Electrically robust ultralong nanowires of NiSi, Ni$_2$Si and Ni$_{31}$Si$_{12}$

III. Ni$_2$Si nanowires of extraordinarily low resistivity

IV. Robust, scalable self-aligned platinum silicide process

V. Schottky barrier height tuning by means of ion implantation into pre-formed silicide films followed by drive-in anneal

VI. A comparative study of two different schemes to dopant segregation at NiSi/Si and PtSi/Si interfaces for Schottky barrier height lowering

VII. SB-MOSFETs in UTB-SOI featuring PtSi source/drain with dopant segregation

VIII. Performance fluctuation of FinFETs with Schottky barrier source/drain
Summary of the Appended Papers

**Paper I.** This paper presents the fabrication of the PtSi$_x$ nanowires by combining the STL technology and the newly developed Pt-SALICIDE process. It begins with revealing the details of the STL technology developed at KTH. It proceeds to describe the fabrication and characterization of PtSi$_x$ nanowires. The nanowires are found to have low resistivities that are comparable to those of the corresponding PtSi$_x$ thin films. The author of this thesis performed 80% of the work on planning, 100% on sample fabrication, 100% on measurement, 90% on analysis, and 100% on manuscript writing.

**Paper II.** This paper presents the robustness, controllability and extendibility of a preparation technique for NiSi$_x$ nanowires. The technique combines the sidewall transfer lithography (STL) and the self-aligned nickel silicide (Ni-SALICIDE) process. The author of this thesis performed 30% of the work on planning, 90% on experimental work on sample fabrication, 100% on measurement, 90% on analysis, and 90% on manuscript writing.

**Paper III.** This paper demonstrates the fabrication of ultralong Ni$_2$Si nanowires with an extraordinarily low resistivity of 10 μΩcm. The mechanism of the low resistivity is experimentally studied and discussed. The author of this thesis performed 50% of the work on planning, 100% on sample fabrication, 100% on measurement, 90% on analysis, and 70% on manuscript writing.

**Paper IV.** This paper demonstrates a robust, scalable self-aligned platinum silicide (Pt-SALICIDE) process. The novelty of the process lies in its addressing issues related to selective etch of remaining Pt against formed PtSi$_x$. The process comprises two consecutive annealing steps in a single run; the first is silicidation of Pt films on Si substrates carried out in N$_2$, whereas the second step is surface oxidation of the resultant PtSi$_x$ in O$_2$. The scalability of the process is confirmed by the successful formation of 400-μm long PtSi$_x$ nanowires. The author of this thesis performed 60% of the work on planning, 100% on sample fabrication, 100% on measurement, 90% on analysis, and 80% on manuscript writing.

**Paper V.** This paper presents an experimental study on modification of Schottky barrier heights (SBHs) using ion implantation followed by drive-in anneal of As, B, In and P in pre-formed NiSi and PtSi films. The process is abbreviated as SADS. The purpose of the work was to establish and quantify a process for the integration of Schottky barrier source/drain (SB S/D) in a novel device structure, i.e., SB S/D MOSFET or simply SB-MOSFET. The SBH tuning effect is concluded to be induced by the formation of interfacial dipoles through substitutional replacement of Si atoms with the dopants studied. The author of this thesis performed 70% of the work on planning, 80% on device fabrication, 70% on measurement, 70% on analysis, and 50% on manuscript writing.
Paper VI. This paper presents a comparative study of two different schemes, SIDS vs. SADS, used for incorporation of a high concentration of dopants at the silicide/Si interface for NiSi and PtSi, i.e., dopant segregation, with the purpose of lowering the SBHs of the contact systems. Here, SADS stands for silicide as diffusion source. The author of this thesis performed 50% of the work on planning, 80% on device fabrication, 40% on measurement, 40% on analysis, and 30% on manuscript writing.

Paper VII. This paper demonstrates the fabrication and characterization of SB-MOSFETs of both polarities on UTB-SOI substrates. PtSi that is usually used for p-MOSFETs was studied as the SB S/D for both types of transistors. Through dopant segregation with appropriate dopants using the SADS process, i.e., B for p-type SB-MOSFET and As for n-type SB-MOSFET, excellent performance was readily achieved. The author of this thesis performed 80% of the work on planning, 80% on device fabrication, 50% on measurement, 60% on analysis, and 80% on manuscript writing.

Paper VIII. This paper reports a considerable performance fluctuation of FinFETs featuring PtSi-based SB S/D. The Fin-channels are measured 27-nm tall and 35-nm wide. Since essentially only one silicide grain is in contact with each Fin-channel at the PtSi/Si interface, an uneven overlap between the PtSi and the gate confirmed from an extensive TEM analysis is proposed as the origin of the performance fluctuation of the FinFETs. The author of this thesis performed 90% of the work on planning, 80% on device fabrication, 50% on electrical measurement, 60% on physical analysis, and 30% on manuscript writing.
Related work not included in the thesis

1. A robust spacer gate process for deca-nanometer high-frequency nMOSFETs

2. Challenges for 10 nm MOSFET process integration
Acknowledgements

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Thank you all!

Zhen Zhang

Stockholm 2007-12-24
Symbols and Acronyms

$A$ The area of a Schottky contact

$A^*$ The Richardson constant

$C$ Capacitance per unit area

$C_{dm}$ Maximum depletion-layer capacitance per unit area

$C_{ox}$ Gate oxide capacitance per unit area

$E$ Energy

$E_C$ Conduction band edge energy

$E_{eff}$ Effective electric field (effective vertical field across gate oxide)

$E_F$ Fermi energy level

$E_i$ Intrinsic Fermi energy level

$E_g$ Band gap energy

$E_V$ Valence band edge energy

$I_{off}$ Off current

$I_{on}$ On current

$I_D$ Drain current

$I_{D,sat}$ Drain current in saturation

$J$ Drive current density

$J_0$ Leakage current of a Schottky diode

$J_{fe}$ The field emission current density tunnelling through the SB.

$J_{GIDL}$ Gate-induced drain leakage

$J_j$ Junction leakage

$J_{off}$ The subthreshold leakage current density

$J_{th}$ The thermionic (or thermal) emission current density

$k$ Boltzmann’s constant (=1.38×10^{-23} J/K)

$L$ Gate length (length)

$L_{CH}$ Effective channel length

$L_G$ Gate length

$m$ MOSFET body-effect coefficient

$n$ Ideal factor of a Schottky diode

$n_i$ Intrinsic carrier concentration

$N$ Number of carriers

$N_a$ Acceptor doping concentration

$N_d$ Donor doping concentration
\( N_{sub} \) Doping concentration in the substrate

\( Q \) Electronic charge (=1.602×10^{-19} \text{ C})

\( Q_d \) The depletion charge

\( Q_i \) Inversion charge per unit area

\( Q_m \) The charge on the surface of the metal,

\( Q_{ox} \) The charge (trapped or fixed) at the SiO\(_2\)-Si interface

\( Q_{ss} \) The charge of the interface states

\( R_{ch} \) Channel resistance

\( t_{ox} \) Gate oxide thickness

\( t_{Si} \) Thickness of the surface Si layer of the UTB-SOI

\( t_{SW} \) Sidewall thickness

\( T \) Absolute temperature

\( V_D \) Drain voltage

\( V_{dd} \) Supply voltage

\( V_{D, sat} \) Drain voltage in saturation

\( V_{fb} \) Flat-band voltage

\( V_G \) Gate voltage

\( V_r \) Reversed bias

\( V_T \) Threshold voltage

\( v \) Carrier velocity

\( W \) Gate width

\( W_{dm} \) Maximum depletion layer width

\( W_{SD,OL} \) Overlap of the source/drain silicide with the gate

\( X_s \) Electron affinity of the semiconductor

\( \varepsilon_s \) Semiconductor Permittivity

\( \varepsilon_{Si} \) Silicon Permittivity (=1.04×10^{-12} \text{ F/cm})

\( \psi_B \) Difference between Fermi level and intrinsic level

\( \psi_{bi} \) Built-in potential

\( \phi_0 \) Neutral level of interface states

\( \phi_B \) Schottky-Barrier Height

\( \phi_{bn} \) Schottky-Barrier Height to electrons

\( \phi_{bp} \) Schottky-Barrier Height to holes

\( \phi_m \) The work function of the metal

\( \phi_{ms} \) Work-function difference between the gate and the Si substrate
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
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<tbody>
<tr>
<td>$\mu_{\text{eff}}$</td>
<td>Effective mobility</td>
</tr>
<tr>
<td>$\mu_{\text{eff, } n}$</td>
<td>Effective mobility of electrons</td>
</tr>
<tr>
<td>$\mu_{\text{eff, } p}$</td>
<td>Effective mobility of holes</td>
</tr>
<tr>
<td>$\xi$</td>
<td>The difference between the Fermi level and the bottom of the conduction band</td>
</tr>
<tr>
<td>$\tau$</td>
<td>Circuit delay time</td>
</tr>
<tr>
<td>CD</td>
<td>Critical dimension</td>
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<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
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<tr>
<td>CVD</td>
<td>Chemical vapor deposition</td>
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<tr>
<td>DS</td>
<td>Dopant-segregation</td>
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<tr>
<td>EBL</td>
<td>Electron-beam lithography</td>
</tr>
<tr>
<td>HR-SEM</td>
<td>High-Resolution Scanning Electron Microscopy</td>
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<tr>
<td>IC</td>
<td>Integrated circuits</td>
</tr>
<tr>
<td>IDP</td>
<td>\textit{In situ} phosphorous doped poly-Si</td>
</tr>
<tr>
<td>LER</td>
<td>Line edge roughness</td>
</tr>
<tr>
<td>LPCVD</td>
<td>Low-pressure chemical vapor deposition</td>
</tr>
<tr>
<td>LWR</td>
<td>Line width roughness</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor field effect transistor</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma-enhanced CVD</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive ion etch</td>
</tr>
<tr>
<td>SADS</td>
<td>Silicide as diffusion source</td>
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<tr>
<td>SALICIDE</td>
<td>Self-aligned silicide</td>
</tr>
<tr>
<td>SBH</td>
<td>Schottky-Barrier Height</td>
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<tr>
<td>SB-MOSFET</td>
<td>Schottky-Barrier Source/Drain MOSFET</td>
</tr>
<tr>
<td>SCE</td>
<td>Short channel effect</td>
</tr>
<tr>
<td>SIDS</td>
<td>Silicidation induced dopant segregation</td>
</tr>
<tr>
<td>SiNW</td>
<td>Si nanowire</td>
</tr>
<tr>
<td>STL</td>
<td>Sidewall transfer lithography</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>TEOS</td>
<td>Tetraethoxysilane (Si(OC$_2$H$_5$)$_4$)</td>
</tr>
<tr>
<td>UTB-SOI</td>
<td>Ultrathin body silicon-on-insulator</td>
</tr>
<tr>
<td>V-L-S</td>
<td>Vapor-Liquid-Solid</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very large-scale integration</td>
</tr>
<tr>
<td>XTEM</td>
<td>Cross-section Transmission Electron Microscopy</td>
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Chapter 1. Introduction

The invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) in early 1960’s broke the barrier to the large-scale integration that the initial integrated circuits (IC) with bipolar transistors could not reach [1]. MOSFET has since then become the fundamental semiconductor component of almost all modern electronic circuits. And the steady dimensional downscaling of the MOSFET has been the main drive of the IC technology and information technology, since shrinking the size especially the distance between the source and drain of a MOSFET means increasing the circuit speed, makes more space available to bringing more transistors on the same area, and reduces the manufacturing cost. As shown in Fig. 1.1 [2], the downscaling of the MOSFETs has been kept in pace with Moore’s law quite well, and the number of transistors on a chip has indeed been doubled about every two years. And each time the transistor size shrinks, the ICs become cheaper and perform better. In 1965, a single transistor cost more than a dollar. By 1975, the cost of a transistor had dropped to less than a cent and almost 100,000 transistors could be integrated on a single die with the transistor size at that time. Today’s Intel processors, integrated with about 1 billion transistors, run at 3.2 GHz and higher; they can be manufactured in high volume with transistors that cost less than 1/10,000th of a cent [3].

Figure 1.1. Number of transistors integrated in Intel’s microprocessors vs. the production year. [2]
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To a large extent, the dimensional downscaling of the MOSFETs was not seriously challenged in the past with the development of new lithography tools, masks, photoresist materials and critical dimension etch processes. Today, we have devices in production that measure several tens of nanometers in the critical dimension, i.e., gate length. It has now become increasingly difficult to meet transistor performance gain with reasonable device leakage [4,5], since neither the thermal voltage \( kT/q \) nor the silicon bandgap \( E_g \) changes with the downscaling. The former leads to non-scalable subthreshold, the latter to nonscalability of the built-in potential, depletion-layer width, and short channel effects [1]. Furthermore, the constant permittivity of gate oxide, doping levels of the gate and source/drain, the mobility of the channel materials would not participate in the downscaling [1]. Due to these challenges with the downscaling of the planar bulk MOSFET, advanced devices such as MOSFETs on ultrathin body (UTB) fully depleted silicon-on-insulator (SOI) and multiple-gate MOSFETs notably FinFETs are expected to be implemented [5]. However, how to reduce the parasitic series source/drain resistance \( (R_{sd}) \) to tolerable values in the UTB-SOI devices or FinFETs becomes extremely challenging. One possible solution is to replace the traditional doped p-n junction source/drain with metallic, or Schottky barrier, source/drain (SB S/D) [5].

The focus of this thesis is on the process integration issues of novel SB S/D MOSFET, SB-MOSFET in short, with a FinFET structure, to control the short channel effects and reduce the parasitic series source/drain resistance \( (R_{sd}) \). The thesis is organized as follow. In Chapter 2, the fundamentals of MOSFETs are first reviewed. It is followed by the downscaling trends as well as major challenges therefrom. Advanced MOSFET structures and concepts aiming at resolving such challenges are then discussed. Chapter 3 describes the structure, the process flow and the principles of operation of SB-MOSFETs.

To manufacture a nanoscale MOSFETs, a prerequisite is the ability to prepare nano-silicon structures. There are several ways to realize the needed nanostructures. Chapter 4 presents a so-called sidewall transfer lithography (STL) process technology for the fabrication of Si nano-wires (SiNWs) in a controllable manner. We have followed the sensational breakthrough of UC-Berkeley and developed this technology in order to go much beyond the resolution limit of the photolithography with an I-line Stepper in our process laboratory. The results in Paper I are referred to while describing the STL process.
Chapter 1. Introduction

To manufacture MOSFETs with SB S/D, the key process is self-aligned metal silicide (SALICIDE). In Chapter 5, the process is detailed for both nickel silicide (NiSi) and platinum silicide (PtSi). Several key points of the SALICIDE process are discussed in connection with the results in Papers I through IV.

The performance including leakage of a SB-MOSFET is mainly determined by the Schottky barrier height (SBH) at the ends of the source and drain. In Chapter 6, the process leading to modification of the effective SBH by dopant segregation (DS) for both NiSi and PtSi is illustrated and verified with Schottky diodes. The discussion is facilitated by referring to the results in Papers V and VI.

With STL, SALICIDE and DS techniques developed are validated, process integration issues towards SB-MOSFETs are dealt with in Chapter 7. These two kinds of SB-MOSFETs, one on UTB-SOI and the other FinFETs, are presented. Both kinds use PtSi as the SB S/D and incorporate appropriate dopants for modification of effective SBHs. The discussion in this chapter refers to the results in Papers VII and VIII.

Finally in Chapter 8, a summary along with future perspective conclude this thesis.
Integration of silicide nanowires as Schottky barrier source/drain in FinFETs
Chapter 2. Device Physics, Downscaling and Novel Concepts

The first MOSFET on a Si substrate using SiO$_2$ as the gate dielectric was fabricated in 1960 [6]. Although it was slower in operation speed compared with the bipolar transistor, the MOSFET technology offered a higher layout density and much simpler fabrication process. The invention of the complementary MOS (CMOS) technology in 1963 [7] was groundbreaking that has facilitated very large-scale integration (VLSI) of ICs and subsequently led to advanced microprocessors and memories [1]. The downscaling of MOSFETs stimulates the growth of Si IC industry and information technology by constantly enhancing the circuit speed, increasing the integration level in the chip and cutting down the manufacturing cost. In this chapter, the basic principle of operation of the MOSFET is briefly presented, the dimensional downscaling is introduced, and the main challenges ahead are outlined. Finally, the emerging advanced device structures and concepts for Si MOSFET are discussed.

2.1 Fundamentals of MOSFETs

2.1.1 MOSFET structure

An ordinary MOSFET is a three-terminal electronic switch: the energy barrier in the channel region controlled by the vertical electric field of the gate electrode modulates the current flow from the source to the drain electrode. A basic bulk MOSFET structure is shown in Fig. 2.1 with an $n$-channel. There are four terminals in this device: gate, source, drain, and substrate. Normally the source and substrate terminals are grounded with only a small leakage current flowing through them. The source and drain regions are heavily doped with an opposite type to the substrate doping. For an $n$-MOSFET (i.e., $n$-type MOSFET), the source/drain are heavily doped $n$-type while the substrate is p-type. The gate electrode, which is traditionally heavily doped $n$-type polycrystalline Si (poly-Si), is separated from the channel with a thin SiO$_2$ as the gate dielectric. The SiO$_2$ is usually formed by thermal oxidation, and acts as an energy barrier between the gate electrode and the Si substrate.
For the $n$-MOSFET, when the applied gate voltage is lower than the threshold voltage $V_T$ (see below for its definition), only a small leakage current can flow between the source and drain; the MOSFET acts as two back-to-back $p$-$n$ diodes with a large energy barrier in-between that prevents the current from flowing from the source to the drain except for a small diffusion current. When a sufficiently large positive bias ($>V_T$) is applied to the gate, the surface of the substrate under the gate region is inverted to form an $n$-type channel with a high density of electrons. Consequently, a conduction path is built allowing for a significant current. The detailed transition of the device from “OFF” to “ON” is described as below.

When the gate voltage is equal to the sum of the work-function difference between the gate poly-Si and the Si substrate and the potential drop caused by the charge (trapped or fixed) at the SiO$_2$-Si interface, the flatband voltage is obtained as:

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$  \hspace{1cm} (2.1)$$

where

$$\phi_{ms} = -0.56 - kT/q \cdot \ln(N_a/n_i)$$ \hspace{1cm} (2.2).$$

The energy band diagram will be flat as shown in Fig. 2.2(a). There is no charge generated at the interface. The transistor is ‘off’.

Figure 2.1. Schematic diagram of an $n$-channel MOSFET on a bulk $p$-type substrate (well).
Chapter 2. Device Physics, Downscaling and Novel Concepts

Figure 2.2. Energy band diagrams illustrating an n-MOSFET biased (a) at flat-band, (b) in depletion and (c) in strong inversion. The pictures to the right show the charge distributions in the MOS structure under these bias conditions.
When the gate voltage is slightly increased, but still kept below $V_T$, the gate potential repels holes from the substrate surface leaving behind a depletion region with fixed negative charge from the ionized dopants. The negative charge causes the energy band in the substrate bend downward towards the surface as shown in Fig. 2.2(b). However, as the charge in the depletion region is fixed, no conduction channel is formed. The transistor is still ‘off’.

When the gate voltage is further increased to $V_T$, the energy band in the substrate bends downward with the surface potential $\psi_s$ reaching $2\psi_B$. As shown in Fig. 2.2(c), $\psi_B$ is the potential difference between the intrinsic Fermi level $E_i$ and the Fermi level $E_F$ of the substrate. As the Fermi level at the surface is closer to the conduction band than to the valence band, the surface is inverted and an $n$-channel is formed. The transistor is now turned ‘on’. $\psi_B$ is a function of substrate doping concentration, $N_a$,

$$\psi_B = kT/q \cdot \ln(N_a/n_i)$$

(2.3)

if a complete ionization is assumed.

With the definition, $V_T$ is given by:

$$V_T = V_{fb} + 2\psi_B + \frac{\sqrt{4\epsilon_d q N_a \psi_B}}{C_{ox}}$$

(2.4)

In Eq. (2.4), the first term is the gate voltage required to achieve the flat-band condition with no potential drop in the oxide and the Si substrate. The second term is the voltage required to invert the substrate. The third term is the voltage required to build up the depletion charge. At the point $V_G=V_T$, the concentration of the inversion carriers is equal to the doping concentration of the substrate. Consequently, a significant current can flow from the source to the drain.
2.1.2 I-V characteristics

The drain current $I_D$ of a MOSFET includes both drift and diffusion current components. When $V_G$ is lower than $V_T$, the $I_D$ is low dominated by the diffusion current. This defines the subthreshold drain current given by:

$$I_D = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} \left( m - 1 \right) \left( \frac{kT}{q} \right)^2 e^{(V_G-V_T)/m k T} \left( 1 - e^{-q V_D / (kT)} \right)$$

(2.5)

When $V_D$ is greater than a few $kT/q$, $\left( 1 - e^{-q V_D / (kT)} \right) \approx 1$. Then, the following is obtained:

$$I_D = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} \left( m - 1 \right) \left( \frac{kT}{q} \right)^2 e^{(V_G-V_T)/m k T}$$

(2.6)

It is apparent that the subthreshold drain current is independent of drain voltage $V_D$. It decreases exponentially with decreasing $V_G$. The off-current ($I_{\text{off}}$) is normally defined as the $I_D$ at $V_G=0$ V. It can be expected that $I_{\text{off}}$ would increase by about 10 times for every 100-mV reduction of $V_T$.

The slope of $I_D$ on the logarithmic scale versus $V_G$ is called subthreshold slope $SS$ as shown in Fig. 2.3. It can be obtained through:

$$SS = \left( \frac{d \log_{10} I_D}{d V_G} \right)^{-1} \approx 2.3 \frac{m k T}{q} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{\text{dm}}}{C_{\text{ox}}} \right)$$

(2.7)

$SS$ is a measure of the ability to turn off a device, with a value typically of 60-100 mV per order of magnitude in current change, normally expressed as 60-100 mV/decade. The lower the $SS$, the steeper the current drop/increase with decreasing/increasing $V_G$, and the higher the on-current at a same gate over-drive ($V_G-V_T$). The $SS$ is sensitive to the presence of charge traps at the SiO$_2$/Si interface, since the capacitance associated with the interface states will be in parallel with the (maximum) depletion-layer capacitance $C_{\text{dm}}$ in Eq. (2.7). It is rather insensitive to other device parameters.
The parameter \( m \) in Eqs. (2.5)-(2.7) is often termed body effect coefficient. It is typically between 1-1.4 and is calculated as:

\[
m = 1 + \frac{\sqrt{E_{so} q N_{sub} / 4q^2 B}}{C_{ox}} \approx 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3m_{ox}}{W_{dm}}
\]  

(2.8)

The parameter \( \mu_{eff} \) in Eqs. (2.5) and (2.6) represents the effective mobility of the carriers in the inversion layer of the MOSFET. The electron and hole mobility in the inversion layer can be described by the following universal relations [8]:

\[
\mu_{eff,n} = \frac{638}{1 + (E_{eff} / 7 \cdot 10^3)^{1.69}}
\]  

(2.9)

for the electron mobility, and

\[
\mu_{eff,p} = \frac{240}{1 + (E_{eff} / 2.7 \cdot 10^5)}
\]  

(2.10)
for the hole mobility. $E_{\text{eff}}$ is the effective electric field perpendicular to the channel direction. It can be seen that $\mu_{\text{eff}}$ decreases very rapidly with increasing $E_{\text{eff}}$ at high $E_{\text{eff}}$.

When $V_G$ is higher than $V_T$, $I_D$ is dominated by the drift current given by:

$$I_D = \frac{W}{L} \mu_{\text{eff}} C_{ox} [(V_G - V_T)V_D - mV_D^2 / 2]$$

(2.11)

The $I_D$-$V_D$ characteristics for an $n$-MOSFET with $V_G > V_T$ are shown in Fig. 2.4. When $V_D$ is low, $mV_D^2/2$ can be neglected and Eq. (2.11) is reduced to,

$$I_D = \frac{W}{L} \mu_{\text{eff}} C_{ox} (V_G - V_T)V_D$$

(2.12)

$I_D$ increases linearly with $V_D$.

---

![Figure 2.4. $I_D$-$V_D$ characteristics for an $n$-MOSFET with $V_G > V_T$](image)
When the $V_D$ is increased further, the increase of $I_D$ follows a parabolic behavior as described in Eq. (2.11), until a maximum or saturation value is reached. This occurs when:

$$V_{D_{\text{sat}}} = (V_G - V_T)/m$$  \hspace{1cm} (2.13)

at which

$$I_D = I_{D_{\text{sat}}} = \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} \frac{(V_G - V_T)^2}{2m}$$  \hspace{1cm} (2.14)

Above $V_{D_{\text{sat}}}$, $I_D$ stays constant at $I_{D_{\text{sat}}}$, independent of $V_D$.

Similar relations to Eqs. (2.1)-(2.14) can be obtained for $p$-MOSFETs.

**2.2 Downscaling of MOSFETs**

**2.2.1 Short channel effect**

The dimensional downscaling of MOSFETs has traditionally been facilitated by the development of new lithography tools, masks, photoresist materials, and critical dimension etch processes. The decrease of the channel length of a MOSFET has constantly challenged by short channel effect (SCE) which is shown as a decrease of $V_T$ as the channel length $L_G$ is reduced. For digital applications, the $V_T$ roll-off is the most undesirable SCE since in the CMOS VLSI technology, $L_G$ varies from chip to chip, wafer to wafer, lot to lot due to process tolerance [1]. One must ensure that $V_T$ does not become too low for the minimum $L_G$ devices on a chip. The SCE is more pronounced at higher drain bias. So, advanced design is needed for scaled devices in order to control the SCE and to minimize the performance degradation.

The physics of the SCE can be understood as follows. In a short-channel device, the source-drain distance is comparable to the depletion width in the vertical direction in the channel region. The drain potential has a strong effect on the band bending over a significant portion of the channel. Thus, the energy barrier which prevents carriers from flowing through under the “off” condition is greatly lowered by the drain field penetration. This causes a substantial
increase of the subthreshold current, thus a reduced \( V_T \). In a long-channel device, the source and drain are so far apart that their depletion regions have no effect on the energy barrier or the electric field pattern in most part of the channel. From theoretic calculations [1], the \( V_T \) roll-off is given by

\[
\Delta V_T = 8(m-1)\sqrt{\psi_{bl}(\psi_{bi} + V_D)}e^{-\frac{d_l}{2mW_{dm}}}
\]  

(2.15)

Because of the exponential factor, the \( V_T \) roll-off is very sensitive to the channel depletion width \( W_{dm} \). To avoid excessive SCE, the substrate doping concentration should be chosen such that the minimum \( L_G \) is about 2-3 times \( W_{dm} \) [1].

2.2.2 Scaling rules for MOSFETs

The classic scaling rule is called “constant-field scaling”. It was proposed by Dennard et al. in 1974 [9]. In constant-field scaling, one can control SCE by scaling down the vertical dimension along with the horizontal dimensions, while also proportionally decreasing the applied voltage and increasing the substrate doping concentration (i.e., decreasing \( W_{dm} \)). The principle is to scale the supply voltage and device dimensions (both horizontal and vertical) by the same factor \( \kappa > 1 \), so that the electric field remains unchanged. The scaling rule is summarized in Table 2.1. As a result, the circuit speeds up by the same factor \( \kappa \), and the power dissipation per circuit is reduced by factor of \( \kappa^2 \).

Even though the constant-field scaling rule provides a basic guideline to the design of scaled MOSFETs, the requirement of reducing the supply voltage by the same factor as the device dimensions is too demanding. Because of the non-scalability of \( V_T \) and the reluctance to depart from the standardized voltage levels of the previous technology generation, the supply voltage has very seldom been scaled in proportion to the channel length. As a result, the oxide field has been increasing over generations rather than staying constant. A more general set of guidelines that allow an increase of the electric field were then proposed by Baccarani et al. in 1984 [10], which is shown in Table 2.2. It is desired that both the vertical and the horizontal electric fields change by the same multiplication factor, \( \alpha > 1 \), so that the shape of the electric field pattern is preserved. This assures that the 2-D effects, such as SCE, do not worsen when...
Integration of silicide nanowires as Schottky barrier source/drain in FinFETs

TABLE 2.1 Constant-field MOSFET Scaling (after[1])

<table>
<thead>
<tr>
<th>Scaling assumptions</th>
<th>Device and Circuit Parameters</th>
<th>Multiplicative Factor (κ &gt; 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Device dimensions (t_{ox}, L, W, x_j)</td>
<td>1/κ</td>
</tr>
<tr>
<td></td>
<td>Doping concentration (N_a, N_d)</td>
<td>κ</td>
</tr>
<tr>
<td></td>
<td>Voltage (V)</td>
<td>1/κ</td>
</tr>
<tr>
<td>Derived scaling behavior of device parameters</td>
<td>Electric field (E)</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Carrier velocity (\nu)</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Depletion-layer width (W_d)</td>
<td>1/κ</td>
</tr>
<tr>
<td></td>
<td>Capacitance (C = \varepsilon A/t)</td>
<td>1/κ</td>
</tr>
<tr>
<td></td>
<td>Inversion/layer charge density (Q_i)</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Current, drift (I)</td>
<td>1/κ</td>
</tr>
<tr>
<td></td>
<td>Channel resistance (R_{ch})</td>
<td>1</td>
</tr>
<tr>
<td>Derived scaling behavior of circuit parameters</td>
<td>Circuit delay time (\tau \sim CV/I)</td>
<td>1/κ</td>
</tr>
<tr>
<td></td>
<td>Power dissipation per circuit (P \sim VI)</td>
<td>1/\kappa^2</td>
</tr>
<tr>
<td></td>
<td>Power/delay product per circuit (P\tau)</td>
<td>1/\kappa^3</td>
</tr>
<tr>
<td></td>
<td>Circuit density (\propto I/A)</td>
<td>\kappa^2</td>
</tr>
<tr>
<td></td>
<td>Power density (P/A)</td>
<td>1</td>
</tr>
</tbody>
</table>

a device is scaled. The most serious issue with the generalized scaling is the drastic increase of the power density, which sets a great burden on the VLSI packaging technology to dissipate the extra heat generated on the chip. The power-delay product is also a factor of \alpha^2 higher than for the constant-field scaling.
### Table 2.2 Generalized MOSFET Scaling (after [1])

<table>
<thead>
<tr>
<th>MOSFET Device and Circuit Parameters</th>
<th>Multiplicative Factor $(\kappa &gt; 1)$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scaling assumptions</strong></td>
<td></td>
</tr>
<tr>
<td>Device dimensions ($t_{ox}, L, W, x_j$)</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Doping concentration ($N_a, N_d$)</td>
<td>$\alpha \kappa$</td>
</tr>
<tr>
<td>Voltage ($V$)</td>
<td>$\alpha / \kappa$</td>
</tr>
<tr>
<td>Electric field ($E$)</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Depletion-layer width ($W_d$)</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Capacitance ($C = \varepsilon A/t$)</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Inversion/layer charge density ($Q_i$)</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Carrier velocity ($\nu$)</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Current, drift ($I$)</td>
<td>$1$</td>
</tr>
<tr>
<td>Circuit delay time ($\tau \sim CV/I$)</td>
<td>$1/\alpha \kappa$</td>
</tr>
<tr>
<td>Power dissipation per circuit ($P \sim VI$)</td>
<td>$\alpha^3 / \kappa^2$</td>
</tr>
<tr>
<td>Power/delay product per circuit ($P\tau$)</td>
<td>$\alpha^2 / \kappa^3$</td>
</tr>
<tr>
<td>Circuit density ($\propto I/A$)</td>
<td>$\kappa^2$</td>
</tr>
<tr>
<td>Power density ($P/A$)</td>
<td>$\alpha^3$</td>
</tr>
</tbody>
</table>

#### 2.3 Necessities for novel materials and device structures

Although the scaling rules discussed above provide a basic guideline for scaling MOSFETs in order to attain higher density and speed, there are several challenges that should be considered in MOSFET design:

1. The non-scalability of the thermal voltage $kT/q$ leads to the non-scalability of $V_T$ [1].

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2. The non-scalability of the bandgap $E_g$ of Si leads to the non-scalability of built-in potential, depletion-layer width, and short channel effect [1].

3. The supply voltage cannot be scaled linearly with the dimensions because of the non-scalability of $V_T$. This results in an increase in electric field, and hence a decrease of the carrier mobility as described in Eqs. (2.9) and (2.10) [1].

4. The SiO$_2$ gate oxide thickness cannot be scaled below ~ 1.5 nm because of the catastrophic gate leakage [11, 12].

5. The channel doping needs to be increased to undesirable high levels in order to control SCE and to set $V_T$ properly. As a result, the mobility of channel carriers will be reduced, the junction leakage due to band-to-band tunnelling increased and the gate induced drain leakage increased [5].

6. The percent stochastic (random) variation in the number and location of dopants in the channel will increase sharply due to the small total number of dopants in extremely small MOSFETs. This will lead to fluctuation of $V_T$ [5].

7. The line edge roughness (LER) of the gate becomes more detrimental for smaller gate length devices [13].

These challenges with scaling planer bulk MOSFETs have called for introduction of new materials such as high-$k$ [14] and metal gate [15] in order to overcome the ‘oxide scaling barrier’. Local and global strains have further been introduced in order to enhance channel mobility in both $n$- and $p$-MOS devices [16,17]. By combining advanced lithography and gate etch process, developments have been actively pursued aiming at controlling the LER. Advanced device structures such as using ultrathin body silicon-on-insulator (UTB-SOI) substrates [1] and multiple-gate MOSFETs notably FinFETs as shown in Fig. 2.5 and Fig. 2.6, respectively, have been employed to effectively control SCE.
The multiple-gate MOSFET represents the most revolutionary device architecture for future MOSFETs. It was first proposed in the early 1980’s [18] and best represented by FinFET in the late 1990’s [19]. It has been recently regarded as the solution for the ultimately scalable MOSFET. Since the gate controls the channel from 3 directions (or 2 directions in a double-gate structure) in the FinFET, it can: 1) greatly reduce the 2-D SCE, leading to a shorter allowable channel length compared to its bulk MOSFET counterpart; 2) generate a sharper subthreshold slope which offers a larger gate over-drive for the same voltage supply and at the same off-current; and 3) allow a reduced channel doping, thus a better carrier transport behavior.
Numerous challenges are expected with the integration of FinFET with the target device performance. Comparing with planar bulk MOSFET, one of the most severe challenge is the parasitic series source/drain resistance $R_{SD}$: how to bring it to a tolerable value? The “Fin” channel of a FinFET is practically a Si nanowire. As in a planar MOSFET, heavy doping along with silicidation of the part of the nanowire-Fin extending from the channel to the source/drain terminals can greatly reduce the otherwise giant resistance. In this configuration, ordinary silicide-contacted $p$-$n$ junction contacts (to the channel) are formed. Using elevated source/drain by means of selective epitaxy around the nanowire-Fin extensions could further lead to a more improved electric link between the channel and the source/drain [20,21]. However, how to electrically activate the degenerately doped nanowire-Fin extensions to form a sharp junction towards the channel is challenging. Achieving a high doping level is critical for a low contact resistance, which is more important than the resistance of the nanowire-Fin extensions. The high temperature processes needed for the dopant activation and the selective epitaxy are not compatible with the high-$k$ gate dielectric present prior to the source/drain formation if the usual process sequence is kept.

An attractive alternative is to use SB S/D technology [22] to overcome the high series resistance problem with the FinFET. With this technology, which will be discussed in more detail in next chapter, the entire nanowire-Fin extensions linking the channel region to the

![Figure 2.7. Schematic drawing of a Schottky barrier source/drain FinFET structure.](image-url)
source/drain terminals will be replaced with metal silicide nanowires through a self-aligned process as shown in Fig. 2.7. Then, the source/drain to the channel contacts will become a Schottky barrier contact. In order to provide low-resistivity contacts, the Schottky barrier junctions to the channel should possess a low energy barrier in order to obtain a high drive current and, at the same time, a low junction leakage current. The silicide source/drain is inherently of low resistance and the metal-channel junction is atomically abrupt. An added advantage with silicide source/drain is its low thermal budget that enables integration of performance-enhancing materials such as high-$k$, metal gate and strained channel.

Considering the process complexity and the process capability in our cleanroom lab along with our long tradition in metal silicide research, the Schottky barrier source/drain FinFET architecture is studied in this thesis, with a purpose of controlling SCE and addressing parasitic series source/drain resistance ($R_{sd}$) problem.
Chapter 3. Schottky-Barrier Source/Drain MOSFET

The SB-MOSFET was first proposed by Nishi in 1966. It was issued as a patent in 1970 [23]. The idea is to replace the p-n junction contacts with Schottky barrier contacts for the source/drain terminals. The metal used for the SB S/D would typically be metal silicides. The superiorities of the SB S/D technology include low parasitic S/D resistance, low-temperature processing for the S/D formation, and inherent scalability to sub-10-nm gate-length dimensions due to the atomically abrupt junctions formed at the silicide-Si interface. The first paper on the SB-MOSFET was published by Lepselter and Sze in 1968, with a focus on bulk p-MOSFET with PtSi as the S/D [24]. The fabricated p-MOSFET suffered from poor performance with room-temperature drive current 10 times lower than that of a conventional MOSFET. The process technology has been greatly advanced since 1994 when Tucker et al. [25-26] realized the SB-MOSFET with excellent scalability. In this chapter, the architecture, process and operation of the SB-MOSFET will be described.

3.1 Device architecture of the SB-MOSFET

A cross-sectional TEM micrograph of a p-channel SB-MOSFET fabricated on UTB-SOI is shown in Fig. 3.1(a). Several key parameters of the device are illustrated in the schematic cross-section in 3.1(b); gate length $L_G$, effective channel length $L_{CH}$, gate oxide thickness $t_{ox}$, thickness of the surface Si layer of the UTB-SOI $t_{Si}$, and sidewall thickness $t_{SW}$. The major innovation of this device architecture is to replace the highly doped S/D electrodes with a metal typically a silicide. This silicide S/D structure provides a promising solution to the parasitic resistance challenge of extremely-scaled MOSFETs because of a low specific resistivity of the silicide and a potentially low SBH of the silicide to the lowly doped channel.

As shown in Fig. 3.1, the source/drain electrodes extend into the channel region with a lateral growth of the silicide. This leads to the formation of an overlap with the gate defined as $W_{SD,OL}$ with $W_{SD,OL} > 0$. If, in the contrary, the lateral growth does not occur and the silicide front stays outside the channel, an underlap is developed with $W_{SD,OL} < 0$. Since the lateral gap between the edge of the gate electrode and the silicide front in the S/D electrodes is highly resistive with lowly doped Si, it can severely deteriorate the drive current as shown by
Figure 3.1 (a) Cross-sectional TEM micrograph of a 0.5-μm gate-length p-channel SB-MOSFET on UTB-SOI. The two back arrows show the silicide edge in the channel region (b) Schematic cross-section of a SB-MOSFET with the key parameters.

Koeneke [27,28]. A smaller gap should result in significantly improved performance in terms of drive current. The size and sign of $W_{SD,OL}$ are especially critical in the design of an SB-MOSFET. Clearly, the underlap is determined by $t_{SW}$ and the degree of silicide lateral growth. A thin sidewall spacer with small $t_{SW}$ helps minimize the underlap and the SB junctions are better controlled by the gate electrode. Ideally, $t_{SW}$ should be less than 10 nm [22].
Chapter 3. Schottky-Barrier Source/Drain MOSFET

The mechanism for controlling the channel current is fundamentally different for SB-MOSFET from a conventional MOSFET with $p$-$n$ junction source/drain. Instead of controlling the channel conductance by the gate electrode as in a conventional MOSFET, the carrier injection through the Schottky barrier at the source end is the rate limiting step. Thus, a high-performance SB-MOSFET requires a low SBH, to electrons for $n$-MOSFETs and to holes for $p$-MOSFETs. Theoretical studies have demonstrated that a low SBH about 0.1 eV is needed in order for SB-MOSFETs to outperform conventional MOSFETs heavily doped S/D [29, 30]. PtSi and a rare-earth silicide such as ErSi$_x$ or YbSi$_x$ have the lowest known SBH to holes (0.15-0.27 eV) and electrons (0.27-0.36 eV), respectively. PtSi has therefore been frequently used for $p$-channel SB-MOSFETs [31,32], while ErSi$_x$ [31] or YbSi$_x$ [32] for $n$-channel SB-MOSFETs in a complementary-silicide scheme. Since the SBH of both groups of silicides is still higher than 0.1 eV, the SBH engineering becomes significantly interesting. A promising approach to engineer the SBH is dopant segregation at the silicide-Si interface aiming at modification of the effective SBH [33-37]. More details about this approach will be discussed in Chapter 6.

Normally, the channel doping of SB-MOSFETs is reduced to $10^{16}$-$10^{17}$ which is 10-100 times lower than that in conventional MOSFETs in order to control the subthreshold leakage current. Halo or pocket implantation is eliminated from the manufacture process. An advantage of reducing channel doping is an improved effective carrier mobility. UTB-SOI substrates [33-35] or multi-gate structure are normally used to assist control of the subthreshold leakage current [36, 37].

3.2 General process flow of SB-MOSFETs

The manufacturing process of a SB-MOSFET is fully compatible with standard Si technology. The process appears to be simpler than for fabrication of conventional bulk MOSFET and no novel process equipment is required. Generally [22], the fabrication of SB-MOSFETs starts with a standard isolation process such as STI, followed by well or channel implantation. Then a dual-doped gate or metal-gate process is utilized. The gate is normally defined by standard lithography and dry-etching technology. The formation of slim gate spacers with $t_{SW}$$<10$ nm is a key step in the process. It is normally realized by deposition of a thin dielectric film followed by an anisotropic dry-etch back to expose the active region. Pocket implantation,
S/D extension implantation and deep contact implantation are not necessary. The SALICIDE process is another key step. For a complementary-silicides application, a dual-silicide exclusion-mask process is needed for the formation of the S/D regions of the $n$- and $p$-MOS devices. The exclusion-mask is typically a deposited oxide layer. It is first patterned to expose the $p$-MOSFET region, followed by a SALICIDE process with PtSi to form the SB S/D. Then, the $n$-MOSFET region is similarly exposed and followed by the formation of ErSi$_x$ or YbSi$_x$ to create the SB S/D. The order can also be reversed with the SB S/D formation for the $n$-MOSFET first. The details of the SALICIDE process will be discussed in Chapter 5. It is important to keep the formation temperature low for the silicide process, keeping in mind the eventual presence of high-$k$ gate dielectric and strained channels. In our processes, this temperature has been kept below 600 °C. Finally, a conventional metallization scheme for the first level metallization completes the fabrication process.

Significant advantages of the process for a SB-MOSFET can be listed as below:

1. Low temperature processing (below 600 °C after the gate-stack formation for our process).

2. Several implantation steps for Halo, extension and deep S/D are skipped, resulting in less damage to the substrate with and without strain, avoiding damage induced mobility degradation, and eliminating high temperature (1000 °C) anneals for the dopant activation in the S/D. The latter in turn enables the integration of new critical materials such as high-$k$ gate dielectric, metal gates and strained channel.

3. Low channel doping concentration and thus improved effective carrier mobility.

### 3.3 Principle of operation

The different nature of the junction between the S/D and the substrate leads to the fundamentally different principle of operation in a SB-MOSFET as compared to a conventional MOSFET with $p$-$n$ junction S/D. The basic operation principle of a $p$-channel SB-MOSFET is understood with the assistance of band diagrams shown in Fig. 3.2. The band diagrams of an $n$-channel SB-MOSFET are the mirror image of Fig. 3.2. Assume that the SB S/D is made of PtSi with $\Phi_{bp}=0.24$ eV to holes and $\Phi_{bn}=0.88$ eV to electrons.
For the $p$-channel SB-MOS device, the drive current density $J$ is the sum of the thermionic (or thermal) emission current density (of holes) over the SB $J_{th}$ and the field emission current density (of holes as well) tunnelling through the SB $J_{fe}$. In both cases, the SB refers to that at the source end. Mathematically, this statement means:

$$J = J_{th} + J_{fe} \quad (3.1)$$

The thermal emission current density can be determined by [38]:

$$J_{th} = A^* T^2 e^{\frac{-q\Phi}{kT}} \left( e^{\frac{qV}{kT}} - 1 \right) \quad (3.2)$$

where $A^*$ is the Richardson constant, $T$ is absolute temperature and $V$ is the applied bias. The tunnelling current density is unfortunately much more complicated to obtain and computational means is often needed to model the $J_{fe}$.

In the “off” state (see the upper panel in the frame of Fig. 3.2), the electric field present over the energy barrier at the source end is very low. There is practically no hole that can tunnel through the thick barrier, $J_{fe}=0$. Thermal emission over the tall barrier is difficult as well, $J_{th}=0$. As a result, $J=0$. When the gate electrode is strongly biased at a negative potential (see the lower panel in the frame of Fig. 3.2), the transistor can be turned “on” because the electric field over the source end is so large that the energy band in the channel region is “pulled up” leading to a considerably thinned energy barrier. Thus, $J_{fe}$ increases rapidly with increasing the electric field leading to conduction of current in the channel. As $J_{th}$ remains low, the drive current is then dominated by $J_{fe}$. Hence, the SB-MOSFET is often referred to as a filed-emission device in the “on” state.
The subthreshold leakage current density $J_{\text{off}}$ at $V_D = V_{dd}$ and $V_G = 0$, as shown in the Fig. 3.2, is determined by three leakage current components [22]: 1) gate-induced drain leakage ($J_{\text{GIDL}}$), 2) junction leakage $J_j$, and 3) S/D thermal-emission leakage $J_{\text{th}}$.

\begin{equation}
J_{\text{off}} = J_{\text{GIDL}} + J_j + J_{\text{th}}
\end{equation}

$J_{\text{GIDL}}$ is caused by the gate induced barrier narrowing at the drain end, which results in the tunneling of electrons though the relatively large but thin barrier at the drain end. It is very sensitive to both the electron barrier height ($\Phi_{bn} = E_g - \Phi_{bp}$) and the barrier width. Semiconductors with low $E_g$ tend to suffer from a significant $J_{\text{GIDL}}$ [39]. Since $W_{SD,OL}$, $EOT$ and $V_D$ influence the electric field over the energy barrier at the drain end, they determine the
Chapter 3. Schottky-Barrier Source/Drain MOSFET

barrier width, thus the $J_{GIDL}$ as well. The junction leakage $J_j$ is caused by the reverse-biased Schottky diode at the drain end, which is normally dependent on the substrate doping concentration. The S/D thermal-emission leakage $J_{th}$, which is determined by the SBH, makes the largest contribution to $J_{off}$.

When the transistor is in the “on” state with the gate electrode biased at $V_D (<0 \text{ V})$, a thin SB is obtained by the strong electric field at the source end. The drive current is dominated by the field-emitted holes tunnelling through the SB. There is still need of physics and models for understanding the “on”-state behavior of a SB-MOSFET. Till now, analytical expressions describing the $I-V$ characteristics over a broad range of bias and device parameters are not yet to emerge. Mostly, the “on”-state performance of a SB-MOSFET is predicted by modeling the field-emission current based on numerical methods.
Chapter 4. Nanowire Fabrication

Manufacturing a nano-scale MOSFET requires the capability of preparing nanostructures especially SiNWs. Much effort has been devoted to the synthesis of SiNWs, and a number of methods have been developed. Despite some detailed differences among the methods, they can be categorized in two approaches: bottom-up primarily based on self-assembly mechanism versus top-down relying on deposition, patterning and etching. In this chapter, both approaches are briefly discussed with their respective pros and cons. Details of our sidewall transfer lithography (STL) technology are described and key process steps are shown, with reference to Paper I.

4.1 Bottom-up vs. top-down

The bottom-up approach is based on the self-assembly growth mechanism. It includes the vapor-liquid-solid (V-L-S) method [40, 41], solid-liquid-solid method [42, 43], solution-liquid-solid method [44, 45], template growth method [46], et al. The V-L-S growth method is the most widely used bottom-up fabrication method. It was first proposed by Wagner in 1964 during his studies of growth of large single-crystal whiskers [47]. The proposed mechanism of the V-L-S growth is summarized in Fig. 4.1. In the V-L-S reaction, a metal is used as catalyst. Silicon in the vapor phase diffuses into the liquid Si-metal alloy droplets and bonds to the solid Si at the liquid-solid interface, causing Si to nucleate and grow from the droplet. The diameter of the nanowire grown with this technique is determined by the diameter of the alloy droplet at its tip. Various modified V-L-S methods have been developed to grow SiNWs, including laser ablation [40], chemical vapor deposition [41], and physical evaporation [48].

Most of the bottom-up methods are very simple and mature. A large variety of NWs have been synthesized with this approach [40-46]. The mean diameters of the grown SiNWs can be roughly controlled by selecting catalyst clusters of desired diameters and/or by managing the growth ambient pressure. But the diameters of the synthesized SiNWs are usually not uniform with a relatively broad diameter distribution. Moreover, the SiNWs fabricated through this process are inevitably contaminated by residuals of
Integration of silicide nanowires as Schottky barrier source/drain in FinFETs

**Figure 4.1. Schematic presentation of the process flow for Vapor-Liquid-Solid growth of Si nanowires by laser ablation [40].** A) Laser ablation of a Si$_{1-x}$Fe$_x$ target to create a hot vapor of dense Si and Fe species. B) Condensation of the hot vapor resulting in nanoscale clusters of Si-Fe through collisions with the buffer gas. The furnace temperature is controlled in order to maintain the Si-Fe nanoclusters in liquid (Liq) state. C) Nanowire growth upon supersaturation of the liquid. The SiNW growth continues as long as the Si-Fe nanoclusters remain in the liquid state and a Si source is available. D) Termination of the growth by moving the nanowires out of the hot reaction zone to a cold finger designed to collect the products.

The metal catalysts. The most significant drawback with this approach is that the grown SiNWs are usually freestanding, randomly distributed, and tangled together. It remains a major effort to manipulate them. As the goal of the thesis is to explore the potential of SB S/D in controllable SiNW-based FinFETs, the bottom-up approach is therefore not considered for the MOSFET fabrication.

The top-down approach is primarily based on the lithography process. The most widely used top-down approach to fabricate SiNWs in research labs is to utilize electron-beam lithography (EBL) [31, 49-51]. Normally with this technology, a hard-mask is firstly formed on top of the desired layer. It is then patterned using a fine high-energy electron beam with a diameter of several nanometers to “write” the desired structures. A dry etch is followed to transfer the nanoscale patterns from the hard mask to the desired layer. Gate length of 15-nm dimension has been fabricated using EBL in 2000 [31]. The EBL has several clear advantages over the
bottom-up approaches for device fabrication as listed below:

(1) It is easily applicable to the fabrication of the electronic devices.

(2) It is possible to make device structures with arbitrary shape and size.

(3) It is highly capable of modification of the patterns at will.

(4) It is highly flexible with definition and placement of the patterns.

However, using EBL still suffers from a low throughput since all the structures need to be written one after another with a controlled electron beam. So it is difficult to generate high-density patterns. Furthermore, it has been shown to be challenging to fabricate sub-30 nm gate lengths with good uniformity. Hard mask ashing and trimming technologies have also been successfully used to make ~17 nm lines, but the uniformity is still rather poor [52]. As shown in Fig. 4.2, the STL technology (or spacer technology), a typical top-down approach, is attractive in overcoming the limits of those other lithography techniques in terms of pattern fidelity, critical-dimension (CD) variation, and pattern density [53]. It is therefore developed and employed in this thesis for fabrication of SiNWs needed for the FinFET, based on the process capability in our cleanroom lab.

![Figure 4.2. Variation of critical dimension (CD) of three lithography technologies in generating nanoscale lines/wires. CD uniformity of the spacer technology is overwhelmingly better than the other two technologies [51].](image)
4.2 Sidewall transfer lithography technology

The STL technology relies on: (1) a good thickness and step coverage control of the various films involved, (2) directional dry-etching to create vertical sidewall supports, (3) selective dry- and wet-etch of one material with respect to the other materials, and (4) complete removal of etch residuals. The process is schematically illustrated in Fig. 4.3. Note that many of the different layers used in this example to illustrate the process can actually be replaced with layers of other materials.

In this example, the goal is to fabricate a SiNW with heavily doped poly-Si that can be used as a nanoscale poly-Si gate electrode. A thermal oxide is grown on a 100-mm Si (100) wafer. An in situ phosphorous doped poly-Si (IDP) layer is then prepared by means of low-pressure chemical vapor deposition (LPCVD). This is followed by the deposition of a 40-nm thick TEOS SiO$_2$ layer and a 150-nm thick poly-SiGe layer, both also by LPCVD. After these steps, a layer stack as illustrated in Fig. 4.3(a) is obtained. It is the IDP layer that is to be patterned into SiNWs. The SiGe layer is now patterned using an I-line stepper optical lithography and plasma dry-etching based on HBr, Cl$_2$ and O$_2$ in He. With the resist mask, the SiGe etch rate is typically 400 nm/min and selectivity towards the TEOS SiO$_2$ hard mask ~4:1. A 10% over-etch is typically employed in order to ensure complete removal of residual SiGe particles. At this point, the photoresist is thoroughly removed by using oxygen plasma ashing followed by wet stripping in 1165 remover at 70 °C. The etched edges in the poly-SiGe layer serve as a sacrificial support for the subsequently formed sidewall spacers made of SiN$_x$ as shown in Fig. 4.3(b). Hence, the location and density of the SiGe openings determine those of the fabricated SiNWs. The SiN$_x$ layer is deposited by means of plasma-enhanced CVD. The thickness of the SiN$_x$ layer will determine the width of the resulting SiNWs. Figure 4.4 shows a cross-sectional TEM micrograph of a vertical step in SiGe as well as of the conformal SiN$_x$ deposition over this step. A reactive ion etch (RIE) step using CHF$_3$, CF$_4$ and O$_2$ removes the surface SiN$_x$ while leaving behind the SiN$_x$ by the sidewalls. This RIE step leads to the formation of the critical SiN$_x$ spacers, cf. Fig. 4.3(c). The etch rate of the SiN$_x$ is ~160 nm/min and the selectivity towards the underlying TEOS SiO$_2$ hard mask 2.4:1. An over-etch, again by 10%, is used to remove all residual SiN$_x$ particles that would otherwise be transferred to the hard mask. The over-etch time is optimized in order to minimize the attack
Chapter 4. Nanowire Fabrication

Figure 4.3. Schematic presentation of the STL technology developed and used for mass-fabrication of SiNWs in this thesis.
of the SiNₓ spacer while still ensuring a complete removal of the SiNₓ residuals. The poly-SiGe is now removed using solutions NH₄OH:H₂O₂:H₂O=1:1:5 and then NH₄OH:H₂O=2:5, both at 75 °C [54]. The etch rate of the TEOS SiO₂ hard mask and SiNₓ is negligibly low since the wet etch only removes less than 1 nm of these materials according to ellipsometry measurements. This assures complete removal of the supporting SiGe layer without etching the hard mask or the SiNₓ spacers. Since during the SiGe deposition, a thin (<50 Å) Si seed layer is first deposited on the TEOS SiO₂ layer in order to provide nucleation sites for the SiGe [55] and since the NH₄OH:H₂O₂:H₂O=1:1:5 etch is extremely selective to poly-Si, using the NH₄OH:H₂O solution is vital in cleaning up the poly-Si islands on the SiO₂ surface. If this Si etch is overlooked, a pattern with dense dots will be transferred to the fabricated structure as shown in Fig. 4.5. With this step, the SiNₓ spacer lines are achieved as shown in Fig. 4.3(d). A second optical lithography step is now employed to define the contact leads and pads to the SiNWs. This is actually the most innovative step first developed by a research group of UC Berkeley [53]. At this point, the SiNₓ spacer lines and the photoresist are used as the etch mask for the formation of the SiNWs and large-area leads and pads, respectively, in the underlying TEOS SiO₂. The TEOS SiO₂ hard mask is etched using CHF₃ and CF₄ in Ar. The etch rate is ~140 nm/min and the selectivity towards the SiNₓ spacers 1.6:1. After stripping the photoresist with O₂-plasma and then the SiNₓ spacer lines in H₃PO₄ at 145°C with a selectivity towards the TEOS SiO₂ hard mask >50:1, another RIE step using again HBr, Cl₂ and O₂ in He transfers the desired patterns in the TEOS SiO₂ down to the IDP layer. The etch rate is ~300 nm/min and the selectivity towards oxide better than 100:1 assure that the etch of the TEOS SiO₂ hard mask is negligible and that the etch stops on the 100-nm thick thermal oxide.
Figure 4.5. AFM micrograph for a spacer nanowire without the NH$_4$OH:H$_2$O=2:5 clean. The size of the picture is 10 μm by 10 μm.

The final structure featuring SiNWs of IDP directly connected to the leads and pads is shown in Fig. 4.3(e), after removal of the TEOS SiO$_2$ hard-mask in a dilute HF (5% in H$_2$O) solution. The SiNWs fabricated with the STL technology is uniform in height and the sample surface is particle-free, according to optical microscope and AFM in Fig. 4.6. The STL process is characterized by a high flexibility in separately controlling the height and width of the final SiNWs through the thickness of the IDP and the SiN$_x$ layer, respectively.

Figure 4.6. (a) Optical micrograph and (b) AFM micrograph of a 10-line SiNW array connected to the large-area Si leads and pads.
The smallest SiNWs we have produced using the STL technology has a dimension about 10 nm. In Fig. 4.7, a SiNW measuring about 15 nm in width is shown.

Finally, the fabricated SiNWs by means of the STL technology are usually characterized by a low line width roughness (LWR) or variation as a result of the conformal deposition of the SiNx layer by means of CVD. This conclusion is supported by the top-view TEM micrograph of a SiNW in Fig. 4.8. However, the NWs often have clear LER as also shown in Fig. 4.8. The LER is primarily caused by the optical lithography step used for the formation of SiGe sidewall supports coupled with the subsequent dry etch steps [56]. It is worth noting that the low LWR is a consequence of the two edges of the wavy nanowire being well correlated. So there is no weak point alone the line.
Chapter 4. Nanowire Fabrication

The good uniformity of the SiNWs over a wafer was verified using resistance measurements of the heavily doped SiNWs in IDP; The measured data displays a confined behaviour with 95% of all values within ±10% [57]. After converting the SiNWs to NiSi$_x$ and PtSi$_x$ NWs, the assessment of the uniformity of the NWs became simpler. The results, along with the fabrication of NiSi$_x$ and PtSi$_x$ NWs based on the STL technology are described in great detail in Papers I through IV.
Chapter 5. Self-Aligned Silicide Technology

Self-aligned metal silicide (SALICIDE) technology has played an important role in the rapid and successful miniaturization of device dimensions in CMOS technology. The incorporation of metal silicides in a MOSFET has a principal purpose of reducing the parasitic resistance of the three terminals of the MOSFET. Since silicides meet the basic requirements for contact metallization (i.e., low specific resistivity, low contact resistance to both p-type and n-type Si, good thermal stability, good processibility and excellent process compatibility with standard Si technology), they have been an important part in today’s electronic devices [58,59]. The SALICIDE technology is a key technology for fabrication of SB S/D MOSFETs as well. In this chapter, the key issues in the SALICIDE technology are first discussed leading to some guidelines for the selection of silicide candidates for SB S/D. The development for both Ni- and Pt-SALICIDE processes is then presented. A combination of the SALICIDE processes with the STL technology described in the preceding chapter leads to the fabrication of NiSi$_x$ and PtSi$_x$ NWs of satisfactory electrical performance for their integration in FinFETs with nanowire-Fins. The discussion will refer to the results in Papers I to IV.

5.1 SALICIDE technology and key issues

A key point of the SALICIDE technology is to form a same kind of metal silicide simultaneously in the gate and source/drain regions. The commonly used SALICIDE process [60] is illustrated in Fig. 5.1. After the MOSFET structure with the three terminals and SiO$_2$ isolation is defined, a metal layer is deposited over the whole structure (a). A thermal annealing induces the formation of silicide in the area where the metal is in direct contact with Si (b). An additional annealing step is often needed to convert the silicide from one phase to another with better conductivity or stability after the selective removal of the unreacted metal (c). The most important contribution of the process is that it renders masking unnecessary, hence is termed self-aligned. The implementation of the SALICIDE technology greatly simplifies the device process, enables the possibility of using extremely thin oxide gate spacers which in turn greatly decreases the series source/drain resistance.
Figure 5.1. Schematic process flow of the SALICIDE technology: a) deposition of a metal layer after the MOSFET structure with the three terminals and SiO₂ isolation are defined, b) thermal anneal to induce silicide formation in the areas where the metal is in direct contact with Si, c) a further annealing to induce transformation of the silicide to a phase of lower resistivity after the selective removal of unreacted metal.
A list of basic requirements for the selection of the formed silicide has been discussed in the literature. In short, the silicide should have the following properties [61]:

1. High conductivity;
2. Low contact resistivity to both types of heavily doped Si;
3. Good chemical stability in contact with Si;
4. Satisfactory thermal and mechanical properties with reference to Si;
5. Satisfactory thermal stability with regard to the morphology;
6. Compatibility with standard Si processing technology including cleaning and etching;
7. No excessive thermal treatments compared to earlier process steps;
8. No detrimental contamination that will affect device performance.

Complementary to these requirements, some other key issues concerning the SALICIDE process can be identified [60-62] as shown in Fig. 5.2. They can be summarized as three main groups:

1) **on the gate:** phase formation in small-dimension features; morphological stability of silicide/poly-Si gate stack; integrity of the gate oxide.

*Figure 5.2. Major process-induced reliability issues with SALCIDE [57].*
2) **on the source/drain**: phase formation in small-dimension features; contact resistance between silicide and source/drain Si; integrity of the source/drain junctions.

3) **between gate and source/drain**: integrity of the gate spacer; bridging effect causing electric shorts between the electrodes.

### 5.2 Choice of silicide for SB S/D

TiSi$_2$, CoSi$_2$ and NiSi have been the three most frequently used contact materials for CMOS devices [62]. The migration from TiSi$_2$ to NiSi is a result of the technological advancement and consequent requirements on contact metallization [61-62]. TiSi$_2$ has been commonly used in earlier CMOS technology generations for contact metallization as well as for local interconnection [63]. But the use of TiSi$_2$ becomes problematic when the gate length is scaled down to 0.2 µm and below [61,62,64]. The problem arises from the difficult nucleation and formation of the desired low-resistivity C54-TiSi$_2$ from its precursor phase C49-TiSi$_2$ [65,66]. Phase C54 is thermodynamically stable and has a resistivity of 15-20 µΩ cm, whereas phase C49 is metastable with a resistivity 4-5 times higher. Kinetically, phase C49 forms as a result of the interaction between Ti and Si typically around 700 °C. The phase transition from C49 to C54-TiSi$_2$ is nucleation-controlled since the free energy change (driving force) is very small [67]. This leads to a low density of C54 nuclei within the C49 background [64,68] and incomplete C49-C54 transformation in narrow Si gates. Thus, a drastically increased line resistance in narrow gates below 0.2 µm has been frequently reported [60]. This effect has been referred to as fine-line effect. Consequently, the temperature for the C49-C54 transformation rapidly increases from about 750 °C to above 900 °C with decreasing gate length. Furthermore, the risk of bridging over the spacers between the gate and the source/drain terminals is persistent since the Si is the diffusion species during the TiSi$_2$ formation [60]. CoSi$_2$ turns out to be advantageous for gate length below 0.2 µm [69]. Recent results, however, show a steep increase of the line resistance when CoSi$_2$ is formed in Si gates below 40 nm [70]. More serious concerns about using CoSi$_2$ are related to the high temperature process (typically above 750 °C), oxygen contamination, Si consumption during silicidation, void formation, and interface roughness [71-73]. The presence of Ge in the materials system will further worsen the formation of CoSi$_2$ [61,62].
Chapter 5. Self-Aligned Silicide Technology

1) NiSi

The formation of NiSi has been known to be well-behaving meaning that it is controlled by diffusion in a layer-by-layer planar growth fashion [74]. It is therefore anticipated to replace CoSi$_2$ for technology nodes beyond 70 nm [60]. NiSi has a slightly lower resistivity (10-15 \( \mu \Omega \) cm) than both C54-TiSi$_2$ and CoSi$_2$ (15-20 \( \mu \Omega \) cm). It has a higher efficiency in using Si for its formation; the thickness ratio of formed silicide to the consumed Si is 0.97, 1.10 and 1.21 for CoSi$_2$, C54-TiSi$_2$ and NiSi, respectively [75,76]. This is an important consideration for devices with ultra-shallow junctions, on SOI substrates or FinFETs where the amount of Si available for silicidation is limited. The diffusion-controlled growth makes the NiSi formation much easier in narrow gates than CoSi$_2$ and TiSi$_2$ [60]. In fact, the line resistance has been found to decrease in narrow gates [60,70] because Ni is more mobile than Si during the formation of all Ni-silicides [77]. The main concern related to the use of NiSi is the relatively poor thermal stability. Two phenomena are related to this stability issue. One concern is the transformation of the low-resitivity NiSi to the high-resistivity NiSi$_2$ above 700 \( ^\circ \)C [77] in the presence of excess Si, since NiSi$_2$ is thermodynamically stable with Si. Another concern is the morphological instability of NiSi thin films that can agglomerate at 600 \( ^\circ \)C [78].

Since the formation of NiSi occurs at rather low temperatures (below 500 \( ^\circ \)C), its SALICIDE process can be simplified by skipping the second annealing in Fig. 5.1(c). In order to improve the control of the growth of NiSi especially to avoid non-uniform formation in narrow gates, a two-step annealing process can be employed in the Ni-SALICIDE process [79]. Here, the first annealing is performed at a much lower temperature, typically 260-310 \( ^\circ \)C, to induce the formation of Ni$_2$Si (growth also diffusion-controlled), whereas the second annealing typically at 450-500 \( ^\circ \)C leads to the transition of Ni$_2$Si to the NiSi phase.

These properties of Ni-SALICIDE make NiSi our choice in this thesis work where a proper silicidation of the fabricated SiNWs is critical. In Papers II and III, silicidation of SiNWs fabricated by means of the STL technique is studied with one-step annealing (cf. Fig. 5.1). The cross-sectional TEM micrograph for the thinnest SiNWs for the Ni-SALICIDE study is shown in Fig. 5.3. This SiNW has a tapered cross-section and measures 32 nm in height (determined by the Si layer thickness) and 17-25 nm in width (determined by the thickness of the SiN$_x$ spacer). The SALICIDE process is simple and straightforward with a wet selective
Figure 5.3. Cross-sectional TEM image of one of the thinnest SiNWs studied for SALICIDE, with a 20-nm thick Ni film deposited on the surface (also see Paper III).

etch to strip the unreacted Ni in $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2=4:1$ for 10 min, after the silicidation at 450 °C for 30 s.

Using SiNWs of different cross-sectional dimensions in combination with adjusting the thickness of the deposited Ni layers, we were able to study the formation as well as electrical properties of polycrystalline NiSi-, Ni$_2$Si- and Ni$_{31}$Si$_{12}$-NWs. since they were directly accessible electrically through the leads and pads formed simultaneously with the NWs. These polycrystalline Ni-silicide NWs were found to be of high conductance with a resistivity of $13\pm2$, $25\pm1$, and $60\pm2$ $\mu\Omega$cm for the NiSi, Ni$_2$Si, and Ni$_{31}$Si$_{12}$ NWs, respectively. The Ni-silicide NWs were further found to be electrically robust since they could support a remarkably high current density despite their polycrystalline nature. The maximum current density that the nanowires could carry immediately prior to their breakdown was $1.6\times10^8$, $1.2\times10^8$, and $8\times10^7$ A/cm$^2$ for the NiSi, Ni$_2$Si, and Ni$_{31}$Si$_{12}$ NWs, respectively. The details of these results are presented in Paper II.

In an effort to examine the robustness of the Ni-silicide NWs, we discovered that the Ni$_2$Si-NWs could display an extraordinarily low wire resistivity of 10 $\mu\Omega$cm after an annealing at 800 °C. Such a drastic decrease in resistivity is attributed to a significant grain growth and a low density of defects in the NWs. Detailed discussions are reported in Paper III.

These properties are promising for Ni-silicide NWs, in particular NiSi-NWs, to be incorporated in NW-FinFETs as the Ni-SALICIDE process remains straightforward for such dimensions and the conductance of the silicide-NWs is high. Therefore, they are not expected...
to impose technological constraints on nano-gate FinFETs such as introducing a high series resistance to the NW Fin-extensions of the S/D electrodes. An added advantage with the Ni-SALICIDE process is the potentially widespread use of NiSi in CMOS technology.

2) PtSi

Although PtSi was one of the first metal silicides studied for Schottky contact in Si technology [61], it has not attracted so much attention as TiSi$_2$, CoSi$_2$ and NiSi for contact metallization in CMOS devices. PtSi has a relatively high resistivity of 30-40 $\mu$Ωcm and a high Schottky barrier of about 0.9 eV to electrons [75]. This latter property makes it unfavorable for Ohmic contact to $n$-type Si. But it is almost ideal as the SB S/D for $p$-channel SB-MOSFETs. In a SB-MOSFET, the resistivity of PtSi should not be a major concern since it is much lower than that of heavily doped Si in the S/D extension of a conventional MOSFET. As a result, PtSi has attracted an increasing attention for its application as the contact material in a $p$-channel SB-MOSFET, also because of its rather low formation temperature, low reactivity towards SiO$_2$ and high efficiency in using Si for it formation (with a thickness ratio of 1.44 for the the formed PtSi to the consumed Si) [80-83]. $p$-channel SB-MOSFETs featuring PtSi S/D have already been demonstrated with promising device performance [84,85]. Integration of PtSi SB S/D has further been shown in $p$-channel MOSFETs fabricated on UTB-SOI [31] or with as the ‘Fin’-extensions in FinFETs [86].

Our attention to PtSi is further based on its formation kinetics. Similarly to the formation of NiSi, the growth of PtSi is diffusion controlled occurring at rather low temperatures [75]. In addition, the Pt atoms are quite mobile during the silicidation; Pt is the dominant diffusion species in the formation of Pt$_2$Si and it is comparably mobile as Si in the formation of PtSi [75]. With sufficient atomic mobility of Pt atoms during the silicidation, the concern with a severe underlap between the silicide front and the gate edge as discussed in Chapter 3 should be lessened. Therefore, efforts have been devoted to the development of a SALICIDE process for PtSi in this thesis.

A critical problem with the Pt-SALICIDE process lies in the selective wet etching to strip unreacted Pt, since the etch solution used, aqua regia, also aggressively attacks Pt-silicides, PtSi$_x$ [82,87]. The most commonly used method to achieve a selective etching is to grow the PtSi$_x$ in an oxidizing atmosphere as shown in Fig. 5.4. During the formation of PtSi$_x$, a SiO$_x$
or PtSiO\textsubscript{y} layer forms between the growing silicide and the remaining Pt. The oxide or silicate formation is facilitated by oxygen diffusion through the unreacted Pt. This SiO\textsubscript{x} or PtSiO\textsubscript{y} layer becomes an effective protection for the silicide layer during the subsequent wet etch in aqua regia, Fig. 5.4(a)-(c) [82]. But the presence of oxygen strongly affects the silicide formation by slowing down the reacting process between Pt and Si [88]. The formation of SiO\textsubscript{x} or PtSiO\textsubscript{y} layer also hinders further growth of the silicide layer [89] leaving behind some unexpected Si as schematically shown in Fig. 5.4(d)-(e). All these make the process unlikely to be easily scalable in thickness. This difficulty can become particularly problematic for device structures where the amount of Si is limited such as in UTB-SOI or SiNW-Fins. So a highly scalable SALICIDE process with a thin starting Pt film is desired for these kinds of device structures.

In this thesis work, a simple, robust and reliable self-aligned PtSi\textsubscript{x} process is developed (see Paper IV). The process is schematically shown in Fig. 5.5. The key idea with this process is to have the silicide formation and surface oxidation as two consecutive steps, but still in a single run. So, the silicidation step carried out in N\textsubscript{2} ensures a controllable formation of PtSi\textsubscript{x}. The oxidation step in O\textsubscript{2} generates a reliable protective SiO\textsubscript{x} layer for the grown PtSi\textsubscript{x} layers. By separately addressing silicidation and oxidation in two consecutive steps, as opposed to letting them occur simultaneously as done in the past, the novel Pt-SALICIDE process is easily scalable in terms of the initial Pt thickness as well as of the final PtSi\textsubscript{x} thickness. This also leads to a controllable formation of different Pt-silicide phases. The fine tuning of the oxidation conditions is discussed in Paper IV.

The robustness and scalability of the process is finally confirmed by silicidation of SiNWs defined by means of STL. Pt\textsubscript{2}Si- and PtSi-dominating NWs were obtained by adjusting the initial Si-Pt ratio. They were found to have a quite decent resistivity of 26±3 and 34±2 µΩ\textsubscript{cm} for the Pt\textsubscript{2}Si- and PtSi-dominating NWs, respectively, in good agreement with the corresponding data of both silicides in their thin-film forms (28-38 µΩ\textsubscript{cm} for PtSi and 29±10µΩ\textsubscript{cm} for Pt\textsubscript{2}Si) [82,90,91]. More experimental data about the Pt-silicide NWs are found in Papers I and IV.
Chapter 5. Self-Aligned Silicide Technology

Figure 5.4. Schematic process flow for the commonly used Pt-SALICIDE process.

Figure 5.5. Schematic process flow for our Pt-SALICIDE process.
Chapter 6. Modification of Schottky Barrier Height

One of the key parameters with a SB-MOSFET is the SBH of the SB S/D junctions. The sum of electron SBH ($\phi_{bn}$) and hole SBH ($\phi_{bp}$) should approximately be equal to the energy bandgap ($E_g$), i.e., $\phi_{bn} + \phi_{bp} \approx E_g$. Increasing $I_{on}$ requires a SBH at the source end as low as possible. This low SBH becomes high when the device is in “off” state yielding a low $I_{off}$, as discussed in Chapter 3 (Fig. 3.2). Theoretical studies have demonstrated that an extremely low SBH (~0.1eV) is needed in order for SB-MOSFETs to outperform conventional MOSFETs with $p-n$ junctions of heavily doped S/D [29, 30]. However, to date, due to undesired high SBH, SB-MOSFETs usually suffer from a low drive current and a large leakage attributed to the drain-to-substrate reverse-biased current [92,93]. Moreover, CMOS technology requires complementary $n$- and $p$-channel SB-MOSFETs. Since no single silicide can meet the low SBH requirement for both conduction polarities, complementary silicides have been investigated using ErSi$_x$ or YbSi$_x$ for $n$-MOSFET [31, 94] and PtSi for $p$-MOSFET [31,95]. However, the process for the formation of complementary silicides is rather complex needing extra lithography steps for implementation of the silicides as discussed earlier in Chapter 3. To circumvent this drawback, SBH-engineering is important for CMOS applications of the SB-MOSFETs. Recent reports indicate that the effective SBHs of metal-Si contacts can be greatly reduced in three different ways by de-pinning the Fermi level through the use of: (1) a thin insulating layer between metal and Si [96], (2) Se and S to passivate the surface states of Si [97,98], or (3) an interfacial dipole to modulate the SBH through the generation of a sheet of highly concentrated dopants confined to the metal-Si interface [99,100]. However, reliably and reproducibly inserting an ultrathin interfacial insulating layer is technologically very demanding for large-scale integration. Surface-state passivation has so far only been shown to lead to a reduced $\phi_{bn}$. In comparison, introduction of an interfacial dipole with dopant-segregation (DS) technology presents a promising approach for SBH modification for both electrons and holes. In this chapter, two different approaches leading to DS for both NiSi and PtSi contacts are presented with reference to the results in Papers V and VI.

6.1 Metal-semiconductor contact

The discussion below refers to a Schottky contact formed on an $n$-type Si substrate. As shown in Fig. 6.1, in an ideal metal-semiconductor system the height of the Schottky barrier formed
between the metal and the semiconductor is simply related to the work function $\phi_m$ of the metal and the electron affinity $\chi_s$ of the semiconductor. The SBH determines the $I$-$V$ and $C$-$V$ characteristics over the Schottky junction. The standard equation relating the current density to the voltage applied across the Schottky contact is [38]:

$$J = J_0 \left( \frac{e^\frac{-\phi'}{kT}}{e^{\frac{\phi'}{kT}} - 1} \right)$$

(6.1)

When the forward bias is not too large, the current transport is assumed to be due to thermionic emission over the effective SBH $\phi'$:

$$J_0 = A'T^2e^{-\frac{\phi'}{2kT}}$$

(6.2)

is the leakage current under any reversed bias. $n$ is the ideal factor which may depend on temperature and is usually greater than unity.
Chapter 6. Modification of Schottky Barrier Height

If the semiconductor of a metal-semiconductor junction is uniformly doped and the junction is reversed biased at $V_r$, the differential capacitance $C = dQ/dV$ is given by [38]

$$C = A \left( \frac{q N_d \epsilon_s}{2} \right)^{1/2} \left( \phi_b - \xi + V_r - \frac{kT}{q} \right)^{1/2}$$ \hfill (6.3)

where $A$ is the area of the contact, and $\xi$ is the difference between the Fermi level and the bottom of the conduction band in the semiconductor bulk as shown in Fig. 6.1. Equation (6.3) is often re-written as

$$\left( \frac{1}{C^2} \right) = \left( \frac{2}{A^2 q N_d \epsilon_s} \right) \left( \phi_b - \xi + V_r - \frac{kT}{q} \right)$$ \hfill (6.4)

$\phi_b$ is normally independent of $V_r$ provided that there is no appreciable interfacial layer. A plot of $C^2$ versus $V_r$ should give a straight line with an intercept $-V_I$ on the horizontal axis equal to $-\left( \phi_b - \xi - \frac{kT}{q} \right)$. The SBH is then given by

$$\phi_b = \xi + V_I + \frac{kT}{q}$$ \hfill (6.5)

Ideally, one could obtain a range of SBH for different applications by selecting metals with desired work function. However, in practice, the spread in SBH is greatly reduced due to Fermi-level pinning (e.g., by interface states) as illustrated in Fig. 6.2 [38]. The continuous distribution of interface states is characterized by a neutral level $\phi_0$. If the interface states are occupied below $\phi_0$, the charge of the interface states $Q_{ss}$ is positive. While the occupancy above $\phi_0$ makes $Q_{ss}$ negative. In the presence of interface states, the electrical neutrality condition is $Q_m + Q_d + Q_{ss} = 0$, where $Q_m$ is the negative charge on the surface of the metal, $Q_d$ is the positive charge in the depletion region of the n-type Si. The occupancy of the interface states is determined by the Fermi level. They are filled up to the Fermi level and empty above it. If $\phi_0$ happens to be above the Fermi level, the surface states contain a net positive charge $Q_{ss} > 0$, then $Q_d$ becomes smaller than that if the $Q_{ss}$ is absent, which means the band bending will also be decreased. The SBH which is equal to the band bending plus $\xi$ will be decreased
as well, which will push $\phi_0$ down towards $E_F$. On the other hand, if $\phi_0$ happens to be below the Fermi level, $Q_s$ becomes negative. $Q_d$ must then be greater, and consequently the SBH is increased and $\phi_0$ is pulled up towards $E_F$. If the density of the surface states becomes very large, the SBH will be pinned and determined by $\phi_b \approx E_g - \phi_0$ independent of the work function of the metal $\phi_m$. This condition is called Fermi lever pinning.

6.2 Shannon diodes

Very few metals have both the appropriate work functions and the necessary metallurgical properties required for device application. So, a convenient method is to select a metal with the most desirable properties for a given device application and then change the SBH between this particular metal and the semiconductor in a controlled way by changing the properties of the interface.

Shannon proposed a technique in the 1970’s [101-103] to determine the interface field and thereby control the effective SBH. It relies on the use of a very thin highly doped surface layer on top of the lowly doped substrate. This highly doped surface layer becomes fully depleted to prevent serious degradation of the reverse characteristics. Such devices are known as Shannon diodes. As schematically illustrated in Fig. 6.3, a highly doped surface layer of the same doping type as in the substrate decreases the effective SBH, while that of an opposite type increases the effective SBH.
6.3 SIDS versus SADS for dopant segregation

A similar technology to that behind the Shannon diodes for introducing an interfacial dipole layer with DS presents a promising approach for SBH modification for both electrons and holes. The employment of the DS technology leads to modulation of the effective SBH by controlling the interfacical electric field with the interfacial dipole. In this thesis, two schemes for the introduction of DS are experimentally studied in Papers V and VI. The pros and cons of these two schemes are discussed in detail in Paper VI.

The interfacial dopants can be introduced either through silicidation induced dopant segregation (SIDS) or using silicide as diffusion source (SADS). Key processing steps are summarized in Fig. 6.4 for SIDS (a) and SADS (b). For SIDS, dopants such as B and As are first implanted into $n$- and $p$-type Si substrate, respectively. The choice of implantation energy is correlated to the target thickness of the silicide layer; it should be kept so low that the entire surface Si with the dopants is consumed by the silicide formation. Since the dopants have low solubility in the silicide layers, they are pushed by the silicide front during silicidation and become accumulated (piled up) at the silicide-Si interface.

For SADS, dopant implantation is performed after the silicide formation. Similarly, $p$-type dopants are implanted into the silicide formed on $n$-type Si substrate whereas $n$-type dopants are implanted into the silicide formed on $p$-type Si substrate to ensure desired modifications.
Integration of silicide nanowires as Schottky barrier source/drain in FinFETs

Figure 6.4. Schematic process flow for schemes (a) SIDS and (b) SADS.
Chapter 6. Modification of Schottky Barrier Height

of the SBHs. The implantation energy should be kept so low that the silicide-Si interface is not damaged and the interface states are not introduced by the implantation. A subsequent drive-in anneal will diffuse the dopants out towards the silicide-Si interface. An advantage with SADS is the separation of silicide formation from dopant segregation, giving an extra freedom to tailor the process for specific needs.

For both silicide systems, the dopant segregation has been found to give rise to a predominant effect leading to an effective SBH>1.0 eV for both polarities \( i.e. \phi_{bn} \) and \( \phi_{bp} \) independent of the original SBHs of PtSi (0.93 eV) and NiSi (0.72 eV). The attained results point to the great potential of dopant segregation in either scheme, SIDS or SADS, for future CMOS technology with SB-MOSFETs [36, 104,105]. Comparing with scheme SIDS, scheme SADS seems to be less efficient in modifying the SBHs with the experimental conditions used in this thesis (i.e., implantation dose, energy and annealing temperature and time). The difference in interfacial concentration of the segregated dopants is an obvious cause. In SIDS the majority of the dopants are always at the silicide/silicon interface, while in SADS the dopants will have to be transported to the interface. By combining these two schemes, a more robust technology of dopant segregation could be anticipated for nanoscale SB-MOSFETs.
Integration of silicide nanowires as Schottky barrier source/drain in FinFETs
Chapter 7. SB-MOSFETs: Fabrication and Characterization

Following the introduction of some of the key technologies developed for the fabrication of nanoscale SB-MOSFETs in the preceding chapters as well as in the associated papers appended at the end, this chapter describes their integration towards competitive SB-MOSFETs. Some key issues related to the process integration are first discussed. Attention is then turned to the fabrication and characterization of the SB-MOSFETs on UTB-SOI substrates with two complementary approaches for SBH modification with DS technique. The results in Paper VII are referred to for comparison. The chapter is concluded with demonstration of SB S/D FinFETs based on the experience from the UTB-SOI devices as well as with identification of key challenging issues for extremely scaled FinFETs, with reference to Paper VIII.

7.1 Key issues related to the process integration

1) Methods for nanowire fabrication. The nano-gate and Fin-channel of a nanoscale MOSFET can be defined by conventional optical lithography with a light source at 193 nm wavelength combined with pattern reduction as done in the industry [106], EBL [37,107], or STL [36,108-113]. As the STL technology automatically yields twin-Fin channels if unless otherwise is wished, it leads to doubling of the drive current for a given lithography pitch. Furthermore, ultimate NW-Fins with much better uniformity can be obtained by means of STL in comparison with EBL or dimensional reduction by ashing [108,111]. Based on these advantages and the process capability of our cleanroom lab, the STL process is employed for the fabrication of nanoscale SB-MOSFETs.

2) Selection of silicides. Ni-silicides, NiSi, have been very well studied, and rich experience in integrating NiSi into the conventional devices has been gained at our lab. However, an aggressive lateral growth of NiSi by up to 600 nm into the channel region which is detrimental especially for short-channel devices fabricated on UTB-SOI was found [114]. Since Ni is more mobile than Si during the formation of all Ni-silicides [77], lateral encroachment of NiSi into the channel region is expected in this kind of structures where the amount of Si in the S/D regions is limited and the amount of deposited Ni is in excess. With
the lack of a reliable low temperature annealing process below 500 °C at our lab, we have been unable to control the lateral growth of NiSi₅. Furthermore, the poor thermal stability of NiSi (typically 550-600 °C for NiSi agglomeration on Si to occur) is another concern for the incorporation of dopant-segregation technique especially SADS. Based on these considerations, PtSi is chosen for our SB-MOSFET fabrication.

3) **Methods to modify effective SBH.** A low SBH is crucial for good device performance of SB-MOSFETs. The process to form complementary silicides with appropriate SBHs, one silicide for p-MOSFET and another for n-MOSFET is rather complex requiring additional process steps. The SBH modification technique via DS can be easily integrated into the device process flow for SB-MOSFETs when appropriate dopants are chosen for both types of devices. The DS could be introduced by two different schemes: SIDS and SADS. Scheme SIDS presents a relatively simple process. However, the silicidation process is known to be dependent on the type and concentration of dopant. PtSi thin films obtained with SIDS were investigated by both TEM and sheet resistance measurements as shown in Fig. 7.1. As seen, As I/I before silicidation greatly affects the grain size and the sheet resistance of the resulting PtSi films. In comparison with the reference without I/I or the sample with B I/I, the grain size is about half and the sheet resistance nearly doubles. Furthermore, implantation damage prior to Pt deposition in Si substrate could cause undesired rapid diffusion of dopants especially B during silicidation at 500-600 °C. Additionally, the cross-sectional TEM micrographs in Fig. 7.2 clearly show uncontrollable lateral growth of PtSi into the channel.

![Figure 7.1](image)

*Figure 7.1. Plan-view TEM micrographs of PtSi thin films fabricated with scheme SIDS. Average grain size measured for a) 40 nm without implantation, b) 42 nm with B I/I, and c.) 22 nm with As I/I.*
region with the dopant I/I. The length of the lateral growth not only is different among the
different devices with and without the B or As I/I, but also displays appreciable asymmetric at
the left and right PtSi/Si contacts. To address these adverse effects, scheme SADS was chosen
for our SB-MOSFET fabrication by arranging silicidation and dopant incorporation as two
separate process steps.

4) Formation of slim gate spacers. As discussed in Chapter 3, a slim gate spacer is also
critical for the SB-MOSFET fabrication. The gate underlap is affected by the gate sidewall
spacer thickness $t_{SW}$ as well as the extent of the silicide lateral growth. A thin sidewall spacer
helps design the process parameters for control and minimization of the S/D-to-gate underlap.
In this way, the SB junctions at the S/D regions are better controlled by the gate electrode as
discussed in Chapter 3. We aimed at a $t_{SW}$ around 10 nm for process controllability. The
development of the slim spacer process was done with a 20-nm thick poly-Si deposited on
oxidized Si substrates to mimic SOI substrates. After gate stack formation with a 140-nm
thick poly-Si on top of a 3-nm thick thermal oxide, dry oxidized at 750 °C was carried out to

Figure 7.2. Cross-sectional TEM micrographs of the central part of a fabricated PtSi
S/D SB-MOSFETs with SIDS scheme. The PtSi edges are marked by the arrows.
Integration of silicide nanowires as Schottky barrier source/drain in FinFETs

Figure 7.3. Cross-sectional TEM micrograph of one side of a gate structure with a slim gate spacer composed of a bilayer of Si$_3$N$_4$/SiO$_2$.

form a 5-nm oxide around the poly-Si gate. A 10-nm thick LPCVD Si$_3$N$_4$ layer was then deposited at 720 °C. A reactive ion etch (RIE) step with an etch rate of about 5 Å/min removed the surface Si$_3$N$_4$. This left the Si$_3$N$_4$/SiO$_2$ gate spacers by the two gate sidewalls shown in Fig. 7.3 with the cross-sectional TEM micrograph of a prepared sample. The formed Si$_3$N$_4$/SiO$_2$ spacers were then qualified by applying the Pt-SALICIDE process. To do this, the thermal oxide on top of the S/D and the gate was first etched in HF, followed by using our standard Pt-SALICIDE process described in Chapter 5 and Paper III. The formation of PtSi in the three terminal regions is successful without electric short between them.

7.2 SB-MOSFETs on UTB-SOI

MOSFETs of both polarities with PtSi-based Schottky-barrier source/drain have been fabricated on UTB-SOI with details reported in Paper VII. A brief overview of the device fabrication process is provided as follows.

The device fabrication started with lightly $p$-type doped ($N_a=1\times10^{15}$ cm$^{-3}$) SOI wafers with a surface Si layer of 400-nm thickness. The surface Si layer was thinned to 20 nm by sequential thermal oxidation and oxide removal. After mesa isolation, a 2.8-nm thick gate oxide was
grown, followed by the deposition of a 150-nm thick in situ phosphorous doped Si (IDP) as the gate electrode. The gate electrode was defined, with assistance of dry etching, by a combination of optical lithography to define normal gates and STL to define 70 nm long gates, see details in Paper I. This led to simultaneous generation of gate lengths ranging from 0.35 to 50 μm along with the 70 nm long nanoscale gates. Slim gate spacers described earlier were created. For the formation of Schottky barrier S/D, PtSi was first formed in the S/D regions (as well as on the gate) using the Pt-SALICIDE process. Boron and As were then implanted into the PtSi for the p- and n-MOSFETs, respectively. The implantation dose was $1 \times 10^{15}$ cm$^{-2}$, at 2 keV for B and 10 keV for As. Rapid thermal annealing at 700 °C for 30 s was carried out for inducing dopant segregation. Control samples without dopant implantation were also processed. The device fabrication was completed with Al-metallization followed by forming gas annealing at 400 °C for 30 min.

In Paper VII, the formed PtSi was found, by means of cross-sectional TEM, to be confined in the source/drain regions without lateral silicide growth under the gate spacers. The PtSi/Si interface was further found to be about 15 nm away from the foot of the 15-nm thick gate spacer, leading to a 30-nm underlap between the PtSi front and the gate edge. The presence of the underlap apparently considerably weakened the gate control of the Schottky barrier of the PtSi/Si contacts and gave rise to an inefficient carrier injection at the source end. As a result, low drive currents for both types of the MOSFETs without DS were measured. The DS attempt by means of SADS was found efficient for both types of devices with an on/off current ratio exceeding $10^6$.

However, a more systematic investigation of the PtSi formation in the S/D regions revealed a varying underlap/overlap between the PtSi front with respect to the gate. This investigation is summarized in Paper VIII in order also to interpret the observation of a large fluctuation of the device performance of SB-FinFETs.

In Paper VII, a large $V_T$-shift was found for the p-MOSFET with DS as compared to that without. Counter doping of the $n^+$ poly-Si gate by implanted B can be ruled out as the cause for the $V_T$ shift. Since the implantation energy was so low that the implanted B atoms were mostly confined in the PtSi film on top of a rather thick $n^+$ poly gate (about 110 nm after silicidation). In addition, the drive-in anneal was carried out at rather low temperature (700 °C). Under these experimental conditions used, the length for massive B diffusion in poly-Si
is estimated to be 10 nm, assuming a diffusivity 10000 higher than B in single crystal Si [115]. Massive B diffusion is needed in order to counter dope the \(n^+\) poly-Si with a concentration well exceeding \(10^{20} \text{ /cm}^3\). Furthermore, should massive B diffusion in the poly-Si gate occur for unknown reasons, one would expect to see a \(V_T\)-shift independent of gate length. As shown in Fig. 7.4, the variation of \(V_T\) with gate length for both \(p\)- and \(n\)-MOSFETs is shown. Two observations can be made with the \(p\)-MOSFETs. First, the \(V_T\) does change with gate length. Second, the \(V_T\) (absolute value) decreases with decreasing gate length. Thus, counter doping of the \(n^+\) poly-Si by B I/I is unlikely to be the reason for the \(V_T\) shift.

The \(V_T\) decrease with decreasing gate length prompts an explanation of the \(V_T\) shift as being primarily caused by the activation of some of the laterally spread B (originated from I/I) in the channel region but close to the vicinity of the S/D ends. The B ions do straggle in the lateral direction during I/I. Furthermore, it is likely that some of the laterally spread B atoms became activated during the drive-in anneal at 700 °C. However, the activated B concentration could not become so high that a normal \(p-n\) junction S/D would form. To confirm this, we made a simple test by measuring the \(I_d-V_g\) characteristics of a \(p\)-MOSFET at positive drain bias. It is seen in Fig. 7.5 that \(I_d\) increases with increasing gate bias at positive gate voltage. This increase is caused by the electron conduction, which can only be observed in a \(p\)-type MOSFET with SB S/D. Hence, from the strong ambipolar conduction behavior, we are led to conclude that the S/D junctions of the \(p\)-MOSFETs after the dopant incorporation are still dominantly SB junctions.

\[\text{Figure 7.4. } V_T \text{ vs. gate length for the SB-MOSFETs with DS.}\]
As for the $n$-MOSFETs, the lateral straggling of As ions is much less pronounced compared to B during I/I. Those that did spread towards the channel should mostly remain electrically inactive since the rapid thermal annealing for drive-in was performed at 700 °C. That no obvious $V_t$ shift can be found in the Fig. 7.4 also confirms this suggestion.

Finally, the 70-nm gate-length SB-MOSFETs with the PtSi S/D were also successfully fabricated by using the STL technology. The cross-section TEM micrograph of such a gate structure is shown in Fig. 7.6.

Figure 7.5. $I_d$-$V_g$ of a p-MOSFET with $L_g$=0.35 μm at opposite drain-bias.

Figure 7.6. Cross-sectional TEM micrograph of the central part of a fabricated MOSFET with a 70-nm gate defined by means of the STL technology.
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The DS is also found to be effective for both polarities of devices as their device characteristics indicate in Fig. 7.7. The effect of the activation of laterally spread B becomes even more serious for the 70-nm gate p-MOSFET as shown in Fig. 7.7(a), as expected. By reducing the temperature of the drive-in anneal for the p-MOSFET from 700 to 500 °C, this problem was partially addressed as evidenced in Fig. 7.8 with a much smaller $V_t$ shift and a much better control of SCE.

![Figure 7.7](image1.png)

Figure 7.7. $I_d-V_g$ for SB-MOSFETs of $L_g=70$ nm with and without DS, for (a) p-type and (b) n-type devices.

![Figure 7.8](image2.png)

Figure 7.8. $I_d-V_g$ for p-channel SB-MOSFETs of $L_g=70$ nm with and without DS, where the drive-in anneal was performed at 500 °C to reduce the activation of laterally spread B.
Chapter 7. SB-MOSFETs: Fabrication and Characterization

7.3 SB-FinFET fabrication

Motivated by the success of SB-MOSFETs on UTB-SOT substrates with gate length down to 70 nm, the attention is now turned to the fabrication and characterization of SB-FinFETs. The process for fabricating the SB-FinFETs is rather similar to that for the UTB-SOI devices, except for the use of the STL technology twice, first for the definition of the Fin-channels and second for the definition of the 70-nm gates. To address the problem with activation of laterally spread B as discussed above, As was first implanted and driven-in at 700 °C for the n-channel FinFETs. Then, B implantation was carried out followed by a drive-in anneal at 500 °C for the p-channel FinFETs. Control samples without dopant implantation were also processed. The major process steps of the process flow are summarized as below:

- Thinning SOI to 27-nm thickness
- Defining 35 nm wide Fin-channels using the STL process
- Gate oxide growth and gate poly-Si deposition with a 150-nm thick IDP layer
- Defining 70 nm gates perpendicular to the Fin-channels with a second STL process
- Formation of 15-nm slim spacers
- PtSi formation ≤600 °C
- As I/I into PtSi for n-type devices: dose 1×10^{15} cm^{-2}
- Drive-in anneal at 700 °C/30 s
- B I/I into PtSi for p-type devices: dose 1×10^{15} cm^{-2}
- Drive-in anneal at 500 °C/30 s
- Metallization
- Forming-gas annealing

The top-view HR-SEM picture of a fabricated FinFET is shown in Fig. 7.9. The fabricated device has two Fins (channels) in parallel. A 70-nm long gate lies perpendicularly on top of the Fin-channels. The cross sectional TEM micrograph of the channel-Fin structure along the NW gate, line A-A’ in Fig. 9, is shown in Fig. 7.10(a), while that of the gate structure along the NW-Fin, line B-B’ in Fig. 9, is depicted in Fig. 7.10(b). From the TEM pictures, the
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Figure 7.9. High-resolution top-view SEM of a fabricated FinFET with double-Fin channels.

Figure 7.10. Cross-sectional TEM micrographs of (a) the Fin-channel and (b) the gate structure of a fabricated FinFET using the STL technology.
following data are obtained: the Fin-width ($W_f$) is 35 nm, the Fin-height ($T_{si}$) is 27 nm, the gate oxide is 2.8 nm thick, and the gate spacer ($t_{sw}$) is 10 nm wide. In addition, the gate length is 70 nm, identical to that in the UTB-SOI devices.

The effect of DS on device performance is evident for $p$-channel SB-FinFETs as shown in Fig. 7.11. The DS is found to be quite effective with an increase of the drive currents by more than 5 times as compared to the device without DS. Overall, the Tri-gate FinFET here shows a better control of SCE in comparison with their single-gate planar MOSFET realized on UTB-SOI. Finally, for the device with DS, the drain-induced barrier lowering (DIBL) is about 100 mV/V.

In Fig. 7.12, the output characteristics $I_d-V_d$ of the $p$-channel SB-FinFET with DS are shown. The observed ‘sublinear’ phenomenon is well known for planar SB-MOSFETs in linear region. This is often due to too high a Schottky barrier and/or too large a gate underlap ($t_{sw}$). As shown in Fig. 7.12, the sublinear behavior remains pronounced even for the SB-FinFET with DS. As seen in Fig. 7.10(b), the formed S/D PtSi shows no lateral growth under the gate spacer. As a result, a 16-nm underlap between the PtSi front and the gate edge is present. This 16-nm gate underlap is suggested to be the dominant reason for the sublinear behavior, as this underlap region is a lightly doped SiNW giving rise to a large series resistance.

![Figure 7.11: $I_d-V_g$ for $p$-channel SB-FinFETs with and without DS.](image-url)
However, a large spread in device performance was found for identical devices as discussed in Paper VIII. For reasons not yet known, our attempt with $n$-channel SB-FinFETs failed. More work is needed to identify the causes responsible for the malfunction in order for $n$-channel SB-FinFETs to reach the desired performance.
Chapter 8. Summary, Conclusions and Future Perspectives

As the dimension of CMOS devices is scaled down to several tens of nanometers in gate-length, FinFET with multiple gates presents an effective solution to controlling the short channel effect. The Schottky barrier source/drain technology has been discussed as the most promising solution to reducing the parasitic series source/drain resistance for nanowire-Fins surrounded by multiple gates. This thesis has a focus on examining the technological challenges in integrating Schottky barrier source/drain in FinFETs. For this purpose, a robust sidewall transfer lithography technology has been developed for routine fabrication of SiNW-Fins in a controllable manner. A scalable self-aligned silicide process dedicated to the PtSi formation has also been developed. The major results of this thesis are summarized below:

1. The STL technology has been developed to allow routine production and characterization of SiNWs. The smallest SiNWs fabricated measure 15 nm by 15 nm in cross-sectional dimension.

2. The scalable SALICIDE process for PtSi has been developed. It comprises two consecutive annealing steps in a single run. By adequately adjusting the annealing steps, a protective SiO layer forms on PtSi of different thicknesses and compositions. This SiO hard-mask allows selective wet etch of Pt for the self-aligned process.

3. Directly accessible, ultralong and uniform NWs of NiSi and PtSi have been mass-fabricated. The silicide NWs are characterized by resistivity values comparable to those of their thin–film counterparts. Furthermore, despite the polycrystalline nature the silicide NWs are able to support an extremely high current density up to $\sim 10^8$ A/cm². An additional annealing of the Ni$_2$Si NWs at 800 °C induces a significant grain growth along the NWs and leads to an extraordinarily low wire resistivity of 10 μΩcm.

4. An experimental study of dopant segregation at the PtSi/Si and NiSi/Si interfaces has led to substantial SBH modifications. Two complementary schemes SIDS and SADS are compared in terms of efficiency of dopant segregation and resultant SBH modification. The achieved
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results of SBH>1.0 eV for both polarities (i.e. $\phi_{bn}$ and $\phi_{bp}$) by means of SIDS and/or SADS are encouraging and promising for future CMOS technology with SB-MOSFETs.

5. SB-MOSFETs with PtSi of both polarities have been fabricated in UTB-SOI. PtSi that is usually used for $p$-channel SB-MOSFET is studied as the SB S/D for both types of transistors. Through DS with appropriate dopants using the SADS process, i.e., B for $p$-type SB-MOSFET and As for $n$-type SB-MOSFET, excellent performance has been achieved for both types of SB-MOSFETs.

6. Finally, integration of PtSi NWs in FinFETs has been carried out by combining the STL technology, the self-aligned PtSi$_x$ process and the DS technology, all developed during the course of this thesis work. The FinFETs have a gate length of 70 nm, a Fin width of 35 nm and a Fin height of 27 nm. Dopant segregation with B improves the performance of the $p$-channel FinFETs with an increase of the drive current by more than 5 times. The FinFETs further show a good control of short channel effects with a drain-induced barrier lowering (DIBL) about 100 mV/V.

Looking down the road, much more needs to be done in order to realize a truly successful integration on the FinFET platform with NW-Fins of several nanometers in diameter. Some of the needed efforts are suggested below:

1. The line edge roughness of the fabricated SiNW-Fins should be reduced below 1 nm, possibly by using another support material (for example, $\alpha$-Si) than SiGe.

2. The etched sidewall in the SiGe support shown in Fig. 4.4 is far from perfectly vertical. This imposes a severe challenge to realizing thin SiNW-Fins below 10 nm. Process fine-tuning including replacing the SiGe support with another material and using hard-mask for the various dry etches will be required.

3. Extensive experiments are required to also make the DS technology work for $n$-channel SB-FinFETs.

4. The morphology of the silicide/Si channel interface needs to be studied for understanding and control of the silicide lateral growth in order to optimize the overlap/underlap between the silicide in the source/drain regions and the gate electrode.
References


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