Design and Calibration of integrated PLL Frequency Synthesizers

FREDRIK JONSSON

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Abstract

Thanks to its ability to generate a stable yet programmable output frequency, Phase Locked Loop (PLL) frequency synthesizers are found in most modern radio transceivers. All practical PLL implementations suffer from unwanted frequency components such as phasenoise and spurious tones, and since these components affect system performance they must be predicted and minimized.

This thesis discuss the design and implementation of fully integrated PLL circuits. Techniques to predict system performance are investigated. The strongly non-linear operation of PLL building blocks are analyzed, using both analytical and numerical methods. Techniques to reduce impact of interferer down-conversion and noise folding are suggested. Methods to perform automatic calibration in order to make circuits less sensitive to process variations are proposed. The techniques are verified through a number of PLL implementations.

The design and implementation of a transceiver targeting a dual band IEEE 802.11 a/b/g wireless LAN operation is discussed. The circuit use two PLL:s operating at 1310 to 1510 MHz and 3.84 GHz respectively. Noise contributions of various PLL building blocks and their impact on over all system performance are analyzed. The combined integrated phase noise is below -34 dBC, and measured transceiver Error Vector Magnitude (EVM) is better than 2.5 dB in both the 2.4 and 5 GHz bands.

A low power frequency synthesizer targeting Frequency Shift Keying applications such as ZigBee and BlueTooth is presented. The synthesizer use open-loop direct modulation of the carrier, but unlike conventional implementations, the proposed synthesizer is open both when transmitting and receiving data. This allows the use of a small area on-chip loop filter without violating noise or spurious requirements. To handle the frequency drift normally associated with open-loop implementations, a low-leakage charge-pump is proposed. The synthesizer is implemented using a 0.18μm CMOS process. Total power consumption is 9 mW and the circuit area including the VCO inductors and on-chip loopfilter is 0.32mm2. Measured leakage current is less than 2 fA.

A small area amplitude detector circuit is proposed. The wide-band operation and small input capacitance make the circuit suitable for embedding in an RF system on-chip, allowing measurement of on-chip signal levels and automatic calibration.

Finally an oscillator topology reducing the phase noise in voltage controlled oscillators is suggested. By using on-chip decoupling and an amplitude control circuit to adjust oscillator bias, the impact of current source noise is eliminated. The theoretical phase noise is reduced 3.9 dB compared to a conventional LC oscillator using the same bias current.