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Low Loss Submodule Cluster for Modular Multilevel Converters Suitable for Implementation with SiC MOSFETs

Keijo Jacobs, Stefanie Heinig, Baris Ciftci, Staffan Norrga and Hans-Peter Nee

Electric Power and Energy Systems

KTH Royal Institute of Technology

Stockholm, Sweden

keijoj@kth.se

Abstract—In this paper, a novel submodule cluster topology for modular multilevel converters is proposed. The cluster is composed of an arbitrary amount of submodule segments. Depending on the amount of capacitors in the cluster, the converter conduction losses can be reduced significantly. The topology enables electronic protection against explosion, thus, reducing the requirements for submodule bypass equipment. Implications for the converter operation and functionality are investigated and a wireless control scheme is proposed.

Index Terms—Modular multilevel converters, Silicon carbide, HVDC transmission

I. INTRODUCTION

Modular multilevel converters (MMC) have given a push to high-voltage direct current (HVDC) transmission systems and triggered research interest in related topics, such as converter topologies, dc-breakers, and HVDC protection. The advantages of the MMC are its modularity, scalability, redundancy, low losses, and good harmonic performance. The MMC consists of two converter arms per phase which act as variable voltage sources. The arms employ a number of converter submodules and an arm inductor. The converter submodules consist of a certain number of active power semiconductors and capacitors. The capacitors can be either bypassed or inserted into the current path in order to adjust the arm voltage to a desired value [1].

Clustering of submodules within an MMC has been proposed in [2]. A cluster consists of an arbitrary amount of submodules bundled together and a cluster controller, introducing another level of modularity between the converter arm and the submodule. Submodule sorting, capacitor voltage balancing, and harmonic cancellation could be done within the cluster, managed by the cluster controller. Only one communication channel is needed between the arm controller and the cluster controller, which effectively reduces the communication requirements. Within the cluster, the communication could have low latency, and lower requirements for insulation as for individual submodules. The complete cluster could be assembled in the factory, up to container size, offering more possibilities for testing before leaving the factory, and faster converter assembly on site.

The relevant submodule topologies for the proposed concept are the half-bridge (HB), full-bridge (FB), semi-full-bridge (SFB), and the double-zero (DZ) submodule topologies, shown in Fig. 1. The HB (Fig. 1a), with two switches and one submodule capacitor, is the simplest submodule topology. It has two switching states, either inserting the capacitor voltage $+V_C$ into the converter arm or bypassing it. This enables the operation of the MMC with a modulation index M in the range of $0, 1$. Since the current passes through only one switch in both states, the HB topology offers extremely low conduction losses. The FB (Fig. 1b) features two additional switches compared to the HB, which leads to increased conduction losses, because there are always two switches in the arm current path. The FB has three switching states, offering the possibility to apply negative voltage $-V_C$ at the submodule terminals. An MMC employing FB submodules can operate with M in the range of $\{0, inf\}$. The DZ topology, which has been presented and investigated in [3], [4], enables to operate the submodule with a low on-state resistance by selecting the double-zero bypass state, i.e., S_{C1} is turned off and the arm current is split into two parallel paths $S_1 + S_3$, and $S_2 + S_4$. For power transmission with only a small amount of reactive power and M close to 1, the highest arm currents can be expected when the arm voltage is close to zero, as seen in Fig. 2. During that time interval most submodules are in double-zero bypass state, reducing conduction losses significantly. The SFB, investigated in [5]–[7], is a topology created by double-connecting two FB submodules and merging the switches between the connections to one (Fig. 1d). Four voltage levels can be achieved, applying a voltage of $-V_C$, $0V_C$, $+V_C$ or $+2V_C$ at the submodule terminals. Hence, the SFB can replace two conventional submodules (Fig. 1a-c). The double-connection can also be applied to the DZ topology, combining the advantages of the SFB and the DZ topologies. This has been presented as the double-connected double-zero (DCDZ) submodule (Fig. 1e) in [8].

In this paper it is assumed that unipolar power semiconductor devices, such as silicon carbide (SiC) MOSFETs, are used. Due to their purely resistive conduction characteristic, they are very suitable to take advantage of conduction loss reduction

Fig. 1. Half-bridge (a), full-bridge (b), double-zero (c), semi-full-bridge (d), double-connected double-zero (e) submodule.

Fig. 2. MMC arm voltage and arm current (rectifier and inverter mode) for $M = 1.4$. Time interval with high current and low voltage (I), and low current and high voltage (II).

through parallel connection. Voltage ratings for available SiC MOSFET modules are in the range of 600 V to 1700 V, with 3300 V approaching [9]. SiC MOSFETs are foreseen to be suitable up to a blocking voltage of 15 kV [10]. The MOSFET is able to conduct current in forward and reverse direction as long as there is a positive gate signal applied. In addition to the inherent body diode, SiC MOSFET power modules may employ antiparallel diodes as freewheeling diodes. Since pn-junctions in SiC have a comparably high voltage drop > 3 V, the MOSFET should be operated in synchronous rectification mode, i.e. diodes should only conduct current during the deadtime of a half-bridge leg. Other possible unipolar power semiconductor types are the SiC JFET and the SiC BJT. Switching losses are disregarded entirely in this paper, since the switching frequency of each switch is very low in transmission applications. Furthermore, the switching losses of SiC MOSFETs are orders of magnitude lower than today's Si IGBTs.

II. THE CASCADED DOUBLE-ZERO CLUSTER

In this paper, a double-zero capable submodule cluster is proposed. By double-connecting DZ segments, the topology presented in Fig. 1e can be extended to an arbitrary amount of capacitors. The topology is from here on denoted as cascaded double-zero cluster, $CDZC_n$, where n is the number of capacitors (or the amount of positive voltage levels). The benefits are

- reduced conduction losses
- increased robustness against short circuits
- reduced requirements for bypass equipment
- reduction of control hardware
- reduced amount and length of cables and fibres
- factory assembly of larger building blocks, reducing on-site converter assembly time
- possibility of advanced in-house testing of assembled cluster prior to delivery

A. General structure

The $CDZC$ consists of the elements shown in Fig. 3, where $n \geq 3$, and $i = \{2, n-1\}$ is the ordinal of the i -th middle segment. For simplicity of the illustration, the MOSFETs and freewheeling diodes are represented by ideal switches. As can be seen, the first and last segments connect to the positive (P) and the negative cluster terminal (N), respectively. The other connection is a double-connection to the middle segments. The middle segment is double-connected on both connection points.

B. Switching states

In Fig. 4a-f, the major switching states are explained on the example of the $CDZC_3$, which is the simplest form of the cluster. With this variant, the voltages $-V_C$, $0V_C$, $+V_C$, $+2V_C$, $+3V_C$ can be applied to the cluster terminals. The negative state

Fig. 3. Modular structure of the CDZC_n consisting of two outer segments and an arbitrary amount of inner segments.

inserting $-V_C$ (a) and the state inserting $+V_C$ (c) are achieved by parallel connecting the capacitors.

In the double-zero bypass state (b) the current splits into the upper and the lower path, reducing the resistance considerably. Additionally switching on the switches in the double connection (not depicted here) yields a further conduction loss reduction. The benefit of this low resistive bypass state becomes clear, when looking at the arm current in Fig. 2 (I). The arm current is highest when the arm voltage is at its minimum, where most of the submodules are bypassed. Thus, a substantial conduction loss reduction can be expected, as discussed in the next section. The previously discussed states (a-c) do not create an imbalance of the capacitor voltages. For other states the capacitors may be charged differently, caused by having different shares of the arm current flowing through the capacitors, e.g., inserting $+2V_C$ (d), and by a mismatch of the capacitor values. The implications of parallel connecting capacitors with a voltage imbalance, and controlling this voltage imbalance to acceptable levels has been discussed in the scope of the SFB in [7]. The CDZC topology has the advantage, that the switches in series to the capacitors provide additional controllability. The switching states (d) and (e) can be alternated in order to balance the capacitor voltages. Since SiC MOSFETs have extremely low switching losses, the impact of additional state transitions is minor. The series connection, depicted in (f), leads to high conduction losses, but this state is only used when the arm current is low, as indicated in Fig. 2 (II).

C. On-state resistance and conduction losses

In order to evaluate the conduction loss of a submodule switching state, the resistive network in Fig. 4 can be reduced to one lumped resistance parameter R_{sm} . For simplicity, the resistances of the busbars and the capacitors are neglected and the on-state resistance of each switch is assumed to be equal and constant. To be able to compare submodule topologies with different amount of levels, R_{sm} is normalized by the amount of positive voltage levels n . To account for different amount of switches and keep the semiconductor area constant, it is multiplied by the amount of switches per level n_{sw}/n . The amount of switches for the CDZC_n is determined by

Fig. 4. Major switching states of the CDZC₃ inserting $-V_C$ (a), $0V_C$ (b), $+V_C$ (c), $+2V_C$ (d-e), $+3V_C$ (f). MOSFETs in on-state are represented by resistances, and paths carrying no current are depicted in grey.

$n_{sw} = 4n + 1$. This yields the equivalent submodule resistance as given by

$$r_{sm,eq} = \frac{R_{sm} n_{sw}}{n^2}. \quad (1)$$

The comparison of the topologies presented in Fig. 1 and the CDZC_{3,4} is given in Fig. 5. On-state resistance measurements on a down-scaled prototype are included. It can be seen that the $r_{sm,eq}$ is decreasing with increasing n for the CDZC_n. For more complex clusters it becomes increasingly difficult to determine the cluster resistance analytically. However, they can still be calculated by recursive use of star-triangle transformation and then solving series and parallel connected resistances.

The arm resistance is a figure of merit for the conduction losses of the converter, and is illustrated in Fig. 6. A HB arm features very low resistance, but does not provide any negative arm voltage. The FB arm, on the other hand, can deliver full negative arm voltage but has a high resistance. For the CDZC_n the arm resistance varies, depending on the arm voltage and the size of the cluster. The larger the cluster, the lower the arm resistance (it should be kept in mind, that the highest arm current for an MMC operating at low power angle can be expected when the arm voltage is at its minimum). It can also be seen that depending on the amount of levels, the arm has different capabilities for negative arm voltage. This is described in more detail in section III.

The MMC conduction losses are shown in figure Fig. 7. A converter arm operating at higher M needs to provide higher peak voltage. The resulting resistance increase caused by a higher number of submodules per arm is accounted for. A saturation of the loss reduction can be seen for clusters with high n , as well as for high M .

Fig. 5. Equivalent submodule resistance $r_{sm,eq}$ for different states.

Fig. 6. Arm resistance for different $CDZC_n$, HB, FB, and SFB.

III. INFLUENCE ON THE OPERATION OF THE MMC

The operation of the MMC in terms of M_{max} and dc-fault current control capability is dependent on the provided arm voltage. Should a whole arm consist solely of one submodule type, then the highest voltage $\hat{V}_{arm}$ and the highest negative voltage $\check{V}_{arm}$ are determined by the amount of positive and negative voltage levels provided by the submodule topology, as given by (2) and (3). The amount of clusters per arm is n_{cl} and the amount of negative voltage levels n_{neg} that is possible with the $CDZC_n$ is determined by (4). M_{max} and the relative maximum negative voltage is given by (5) and (6) respectively.

Fig. 7. MMC conduction losses as a function of M for different submodule topologies (load angle $\varphi = 0$).

$$\hat{V}_{arm} = n_{cl}nV_c \geq \hat{V}_{ac} + \frac{V_{dc}}{2} = (M_{max} + 1) \frac{V_{dc}}{2} \quad (2)$$

$$\check{V}_{arm} = n_{cl}n_{neg}V_c \geq \hat{V}_{ac} - \frac{V_{dc}}{2} = (M_{max} - 1) \frac{V_{dc}}{2} \quad (3)$$

$$n_{neg} = \text{floor}\left(1 + \frac{n-1}{3}\right) = \begin{cases} \frac{n+2}{3}; & n = 1, 4, \dots \\ \frac{n+1}{3}; & n = 2, 5, \dots \\ \frac{n}{3}; & n = 3, 6, \dots \end{cases} \quad (4)$$

$$M_{max} = \frac{n + n_{neg}}{n - n_{neg}} = \begin{cases} 2 + \frac{3}{n-1}; & n = 1, 4, \dots \\ 2 + \frac{3}{2n-1}; & n = 2, 5, \dots \\ 2; & n = 3, 6, \dots \end{cases} \quad (5)$$

$$\frac{\check{V}_{arm}}{\hat{V}_{arm}} = \frac{n_{neg}}{n} = \begin{cases} \frac{1}{3} + \frac{2}{3n}; & n = 1, 4, \dots \\ \frac{1}{3} + \frac{1}{3n}; & n = 2, 5, \dots \\ \frac{1}{3}; & n = 3, 6, \dots \end{cases} \quad (6)$$

Fig. 8 shows the relative maximum negative arm voltage, and Fig. 9 M_{max} for different variants of the $CDZC_n$, the DZ or FB ($n = 1$), and the DCDZ or SFB ($n = 2$). An interesting observation is that the $CDZC_4$ performs like the DCDZ in terms of modulation index. Hence, it can be regarded as a promising option. The $-V_c$ state, shown in Fig. 4a, is advantageous in terms of losses and capacitor voltage balancing compared to states with lower voltage, e.g., the $-2V_c$ state of $CDZC_4$. Therefore, it could be considered to use the $-V_c$ state during normal operation and use the more negative states during fault cases, only. The dotted line in Fig. 9 depicts the MMC operation limits if only this parallel negative state is used.

To successfully block and control dc-side faults, the counter-emf, V_{emf} , formed by all the capacitors along the fault current path must counteract the loss of voltage due to the fault [11]. The highest possible negative capacitor voltage each arm of the converter can insert is $V_{emf} = \check{V}_{arm}$. If this voltage is higher than the difference between the ac terminal and the dc terminal, the fault can be controlled during a stiff dc-side

Fig. 8. Relative maximum negative arm voltage as a function of n .

Fig. 9. Maximum modulation index $M_{\max}$ as a function of n .

fault as during the normal operation with full dc-side voltage. In the case of a pole-to-ground fault, the converter arm needs to provide an ac voltage equal to the peak of the ac line-to-neutral voltage $\hat{V}_{ac}$, which is determined by M , see (7). Combined with (5), this yields that M is limited to less than $M_{\max}$ if such a fault should be controllable (8).

$$\hat{V}_{arm} \stackrel{!}{\geq} \hat{V}_{ac} = M \frac{V_{dc}}{2} \quad (7)$$

$$M \leq M_{\max} - 1 \quad (8)$$

Note that for a pole-to-pole fault, the converter arm needs to additionally provide $V_{dc}/2$, resulting in a limitation $M \leq M_{\max} - 2$, which is smaller than unity for $n > 1$. Some of the variants of the CDZC_n ($n = 3, 6, \dots$) are unable to provide controllability for such faults.

If such limitations are not desirable, clusters with different topologies can be employed in one arm, similar to a hybrid arm consisting of FB and HB submodules [12]. The described modulation index limitations are visualized in Fig. 10 for the most promising CDZC variants ($n = 1, 4, \dots$).

Fig. 10. Maximum modulation index for operation with pole-to-ground dc-fault control capability, pole-to-pole dc-fault control capability, and use of only the $-V_C$ negative state ($n = 1, 4, \dots$).

IV. INTERNAL FAULT HANDLING

The most severe fault that can occur on a submodule/cluster level is a short circuit between the positive and the negative terminal of one of the capacitors. Such a fault can be caused by a failing semiconductor module. Usually, power modules fail into an open circuit due to bond-wire lift-off, but subsequent arcing overheats these modules locally. The energy stored in the capacitor is then discharged rapidly through the path provided by the arc destroying the semiconductor modules entirely [13]. The resulting explosion may also destroy neighboring equipment. Therefore, it should be avoided at all cost.

In the CDZC there are always three switches between a positive and a negative terminal of a capacitor. Hence, internal short circuits are a lot less likely, compared to the HB, FB and the SFB. But in certain states two of the three switches are conducting, so that a failure of the third closes the path between the capacitor terminals. If detected fast enough, the two conducting modules can be turned off and a short circuit is avoided. However, the issue with turning-off a short circuit is the continuous flow of the arm current, which can be assumed constant for the duration of the fault. A path for the arm current should always be provided.

Fig. 11 shows how the discharge of C_i as a result of a semiconductor module failure at either a), b) or c) can be avoided. When the fault is detected, the cluster control determines a node that has to be isolated from the rest of the circuit. The switches connected to that node are then opened and the switches on the other side closed, to provide a path for the arm current. The cluster should not be operated in this state for too long, since another failure close to the isolated node could interrupt the current path for the arm current. Subsequently, mechanical bypass switches (not depicted here) between P_{i-1} , P_i , and P_{i+1} can bridge some parts of the cluster, effectively cutting it in two parts which can be operated normally. These mechanical switches do not need to be very fast.

Fig. 11. Handling of internal fault caused by semiconductor module failure at either a), b), or c), and required isolation of neighboring node and C_i .

V. WIRELESS CLUSTER CONTROL

The control of the MMC can be distributed to different control levels, a central controller and cluster controllers located in the CDZC. The central controller executes the control algorithms based on the operator-defined set-points and converter-level measured signals, and provides reference cluster voltages such that the energy balance of the clusters is observed. The cluster controllers are responsible for their internal dynamics, such as modulation, individual capacitor voltage balancing, and handling of submodule faults. Since the CDZC_n can operate a high number of voltage levels with a single controller, the total number of controllers in the converter is reduced, compared to an MMC with a local controller in each submodule. In combination with the distributed control approach this relaxes the communication requirements such as the data rate and cycle time between the central controller and the cluster controllers. The control data sent from the central controller to the clusters are voltage references which can have a cycle time in the range of hundreds of μ s [14].

Wireless control for MMCs has been proposed in [15]. Low-latency, high-reliability wireless communication methods can be used for the transfer of data from the central controller to the cluster controllers. The central controller broadcasts the control data to the clusters. The converter can easily be scaled up with the addition of wireless controlled clusters and re-calculation of reference cluster voltages in the central controller. Since the submodules should receive their switching pulse patterns from the cluster controllers, cluster-internal communication is proposed to be tethered.

The described approach, shown in Fig. 12, enables excellent scalability, reduced control hardware, reduced cabling, reduced insulation requirements for cluster-internal communication, and independence of the control method from the number of submodules.

VI. CONCLUSION

This paper presents a novel type of submodule cluster, the CDZC, for MMCs. The use of SiC MOSFETs and the proposed wireless distributed control scheme enhances the benefits of the CDZC. The advantages are

- low conduction losses for small load angles and modulation index close to unity and above

Fig. 12. Proposed wireless control scheme for an MMC employing CDZC.

- cluster-internal short circuits are less likely
- reduced auxiliary equipment, such as control hardware and cabling
- cluster with local controller enabling advanced pre-testing before delivery
- larger building blocks enabling faster converter assembly times

The capabilities of the MMC regarding dc-fault handling and modulation index are determined by the amount of negative voltage levels of the cluster. The CDZC with 4,7,... submodules is identified as an attractive variant, since it features the named advantages and best dc-fault controllability.

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