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Multivoltage Aware Resistive Open Fault Model

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Abstract—Resistive open faults (ROFs) represent common interconnect manufacturing defects in VLSI designs causing delay failures and reliability-related concerns. The widespread utilization of multiple supply voltages in contemporary VLSI designs and emerging test methods poses a critical concern as to whether conventional models for resistive opens will still be effective. Conventional models do not explicitly model the V_{DD} effect on fault behavior and detectability. We have empirically observed that a sensitized ROF could exhibit multiple behaviors across its resistance continuum. We also observe that the detectable resistance range versus V_{DD} varies with test speed. We consequently propose a voltage-aware model that divides the full range of open resistances into continuous behavioral intervals and three detectability ranges. The presented model is expected to substantially enhance multivoltage test generation and fault distinction.

Index Terms—Open resistance intervals, resistive open faults (ROFs), small delay faults, voltage-aware modeling.

I. INTRODUCTION

RESISTIVE opens are common manufacturing failures that induce voltage-dependent delay faults and pose potential reliability risks due to their partial break-like nature, [1]–[4]. Distinguishing such faults is important in reducing infant mortality failures. Therefore, promising techniques for distinguishing delay failures induced by resistive open faults (ROFs) from those induced by other mechanisms have been proposed [5], [6]. These techniques have relied on empirical observations of delay pattern versus V_{DD} for resistive opens compared to other fault mechanisms. However, inductive fault analysis on ROFs shows that the voltage-delay dependencies are significantly sensitive to other test conditions [7]. Due to the absence of a comprehensive behavioral fault model considering these critical dependencies, such techniques could be less reliable and less effective in distinguishing the cause of detected delay faults.

On the other hand, due to the supply voltage-dependent delay behavior, previous work has demonstrated that fault coverage could be improved using selective testing at multiple V_{DD} values [8]–[13]. With the emergence of low power designs that utilize multiple supply voltage levels [14], such

multi- V_{DD} testing could become necessary for effective fault testing. Nevertheless, the delay fault detectability is also sensitive to the speed of the test [15]. The unavailability of a comprehensive model describing the fault detectability with test conditions, including test speed, has impeded the development of effective test generation algorithms.

The behavior and detectability of ROFs depend on the technological and electrical characteristics of the design and test conditions, as well as the supply voltage [7], [8], [13], [16]. Given such dependencies, comprehensive modeling of the fault behavior and detectability becomes challenging. Previous models [17]–[21] for ROFs did not explicitly account for V_{DD} and have not considered the behavioral aspect of the fault. Therefore for efficient multi- V_{DD} fault detection and testing, a voltage-aware model which considers these issues has to be developed.

The aim of this paper is to present a parametric, voltage-aware model, including both the behavioral and detectability aspects of the delay caused by ROF. The premise of the technique is that the full resistance continuum can be divided into intervals, each having a unique behavior with respect to V_{DD} , and can have detectability ranges for each V_{DD} depending on the test speed. Additionally we explain a methodology to determine the various behavioral and detectability parameters of the model. The model assumes a limited number of V_{DD} values. The behavioral information revealed by this model assists in defining the exact test pattern that can be used to excite a particular fault behavior. The detection information helps to identify the right test conditions for a given test speed that maximizes the fault coverage. Hence, this model improves the test pattern generation and fault detection algorithms.

A preliminary version of this paper was published in ETS 2012 [22]. The work presented in this paper brings the following extensions. Preliminary verifications on benchmark circuits, computation of the critical resistance for behavior intervals, and an algorithm for identifying the behavioral parameters for each fault and test pattern. The organization of this paper is as follows. Background and preliminary work are given in Section II. In Section III, the motivation for developing the voltage-aware model based on delay-voltage dependencies of resistive opens is explained. An illustration of the model followed by a methodology used to identify the behavior intervals and detection ranges is discussed in Section IV. Simulation results on benchmark circuits using different technology models are discussed and analyzed in Section VI. Concluding remarks are given in Section VIII.

II. BACKGROUND

An ROF is a parametric model representing a partial-open failure, in which the size of the open (break) is represented

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by a resistance. In previous work, the resistances of opens (RO) have been experimentally characterized for an aluminum process and it was reported that for ROFs, RO can vary in the range of Ohms to Megohms [2]. The distribution of resistance values can be used statistically to compute the fault coverage [23]. According to the resistance of the partial-open fault and the relative length of the sensitized faulty path to the longest path, an ROF can cause extra delays over several orders of magnitude. A gross delay fault is defined to have a cumulative propagation delay exceeding the longest path delay. Other faults are defined as small delay faults [3]. Gross delay faults are detected by at-speed transition delay fault testing, whereas small delay faults are tested using faster-than-at-speed testing. Generally delay faults due to ROF show some sensitivity to test patterns and to V_{DD} , as will be discussed later in this section.

Kruseman and Heiligers [7] conducted an inductive fault analysis for resistive opens on several standard cells using a wide range of technologies. They highlighted different voltage-delay dependencies with different fault locations and test patterns. In that work, the additional delay caused by ROFs was characterized and several delay behaviors were identified. An increasing delay pattern corresponds to an increase in delay for reduced voltage; a constant delay pattern means an almost constant delay for high voltages, but an increase in delay with smaller voltages; and a constant inverse delay means a decrease in delay for reduced voltage. The listed behaviors are sensitive to the transition test pattern and intra-gate location.

The effect of fault resistance on the additional delay at different V_{DD} can generally be assumed to be relative [7]. This means at each V_{DD} , the larger the resistance, the larger the additional delay. A more accurate relationship is, however, reported in [24]. Arumi *et al.* [24] assessed the behavior (delay) of ROFs at a single V_{DD} using an experimental chip and reported that high and low resistance values have different timing responses and have to be modeled differently. This is attributed to the ON resistance of MOS transistors driving a faulty node as well as the capacitance of the driven gates [24]. This shows that the range of open resistances can exhibit different behaviors with V_{DD} according to the relative value of RO with respect to the transistor ON resistance (R_{ON}).

Other factors affecting the behavior include: the location of an ROF within the interconnect [24], the threshold voltage [25], capacitance of driven gates [26], and the technology used [16]. Each of the named factors affects the delay differently, and therefore questions whether assuming a fixed behavior for a fault is correct.

Li *et al.* [8] demonstrated that resistive opens in wire delay-dominant (WDD) paths are better detected at the highest V_{DD} . On the other hand, for gate delay dominant (GDD) paths, a low V_{DD} gives better detection. It may be noted that WDD paths have a high wire resistance, while GDD paths have a low wire resistance. This implies that the delay-voltage dependency can be different for different RO values.

It can be concluded that the delay behavior due to ROF differs with V_{DD} and also depends on the fault location and the applied test pattern, as well as the actual resistance. On the other hand, the intrinsic delay of a fault-free path

decreases with V_{DD} and its magnitude depends on the length of the path [14], [27]. Consequently this makes prediction of the observable behavior of a faulty path difficult. This in turn could cause different fault detectability at different V_{DD} values. Therefore, two hypotheses can be proposed. First, if the behavior of an ROF is a function of the resistance, then the ROF behavior can be modeled by dividing the range of open resistance values into intervals, each having its own observable fault behavior. Second, if the detectable resistance range varies with the supply voltage, the ROF detectability can be modeled by identifying the minimum detectable resistance value at each V_{DD} . In the next section, these hypotheses are investigated using a set of benchmark circuits.

III. PRELIMINARY WORK

A prior investigation of the fault behavior and detectability, considering the full resistive range, for a complete circuit and multiple voltage settings was carried out. The aim of this investigation was to ascertain whether a fault behavior is sensitive to its fault size (the resistance of the open). An additional aim was to ascertain whether the fault detectability with respect to V_{DD} is sensitive to the test speed. The results of this investigation have been published elsewhere [13], [15].

In this section, the simulation setup, the results, and implications from [13] and [15] will be discussed, followed by an experiment on an inverter chain.

A. Benchmark Designs Simulations

Simulations on benchmark circuits [28]–[30] were performed to determine the identifiable number of behaviors per fault for each circuit. Additionally, the average detectable resistance range per V_{DD} for a large number of fault locations was computed for each circuit. Spice-level simulations were used. The delays of faulty paths were calculated at the different V_{DD} values. The methodology for identifying a resistance interval was as follows: all consecutive resistance values resulting in a delay that is largest (maximum) at the same V_{DD} were grouped under one resistance interval. For example, if the delay with respect to V_{DD} for fault values of 100 k Ω and 200 k Ω were maximum at the highest V_{DD} (V_H), then they are both grouped under the same resistance interval marked, for example, as “Max at V_H .” To verify the detectability at different V_{DD} s and test speeds, the detectable resistance ranges for all faults and test patterns were captured at each V_{DD} . The detectable resistance range at a particular V_{DD} is the percentage of detectable resistance values compared to the total number of inserted resistance values. For example, a 50% detectable range at V_H means that half of the inserted resistance values were detectable at the highest V_{DD} .

The simulations were conducted on different transistor technology models, namely, a commercial 130 nm technology and the bulk 65, 32, and 16 nm Hi-K metal gate strained Si technologies from the Berkeley Predictive Technology Models (BPTM) [31]. Three V_{DD} values were used in each simulation: a high V_{DD} value, equal to the nominal V_{DD} , denoted by V_{DDH} ; a middle V_{DD} value chosen to be in between the high and the low V_{DD} , denoted by V_{DDM} ; and low V_{DD} which is twice the

TABLE I

TECHNOLOGY MODELS AND V_{DD}/V_t SETTINGS USED IN SIMULATION, HIGH V_t AND STANDARD V_t ARE FROM THE TECHNOLOGY MODELS

Tech	V_{DD}			Standard V_t		High V_t	
	H	M	L	$ V_{tn} $	$ V_{tp} $	$ V_{tn} $	$ V_{tp} $
130 nm	1.20	1.00	0.80	0.28	0.27	0.39	0.41
65 nm	1.00	0.85	0.70	0.42	0.37	-	-
32 nm	0.90	0.80	0.70	0.51	0.37	0.63	0.58
16 nm	0.70	0.65	0.59	0.48	0.43	0.68	0.69

TABLE II

RESISTANCE INTERVALS ON DIFFERENT BENCHMARK CIRCUITS

Ckt	Max at			#Intrv ROF
	V_L (%)	V_M (%)	V_H (%)	
c17	50.0%	0.0%	50.0%	2.00
s27	66.0%	2.1%	31.9%	1.96
b01	57.0%	1.0%	42.0%	2.33
c432	70.5%	0.0%	29.5%	1.97
c499	52.2%	0.0%	47.8%	1.92
c880	51.5%	0.0%	48.5%	1.94
c1355	52.7%	0.2%	47.1%	1.90
c1908	52.7%	0.0%	47.3%	1.90

threshold voltage and denoted by V_{DDL} . Table I shows the V_{DD} values used in the simulation for each technology.

In the simulation work presented throughout this paper, standard V_t cells were used. The high V_t cells were only considered in the latter part of this paper.

A list of faults is generated from the output nodes of each standard cell in each design. Discrete samples are chosen for RO so that they approximately represent a typical logarithmic distribution of open resistances [2]. Typically, ten resistance values [0 Ω , 50 Ω , 1 k Ω , 10 k Ω , 50 k Ω , 100 k Ω , 500 k Ω , 1 M Ω , 5 M Ω , and 10 M Ω] were considered. A set of eight resistance values [0 Ω , 500 Ω , 10 k Ω , 100 k Ω , 400 k Ω , 800 k Ω , 1 M Ω , and 3 M Ω] was also used and similar results were observed. Transition test patterns were obtained by a conventional stuck-at fault-based automatic test pattern generator (ATPG) [32]. During the pattern generation process, each fault site is translated into stuck-at-0 and stuck-at-1 inputs for the ATPG. For detecting gross delay faults, the longest path delay at each V_{DD} is used as the test clock period (TCP), whereas for detecting small delay faults the 50th path delay percentile is used instead. For the latter case, any test patterns that sensitize paths longer than the 50th path delay percentile are not considered and therefore, the number of detectable faults will be reduced.

Table II reports the percentage of intervals identified at the low, medium, and high V_{DD} values, V_L , V_M , and V_H , and the average intervals per ROF observed. All resistive opens are injected at inter-gate locations and sensitized using falling

TABLE III

VERIFICATION OF THE DETECTABILITY VERSUS V_{DD} ON DIFFERENT BENCHMARK CIRCUITS

Ckt	Gross Delay Faults				Small Delay Faults			
	#ROF	V_{DDL}	V_{DDM}	V_{DDH}	#ROF	V_{DDL}	V_{DDM}	V_{DDH}
c17	9	45.2%	47.3%	47.6%	4	58.7%	58.7%	58.7%
s27	14	43.8%	45.2%	45.8%	6	52.4%	56.6%	56.6%
b01	40	42.9%	44.6%	45.5%	19	50.1%	50.9%	51.3%
c432	184	29.4%	31.1%	36.5%	92	48.5%	51.0%	54.6%
c499	124	36.6%	39.4%	39.4%	60	41.8%	41.8%	66.7%
c880	343	31.4%	37.6%	39.8%	172	43.0%	44.1%	45.0%
c1355	291	33.7%	34.0%	39.5%	143	28.8%	40.7%	40.8%
c1908	804	26.0%	30.9%	37.6%	401	44.5%	45.6%	48.5%

Fig. 1. Inverter Chain Examples for (a) faulty path, (b) short path, and (c) long path.

transitions. For the given V_{DD} range, these conditions should manifest themselves as additional delays with similar behavior. Despite this, Table II shows that multiple behavioral intervals can be observed. On average all ROFs exhibit about two-to-three behaviors per fault location, as highlighted in the last column. This can be attributed to the contribution of delays due to faults, compared to the delays contributed by the path. That is, the delays due to opens are a function of the fault size (open resistance). For small values of open resistance, the fault contribution in the total path delay is low, therefore resulting in the dominance of intrinsic delay behavior of the fault-free path. However, when the open resistance becomes large, the faulty path delay behavior gets dominated by the behavior of opens. For intermediate values of RO, the behavior might exhibit more complex behaviors, which would increase the types of behavior to more than two per fault.

On the other hand, Table III reports the detectability results versus V_{DD} in different circuits (column 1) and different numbers of faults (columns 2 and 6) for the detection of gross delay faults (columns 3–5) and small delay faults (columns 7, 8, and 9). The metric used in evaluating the detectability is the resistive open coverage (ROC). Table III shows that the average detection coverage generally varies with V_{DD} . Additionally, it shows that the detectable resistance range for small delay faults is more than for gross delay faults. This is because the test clock period is shorter in testing small delay faults, which enables detection of more subtle delays and therefore resistance ranges.

Fig. 2. Propagation delay for inverter design using falling transition pattern. (a) Fault-free case. (b) Faulty case. Dashed line represents $RO = 1 \text{ k}\Omega$. Solid line represents $RO = 1 \text{ M}\Omega$.

Fig. 3. Resistance detection thresholds using a falling transition pattern, considering: (a) small delay fault and (b) gross delay fault.

B. Inverter Chain Design Experiment

The aim of this experiment is to visualize the various parameters required to fully represent the detectability and behavior of an ROF with respect to V_{DD} . In this experiment, three inverter chains are considered, as shown in Fig. 1. The circuit has three paths, a faulty path where the fault resides a short path and a long path. This is to enable simple observation of the behavior and to evaluate the fault detectability in at-speed testing and faster-than-at-speed testing methods. In order to examine the faulty behavior, two values of open resistances (denoted as RO in Fig. 1) are injected: $1 \text{ k}\Omega$ and $1 \text{ M}\Omega$. These values are selected to observe faulty behavior for small and large open resistances. Two consecutive vectors are applied to set the faulty node to 1 and 0, respectively, causing a falling transition at the driving node of fault. The delays of the fault-free and faulty paths are measured and shown in Fig. 2(a) and (b), respectively.

Fig. 2(b) shows that for $RO = 1 \text{ M}\Omega$, the propagation delay increases as the supply voltage increases, whereas $RO = 1 \text{ k}\Omega$ produces an inverse relationship. To explain these differences, recall that the observable behavior of the faulty path comprises two components: the fault-free path behavior and the addi-

Fig. 4. Identified behaviors.

tional behavior of the open resistance. The delay of the fault-free circuit decreases with increasing voltage as in Fig. 2(a). On the other hand, the delay due to the resistive open increases with voltage as described in [7]. However, the delay strength (magnitude) is low for $1 \text{ k}\Omega$ and high for $1 \text{ M}\Omega$. This consequently results in different total delays with voltage for the faulty path. It would be expected that the behavior of a range of resistance values around $1 \text{ k}\Omega$ will be similar to that at $1 \text{ k}\Omega$. We would expect a change in behavior when the fault effect has an equal delay strength to that of the fault-free path. Then

Fig. 5. Behaviors considered in the proposed model. (a) Decreasing delay behavior. (b) Increasing delay behavior. (c) Mid-bump delay behavior. (d) Mid-bump-inv delay behavior.

the behavior for another range of resistances would be similar to that at 1 M Ω . The behavior identified for the full range of ROF using large number of resistances is illustrated in Fig. 4.

Fig. 4 shows that the resistance intervals [50 Ω , 64 k Ω] and [345 k Ω , 10 M Ω] have decreasing and increasing delay behaviors, respectively. Additionally, the resistance interval [97.6 Ω , 226.4 k Ω] has a “mid-bump” behavior, marked as “others” in the figure. In this “mid-bump” range, neither the intrinsic fault behavior nor the intrinsic fault-free path behavior dominates. The size of such intervals is expected to vary according to the path length where the fault resides. From this experiment, a key observation is that the behavior for a particular fault location and test pattern is dependent on the open resistance value itself, i.e., it is interval-dependent. This effectively allows the full domain of open resistances in sub-intervals which have similar delay behavior to be treated as a function of V_{DD} . The intermediate resistance value at which the delay- V_{DD} behavior changes is defined as the critical resistance (RO_{cr}). For two consecutive intervals i and j showing distinct behavior, the critical resistance is denoted as RO_{cr}^{i-j} .

The fault detectability was evaluated at three V_{DD} values ($V_{DDL} = 0.8$ V, $V_{DDM} = 1.0$ V, and $V_{DDH} = 1.2$ V). The V_{DD} values were selected to be in the range of $2 \times V_t$ to the nominal V_{DD} . Transition test patterns causing falling transitions at the faulty node were applied. The selection of the specified values for V_{DD} along with the falling transition test pattern allows the fault to manifest inverse behavior compared to the fault-free path [7]. To emulate detectability in at-speed and faster-than-at-speed testing scenarios, the captured delay values for a large number of resistance values at each V_{DD} are normalized to the delays of the long and short paths, respectively. The detectability of the ROFs is shown in Fig. 3. The figures show the normalized faulty delay on the vertical axis and the corresponding RO values on the horizontal axis for three V_{DD} values. The behavior for small delay faults is shown in Fig. 3(a), while that for gross delay faults is shown in Fig. 3(b). For both cases, the normalized delay fault is detected when it exceeds the test clock period (TCP). The resistance at which the propagated delay is equal to the TCP is called the open resistance detection threshold (RO_{TH}). From Fig. 3(a) and (b), it can be shown that detection threshold RO_{TH} is different for the three V_{DD} values for both small and gross delay fault detection. That is, the detection thresholds

at V_{DDL} , V_{DDM} , and V_{DDH} are $RO_{TH}^S(V_{DDL})$, $RO_{TH}^S(V_{DDM})$, and $RO_{TH}^S(V_{DDH})$, respectively, for small delay faults and $RO_{TH}^G(V_{DDL})$, $RO_{TH}^G(V_{DDM})$, and $RO_{TH}^G(V_{DDH})$, respectively, for gross delay faults. A key observation is that the detectable resistance range can vary with the voltage used in testing. This knowledge helps in selection of optimum test patterns and V_{DD} especially for dynamic voltage scaling-aware designs. For example, for the delay fault scenarios in Fig. 3(a) and (b), V_{DDH} should be selected for test, since the detection threshold (RO_{TH}) is minimum and thus maximum resistance range can be detected.

IV. PROPOSED VOLTAGE-AWARE MODEL

In the previous section, it was shown that the full range of ROFs can exhibit various behaviors and detection thresholds in a voltage-aware environment. In this section, a model representing the behavior and detectability of ROF per test pattern in a multi- V_{DD} operating environment is explained. The full resistance range of ROF is divided into intervals representing distinct delay behaviors and detection thresholds. The concept of dividing the whole resistance range into resistance intervals is not new [11], [20], but here the concept relies on the combined observation of the delay behavior and detectability of the open resistances with respect to the supply voltage. The resistance range can be divided into N behavioral intervals and three detectability ranges.

For the behavior, it is observed that all ROF behaviors reported in [7] can be represented by one of the four behaviors shown in Fig. 5. That is, for three V_{DD} values, the delay behavior Bhv can only be:

- 1) maximum at V_{DDL} and minimum at V_{DDH} resulting in decreasing behavior;
- 2) maximum at V_{DDH} and minimum at V_{DDL} resulting in increasing behavior;
- 3) minimum at V_{DDM} resulting in mid-bump behavior; or
- 4) maximum at V_{DDM} resulting in mid-bump-inv behavior.

Therefore, for the full resistance domain, $[RO_{min}, RO_{Full}]$, of ROF sensitized by a test pattern TP , the different resistance intervals, $i \in \{01, 02, 03, \dots, N\}$, exhibit the behaviors $\{Bhv(01), Bhv(02), \dots, Bhv(N)\}$, where, $Bhv(i-1) \neq Bhv(i)$, $\forall i \in \{02, 03, \dots, N\}$. Consecutive intervals $i-1$ and i are separated by the critical resistance RO_{cr}^{i-1-i} , $N \geq i > 1$.

Fig. 6. Graphical illustration of the proposed voltage-aware ROF model [22].

As far as detectability is concerned, the resistance continuum exhibits three detectability ranges (i.e., gross delay faults, small delay faults, and undetectable delay faults). The proposed model represents those detectability ranges by the resistance detection threshold for gross delay faults (at-speed testing) and small delay faults (faster-than-at-speed testing). The minimum detected resistance when targeting gross delay faults is denoted as RO_{TH}^G and for small delay faults as RO_{TH}^S . Since each V_{DD} has its own RO_{TH}^G and RO_{TH}^S , the $RO_{TH}^G(V_{DD})$, and $RO_{TH}^S(V_{DD})$ notations are used in the model. That is, the gross delay fault range is $RO_{TH}^G(V_{DD}) < RO \leq RO_{Full}$, the detectable small delay fault range is $RO_{TH}^S(V_{DD}) < RO \leq RO_{TH}^G(V_{DD})$ and the undetectable range is $RO_{min} < RO \leq RO_{TH}^S(V_{DD})$.

A general graphical illustration of the proposed model is shown in Fig. 6. In this model, the full range of the ROF resistance domain is depicted on the circular axis from RO_{min} to RO_{Full} . Different continuous RO intervals are depicted by the circular segments (01, 02, ..., N) with behaviors ($Bhv(01)$, $Bhv(02)$, ..., $Bhv(N)$), respectively. For example, the first identified resistance interval, 01, is shown on the leftmost circular section. This 01 interval covers the resistances from RO_{min} up to RO_{cr}^{01-02} and has a behavior $Bhv(01) \in \{\text{dec, inc, mid-bump, mid-bump-inv}\}$. RO_{cr}^{01-02} is the critical RO value at which the observable delay behavior changes. For detection, the model also identifies the RO_{TH}^S and RO_{TH}^G resistances at each V_{DD} , indicating the detection regions for small and gross delay faults and assuming faster-than-at-speed and at-speed testing scenarios, respectively.

V. IDENTIFICATION OF BEHAVIOR INTERVALS AND DETECTION RANGES

Determining the exact values of the model parameters requires time-intensive circuit-level simulations, thus incur-

ring prohibitively high costs, especially for large designs. Therefore, we propose a parameter identification method based on parametric circuit-level simulations combined with SPLINE cubic interpolation to achieve reasonable trade-offs between accuracy and simulation time. The procedure used to identify the model parameters for every fault site/test pattern is described by the algorithms in Figs. 7 and 8. For a post-synthesis netlist, operating at a given V_{DD} value, our method identifies the model parameters ($Bhv(i)$, RO_{cr}^{i-02} ($\forall i \in (1..N-1)$), $RO_{TH}^S(V_{DD})$ and $RO_{TH}^G(V_{DD})$) for each ROF and the corresponding test patterns (TPs^G and TPs^S). The method is divided into two main parts: a prior circuit-level simulation part (Fig. 7) and the parameter identification part (Fig. 8). The aim of the circuit-level simulation to obtain the path delay information for all faults and test pattern pairs. The aim of the second part is to evaluate the model parameters.

The ROFs fault list that is an input to the algorithm in Fig. 7 can be generated exhaustively for comprehensive fault coverage or selectively using layout-aware methodology for realistic fault locations. If the Netlist corresponds to a multi-voltage design, its operating V_{DD} levels are used in this algorithm. However, for a multivoltage design with a large number (e.g., hundreds) of V_{DD} levels, it is proposed that only three V_{DD} levels are used (the highest, middle, and lowest). While ROFs, TPs^G , TPs^S , and VDDs are passed to the algorithm as inputs, the set of open resistances, ROs, is generated locally to obtain a discrete representation of the ROF delay. Typically, eight to ten resistance values covering a logarithmic distribution are used in the simulation and reasonable results were observed for both cases. Two test patterns are considered in this method, one (TPs^G) for at-speed testing (detection of gross delay faults) and one (TPs^S) for faster-than-at-speed testing (detection of small delay faults). Those test patterns can be obtained using dedicated path delay-aware automatic

Input: Netlist, VDDs, ROFs, TPs^G , TPs^S
Output: PD(VDDs, ROFs, TPs^G || TPs^S , RO)
1: Select discrete values for ROs
2: //Circuit-level simulation()
3: **for all** ROF $\in$ ROFs **do**
4: **for all** TP $\in$ (TPs^G (ROF) $\cup$ TPs^S (ROF)) **do**
5: **for all** VDD $\in$ VDDs **do**
6: **for all** RO $\in$ ($0 \cup ROs$) **do**
7: Simulate(Netlist, ROF, TP, VDD, RO)
8: Capture PD(ROF)(TP)(VDD)(RO)
9: **end for**
10: **if** TP $\in$ TPs^G **then**
11: $PDs^G(VDD) \leftarrow PD(ROF)(TP)(VDD)(0)$
12: **end if**
13: **if** TP $\in$ TPs^S **then**
14: $PDs^S(VDD) \leftarrow PD(ROF)(TP)(VDD)(0)$
15: **end if**
16: **end for**
17: **end for**
18: **for all** VDD $\in$ VDDs **do**
19: $LPD^G(VDD) := \max(PDs^G(VDD))$
20: $LPD^S(VDD) := \max(PDs^S(VDD))$
21: **end for**

Fig. 7. Prior circuit-level simulation step for the VA ROF modeling.

test pattern generation engines.

After generating the discrete open resistance set (line 1), the procedure starts by fault simulating all fault locations (ROFs), and all test patterns (TPs) using VDD settings (VDDs) and open resistance values (ROs) to obtain the path delay information (PD) as shown in lines 3–18. Once the delay values (PD) for the fault-free paths ($\forall RO = 0$) and faulty paths ($\forall RO \in ROs$) are obtained, the longest path delays at each VDD of long paths ($LPD^G(VDD)$) using ($TP \in TPs^G$) and of short paths ($LPD^S(VDD)$) using ($TP \in TPs^S$) are identified using the fault-free path delay data PD ($\forall RO = 0$) as shown in lines 19–22. Ideally, some margins should be taken into account to compensate for the resolution of automatic test equipment. These margins are assumed to be static and voltage insensitive and for the sake of simplicity, they have been assumed to be zero here. Once the delays of the faulty paths and the delays of the longest paths with respect to VDD are obtained, then it is possible to determine the model parameters. It is important to note that this method of fault simulation is time consuming and is not suitable for large circuits. But since accuracy is crucial to this paper, we have employed it as is. We will consider some optimization methods in future work.

By taking the circuit-level simulation output of Fig. 7, the detection thresholds, interval behaviors, and critical resistances are obtained. The open resistances detection threshold (i.e., RO_{TH}^G and RO_{TH}^S) for each ROF and TP is computed using a cubic spline interpolation to find the resistances corresponding to $LPD^G(VDD)$ and $LPD^S(VDD)$, given the faulty path delays and the corresponding open resistances

Input: PD(VDDs, ROFs, TPs^G , TPs^S , RO)
Output: $RO_{TH}^G(VDD)$, $RO_{TH}^S(VDD)$,
 RO_{cr}^{i-i+1} , $Bhv(i)$
1: **for all** ROF $\in$ ROFs **do**
2: **for all** TP $\in$ (TPs^G (ROF) $\cup$ TPs^S (ROF)) **do**
3: //Identifying: RO_{TH}^G , RO_{TH}^S
4: **for all** VDD $\in$ VDDs **do**
5: $RO_{TH}^G(VDD) :=$
 $Intrp(LPD^G(VDD), PDs(ROF)(TP)(VDD))$
6: $RO_{TH}^S(VDD) :=$
 $Intrp(LPD^S(VDD), PDs(ROF)(TP)(VDD))$
7: **end for**
8: //Identifying: RO_{cr}^{i-i+1} , $Bhv(i)$
9: $i := 1$, $PrevRO := \phi$
10: **for all** RO $\in$ ROs **do**
11: **if** $ROBhv(PrevRO) = ROBhv(RO)$
12: **then**
13: $PrevRO := RO$, $Bhv(i) := ROBhv(RO)$
14: **else**
15: $RO_{cr}^L := PrevRO$, $RO_{cr}^H := RO$
16: $RO_{cr}^{i-i+1} := \text{avg}(RO_{cr}^L, RO_{cr}^H)$
17: **for iter** = 1 $\rightarrow$ MAX **do**
18: **if** $ROBhv(RO_{cr}^L) = ROBhv(RO_{cr}^{i-i+1})$
19: **then**
20: $RO_{cr}^L := RO_{cr}^{i-i+1}$
21: **else**
22: $RO_{cr}^H := RO_{cr}^{i-i+1}$
23: **end if**
24: $RO_{cr}^{i-i+1} := \text{avg}(RO_{cr}^L, RO_{cr}^H)$
25: **end for**
26: $i := i + 1$
27: **end if**
28: **end for**

Fig. 8. Proposed method to obtain the parameters of the voltage-aware ROF model.

(ROs), as shown in lines 1–7 of Fig. 8. Subsequently, the algorithm identifies the various possible resistance intervals (i) and their respective behaviors ($Bhv(i)$) and critical resistances (RO_{cr}^{i-i+1}). To identify the behavior, a function $ROBhv(RO)$ is used to check the behavior of that RO value. The possible behaviors are “inc,” “dec,” “mid-bump,” and “mid-bump-inv,” as explained in previous section. The behavior is checked $\forall RO \in ROs$. When the behavior changes (i.e., $ROBhv(RO) \neq ROBhv(PrevRO)$) then a critical resistance (RO_{cr}^{i-i+1}) between $PrevRO$ and RO is identified. The algorithm searches for more accurate value by successively narrowing the range of the solution by reducing the upper limit RO_{cr}^H or increasing the lower limit RO_{cr}^L , as shown in the remainder of the algorithm. The range is narrowed at each iteration by MAX times. MAX was arbitrarily set to 10 and 15 and showed almost identical results (to within 10 Ω), and was therefore set to 10 for the results in the rest of this paper.

Following this procedure, the behavior and corresponding critical resistances, along with the detection thresholds are

obtained for all fault locations and test patterns. Next, we consider the simulation results of the procedure and the possible implications for behavior and fault detectability across technologies.

VI. MODELING ANALYSIS

Simulations were carried out on several benchmark circuits to verify the effectiveness of the proposed methodology in modeling the behavior and detectability characteristics of ROF with V_{DD} . The simulation procedures have been explained in Section III-A. The results of the obtained model parameters for different benchmark circuits are reported in this section, however for reasons of space, results are analyzed in detail for the c17 circuit only.

For circuit c17, it was found that rising transition test patterns resulted in a single behavior for all faults. Falling transition test patterns induce more behaviors and imply a more challenging modeling scenario. Table IV shows the identified behavior parameters (i.e., resistance intervals and corresponding behavior) in columns 2–4, and the resistance detection threshold for small and gross delay faults per V_{DD} ($RO_{TH}^S(V_{DD}), RO_{TH}^G(V_{DD})$) in columns 5–10 for each fault in column 1. For example, the first two rows entry in the table shows that for ROF 1, two distinct resistance intervals were identified. The first identified behavior is a decreasing delay behavior “dec,” which is manifested by resistances from 50 Ω (minimum modeled open resistance: σ or RO_{min}) up to 460 k Ω . For resistances from 460 k Ω to 10 M Ω (maximum open resistance: RO_{Full}), an increasing delay behavior “inc” is detected. A “dec” behavior for a small range of RO was observed due to the dominance of the fault-free path delay behavior for that range; the range of that interval increases with the path length. For example, for fault location 3, which is sensitized along a long path, the change in behavior from “dec” to “inc” occurs around 2 M Ω ; for fault location 8, sensitized along a middle-length path, the change occurs at around 700 k Ω ; and for a fault location sensitized along a short path, the change is at approximately 400 k Ω . It is also observed that ROFs, especially those sensitized via long paths (e.g., faults no. 3, 4, and 6), undergo transient “mid-bump” behavior when changing from “dec” behavior (for small RO) to “inc” behavior (for large RO). However, for other faults, especially those sensitized via shorter paths (e.g., faults no. 1, 2, and 8), this transient “mid-bump” behavior interval is reduced or not detected. This again can be attributed to the different strength of the fault-free path delay contribution. Another observation is that, for some fault locations, a change in fault behavior when approaching the full open range ($RO = 10$ M Ω) is detected. This is consistent with the findings reported in [24].

An important conclusion from this table is that assuming a fixed behavior for an ROF is not always realistic and could be misleading, especially if the transition test pattern/fault locations are not carefully considered.

The ROF detectability with V_{DD} is presented in Table IV columns 5–10. The open resistance detection threshold is presented for small delays in columns 5–7 and gross delay faults in columns 8–10. It can be observed that the detection

TABLE IV
BEHAVIORAL AND DETECTABILITY PARAMETERS OF THE ROF VAMODEL
FOR C17 CIRCUIT ($\sigma = RO_{min} = 50\Omega$)

#	Behavior Intervals			Detection Thresholds (k Ω)					
	Interval (k Ω)		Behavior	RO_{TH}^S			RO_{TH}^G		
	Lower	Upper		V_L	V_M	V_H	V_L	V_M	V_H
1	σ	460	dec	1.3	0.8	0.6	28.5	19.6	15.3
	460	10 000	inc						
2	σ	442	dec	1.9	1.2	0.8	29.0	20.2	15.7
	442	10 000	inc						
3	σ	517	dec	-	-	-	σ	σ	σ
	517	2141	mid-bump						
	2141	9997	inc						
	9997	10 000	mid-bump						
4	σ	280	dec	-	-	-	1.1	1.1	1.0
	280	1193	mid-bump						
	1193	8321	inc						
	8321	10 000	mid-bump						
5	σ	355	dec	0.4	0.6	0.6	21.2	16.5	13.9
	355	1243	mid-bump						
	1243	10 000	inc						
6	σ	384	dec	-	-	-	19.5	15.0	12.5
	384	1492	mid-bump						
	1492	10 000	inc						
7	σ	515	dec	-	-	-	15.3	12.3	10.6
	515	1906	mid-bump						
	1906	9349	inc						
	9349	10 000	mid-bump						
8	σ	178	dec	σ	σ	σ	12.0	9.2	7.6
	178	708	mid-bump						
	708	9124	inc						
	9124	10 000	mid-bump						
9	σ	50	dec	-	-	-	13.6	9.5	7.5
	50	176	mid-bump						
	176	10 000	inc						

threshold for each fault varies with V_{DD} . This has a significant implication for testing: the maximum fault coverage depends on selecting the best test patterns/ V_{DD} pairs. The maximum fault coverage is given by the minimum resistance detection thresholds, which are boldface in Table IV.

For gross delay faults, it can be observed that for fault number 3, the minimum $RO_{TH}(\sigma)$ is obtained for all V_{DD} . This is because the fault in this case was propagated along the longest path, therefore, any resistance value exceeding 0 Ω would be detected. For other faults, it is observed that the minimum RO_{TH} can be found at V_{DDH} , which substantiates the observations/expectations in [7], [10], and [13]. Only half of the small delay faults have reported results, because, only test patterns sensitizing short paths were considered. This results in a lower detection threshold (i.e., $RO_{TH}^S < RO_{TH}^G$ for each V_{DD}), as shown in the table. An interesting observation is that the minimum RO_{TH} is not always achieved at V_{DDH} . For example, for fault number 5 the minimum threshold is found at V_{DDL} . This highlights some

Fig. 9. ROF behaviors' proportions for different benchmark circuits.

Fig. 11. ROF behavior analysis for different transition test patterns.

Fig. 10. Average ROF detection thresholds for different benchmark circuits (falling transitions).

Fig. 12. ROF detection threshold analysis for different transition test patterns.

challenges in selecting the optimal test pattern/ V_{DD} for test, especially when considering multi-voltage designs.

Fig. 9 shows the behavior interval statistics for different benchmark circuits in 130-nm technology, using falling transition test patterns. The figure shows the dominance of the “dec” behavior over all the other behaviors. On average, the probability of encountering “dec” behavior is 5 times more than the probability of encountering “inc” behavior. This is because a logarithmic distribution probability is assumed for RO. Since the “dec” behavior is dominant for small RO values, this results in a high global occurrence for “dec.” One implication is that exploiting the “inc” behavior to distinguish ROFs from other types of faults can miss a significant range of faults. Therefore, exploiting the “mid-bump” behavior—in addition to the “inc” behavior—is promising.

The average detectability (i.e., resistance detection threshold) for small delay faults (SDF) and gross delay faults (GDF) with respect to V_{DD} for a number of benchmark circuits is depicted in Fig. 10. For each circuit, the RO_{TH} is shown at each V_{DD} for SDF as [SDF(VDDL), SDF(VDDM), and SDF(VDDH)] and for GDF as [GDF(VDDL), GDF(VDDM), and GDF(VDDH)]. A general observation from the individual circuits and from the average is that the minimum average

detection threshold for both SDF and GDF is always achieved at the highest V_{DD} , i.e., V_{DDH} . Testing at the highest V_{DD} is, therefore, the most effective single voltage test strategy. However, for optimum fault detection, individual consideration of faults has to be made to avoid test escapes for faults such as that reported in Table IV (fault number 5).

The effects of the transition test patterns on the observability and detectability are illustrated in Figs. 11 and 12, respectively. For each circuit, rising transitions (R) and falling transitions (F) were applied to all fault locations. Fig. 11 shows the proportion of the identified behavior intervals in the resistance domain for falling (F) and rising (R) transitions. Fig. 11 shows that the observability of different behaviors is significantly reduced when using rising transition test patterns compared to falling. While the intrinsic fault-free path delay behavior is almost insensitive to the transition type, the intrinsic fault behavior exhibits different patterns (“inc” and “constant” behaviors) with falling and rising transitions. This leads to a significant reduction of the observable “inc” behavior in faulty paths. The ROF detectability with V_{DD} is illustrated in Fig. 12. For some circuits (e.g., c17, s27, and b01), falling transitions result in lower detection thresholds, whereas in other circuits (e.g., c432) lower thresholds are achieved by rising transitions. The results show that,

Fig. 13. ROF behavior analysis for different technologies.

Fig. 14. ROF detection threshold analysis for different technologies.

in general, different test patterns and particularly transition patterns induce different fault behaviors and detectability. This highlights the significance of selecting the proper test pattern.

To investigate the fault behavior and detectability across technologies, technologies in Table I were considered. Similar results were observed when using falling and rising transitions. However, only results for falling transitions are presented. Fig. 13 shows the behavior for different technologies and the ROF detectability for the same circuits and technology models is depicted in Fig. 14. The observability of different behaviors (especially the “inc” behavior) is reduced for small nanometric technologies (32 and 16 nm) compared to larger technologies (130 nm and 65 nm). On the other hand, from Fig. 14, 32- and 16-nm technologies have larger detection thresholds—the detectable resistance range is reduced.

The results reported in Figs. 13 and 14 can be attributed to the difference in the electrical characteristics of the newer technologies (e.g., metal gates, strained Si, and hi-K dielectric insulator). A possible implication from the results is that the reduced observability is likely to limit the effectiveness of fault distinguishing methodologies and therefore a concern is raised about how to distinguish and screen faults with such non-unique behaviors. The observed reduction in the average detectable resistance range in new technologies could

raise the importance of detecting larger resistance ranges by means of small delay fault testing. Undetectable ROFs are likely to cause infant mortality failures and thus pose potential reliability risks.

VII. DISCUSSION—PRACTICAL CONSIDERATIONS

A. Process Variability

Process variability will degrade circuit performance, especially at low V_{DD} [25]. Hence, the relative fault detectability at different V_{DD} values will be critically affected. Additionally, variations in transistor threshold voltages could potentially affect the fault behavior. However, conceptually the model would still be the same. The only practical difference would be that the model parameters would be expressed as ranges instead of as points.

To verify this, the effect of process variation has been investigated by considering two cases:

- 1) by assuming that process variation only worsens the longest path and that the faulty path is not affected;
- 2) by assuming that process variation worsens both the faulty and longest path delays.

The variation in case 1 can be simply modeled by scaling the delay of the longest path. In this case, the scaling was 1.2, 1.22, and 1.24 for delays at high, mid, and low V_{DD} values, respectively. These ratios were obtained from a Monte Carlo analysis, which considered a 130-nm technology for a 12 inverter chain circuit [25]. The variations in case 2 were implemented using high V_t transistor models.

It was found that process variations cause the model parameters to shift from being point values to being distributed values. For example, without considering process variation, the first critical behavioral resistance (RO_{cr}^{01-02}) for fault#1 in Table IV, column 3, is 460 Ω . When considering process variations, this becomes a range from 460–780 Ω . Similar observations for other detectability parameters can be made, e.g., for the resistance detection threshold ($RO_{TH}(V_{DD})$).

B. Simulation

The modeling work discussed in this paper has been done using exhaustive analog simulations. This is fine for this investigation, as simulation accuracy was crucial for our analysis and deductions. However, considering this model for test generation applications would clearly be inefficient for large designs, due to the excessive time required in the adopted analog simulation. To overcome this problem, cell-based statistical timing simulators can be used. The premise of these simulators is that propagation delays can be calculated for a circuit, given extensive simulation results for different input transitions/output loading possibilities of all standard cells. An example of such a simulator uses a comprehensive Monte Carlo-based SPICE simulation library for all instantiated standard cells, [33]. For a given transition test pattern applied to a circuit, the simulator provides the worst delay for different circuit instances. Essentially, the simulation efforts would be mainly on small standard cells which would typically be run once. Eventually, a significant reduction in the overall

simulation time would be achieved. A rough estimate from simulator performance [33] shows that the use of a cell-based-like simulator could make the simulation of the largest s38584 circuit (from ISCAS-89) comparable to that of a circuit as small as the c432 circuit (from ISCAS-85) considered in this paper.

VIII. CONCLUSION

With the increasing use of multiple supply voltages in testing low power design and distinguishing resistive open faults, the effect of supply voltage on fault behavior and detectability must be clearly presented. ROFs, which represent frequent manufacturing failures and cause delay violations and potential reliability risks, were considered. The behavior and detectability of ROF were analyzed as a function of a discrete set of supply voltages. Simulations showed that the behavior of an ROF is a function of the resistance and the detectable resistance range varies with V_{DD} . These observations were used in a general voltage-aware fault model. It is demonstrated that the full resistance continuum of open faults can be treated as set of continuous intervals representing the behaviors and that three detection ranges are sufficient. The methodology of identifying the model parameters using exhaustive circuit-level simulations, searching and interpolation was described.

Using the model, it was shown that the observability of resistive open delays that increase with V_{DD} is reduced in new technologies. This poses a concern as to whether screening methods that rely on that unique behavior of resistive opens will still be effective for future technologies.

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