Improvement on Ge/GeO_x/Tm₂O₃/HfO₂ Gate Performance by Forming Gas Anneal

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Abstract—The improvement of forming gas anneal (10 % H₂ in N₂) at 400 °C on electrical properties of Ge/GeO_x/Tm₂O₃/HfO₂ gate stacks is investigated. It is found that forming gas anneal effectively suppresses fixed charge density, oxide trap density and interface state density. Hydrogen is demonstrated to efficiently passivate the negative fixed charge density and reduce the global variability of the flatband voltage down to 90 mV over a wafer. A forming gas anneal is also found to reduce equivalent oxide thickness in scaled gate stacks.

Keywords—germanium, Tm₂O₃, MOS, high-*k*, interface state density, fixed charge density, forming gas anneal

I. INTRODUCTION

Recently, Ge has received significant research interest as a high-mobility channel material for CMOS applications. One of the main challenges in Ge-based device fabrication is high quality Ge/high-*k* gate stack formation. Sufficient Ge passivation has been demonstrated by using GeO_x interfacial layer between Ge and high-*k* dielectric, and interface state density (*D*_{it}) in the range of 10¹¹ eV⁻¹cm⁻² has been achieved by using plasma post-oxidation in Ge/GeO_x/Al₂O₃ gates [1]. Further improvement in the gate stack performance was realized by integrating HfO₂ in the gate stack fabrication resulting in equivalent oxide thickness <1 nm [2]. Moreover, by using thermal oxidation by rapid thermal anneal (RTA), we have demonstrated Ge/GeO_x/Tm₂O₃ gates with *D*_{it} < 5·10¹¹ eV⁻¹cm⁻² [3].

All results were achieved without including a forming gas anneal (FGA) in the device fabrication scheme. While the positive effects of FGA in H₂ atmosphere on Si devices are well known [4]–[6], the impact of FGA on Ge gates is still debatable [7]. No interface state density improvement was observed after N₂, H₂, D₂, atomic-H and atomic-D post deposition anneal (PDA) in Ge/GeO_x/Al₂O₃ gates [8]. On the other hand, interface state density reduction has been demonstrated in Ge/Ge-nitride gates after FGA [9]. A further investigation of the effect of FGA on Ge/GeO_x interfaces could be beneficial for Ge gate stack advancement and is therefore conducted in this study.

We have investigated the impact of FGA on interface state density, oxide trap density (*N*_{ox}), fixed charge density (*N*_f) and EOT in Ge/GeO_x/Tm₂O₃/HfO₂ gates. FGA is shown to significantly improve the electrical characteristics of Ge gate stacks.

II. EXPERIMENTAL

Ge MOS capacitors were fabricated on virtual Ge substrates. The virtual substrates of 2.5 μm thickness were created by growing Ge strain relaxed buffers on 100 mm Si wafers in a two-step process by chemical vapor deposition (CVD) at 20 Torr pressure using germane precursor (10 % GeH₄ in H₂) and H₂ carrier gas, ending in a post epitaxial bake at 890 °C [10]. The virtual substrates exhibited a background p-type doping of ~10¹⁵ cm⁻³, a threading dislocation density of ~10⁷ cm⁻² and an RMS surface roughness <1 nm. After the virtual substrate growth, the wafers were stored in an N₂ purged load lock in order to reduce contamination and oxidation of Ge surface.

The MOS capacitor fabrication flow and the resulting device structure is displayed in Fig. 1. First, 400 nm plasma-enhanced CVD SiO₂ was deposited on Ge virtual substrates and active areas were defined by a combination of reactive ion etching (RIE) and 1 % HF etching. Immediately after HF dip, the wafers were loaded in an atomic layer deposition (ALD) reactor where Tm₂O₃ layer (0.4–7.4 nm thickness) was deposited using (C₃H₅)₃Tm and H₂O precursors at 225 °C [11]. After Tm₂O₃ deposition, the wafers were oxidized in O₂ ambient using lamp heated RTA system at 475 °C for 1–5 min. High-*k* HfO₂ (5.6 nm) was deposited by ALD at 350 °C using Hf[C₅H₄(CH₃)₂]₂(OCH₃)CH₃ and H₂O precursors, followed by annealing in O₃ for 10 min at the same temperature without breaking vacuum. After gate metal TiN (14 nm) deposition by ALD at 425 °C using TiCl₄ and NH₃, 500 nm Al was deposited by sputtering and the metal stack was patterned by RIE. Finally, FGA (10 % H₂ in N₂)

Fig. 1. Fabrication process flow and resulting Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitor structure (not to scale).

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was performed for 30 min at 400 °C.

MOS capacitors ($100 \times 200 \mu\text{m}^2$) were electrically characterized with capacitance-voltage (CV) measurements at 10 kHz frequency before and after FGA. Interface state density in the midgap was evaluated by comparing calculated CV characteristics with superimposed D_{it} distribution to the measured ones, as described in [12]. Oxide trap density was extracted from the hysteresis of dual CV sweep from inversion to accumulation and back. Fixed charge density was evaluated using the shift of the flatband voltage from a calculated value given the known work function of our ALD TiN (4.4 eV) and assuming no defects in the gate oxide.

III. RESULTS AND DISCUSSION

A. Impact of Forming Gas Anneal on Fixed Charge Density

CV characteristics of 100 Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors over a 100 mm wafer were measured before and after FGA. A thick 7.4 nm Tm₂O₃ layer was employed in the gate stack and a 5 min long post deposition O₂ oxidation was performed, resulting in well behaved CV characteristics and low gate leakage current below the noise level of the measurement set-up ($< 1 \cdot 10^{-8}$ A/cm²). CV characteristics are displayed in Fig. 2 where flatband voltage shifts ΔV_{FB} due to the fixed charge in the gate stack are indicated. A striking feature of CV characteristics before FGA is the large variation in the flatband voltages with a V_{FB} range of ~600 mV. After FGA this variation is greatly reduced resulting in the range of 90 mV.

Flatband voltage before FGA also exhibits a large positive voltage shift compared to calculated V_{FB} where no fixed charge density is assumed (calculated V_{FB} is indicated by solid blue line in Fig. 2). Positive voltage shift is a result of negative fixed charge density (N_f) of $3.9 \pm 1.1 \cdot 10^{12} \text{ cm}^{-2}$ in Ge/GeO_x/Tm₂O₃/HfO₂ gates. After FGA, flatband voltage shifts negatively, resulting in positive N_f of $8.5 \pm 1.7 \cdot 10^{11} \text{ cm}^{-2}$. Ab-initio calculations has shown that positive fixed charge density in Ge/GeO₂ interfaces is related to oxygen vacancies in GeO₂ layer [13]. Oxygen vacancies can possibly be created during the initial gate stack formation, or during FGA due to GeO_x reduction by more stable Tm₂O₃. Nevertheless, hydrogen in FGA effectively

Fig. 2. CV characteristics of 100 Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors before and after forming gas anneal. Flatband voltage V_{FB} , calculated assuming TiN work function of 4.4 eV and no fixed charge density, is displayed as a solid blue line, and flatband voltage shifts ΔV_{FB} due to fixed charge density are indicated. A large spread in V_{FB} as well as large ΔV_{FB} is observed before FGA. After FGA ΔV_{FB} and the variation in V_{FB} is reduced.

passivates the defects associated with the large amount of negative fixed charges created during the gate stack formation, leading to a significant (> 4 times) reduction of N_f and its variability over a wafer, as summarized in Table I.

B. Impact of Forming Gas Anneal on Oxide Trap Density

Dual CV hysteresis sweeps were used to extract oxide trap density in Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors before and after FGA. Hysteresis at 3 MV/cm oxide field was reduced by FGA from 370 mV to 76 mV, which corresponds to 5 times reduction in N_{ox} , as shown in Table I. Oxide trap density as a function of oxide electric field is displayed in Fig. 3, showing even higher N_{ox} reduction at higher electric fields.

C. Impact of Forming Gas Anneal on Interface Trap Density

The impact of forming gas anneal on the interface state density is depicted in Fig. 4 where D_{it} before and after FGA is compared. The exact same 20 devices were characterized before and after FGA. The average interface state density is reduced about two times after FGA, from $4.2 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ to $1.8 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. Even though interface state density reduction in Ge/GeO_x/Tm₂O₃/HfO₂ gates is lower compared to Si/SiO₂/HfO₂ gates [6], hydrogen still plays a role in interface trap annealing.

To further investigate interface state density at thinner EOT, Ge/GeO_x/Tm₂O₃/HfO₂ gates were scaled by reducing the Tm₂O₃ thickness. D_{it} as a function of Tm₂O₃ thickness is displayed in Fig. 5 before and after FGA. D_{it} exhibits an increasing trend when the Tm₂O₃ thickness is reduced, reaching $9 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ and $6 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ at 0.4 nm Tm₂O₃ thickness before and after FGA, respectively. Even though interface state density reduces at all Tm₂O₃

TABLE I. FIXED CHARGE DENSITY, OXIDE TRAP DENSITY AND INTERFACE STATE DENSITY BEFORE AND AFTER FGA

	N_f	N_{ox} at 3 MV/cm	D_{it}
Before FGA	$-39 \pm 11 \cdot 10^{11} \text{ cm}^{-2}$	$15 \cdot 10^{11} \text{ cm}^{-2}$	$4.2 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$
After FGA	$+8.5 \pm 1.7 \cdot 10^{11} \text{ cm}^{-2}$	$2.8 \cdot 10^{11} \text{ cm}^{-2}$	$1.8 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$

Fig. 3. Oxide trap density N_{ox} versus oxide electric field E_{ox} before and after FGA. Forming gas anneal reduces N_{ox} over the whole measured E_{ox} interval, and the reduction increases at higher oxide field.

Fig. 4. Interface trap density D_{it} versus equivalent oxide thickness EOT of Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors before and after FGA, showing D_{it} reduction by a factor of 2 after FGA. The same 20 devices were characterized before and after FGA.

Fig. 5. Interface trap density D_{it} as a function of Tm₂O₃ thickness in Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors before and after FGA. All samples received 5 min oxidation after Tm₂O₃ deposition. Interface state density is reduced for all Tm₂O₃ thicknesses. The lines are guides for the eye.

thicknesses, the relative improvement is lower when Tm₂O₃ layer is thinner.

Another way to scale EOT in Ge/GeO_x/Tm₂O₃/HfO₂ gates is by reducing the O₂ oxidation time after Tm₂O₃ deposition. O₂ oxidation is responsible for creating GeO_x layer between Ge and Tm₂O₃. By reducing the oxidation time, a thinner GeO_x layer can be realized. Varying O₂ oxidation times (1-5 min) were employed in MOS capacitors with 1.4 and 2.4 nm Tm₂O₃ thickness. Interface state density in MOS capacitors with different Tm₂O₃ thicknesses and oxidation times is summarized in Fig. 6 as a function of EOT before and after FGA. Interface state density increases drastically when EOT is scaled down to 1.5 nm. While FGA is effective in reducing D_{it} to below $5 \cdot 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ in gates with $\text{EOT} \geq 2 \text{ nm}$, D_{it} reduction in gates with thinner EOT is less significant.

As evident from the sharp interface state density increase at thin EOT, it is challenging to passivate the Ge surface with a combination thin Tm₂O₃ barrier and short O₂ oxidation time. Degraded interface state density at thin EOT is possibly

Fig. 6. Interface trap density D_{it} versus equivalent oxide thickness EOT of Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors with different Tm₂O₃ thicknesses and oxidation times. Open and filled symbols mark the measurement results before and after FGA, respectively. While D_{it} is reduced by FGA in all EOT interval, a significant D_{it} degradation occurs when EOT approaches 1.5 nm.

also linked to the surface roughness of the employed Ge virtual substrate (RMS $\sim 1 \text{ nm}$), which results in one or more monolayers surface steps. When Tm₂O₃ thickness and O₂ oxidation time are scaled, the larger surface steps might not be uniformly covered by GeO_x/Tm₂O₃ stack and some intermixing between GeO_x and HfO₂ can occur. This intermixing would then result in degraded interface state density [2]. It is possible that if substrates with lower surface roughness were used (e.g. by employing chemical mechanical polishing of the Ge surface), interface state density increase would occur at even lower EOT.

D. Impact of Forming Gas Anneal on Equivalent Oxide Thickness

Equivalent oxide thickness before and after FGA is displayed in Fig. 7 as a function of Tm₂O₃ thickness. A nonlinear reduction of EOT is observed when Tm₂O₃ layer thickness is reduced, reaching $\sim 2 \text{ nm}$ at Tm₂O₃ layer

Fig. 7. Equivalent oxide thickness as a function of Tm₂O₃ thickness in Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors before and after FGA. All samples received 5 min oxidation after Tm₂O₃ deposition. EOT nonlinearly depends on Tm₂O₃ thickness. After FGA, EOT is slightly reduced for Tm₂O₃ thickness $< 1.5 \text{ nm}$. The lines are guides for the eye.

Fig. 8. Equivalent oxide of Ge/GeO_x/Tm₂O₃/HfO₂ MOS capacitors with 1.4 nm Tm₂O₃ layer as a function of oxidation time before and after FGA. Each point represents an average over 5 MOS capacitors while the error bars indicate the range. Forming gas anneal reduces EOT by ~0.2 nm.

thickness ≤ 1.4 nm. This trend can be explained by the fact that GeO_x formation during O₂ oxidation step is dependent on Tm₂O₃ layer thickness. Ge is further oxidized when the Tm₂O₃ layer is thinner and vice versa. Consequently, a lack of EOT dependence on Tm₂O₃ thickness is observed when Tm₂O₃ layer is thin.

Forming gas anneal has no significant effect on EOT when Tm₂O₃ layer thickness is above 2 nm, as evident from Fig. 7. However, a small EOT reduction is observed after FGA in MOS capacitors with thinner Tm₂O₃ layer. This can be seen more clearly in Fig. 8 where EOT of MOS capacitors with 1.4 nm Tm₂O₃ thickness is displayed as a function of oxidation time before and after FGA. Here the same MOS capacitors were measured before and after FGA, and each point represents the average EOT while error bars indicate the range. As can be seen from Fig. 8, EOT is reduced by ~0.2 nm after FGA. Forming gas anneal is thus not only efficient in reducing fixed charge, oxide trap and interface charge densities but also equivalent oxide thickness in scaled Ge/GeO_x/Tm₂O₃/HfO₂ gates.

IV. CONCLUSION

The impact of forming gas anneal on fixed charge density, oxide trap density, interface trap density and equivalent oxide thickness in Ge/GeO_x/Tm₂O₃/HfO₂ gates has been investigated. FGA has been shown to efficiently passivate the negative fixed charge density, achieving a positive fixed charge density of $8.5 \cdot 10^{11} \text{ cm}^{-2}$ and reducing the global variability in flatband voltage down to 90 mV over a wafer. Furthermore, FGA reduces the oxide trap density 5 times and interface trap density by a factor of 2. Moreover, in

Ge/GeO_x/Tm₂O₃/HfO₂ gates with thin equivalent oxide thickness ≤ 2 nm, an EOT reduction by 0.2 nm after FGA has been demonstrated.

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