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Noise Analysis of Current-Feedback DC-Servo Loop in Current-Balancing Chopper Amplifiers

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Abstract—Chopper amplifiers for biopotential acquisition commonly suppress differential electrode DC offsets by using a DC-servo loop (DSL). However, the noise contribution of the DSL is always neglected in noise analysis. The noise introduced by the DSL, in particular at low frequencies, is of great importance in biosensor applications. This work presents the noise modeling of a current-balancing chopper amplifier with DSL and describes the effect of the DSL on the noise performance. Two different DSL implementations are analyzed. It is found that the exact placement of the chopper in the DSL has a strong impact in the noise performance; therefore, its placement cannot be arbitrarily selected. A circuit topology to minimize its noise contribution is then proposed and verified by simulation.

Index Terms—biopotential acquisition, low-noise chopper amplifier, dc-servo loop, noise analysis, noise modeling

I. INTRODUCTION

Biopotential signals such as electrocardiography (ECG), electromyography (EMG), and electroencephalography (EEG) are typically weak and mainly distributed in a low-frequency range [1]. Accordingly, they are vulnerable to low-frequency noise, especially the 1/f noise present in CMOS amplifiers. A commonly used circuit design technique to cope with this problem is to employ chopper stabilized amplifiers. These amplifiers have been extensively used in biosensor front-ends due to their advantages of 1/f noise suppression, low-offset, continuous-time operation, and low noise-folding compared to autozeroing technique [2].

In addition to stringent 1/f noise requirements, biopotential amplifiers suffer from the electrode DC offset (EDO) that comes from the difference in the electrode half-cell potentials at the electrode-electrolyte interface, generally up to tens of mV for gel electrodes [3]. Therefore, the amplifier requires AC-coupling characteristic to eliminate the EDO as it can saturate the amplifier chain and distort the signal.

Conventionally, AC-coupled amplifiers are realized by placing a series DC-blocking capacitor at the input as illustrated in Fig. 1a. However, very large capacitors are commonly required in order to achieve extremely low cut-off frequencies, which is something undesirable in multi-channel recording applications as they take up a large silicon area. Besides the area penalty, capacitively-coupled chopper instrumentation amplifiers (CCIA) have low input impedance since a switched-capacitor resistance presents at the input. The input impedance of a CCIA is approximately $1/2f_{chop}C_{in}$, where $f_{chop}$ is the chopping frequency and $C_{in}$ is the series DC-blocking capacitor [4]. In addition, the mismatch between the series capacitors, $C_{in}$, makes the CCIA sensitive to large common-mode interference.

Alternatively, the AC-coupling can be attained by using active feedback as demonstrated in Fig. 1b. This topology is also known as DC-servo loop (DSL) and consists of an integrator in a negative feedback loop. The DC component and low frequency offset at the output are extracted by the integrator and fed back to the input where they are subtracted [5]. This approach does not require huge capacitors and also offers the benefit of rejecting both EDO and input offset.

Despite the benefits gained from the DSL, one of the major drawbacks is the additional electronic noise that is introduced, which can easily dominate and become very detrimental in low-noise biosensor applications. Many efforts have been put into noise analysis and optimization of chopper amplifiers [6]–[8]. Unfortunately, a comprehensive analysis of the noise contribution of the DSL has not gained much attention. However, the noise of a poorly designed DSL might become the main noise contributor. In this study, the noise contribution of the DSL is carefully investigated and a circuit topology to minimize its contribution will be proposed.

This work is structured as follows. Section II briefly describes the operation principle and the circuit implementation of a chopper amplifier with DSL. In Section III, the noise analysis of a chopper amplifier is presented and the effect of the DSL including its noise contribution is discussed. The proposed design to improve the noise performance is then shown in Section IV and verified with simulation results. Finally, a brief summary and a conclusion are presented in Section V.

![Fig. 1: Block diagram of AC-coupled amplifiers.](image-url)
II. BASIC PRINCIPLE & CIRCUIT IMPLEMENTATION

A. Chopper Stabilization Technique

The basic principle of a chopper-stabilized amplifier is illustrated in Fig. 2. The input signal is up-converted by the input chopper to the chopping frequency $f_{\text{chop}}$. The electronic noise, including 1/f noise and thermal noise, of an amplifier is then added to the chopping-modulated signals. Thanks to the up-modulation of the signal before being amplified, the 1/f noise does not present in the frequency band of interest if the condition of $f_{\text{chop}} > f_c$ is fulfilled, where $f_c$ is the corner frequency of the 1/f noise. After amplification, the signal of interest is down-converted to baseband while the unwanted 1/f noise is up-converted to $f_{\text{chop}}$. The signal of interest can be extracted and the noise located at odd harmonics of $f_{\text{chop}}$ can be suppressed by a low-pass filter.

![Fig. 2: Conceptual diagram of chopper stabilization technique.](image)

B. DC-Servo Loop

The DC component accompanying the biopotential signals is amplified by the DSL amplifier; therefore, a negative feedback DC cancellation loop is implemented in order to eliminate it as depicted in Fig. 3. Assuming that $f_{p1} \gg f_{p2}$, the overall transfer function is given by:

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 + s/2\pi f_{p2}}{A_2 + \frac{1}{1 + (1 + s/2\pi f_{p1})(1 + s/2\pi f_{p2})}/A_1 A_2}$$

$$\simeq \begin{cases} \frac{1}{A_2} & \text{for } f < f_{p2} \\ \frac{1}{1 + s/2\pi f_{p1}} & \text{for } f > f_{p1} \end{cases}$$

(1)

Accordingly, the cut-off frequency of the high-pass response is $A_1 A_2 f_{p2}$ and the DC component is suppressed by $20\log(1/A_2)$ dB.

The noise contribution of the DSL can be analyzed by extracting the transfer function from the input-referred noise of the DSL, $V_{n,DSL}$, to the output of the amplifier $V_{\text{out}}$. For low frequencies the noise transfer function is:

$$NTF_{DSL} = \frac{V_{\text{out}}}{V_{n,DSL}} = -\frac{A_1 A_2}{1 + A_1 A_2} \simeq -1$$

(2)

Consequently, the low-frequency noise of the DSL appears at the output without attenuation and it may become a significant noise contributor to the core amplifier.

C. Circuit Implementation of Current-Balancing Chopper Amplifier with DC-Servo Loop

The current-balancing instrumentation amplifier (CBIA) is depicted in Fig. 4, consisting of a transconductance amplifier (Gm) and a transimpedance amplifier (TIA). This is a popular architecture for low-power and low-noise biopotential amplifier as it offers higher CMRR compared to the traditional three-OPAMP IA structure. The implementation of the DSL in a CBIA is realized either through a current feedback (CF-DSL) [9] or through a voltage feedback (VF-DSL) [7] as shown in Fig. 4a and Fig. 4b respectively. In CF-DSL, the DC offset cancellation takes place at the internal nodes of CBIA. On the other hand, in VF-DSL the DSL is directly fed back to the input of the CBIA through capacitors. The CF-DSL has the advantage of eliminating the need for capacitors, saving the silicon area and avoiding CMRR degradation due to capacitor mismatch. In this work, CF-DSL is selected as the circuit architecture under investigation.

![Fig. 3: Signal flow of an amplifier with DSL.](image)

![Fig. 4: Block diagram of a current-balancing IA with DSL.](image)
The chopper stabilization technique is applied to the CBIA in order to achieve noise immunity to 1/f noise. The choppers, consisting of four switches, are added to the circuit for chopping modulation. As discussed in Section II, the input chopper up-converts the input signal, comprising of biopotentials and unwanted EDO, to $f_{chop}$. Subsequently, the EDO is modulated from DC to $f_{chop}$ and becomes a square wave at the input of the amplifier. Therefore, the extracted DC component in the DSL requires an up-conversion so as to subtract the modulated EDO. However, it brings out a design choice of where to place the chopper within the loop. The modulation can happen either at the output of the loop or at the output of the integrator. The main difference is the noise modulation, which affects the overall noise performance and that will be discussed thoroughly in Section III.

### III. Noise Analysis

The thermal noise and 1/f noise are the most critical noise sources in CMOS low-noise amplifier design. In this section, the effects of chopping modulation and the DC-servo loop on the noise performance of an amplifier will be theoretically analyzed.

#### A. Effect of Chopping Modulation on the Amplifier’s Noise

The noise model of a chopper instrumentation amplifier is depicted in Fig. 5. The noisy amplifier is equivalently represented by its input-referred voltage source ($V_{n,IA}$) in series and its input-referred current source ($I_{n,IA}$) in parallel to a noiseless amplifier. The total input-referred noise PSD is then calculated by:

$$S_{N,in}(f) = \frac{V_{n,IA}^2}{2} + 2I_{n,IA}Z_s^2$$

where $Z_s$ is the source’s impedance. For low frequencies and high input impedance, the first term in (3) dominates. Equation (3) can be rearranged to a thermal noise term, $S_{N0}$, added with a low-frequency 1/f noise term as given in (4) where $f_c$ implies the corner frequency. The equivalent input noise is then amplified by the voltage gain, $A_0$, and modulated with the output chopper. The output noise PSD is the summation of the replicas of the noise spectrum located at odd harmonic frequencies of $f_{chop}$.

$$S_{N,out}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{k=-\infty}^{\infty} \frac{1}{k^2} A_0^2 S_{N,in}(f - kf_{chop})$$

where $k = 1, 3, 5, ...$

After the chopping demodulation at the output, the signal spectrum is shifted back to baseband. Accordingly, the output noise at baseband is crucial to the design. At baseband where $f \leq 0.5f_{chop}$, equation (5) is nearly constant and can be approximated by a white-noise PSD [2].

$$S_{N, out, baseband}(f) = A_0^2 S_{N0}(1 + \frac{17f_c}{2\pi^2 f_{chop}})$$

for $f_{cutoff} \gg f_{chop}$

where $f_{cutoff}$ is the cut-off frequency of the amplifier. It can be observed from (6) that the noise level at baseband is approximately equal to the thermal noise, $S_{N0}$, if the bandwidth of the amplifier is sufficiently larger than the chopping frequency.

#### B. Effect of DC-Servo Loop on Noise Contribution

Fig. 6 presents the noise model of the current-feedback DSL in which the DC offset-induced current is compensated by the output current of the $Gm_2$ stage. As discussed in Section II, the up-conversion in DSL can possibly take place at two locations as demonstrated in Fig. 6a and Fig. 6b respectively. In the circuit topology I, the chopper is located at the output of the $Gm_2$ stage. Since there is no noise modulation process between the $Gm_2$ stage and the integrator, the input-referred noise (IRN) of the DSL is directly calculated by:

$$V_{n, in, DSL}(s) = V_{n, in, INT}(s) + (s\tau)V_{n, in, Gm_2}(s)$$

where $\tau$ is the time constant of the integrator. The chopper up-conversion at the output of the DSL and the chopper down-conversion at the output of the amplifier result in $V_{n, in, DSL}$...
appearing at the output of the amplifier almost without attenuation. Therefore, 1/f noise from the integrator and the $Gm_2$ stage appear at low frequencies, resulting in a significant degradation in noise performance.

Alternatively, the chopper can be placed between the integrator and the $Gm_2$ stage as shown in Fig. 6b. In this topology, the noise of the $Gm_2$ stage is not modulated; therefore, 1/f noise of the $Gm_2$ stage remains at low frequencies. The equivalent input referred noise of the DSL is given by:

$$V_{n,\text{in},DSL}(s) = \left(\frac{\pi}{2}\right) \frac{s^7 V_{n,\text{out},DSL}}{Gm_2(s)}$$

$$= \sum_{k=-\infty}^{+\infty} -\frac{1}{2} V_{n,\text{in},INT}(f - kf_{\text{chop}}) + \left(\frac{s^7\pi}{2}\right) V_{n,\text{in},Gm_2}(f), k = 1, 3, 5, ...$$

$$V_{n,\text{in},DSL}$$ passes through the loop as described in (2), and its contribution to the output noise PSD is derived by:

$$S_{n,\text{out}}(f) = \left(\frac{2}{\pi}\right)^2 NTF_{\text{DSL}}^2 \sum_{k=-\infty}^{+\infty} \frac{1}{k^2} S_{n,\text{in},DSL}(f - kf_{\text{chop}})$$

$$k = 1, 3, 5, ...$$

Similar to the chopper amplifier, the output chopper transposes the noise of the $Gm_2$ stage to the odd harmonics of $f_{\text{chop}}$. Therefore, 1/f noise is up-converted and does not appear at baseband. The noise contribution of the $Gm_2$ stage at the frequencies of interest is mainly white noise. On the other hand, integrator’s noise is up- and down-converted. Hence, the 1/f noise and DC offset of the integrator appear at baseband and they can not be suppressed. The output PSD at baseband can be approximated by:

$$S_{n,\text{out,baseband}}(f) \approx (s^7)^2 S_{N0,Gm_2} \left(1 + \frac{17f_c}{2\pi^2 f_{\text{chop}}^2}\right)$$

$$+ \left(\frac{2}{\pi}\right)^2 S_{n,\text{INT}}(f)$$

Fig. 7 shows the comparison between topology I and II, topology II takes advantage of the chopper for improving noise performance, especially the low-frequency noise. According to the noise analyses of these two topologies, we can draw a conclusion that a CBIA can not be fully free from 1/f noise if a DC-servo loop is present in a CBIA for EDO cancellation, but the noise can be reduced by proper selection of circuit architecture, sizing of components, and biasing.

So far, the noise contribution of the DSL to the output noise PSD has been identified. For further noise optimization, we are interested in the effect of DSL’s noise on the input-referred noise of the amplifier, especially at low frequencies where the 1/f noise of the integrator dominates. The input-referred noise is calculated as $V_{n,\text{out},DSL}(s)/H(s)$, where $H(s)$ is the transfer function of the CBIA with DSL. As we have derived in (1), the transfer function is inversely proportional to the gain of DSL at low frequencies. Accordingly, the 1/f noise components of the input-referred noise can then be calculated by:

$$S_{1/f,\text{CBIA}}(f) \cong S_{1/f,\text{INT}}(f) \left(\frac{Gm_2}{s^7 Gm_1}\right)^2$$

The 1/f noise component is proportional to the ratio of $Gm_2/Gm_1$. Therefore, minimizing this ratio is desired for noise optimization. However, $Gm_2$ is related to the loop gain of DSL and hence the attenuation of the EDO as given in (1). On the other hand, power consumption can be traded off for maximizing $Gm_1$. It can be concluded that there are two design considerations for the design of CBIA with CF-DSL: (i) trade-off between noise and EDO attenuation (ii) trade-off between noise and power consumption.

IV. SIMULATION RESULTS & DISCUSSION

A conventional CBIA with a CF-DSL is designed and simulated using a standard 180nm CMOS process. The transistor-level circuit schematic is presented in Fig. 8. The chopping frequency is chosen to be 10kHz and the core CBIA is designed to have sufficient bandwidth such that $f_{\text{chop}} > f_{\text{chop}}$. A Spectre®RF simulation is performed on three possible topologies: (i) CBIA with CF-DSL without chopping modulation, (ii) Chopper CBIA with CF-DSL topology I (blue chopper), and (iii) Chopper CBIA with CF-DSL topology II (brown chopper). The periodic steady-state (PSS) response of the circuits is determined first. Then the noise performance and AC response are simulated according to the periodic operating points obtained from the PSS simulation. All the simulation results presented below are based on the same PSS analysis setup (shooting method with $f_{\text{beat}} = f_{\text{chop}}$ and maxsideband = 20).

Fig. 9 shows simulated pnoise of three amplifier topologies. The noise of each topology and its corresponding noise breakdown is presented in Fig. 10. The noise of the amplifier without chopping modulation is relatively high in the low-frequency range due to the 1/f noise from the core $Gm_1$ and the CF-DSL. In this sample design, it can be reduced by around 13% when the chopping technique is applied to the core $Gm_1$ and the CF-DSL is configured as topology I. In this topology, the 1/f noise of the core $Gm_1$ is suppressed significantly because of the up-modulation process, but the 1/f noise of the $Gm_2$ stage and the integrator within the feedback loop still remain at low frequencies. In order to further improve the noise performance,
the chopper in the DSL is moved to the input of the $Gm_2$ stage as shown in the circuit topology II. As we have derived in (10), the 1/f noise of the $Gm_2$ stage disappears at baseband by using topology II, and the major noise contributor is the 1/f noise of the integrator. As a result, an additional 22% reduction in total integrated noise is reached under the condition that identical circuit blocks are used in the design.

The previous comparison shows that topology II offers the best noise performance. To further optimize noise, the noise contribution of the DSL using topology II is evaluated. As shown in (11), the input-referred noise is linearly proportional to the transconductance of the $Gm_2$ stage at low frequencies. Simulation results in Fig. 11 verify that the noise contribution of the DSL to the input-referred noise is reduced linearly as the transconductance decreases, and it also presents the relationship between the transconductance and suppression of low frequency components including DC. Accordingly, the design trade-off between noise performance and EDO attenuation can be clearly identified.

Fig. 9: Simulated input-referred noise of CBIA with CF-DSL.

Fig. 10: Comparison of integrated input-referred noise.

V. CONCLUSION

In this work, we presented a theoretical analysis for the noise contribution of the DC-servo loop (DSL) on chopper-stabilized CBIAIs used in biosensor applications. The noise contribution of two different circuit architectures of CF-DSL were thoroughly investigated. We found that low-frequency noise from the DSL can have a strong impact in the total noise performance. Therefore, its modeling and mitigation strategies are important for circuit design. In particular, we found that the exact placement of the chopper within the DSL is of paramount importance, and significant noise reduction can be
achieved by selecting the right architecture. These findings are validated through circuit simulation of both architectures. Finally, we demonstrate the design trade-off between noise optimization and DC rejection/power consumption. These are important results that can serve as general guidelines for designing low-noise biopotential amplifiers based on chopper-stabilized CBIAs.

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