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Fabrication and characterization of $GaAs_xP_{1-x}$ single junction solar cell on GaAs/Si for III-V/Si tandem solar cell

ELAHEH AGHAJAFARI

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Fabrication and characterization of $GaAs_xP_{1-x}$ single junction solar cell on Si for III-V/Si tandem solar cell

Elaheh Aghajafari

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Examiner:
Prof. Anand Srinivasan

Supervisors:
Prof. Sebastian Lourdudoss– Dr. Yanting Sun-
Axel Strömberg

KTH Royal Institute of Technology
School of Engineering Science
Department of Applied Physics

SE-100 44 Stockholm, Sweden

Abstract

Silicon based solar cells have been used as photovoltaic devices for decades due to reasonable cost and environment- friendly nature of silicon. But the conversion efficiency of silicon solar cell is limited; for instance, the maximum conversion efficiency of a crystalline silicon solar cell available in the market developed by Kaneka Corporation is 26 % [1]. In comparison, III-V compound semiconductor multi-junction solar cells are the most efficient solar cells with efficiency of 47.1% [2]. However, due to high-cost substrate materials, III-V solar cells are not the best option for large scale production in real life. Therefore, integration of III-V compound semiconductors on silicon substrate has been studied to obtain III-V/Si multi junction solar cells with high conversion efficiency with reasonable price. To this end, we studied epitaxial growth of $GaAs_xP_{1-x}$ on GaAs deposited on Si.

This thesis presents the characterization results of the above $GaAs_xP_{1-x}$ epitaxial layer and fabrication of a $GaAs_xP_{1-x}$ single junction solar cell on GaAs coated Si substrate and its performance.

In the first part of the project, $GaAs_xP_{1-x}$ epitaxial layer grown by Hydride Vapor Phase Epitaxy (HVPE) on different kinds of substrates at different growth conditions are characterized to identify the optimized growth conditions and a suitable substrate. Samples are characterized by High Resolution X-ray Diffraction (HRXRD) and photoluminescence (PL) to determine the composition of $GaAs_xP_{1-x}$ and its crystalline quality and by optical microscope to assess the surface morphology. Scanning Electron Microscope (SEM) is used to study the depth of the dry etched structures.

The second part of the project deals with the fabrication process consisting of 21 steps to obtain a $GaAs_xP_{1-x}$ single junction solar cell structure on GaAs/Si. This process flow will be explained in some detail along with a brief description of several tools in cleanroom that have been used for this purpose.

Finally, in the third part, devices are characterized to investigate their performance. Transmission Line Method (TLM) is used to obtain important parameters such as specific contact resistance. Current-voltage (I-V) relation of solar cell is investigated to acquire its efficiency. The lowest specific contact resistance measured in this project is $7.4 \times 10^{-8}\ \Omega.cm^2$ for p-contact (for 4041DV- cell 8) and the highest efficiency measured is 1.64% (for 4041DV- cell 6).

In conclusion, although the results obtained are far from the state-of-the art results, this work has laid the foundation for future work that can lead to a breakthrough in fabricating multi-junction tandem solar cell on silicon.

Key words: III-V semiconductor, $GaAs_xP_{1-x}$ heteroepitaxy, hydride vapor phase epitaxy, III-V/Si solar cell.

Abstrakt

Kiselbaserade solceller har använts i årtionden på grund av dess rimliga kostnad och miljövänliga natur. Omvandlingseffektiviteten för kiselsolcell är begränsad; till exempel är den maximala omvandlingseffektiviteten för solceller av kristallin kisel utvecklad av Kaneka Corporation 26 % [1]. Som jämförelse är III-V sammansatta halvledare multi-junction solceller de mest effektiva solcellerna med en effektivitet på 47,1 % [2]. På grund av de höga substratmaterialen är III-V-solceller i realiteter inte det bästa alternativet för storskalig produktion. Därför har integration av III-V sammansatta halvledare på kiselsubstrat studerats för att erhålla III-V/Si multi junction solceller med hög omvandlingseffektivitet till rimligt pris. För detta ändamål studerade vi epitaxiell tillväxt av $GaAs_xP_{1-x}$ på GaAs avsatt på Si.

Denna avhandling presenterar karaktäriseringsresultaten av ovanstående $GaAs_xP_{1-x}$ epitaxiella skikt och tillverkning av en $GaAs_xP_{1-x}$ enkel förbindelse solcell på GaAs-belagt Si-substrat och dess prestanda.

I den första delen av projektet karaktäriseras $GaAs_xP_{1-x}$ epitaxiallager odlat med Hydride Vapor Phase Epitaxy (HVPE) på olika typer av substrat vid olika tillväxtförhållanden för att identifiera de optimerade tillväxtförhållandena och ett lämpligt substrat. Prover kännetecknas av högupplöst röntgendiffraktion (HRXRD) och fotoluminescens (PL) för att bestämma sammansättningen av $GaAs_xP_{1-x}$ och dess kristallina kvalitet och med optiskt mikroskop för att bedöma morfologin. Scanning Electron Microscope (SEM) används för att studera djupet av de torretsade strukturerna.

Den andra delen av projektet behandlar tillverkningsprocessen som består av 21 steg för att erhålla en $GaAs_xP_{1-x}$ enda förbindelse solcellsstruktur på GaAs/Si. Detta processflöde kommer att förklaras i detalj tillsammans med en kort beskrivning av flera verktyg i renrum som har använts för detta ändamål.

Slutligen, i den tredje delen, karaktäriseras enheter för att frilägga dess prestanda. Transmission Line Method (TLM) används för att erhålla viktiga parametrar som specifikt kontaktmotstånd. Förhållandet mellan ström och spänning (I-V) hos solcellen undersöks för att uppnå optimal effektivitet. Den lägsta specifikt kontaktmotstånd som uppmätts i detta projekt är $7{,}4 \times 10^{-8}\ \Omega.cm^2$ för p-kontakt (för 4041DV-cell 8) och den högsta uppmätta effektiviteten är 1,64% (för 4041DV-cell 6).

Sammanfattningsvis, även om de erhållna resultaten är långt ifrån de senaste resultaten inom forskning, lägger detta arbete grunden för framtida arbete som kan leda till ett genombrott i tillverkningen av multi-junction tandemsolcell på kisel.

Nyckelord: III-V halvledare – $GaAs_xP_{1-x}$ epitaxiallager- hydridångfasepitaxi -III-V/Si solcell.

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List of acronyms and abbreviations

Si	silicon
GaAsP	Gallium arsenide phosphide
GaAs	Gallium arsenide
AsH_3	arsine
PH_3	phosphine
HRXRD	High resolution x-ray diffraction
SEM	Scanning electron microscopy
MOVPE	Metal organic vapor phase epitaxy
CMP	Chemical mechanical polishing
PECVD	Plasma enhanced chemical vapor deposition
HVPE	Hydride vapor phase epitaxy
ICP	Inductively coupled plasma etching
TLM	Transmission line method
FF	Fill factor
BSF	Back surface field

1 Introduction

Nowadays environmental problems caused by non-renewable energy sources have become a major issue around the world and investigating sustainable energies such as wind, sun etc., is inevitable. Sun is an essential source of renewable energy which is free and available widely in all parts of the earth and technology of using sunlight in industry has been improved significantly. The concept of photovoltaic effect was observed in 1839 for the first time and first solar cell was invented in 1883 [3] which was too inefficient. About seventy years later in 1954, first silicon (Si) solar cell was invented by researchers in Bell laboratory [4] that have been used widely around the world.

Traditional solar cells are fabricated of n-type and p-type Si to create a pn-junction and metal contacts on their top and bottom. Since only photons with energy higher than the bandgap of Si could be absorbed, the efficiency of single junction Si solar cell is so limited. Then many studies were done on III-V compound solar cells and their functionality. The materials used in III-V solar cells are compounds of elements of group III and V of the periodic table such as GaAs and GaAsP etc. Because of different bandgap energies, III-V solar cells absorb a broader range of solar spectrum and provide higher efficiency. However, due to their higher costs these have been exploited mainly in space applications and satellites and could not enter into terrestrial applications. Recently, scientists have been working on integrating III-V compound semiconductor on Si substrate to obtain high conversion efficiency at reasonably low price.

1.1 Basic knowledge of solar cell

The basis of a solar cell functionality is founded by generation of the voltage and electrical current in a material caused by the exposure to the light, a phenomenon that is referred to as the photovoltaic effect. Electrons and holes are separated from each other by the inherent field existing at the pn-junction in a solar cell and therefore voltage and electrical current will be created. By putting a n-type next to a p-type semiconductor a pn-junction is created which is the building blocks of a solar cell.

In the absence of any external load, free electrons (holes) in n-type (p-type) diffuse into the p-type (n-type) which creates a depletion region close to the interface containing positive charges in n-type and negative charges in p-type.

This charge imbalance produces an electric field inside the depletion region from n-side to p-side. When a photon with energy ($E = h\nu = \frac{hc}{\lambda}$) larger than the bandgap energy (E_g)of material shines on the material, it will excite electron in valence band and send it to conduction band and will leave a hole in valence band instead, this is called the absorption effect which creates electron-hole pairs.

When sunlight shines on solar cells, different wavelengths of photon are absorbed by pn-junction and electron-hole pairs are created. Electron goes to n-side (opposite side of electric field) and hole goes to p-side, as shown in yellow charges in Figure 1-1.

Now imagine there is a connection between metal contacts with wire, electrons will flow through the wire. Electrons are attracted to positive charges in p-type, so an electrical current will flow from p-side to n-side which is called photo current (I_{ph}) and in the absence of any external load, photo current is called short circuit current (I_{SC}). The potential between two metal contacts formed on p and n-sides, is called open circuit voltage (V_{OC}).

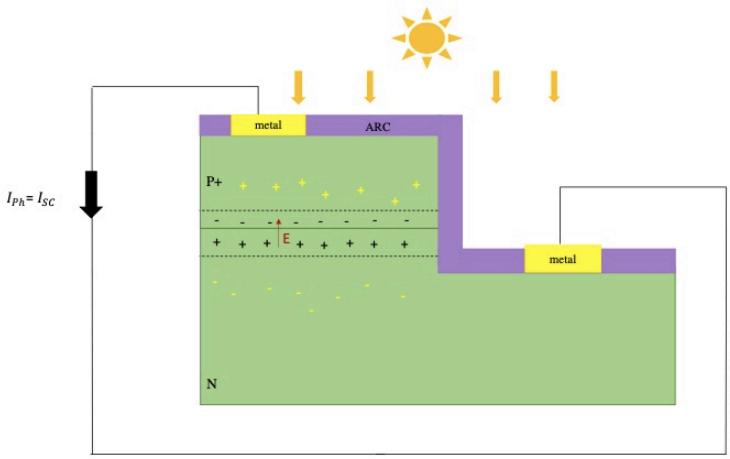


Figure 1-1: **Cross section of a solar cell at zero bias, where ARC means Anti Reflection Coating.**

When a solar cell contains only one pn-junction it is called a single-junction solar cell whereas multi-junction solar cell is a cell with more than one pn-junction made of several semiconductor materials of different bandgaps.

The efficiency of a solar cell is the most important feature of it and could be defined as amount of electric power ($P = I \times V$) coming out of the cell compared to energy from the shining light on the cell. Undoubtedly solar cells with higher efficiency are desired.

In a single-junction solar cell, e.g., conventional Si solar cell of 1.1[ev] bandgap, the maximum efficiency that can be obtained by using the spectrum of light having higher energy than that of the bandgap of semiconductor material is limited to 30%, a constraint that is referred to as the Shockly-Queisser limit [5]. To overcome this limitation and use the absorption of a broader spectrum of light, we can use different semiconductor materials on top of each other and accordingly generate more electrical current.

Multiple semiconductor materials would have multiple bandgaps which response to variety of light wavelengths. Since the photon energy should be larger than the bandgap of the semiconductor material to be able to create electron-hole pairs, high energy photon which has lower wavelength will be absorbed by a larger bandgap material and photon with higher wavelength will be absorbed by lower bandgap material. Therefore, multi-junction solar cells can absorb a broader range of light wavelengths and convert it to electricity.

In designing multi-junction solar cells, material with larger bandgap is integrated on top along with the material with the lower bandgap at the bottom. This configuration allows higher energy photons to be absorbed by the top material and low energy photons by the bottom material. Figure 1-2 shows the solar spectrum absorbed by a multi-junction solar cell. In this case, the top cell consisting of InGaP with bandgap of 1.86 eV absorbs wavelength less than 800 nm and the bottom cell consisting of Ge with bandgap of 0.65 eV absorbs wavelength between 1100 nm and 1800 nm.

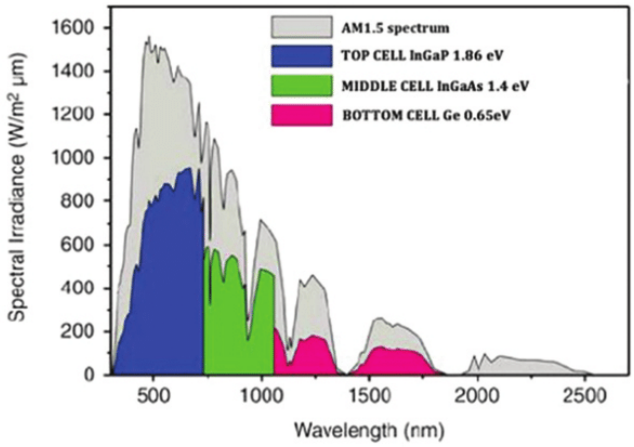


Figure 1-2: **Multiple layers of multi-junction solar cell absorbing specific range of Air mass 1.5 solar spectrum [6].**

In conclusion, multi-junction solar cells are more efficient at converting sunlight to electricity compared to the single-junction solar cells. A single-junction solar cell with non-concentrated sunlight has efficiency about 33.5% [7], whereas the efficiency for a multi-junction cell is over 46% [8].

By increasing the number of pn-junctions a broader spectrum can be absorbed, and the efficiency of the solar cell will increase. Figure 1-3 shows a relation between number of pn-junctions and the projected efficiency, that could be a theoretical projection.

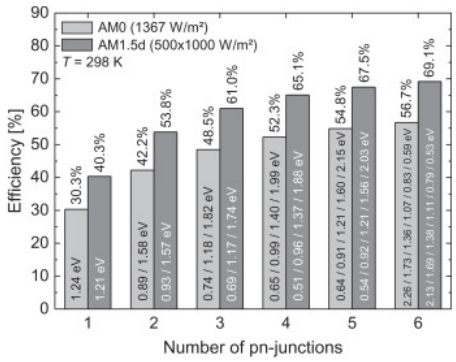


Figure 1-3: **Relation between number of pn-junctions in solar cell and the efficiency of it [9].**

Tandem solar cell is a type of multi-junction solar cell which two or more pn-junctions are on top of each other. Basic designs of tandem solar cells are either by growing layers on top of a substrate which is called monolithic or by stacking devices mechanically, e.g., by bonding. Choosing suitable semiconductor materials for tandem solar cells could be a challenge and here are some factors to be

considered. For example, bandgaps of materials should be matched with the spectrum and crystal lattice constants must be the same to avoid crystalline defects.

III-V compounds have wide range of bandgaps and hence are amenable for combining to create tandem solar cells to match specific solar spectrum with specific bandgap. Therefore, III-V semiconductors have been used in multi-junction solar cells showing high conversion efficiency.

The most application of III-V solar cells are in space and satellites due to their high conversion efficiency and better radiation resistance.

Even though III-V semiconductor multijunction solar cells are the most efficient solar cells, they are expensive due to the high cost of the fabrication techniques and materials. Typically, GaAs or Ge are used as substrate in III-V multi junction solar cells which are expensive. Nonetheless Si can be used as a substrate which could lower the costs to some extent.

In this work, compound semiconductor material, $GaAs_xP_{1-x}$ is used as the material to absorb light on GaAs/Si substrate and design of the solar cell devices in this project is shown in Figure 1-4. However, the p-contact mask used in this project contains three different patterns in terms of distance between contact fingers which might have effect on the performance of the cells.

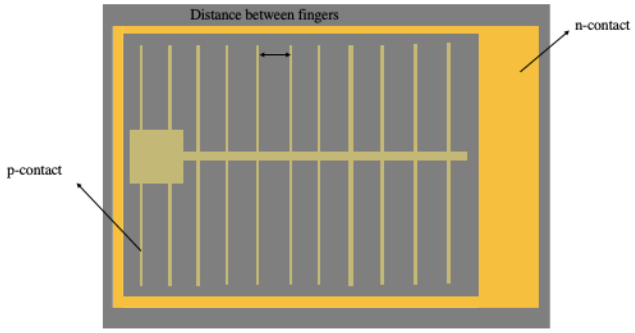


Figure 1-4: Top view of a fabricated solar cell device in this project.

To investigate the functionality of the solar cell device, two kinds of measurements are usually performed, TLM measurement and IV characterization, which will be discussed later.

1.2 Objective of the thesis

According to Figure 1-5, for Si bottom cell with bandgap 1.1[ev], the ideal top cell bandgap value is 1.7ev. Therefore, we aim for $GaAs_{0.75}P_{0.25}$ in this project.

However, in experiment we managed to fabricate and characterize $GaAs_{0.74}P_{0.26}$/GaAs/Si solar cell. This is a main building block towards the final goal of fabricating a tandem multijunction solar cell.

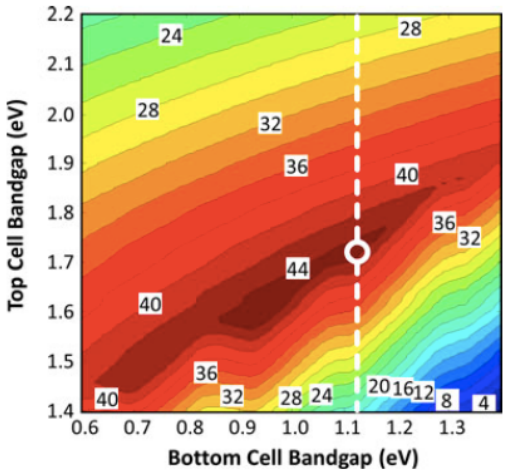


Figure 1-5: **Detailed balance efficiency for dual junction series-connected solar cell under 1-sun AM1.5G. [10]**

Metal contacts are formed on the sample through different steps in fabrication process and at the end performance of the fabricated devices is investigated.

The schematic form of initial sample and fabricated solar cell in this work is shown in Figure 1-6.

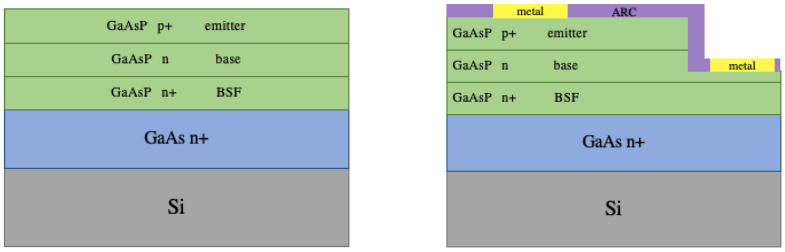


Figure 1-6: **Cross section of initial sample (left) and solar cell device (right).**

Basically, the thesis is about the fabrication of $GaAs_xP_{1-x}$ solar cell on GaAs coated Si substrate where the $GaAs_xP_{1-x}$ epitaxial layer is grown under different growth conditions on top of different kinds of GaAs/Si substrates. Therefore, the objective of the thesis is:

1. Investigation of crystal quality of the $GaAs_xP_{1-x}$ epitaxial layer grown on different kinds of GaAs/Si substrates by characterizing it to obtain the optimized growth conditions and finding the best substrate.
2. Fabrication of $GaAs_{0.75}P_{0.25}$ solar cell on GaAs coated Si substrate.
3. Investigation and comparing the performance of fabricated solar cells.

In addition to chapter 1 which is introduction, there are 6 other chapters. Contents of these 6 chapters are as follow:

In chapter 2, scientific theory of experimental methods and tools that are used in this project are discussed. Chapter 3 describes the process of optimizing the crystal quality of the grown epitaxial layer. In chapter 4, samples chosen for the solar cell fabrication are characterized and relative results reported. Chapter 5 describes the fabrication process, step by step. Chapter 6 is about device characterization to assess the performance of fabricated solar cells. Chapter 7 gives a general conclusion and some suggestions for future works.

2 Experimental set up

2.1 Low pressure Hydride Vapor Phase Epitaxy (LP-HVPE)

HVPE is an epitaxial growth method to prepare low cost, high efficiency III-V solar cells. In this work $GaAs_xP_{1-x}$ layers are grown on on-axis and off cut GaAs (001) and Si (001) substrates. In HVPE reactor, group V precursors which are arsine (AsH_3), and phosphine (PH_3) are used to produce As and P, respectively. The other precursor is GaCl which is generated by the reaction between HCl and molten Ga.

$$2Ga(l) + 2HCl(g) \rightarrow 2GaCl(g) + H_2(g)$$

And the growth reaction to get $GaAs_xP_{1-x}$ can be written as below:

$$xAsH_3(g) + GaCl(g) + (1-x)PH_3(c) \rightarrow GaAs_xP_{1-x}(s) + HCl(g) + H_2(g)$$

In HVPE reactor, first GaCl is generated by the reaction between HCl and melted Ga and then GaCl will be mixed with group V gases such as arsine and phosphine to produce $GaAs_xP_{1-x}$ that is deposited on GaAs/Si substrate.

Desired $GaAs_xP_{1-x}$ composition can be achieved by changing the flow of arsine and phosphine in the reactor. The strength of HVPE technique can be mentioned in two aspects: high growth rate can be achieved by HVPE since the growth rate is determined by mass input rate of reactants [11]. Moreover, by changing the gas phase components one can get desired composition. To be able to deposit III-V semiconductors in large scale, it is essential to decrease the epitaxial cost. Since HVPE reactor uses low-cost elemental source materials and produces a high quality III-V growth, so epitaxial growth using HVPE is more reasonable compared to metal organic vapor phase epitaxy (MOVPE) which is more expensive.

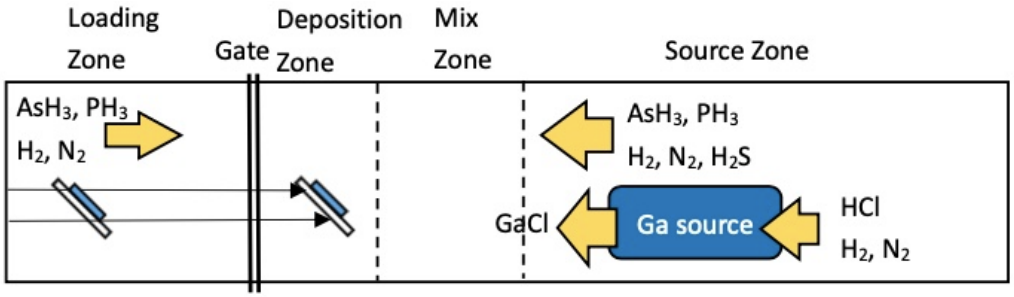


Figure 2-1: Schematic form of HVPE reactor [11]

In this work, samples are grown using HVPE reactor in Electrum Lab and are schematically shown in Figure 2-1.

2.2 Characterization methods

2.2.1 High Resolution X-Ray Diffraction (HRXRD)

HRXRD is a popular characterization tool to study the crystalline quality, composition, thickness (in certain cases), etc. of a sample. Consider parallel planes of atoms with space "d", constructive interference occurs when Bragg's law is satisfied.

$$2d\ sin\ \theta = n\lambda$$

where, θ is the incident angle, λ is the wavelength of incident radiation and n is the diffraction order (an integer). When an incident beam strikes a crystal plane, reflected beams will interfere constructively and have maximum intensity only if the incident angle satisfied Bragg's law. Figure 2-2 shows schematic form of Bragg's law.

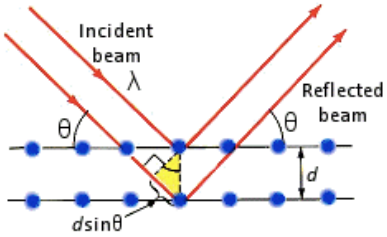


Figure 2-2: Schematic form of Bragg's law [12]

In HRXRD tool, X-Ray beam is produced by X-Ray tube (source) shown at the left side of Figure 2-3. Then the produced X-Ray passes through a monochromator and strikes the crystal placed on sample stage at angle ω and then are diffracted and collected by X-ray detector at angle 2θ.

Sample stage can be tilted in ω, φ, ψ angles and move along z direction. To get the maximum intensity, these directions need to be optimized before doing the real measurement.

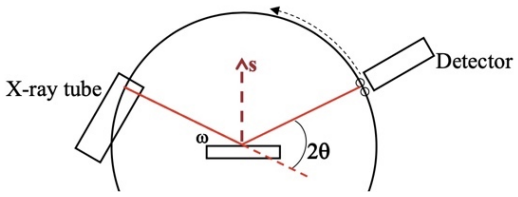


Figure 2-3: Schematic form of HRXRD tool [13].

Two configurations are used for HRXRD measurement, double axis, and triple axis. In the rocking curves collected on double axis, detector can collect different angles, so all the peaks can be observed and is called ω-2θ (omega-2theta). In this project, ω-2θ scan in double axis has been used to see three possible peaks of $GaAs_xP_{1-x}$/GaAs/Si samples and deduct information about composition of the grown layer. The composition of the epitaxial layer is calculated from separation between layer peak and substrate peak in Omega-2theta scan where substrate peak (Si) is reference. For instance, in Figure 2.4 (a-right) the right peak is Si peak considered as reference and the GaAs peak on the left show "x" value

in $GaAs_xP_{1-x}$. Therefore, the composition of the epitaxial layer can be determined easily and should be confirmed by PL measurement later.

In rocking curve on triple axis, the analyzer constrains detector, so only one 2θ angle can be collected. In this project, an Omega scan on $GaAs_xP_{1-x}$ layer is done in triple axis. In ω scan, intensity versus ω is plotted and any defect in the crystal makes the curve wider, so the wider FWHM value shows the worse crystalline quality.

Figure 2-4 shows HRXRD configurations and produced plot using these configurations in this project.

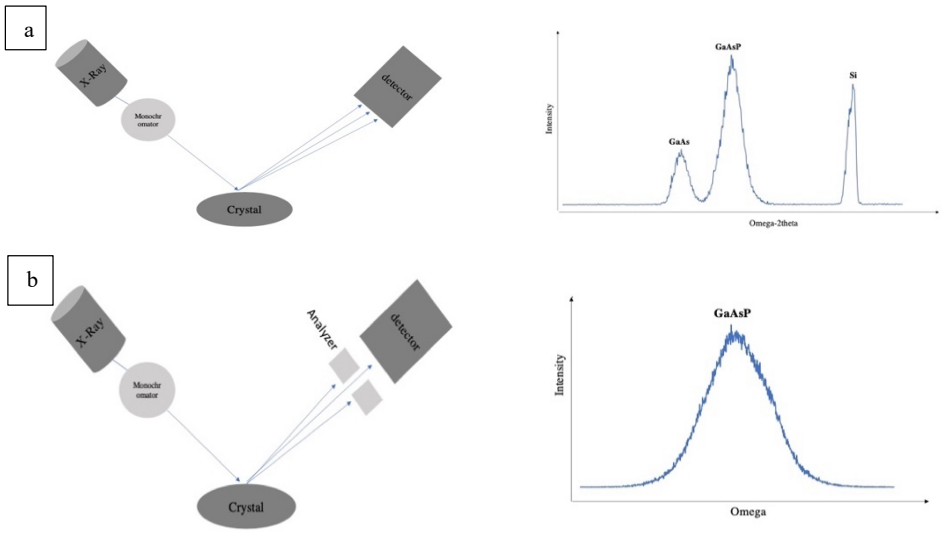


Figure 2-4: Configuration of HRXRD in double axis (a) and in triple axis (b) and their application in the thesis.

In this project most samples are characterized by high resolution XRD tool that has both double axis and triple axis. A few samples are also characterized by other tool that has only double axis, but by limiting the number of pixels used in the detector, 2Theta range is limited and the resolution is acceptable for the samples.

HRXRD characterization results are reported in the next chapters.

2.2.2 Scanning Electron Microscopy (SEM)

Scanning electron microscope is a kind of microscope using electron beams to scan the surface of sample. Scientists can observe the structure with higher resolution and better depth of field compared to optical microscope in micrometer level. SEM configuration consists of different parts such as electron source, lenses, and aperture. Electron beams generated by electron source (or electron gun) are focused by condenser lens, then passe through the aperture and scan coils, then primary electron beam is formed. This primary electron beam reaches the sample and interacts with surface of the sample. Interaction of electron beams with sample surface generates beams such as secondary electrons (SE), back scattered electrons (BSE), etc. The detector positioned above the sample collects the generated beams and the result will be shown on the screen.

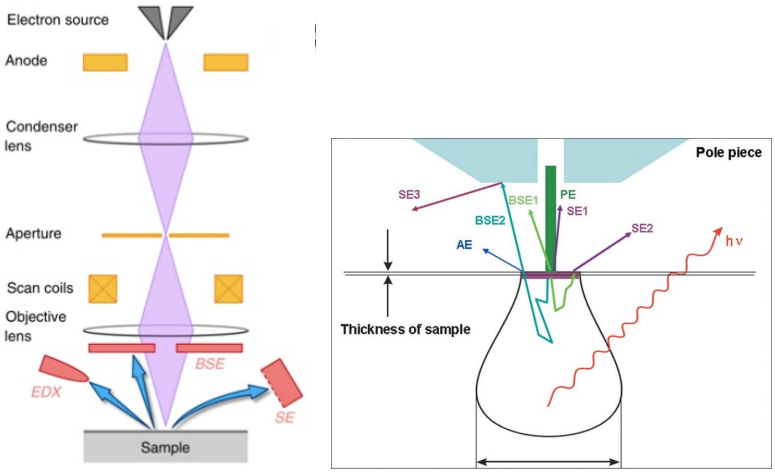


Figure 2-5: **(Left) Structure of scanning electron microscope (SEM) [14], (right) generation of various electrons in SEM [15].**

As was mentioned above different types of electrons are generated because of interaction between primary electron and sample surface. In general, secondary electrons (SE) are generated at shallow depths in the sample whereas back scattered electrons (BSE) are generated from deeper depths in the sample and can provide better information as can be seen in Figure 2-5 (right).

In this thesis Gemeni- Ultra 55 manufactured by Zeiss is used to observe and measure cross section and the depth of some dry-etched III-V samples and InLens mode was used in measurements.

2.2.3 Photoluminescence spectroscopy (PL)

PL is a characterization method in which crystalline quality and the bandgap of the semiconductor materials are investigated. The latter can yield the composition of the material. When a photon with energy higher than bandgap energy of material strikes the material, electrons in valence band get photon's energy and jump to conduction band, this effect is called absorption which is shown in Figure 2-6 (left). After a while these stimulated electrons relax and get back to valence band, releasing the energy as light, which is shown in Figure 2-6 (right). The emission light is detected in PL tool and gives information about the bandgap of the semiconductor material.

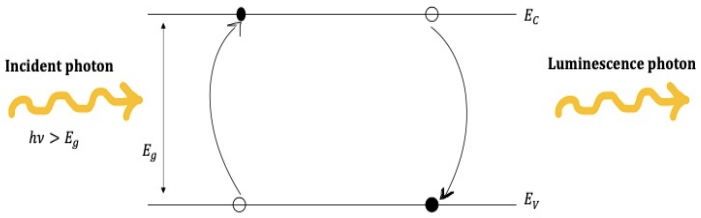


Figure 2-6: **(Left) Absorption and electron excitement, (right) light emission.**

PL is complementary to HRXRD technique to identify the composition of the studied $GaAs_xP_{1-x}$ layer. Since the bandgap E_g of $Ga_xAs_{1-x}P$= f (a, x,) where a is the lattice constant and x, the composition, knowing a from HRXRD and E_g from PL, x can be calculated.

2.2.4 Transmission Line Method (TLM)

Once a solar cell device is fabricated, important parameters such as specific contact resistance between metal and semiconductor as well as sheet resistance should be measured and TLM is a method to measure such parameters.

By applying a voltage across the contacts and knowing the current flow through the device, one can calculate the resistance of the metal contacts.

Two probe measurement stations are used for TLM measurement in this project. Consider two metal contacts with distance "L" apart from each other in TLM pattern of the device as shown in Figure 2-7. Electrical current flows from one probe to a metal contact, passes contact-semiconductor interface, goes through the semiconductor sheet, passes contact-semiconductor interface again and goes to the second metal contact.

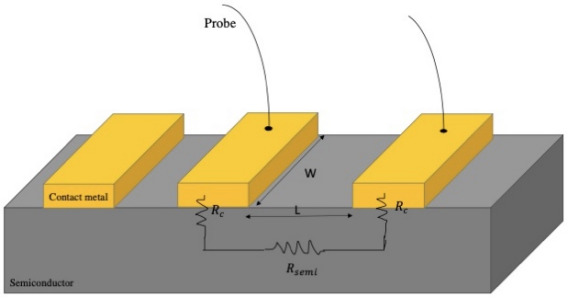


Figure 2-7: Schematic form of the TLM pattern of a solar cell.

The total resistance (R_T) includes the semiconductor resistance (R_{semi}) and two contact-semiconductor resistances (R_C).

$$R_T = R_{semi} + 2R_C \qquad [1]$$

Semiconductor resistance is $R_{semi} = \rho\frac{L}{A} = \rho\frac{L}{W \times thickness}$ [2], where ρ is the resistivity.

Since the sheet resistance is defined as $R_{sheet} = \frac{\rho}{thickness}$ [3]

total resistance can be written as below:

$$R_T = \frac{L}{W}R_{sheet} + 2R_C \qquad [4]$$

By knowing the L values from photomask or measured on optical microscope and total resistance measured by two probe stations, total resistance as a function of contact spacing is obtained.

Total resistance as a function of contact spacing can be plotted as shown in Figure 2-8.

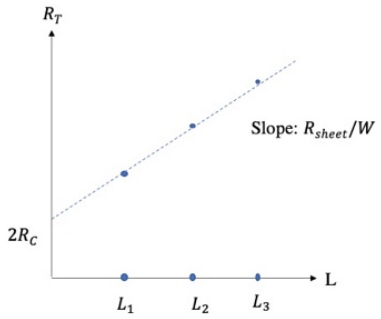


Figure 2-8 **Plot of total resistance of the device vs contact distances.**

The slope of the graph is $\frac{R_{sheet}}{W}$, which can be calculated from the plot.

However, since the current does not flow in the contact uniformly, the physical geometry of contact cannot be used to determine the contact area and that brings us to the concept of transfer length.

Transfer length is the average distance that electron travels in semiconductor under the metal contact before reaching the contact and is defined as $L_T = \sqrt{\frac{r_c}{R_{sheet}}}$ $[\mu m]$ [6],

where r_c is specific contact resistance, given as $r_c = R_c . A$ $[\Omega . cm^2]$

For the cases that L_T is very small compared to contact pad dimensions, the effective area of the contact can be calculated as WL_T.

Therefore, total resistance can be written as below:

$$R_T = \frac{R_{sheet}}{W} (L + 2L_T) \qquad [7]$$

In this project, TLM measurement is performed for solar cell devices and parameters such as sheet resistance, specific contact resistance as well as transfer length and contact resistance are obtained.

2.2.5 IV characterization

Investigation of current- voltage (IV) relation of a solar cell provides information about the functionality of the device. Two kinds of IV measurement are usually performed, dark current and light current.

Dark current curve:

Solar cell in the absence of light works like a diode, therefore checking the dark current curve is a method to check the functionality of the pn-junction of the solar cell. By applying a positive voltage to p-side and negative voltage to n-side, pn-junction is under forward bias, and current is allowed to pass through the junction. The relation between applied voltage and generated current is shown in an IV curve called dark current curve.

In the absence of light, solar cell works like an ideal diode, but if the IV curve of a solar cell does not look like the IV curve of an ideal diode, there are three possible cases:

1. If there is a deviation at higher current, it indicates a series resistance with pn-junction.
2. If there is a hump at lower current, it shows a parallel (shunt) resistance with pn-junction.
3. If there are both deviations at higher current and hump at lower current indicates both series and shunt resistance.

Dark current curves of a solar cell in linear scale are shown in Figure 2-9.

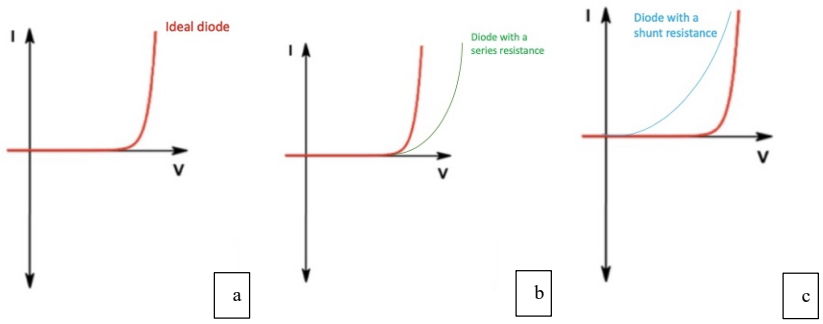


Figure 2-9: **Dark current curve of an ideal diode (a), diode with a series resistance (b) and diode with a shunt resistance (c) in linear scale.**

Light current curve:

Air-mass (AM1.5) spectrum is a global spectrum which simulates sunlight and has been used to test photovoltaic devices. In this work also, solar cells have been exposed by AM1.5 spectrum to be tested and characterized and result is reported as light current curve.

When the device is characterized under standard spectrum (AM1.5), in the absence of any external voltage, a current is generated flowing through the device which is called photo current (I_{ph}) which is short circuit current but in reverse direction ($I_{ph} = -I_{SC}$). The relation between current and voltage of the solar cell is presented in light current curve in the first quadrant as shown in Figure 2-10. Key parameters are deduced from light current curve such as efficiency of the cell which could be defined as amount of electric power ($P = I \times V$) coming out of the cell compared to energy from the shining light on the cell. The other important parameter is fill factor (FF) which is a measure of quality of solar cell and is calculated as below,

$$FF = \frac{P_{max}}{P} = \frac{I_{mp} \times V_{mp}}{I_{SC} \times V_{OC}}$$

Where I_{mp} and V_{mp} are current and voltage of the maximum power, respectively.

As it can be seen in Figure 2-10, the interception of light current curve with x and y axis are V_{OC} and I_{SC}, respectively.

The area of blue rectangular is maximum power ($P_{max} = I_{mp} \times V_{mp}$) that solar cell can provide and the area of yellow rectangular is solar cell power ($P = I_{SC} \times V_{OC}$).

The larger number of FF indicates the better quality of solar cell. The light current curve of a solar cell as well as maximum power point are shown in Figure 2-10.

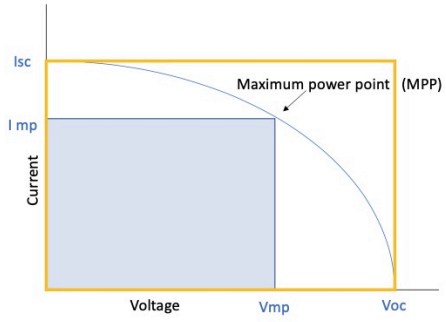


Figure 2-10 **Light current curve of a solar cell in log scale.**

The schematic form of solar cell in absence of light and corresponding dark current curve (a) and also under standard spectrum (AM1.5) and corresponding light current curve (b) are shown in Figure 2-11.

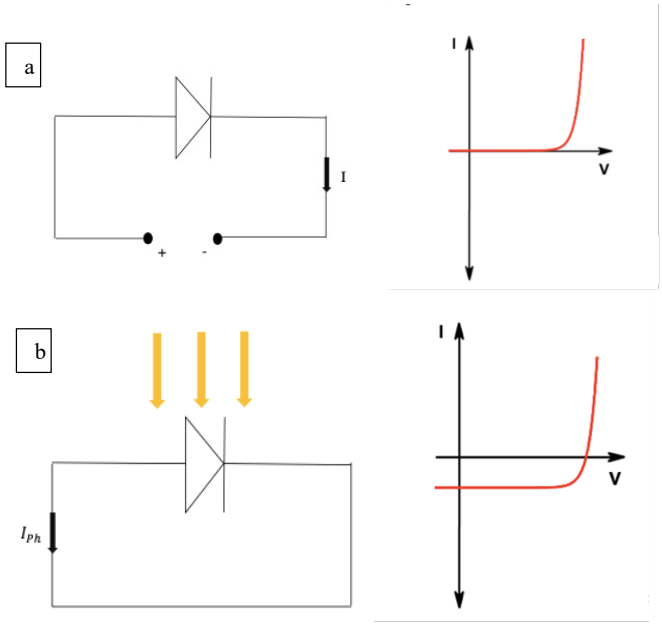


Figure 2-11: **PN junction of a solar cell in darkness (a) pn- junction of solar cell under illumination (b) and corresponding IV curves in linear scale.**

In this project for each fabricated solar cell a dark and light curve is plotted in linear and log scale to interpret the functionality of the device.

In light current curve in linear scale the intersection of the curve with voltage axis and current axis shows open circuit voltage (V_{OC}) and short circuit current (I_{SC}), respectively, as it is shown in Figure 2-12 (left).

In light current curve in log scale the minimum point of the plot shows open circuit voltage (V_{OC}) and intersection of the plot with current axis shows short circuit current (I_{SC}), as you can see in Figure 2-12 (right).

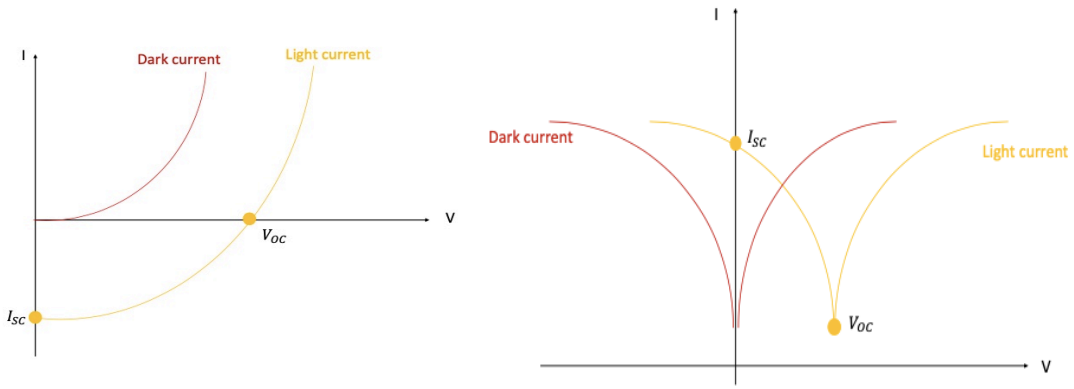


Figure 2-12: Dark and light current curve of a solar cell in linear scale (left) and in log scale (right).

2.3 Fabrication tools

During the fabrication process of the solar cells number of tools in cleanroom have been used and here the operating principles of the most important ones is described.

2.3.1 Plasma Enhanced Chemical Vapor Deposition (PECVD)

PECVD is a chemical deposition method to deposit thin film such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) on a substrate. In PECVD, thin film is deposited uniformly all over the substrate and the process occurs at temperature of 300°C. The tool consists of two electrodes parallel to each other and a substrate is placed on one electrode. Reactant gaseous such as SiH_4, NH_3, N_2O, etc. are introduced to the space between two electrodes, just above the substrate. When reactant gaseous are ionized, plasma is generated. Then the generated plasma will react chemically with the substrate and thin film is deposited. Figure 2-13 shows schematic form of PECVD.

Chemical reaction to produce SiO_2 and Si_3N_4 can be written as below.

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$$

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$$

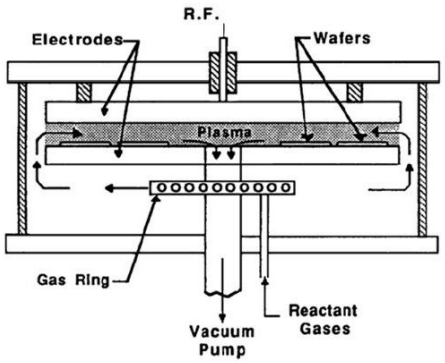


Figure 2-13: Schematic form of PECVD [16].

In this thesis, Plasma lab 80Plus (Oxford PECVD System) chamber A, is used to deposit silicon dioxide (SiO_2) as hard mask for mesa etching and silicon nitride (Si_3N_4) as anti-reflection coating (ARC) on samples. The information about depositions will be discussed later.

2.3.2 Photolithography

Photolithography is one of the most used techniques to pattern a wafer with the help of a designed photo mask. In this method wafer is covered by a photoresist (resist) and will be exposed by light through the mask to replicate its pattern.

There are two types of the resist, positive and negative. When exposure is performed there will be a chemical reaction in positive resist and exposed part of resist will be removed by a developer whereas in negative resist unexposed parts will be removed.

As figure 2-14 shows, a photo mask is placed at a specific distance called alignment gap (AG) above the wafer. First alignment needs to be done by moving the wafer stage to transfer the pattern on the right position on the wafer. Light source is above the mask and during the exposure, light will shine through the mask into the wafer.

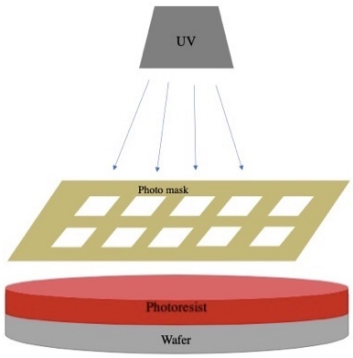


Figure 2-14: Schematic form of Photolithography.

After exposure for a desired time, resist will be removed by a developer and the desired pattern can be seen on the wafer. After that, possible residual resist will be removed by plasma treatment in an equipment called Tepla.

In this project tool Mask aligner MA6/BA6 Karl Suss is used which has UV light as source. In addition, in mesa patterning positive resist and in top and middle contact patterning negative resist are used.

2.3.3 Inductively Coupled Plasma Etching (ICP)

ICP which is also called dry plasma etching is a technique using plasma to etch III-V semiconductors.

Gases are introduced above an inductive coil and sample is placed on a chuck. Radio frequency (RF) is applied to coil and the chuck to create plasma. By introducing gases such as Argon (Ar) chemical reactions take place which generate plasma.

Figure 2-15 shows an ICP tool schematically.

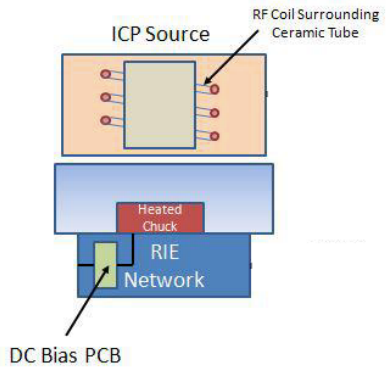


Figure 2-15: Schematic form of ICP [17].

The advantage of using plasma in dry etching is having control of etch profile, which does not happen in wet etching. The profile in this technique is usually anisotropic.

In this project Oxford Instrument ICP380 Etch System has been used to etch GaAsP layer with an etch rate around 0.7 μm/min. Information about dry etching of the samples will be discussed in detail in next chapters.

2.3.4 Metal evaporation

Metallization is the final step in the fabrication of solar cell devices in which a thin layer of desired metal(s) is(are) deposited on device to collect the photo generated current.

In this project, first through different process steps, p-contact is implemented. For this, a P-type semiconductor (GaAsP) and metal (Cr/Au) Junction is created. Then N-contact is implemented. For this a N-type semiconductor (GaAsP) and metal (Au/Ge/Ni/Au) junction is created.

When a metal is in contact with a wide bandgap semiconductor (such as III-V) results in a Schottky contact, but since the electrical current needs to flow into and out of the semiconductor, an ohmic contact should be created. To create an ohmic contact, a highly doped semiconductor is placed in contact with metal.

P- type Schottky junction:

To form a P-type Schottky junction (barrier), the distance between vacuum and fermi level (work function) of metal is less than the work function of semiconductor. When a metal is in contact to P-type semiconductor, their vacuum levels (E_0) are aligned to each other as it is shown in Figure 2-16 (left). Since holes like to go up a slope which means higher energy, they go from valence band of P-type semiconductor up to metal easily. Therefore, due to depletion of holes, the fermi level of P-type semiconductor goes up and aligns with fermi level of metal. As it is shown in Figure 2-16 (right), the magnitude of the potential is "Schottky barrier height"

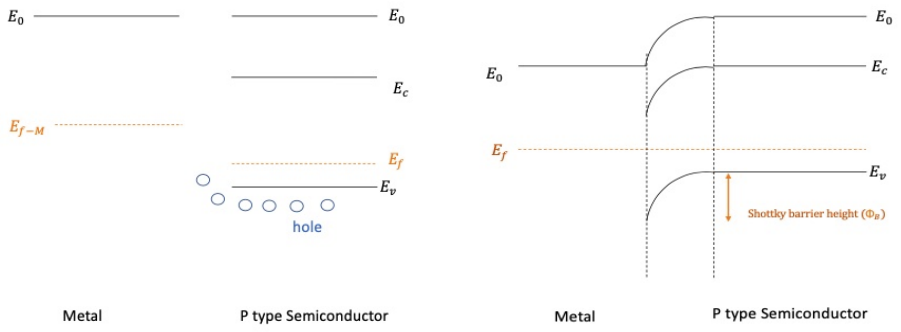


Figure 2-16: Energy band diagram of metal and P-type semiconductor Schottky junction before (left) and after (right) equilibrium.

P- type Ohmic junction:

To form a P-type ohmic junction, one way is to dope the semiconductor highly to get tunneling. When the semiconductor is highly doped, the barrier will be very thin and charge carriers (in this case holes) could tunnel through the barrier.

Since P-type GaAsP is highly doped, instead of overcoming the barrier holes could tunnel through the barrier between metal to P+ type semiconductor. Therefore, an ohmic junction is created.

Figure 2-17 shows energy band diagram of a P-type Ohmic junction.

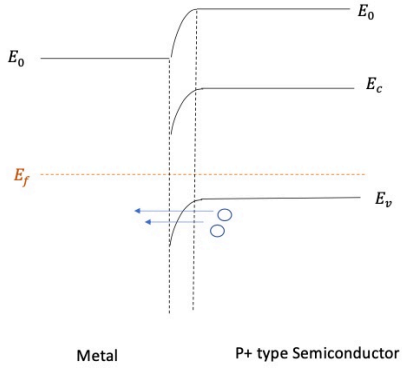


Figure 2-17: Energy band diagram of metal and P-type Ohmic junction, tunnelling effect.

N- type Schottky junction:

To form a N-type Schottky junction (barrier), the distance between vacuum and fermi level (work function) of metal is more than the work function of semiconductor.

When a metal is in contact to N-type semiconductor, their vacuum levels (E_0) are aligned to each other as it is shown in Figure 2-18 (left). Since electrons like to go down slope which means lower energy, they go from conduction band of N-type semiconductor come down to metal easily. Therefore, there will be lack of electrons in semiconductor, so its fermi level will go down and align with fermi level of metal and therefore conduction band, valence band and vacuum level would also go down, Figure 2-18 (right). The vacuum levels must be in the same, so they are connected as Figure 2-18 (right) shows and this is how a barrier is created.

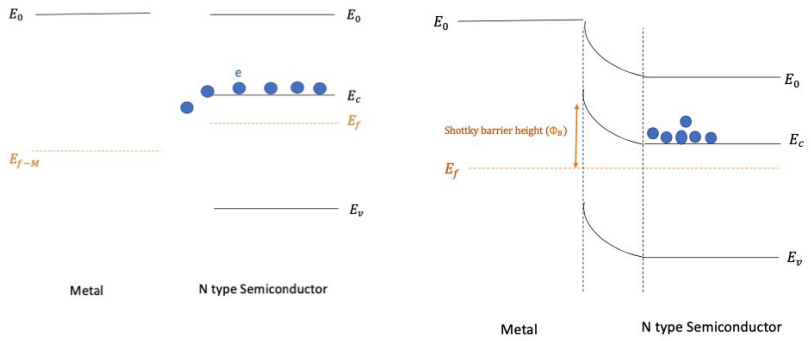


Figure 2-18: **Energy band diagram of metal and a N-type semiconductor Schottky junction before (left) and after (right) equilibrium.**

N- type ohmic junction:

To form a N-type ohmic junction, one way is to dope the semiconductor heavily to get tunneling. When the semiconductor is highly doped, the barrier will be very thin and charge carriers (in this case electrons) could tunnel through the barrier.

Adding Ge (germanium) to metals would locally enhance the doping of the semiconductor and electrons could tunnel through barrier between metal and n+ type semiconductor. Therefore, an ohmic contact is created.

Figure 2-19 shows N-type Ohmic junction.

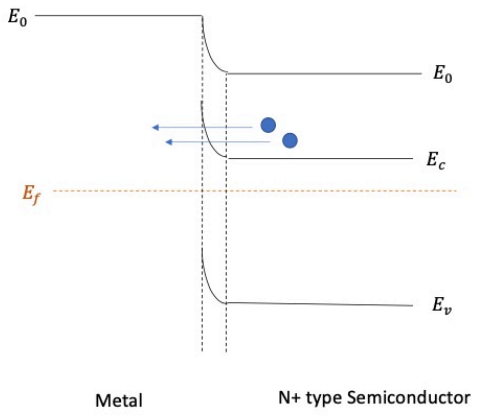


Figure 2-19: Energy band diagram of a N-type ohmic junction.

In this project, the contact between metals (Cr and Au) and p-type GaAsP (p-contact) as well as the contact between metals (Au/Ge/Ni/Au) and n-type GaAsP (n-contact) need to be ohmic with low resistance.

Metals in p and n-contact are deposited by e-beam evaporation, shown in Figure 2-20. In this method an energetic electron beam is generated from a filament and is conducted to source material (Au, Ni) by magnetic field and vaporize it. Samples are placed on a stage facing down on top of the chamber and the stage is rotating very slowly to deposit the metals homogeneously on samples.

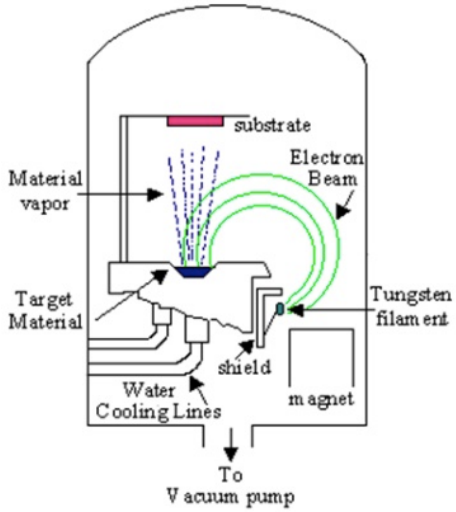


Figure 2-20: Schematic form of metal evaporation tool [18].

In this thesis Provac PAK 600 Coating System has been used to deposit metals as below: For p-contact Cr 40nm/ Au 180nm are deposited and for n-contact Au 100nm (bottom layer)/ Ge 50nm/ Ni 50nm/ Au 100nm (top layer) is deposited. However, the thickness of top layer Au for one sample increased to 600nm. Results and information about metallization will be discussed in the next chapters.

3 Crystal quality optimization

3.1 Growth conditions

Growth conditions such as temperature and precursor flows could affect the crystalline quality of the epitaxial layer. To fabricate a decent solar cell device out of a sample, $GaAs_xP_{1-x}$ layer from which solar cell structure is based on, should be grown under an optimized growth condition. Therefore, by investigating the crystalline quality of the grown $GaAs_xP_{1-x}$ layer and finding the best result, one can obtain the optimized growth conditions. Information about $GaAs_xP_{1-x}$ samples grown in HVPE including run number and kind of substrate is presented in Table 3.1.

Run number	Sample
3957	$GaAs_xP_{1-x}$/ GaAs on On-axis Si substrate
	$GaAs_xP_{1-x}$/ GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ thickened GaAs on off-cut Si substrate
	$GaAs_xP_{1-x}$/ n+ GaAs substrate
3963	$GaAs_xP_{1-x}$/ GaAs on On-axis Si substrate
	$GaAs_xP_{1-x}$/ GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ thickened GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ n+ GaAs substrate
3969	$GaAs_xP_{1-x}$/ GaAs on On-axis Si substrate
	$GaAs_xP_{1-x}$/ GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ thickened GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ GaP on Si substrate
	$GaAs_xP_{1-x}$/ n+ GaAs substrate
3971	$GaAs_xP_{1-x}$/ GaAs on On-axis Si substrate
	$GaAs_xP_{1-x}$/ GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ thickened GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ GaP on Si substrate
	$GaAs_xP_{1-x}$/ n+ GaAs substrate
3979	$GaAs_xP_{1-x}$/ GaAs on On-axis Si substrate
	$GaAs_xP_{1-x}$/ GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ thickened GaAs on Off-cut Si substrate
	$GaAs_xP_{1-x}$/ thickened GaAs on polished Off-cut Si substrate
	$GaAs_xP_{1-x}$/ n+ GaAs substrate

Table 3.1: information about samples grown for crystalline quality optimization.

Since in each run $GaAs_xP_{1-x}$ has been grown on different substrates, in this thesis samples are named as E, F, T, MBE and n+ GaAs to be clearer. In MBE wafer, material is grown by molecular beam epitaxy. Table 3.2 shows the name of the samples in the thesis.

Sample	Name of the sample in the thesis
$GaAs_xP_{1-x}$/GaAs on On-axis Si substrate	Wafer E
$GaAs_xP_{1-x}$ /GaAs on Off-cut Si substrate	Wafer F
$GaAs_xP_{1-x}$/thickened GaAs on Off-cut Si substrate	Wafer T
$GaAs_xP_{1-x}$/ n+ GaAs substrate	Wafer n+ GaAs
$GaAs_xP_{1-x}$/ GaP on Si substrate	Wafer MBE
$GaAs_xP_{1-x}$/ Polished thickened GaAs on Off-cut Si substrate	Wafer U

Table 3.2: Name of the samples in this thesis.

The difference between wafer F and wafer T is the thickness of GaAs substrate. In wafer T, in thicker GaAs, which is around 6 microns, dislocations will have more space to cancel out each other. In next chapters by comparing the crystalline quality of wafer F and T, it will be shown that FWHM of wafer T is less which shows the better crystalline quality.

In wafer U the substrate has been polished. In the next chapters the crystalline quality of these wafers will be compared and reported.

Growth conditions such as temperature and precursor flow for each growth run are represented in Table 3.3.

Run number	Temperature (°C)	precursor flow (sccm)		
		AsH_3	GaCl	PH_3
3957	660	15	15	85
3963	610	15	15	85
3969	710	15	15	85
3971	610	15	25	85
3979	610	25	25	75

Table 3.3: Growth conditions of sample grown for crystalline quality optimization.

Runs number 3963, 3971 and 3979 are performed at 610 °C temperature whereas runs 3957 and 3969 are performed at higher temperature, 660 °C and 710 °C, respectively. The precursor flows are the same for all the runs except for 3979 in which arsine flow has been increased while phosphine flow has been decreased.

After investigating the characterization results, we can figure out the effect of growth conditions on the crystalline quality of the epitaxial layer.

3.2 Characterization of the grown samples

HRXRD measurement can yield information on about crystalline quality and composition and optical microscope on surface morphology of the epitaxial layer. By comparing the results of the samples and finding the best one, growth condition related to that sample could be considered as optimized growth conditions which can be used for future growth runs.

3.2.1 Crystal quality and composition

As it was mentioned in 2.2.1 information about crystalline quality of the epitaxial layer can be deduced from full width at half maximum (FWHM) value, in Omega scan in HRXRD. Besides, composition of the epitaxial layer can be obtained from Omega-2theta scan. Therefore, omega scan in triple axis on $GaAs_xP_{1-x}$ layer and omega-2theta scan in double axis have been done on all the samples.

Information about HRXRD measurement is summarized in Table 3.4.

HRXRD results of samples grown for crystalline quality optimization			
Run number	Sample	$GaAs_xP_{1-x}$ layer FWHM (arcsec)	Composition $GaAs_xP_{1-x}$
3957	Wafer E	576	$GaAs_{0.63}P_{0.37}$
	Wafer F	468	$GaAs_{0.48}P_{0.52}$
	Wafer T	576	$GaAs_{0.58}P_{0.42}$
	Wafer n+ GaAs	342	$GaAs_{0.60}P_{0.40}$
3963	Wafer E	576	$GaAs_{0.67}P_{0.33}$
	Wafer F	540	$GaAs_{0.46}P_{0.54}$
	Wafer T	612	$GaAs_{0.63}P_{0.37}$
	Wafer n+ GaAs	396	$GaAs_{0.72}P_{0.28}$
3969	Wafer E	432	$GaAs_{0.66}P_{0.34}$
	Wafer F	828	$GaAs_{0.42}P_{0.58}$
	Wafer T	756	$GaAs_{0.68}P_{0.32}$
	Wafer MBE	648	$GaAs_{0.57}P_{0.43}$
	Wafer n+ GaAs	288	$GaAs_{0.59}P_{0.41}$
3971	Wafer E	612	$GaAs_{0.56}P_{0.44}$
	Wafer F	504	$GaAs_{0.59}P_{0.41}$
	Wafer T	936	$GaAs_{0.56}P_{0.44}$

	Wafer MBE	1080	$GaAs_{0.40}P_{0.60}$
	Wafer n+ GaAs	288	$GaAs_{0.64}P_{0.36}$
3979	Wafer E	540	$GaAs_{0.73}P_{0.27}$
	Wafer F	468	$GaAs_{0.90}P_{0.10}$
	Wafer T	684	$GaAs_{0.73}P_{0.27}$
	Wafer U	468	$GaAs_{0.64}P_{0.06}$
	Wafer n+ GaAs	396	$GaAs_{0.80}P_{0.20}$

Table 3.4: HRXRD results of grown samples for crystalline quality optimization.

3.2.1.1 Comparing Si substrate samples in each growth run

By looking at Table 3.4 it is shown that in run 3957, comparing FWHM value for wafers E, F and T shows that wafer F has the lowest value, which is 468 arcsec and has the larger phosphorus fraction showing 52%. Wafer E shows the lowest phosphorus fraction which is 37%.

In growth 3963, again wafer F has the lowest FWHM value among the Si substrate wafers and has the largest phosphorus fraction, which is 54% among the Si substrate samples. The lowest phosphorus fraction is for wafer E, 33%.

Looking at run 3969, the lowest FWHM value belongs to wafer E and its phosphorus fraction is 34% and is the second lowest among the Si substrate wafers in this run. The lowest phosphorus fraction belongs to wafer T and is 32%.

In run 3971, the lowest FWHM value is for wafer F. The same sample shows the lowest phosphorus fraction, which is 41%.

In growth run 3979, wafer F and wafer U have the lowest FWHM value among other Si substrate wafers which is 468 arcsec whereas lowest phosphorous fraction belongs to wafer U and is 6%.

Generally, in all the growth runs n+ GaAs wafer shows lower FWHM value compared to Si substrate wafers. This is expected since the lattice mismatch between $GaAs_xP_{1-x}$ and GaAs is lower than that between $GaAs_xP_{1-x}$ and Si.

Figure 3-1 shows the Omega scan on $GaAs_xP_{1-x}$ layer in triple axis of samples from different growth runs and results are plotted in logarithmic scale.

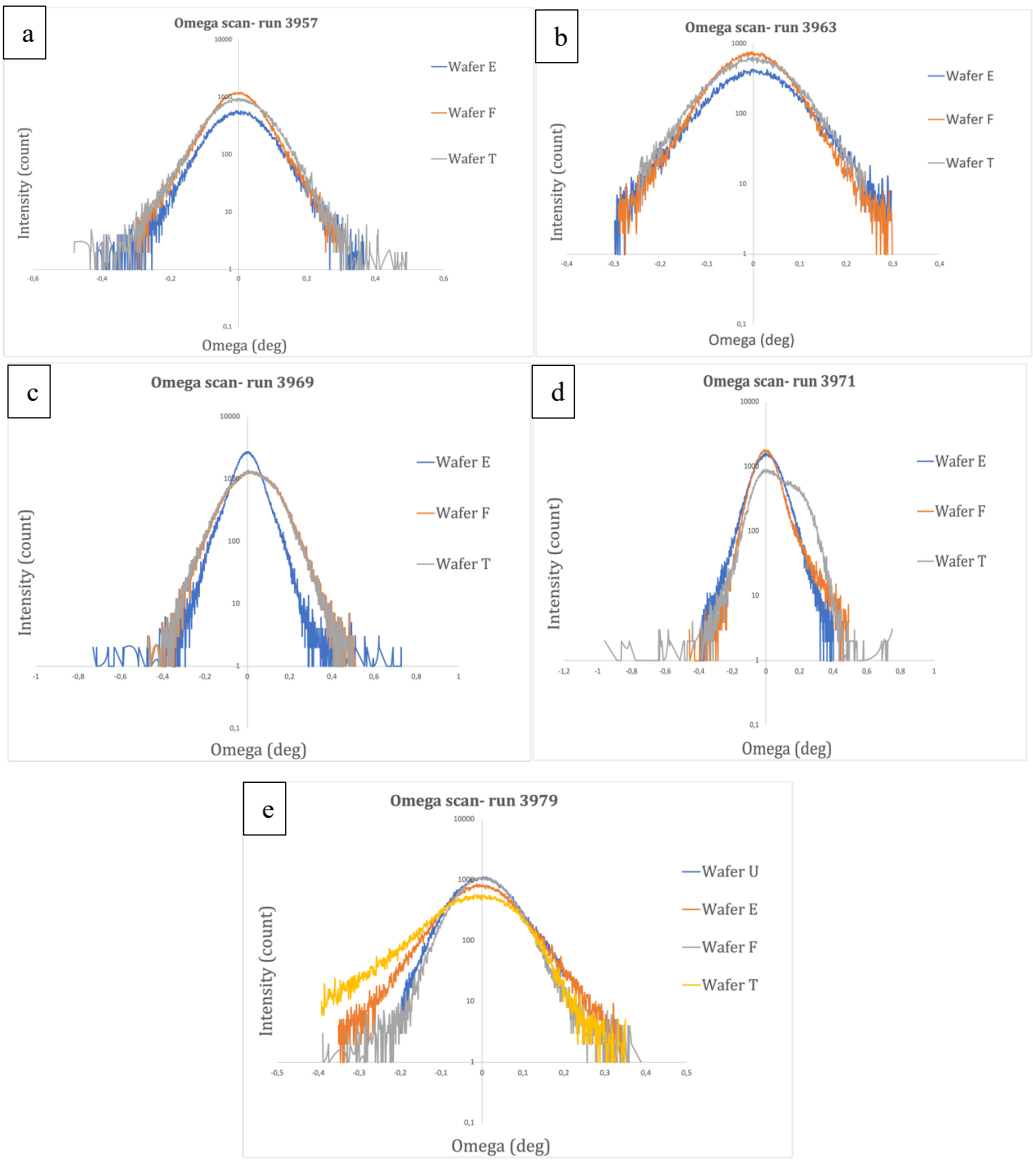


Figure 3-1: Omega scan of samples in different runs.

The most important information can be deduced from Omega scan is FWHM value which shows the crystalline quality of the wafer to some extent, and related data is reported in Table 3.4.

In Figure 3-1 (a) run 3957, wafer E and T have higher FWHM values which indicates the poorer crystalline quality. The same result is true for run 3963 and Figure 3-1 (b) shows wafer E and T have higher FWHM value. Looking at figure 3-1 (c) it shows in run 3969 wafer E has the lowest FWHM value which indicates the best crystalline quality among others and wafer F in run 3971 has the lowest FWHM value as it can be seen in Figure 3-1 (d). In run 3979 wafer F and U have the lowest FWHM value indicating better crystalline quality among other wafers in this run as it can be seen in Figure 3-1 (e).

Omega- 2theta scan in double axis of Si substrate samples for each run has been done and results are plotted in logarithmic scale shown in Figure 3-2.

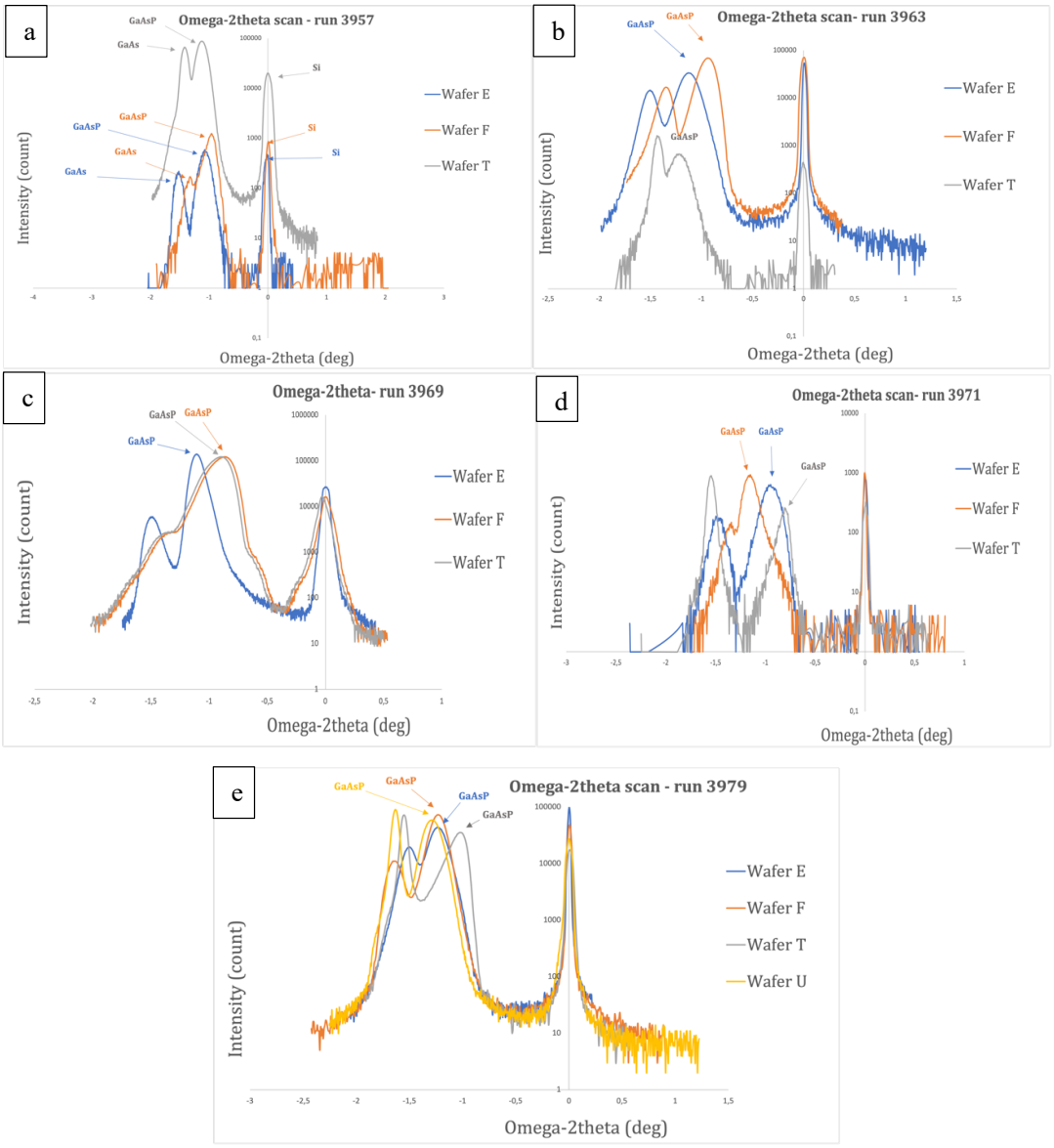


Figure 3-2: Omega-2theta scan of samples in different runs.

As Figure 3-2 (a) shows in run 3957, wafer T has the highest intensity and even though wafer F has the lowest FWHM value, it does not have the highest intensity.

In Figure 3-2 (b), highest intensity in run 3963 belongs to wafer F and it also has the lowest FWHM values. In addition, P-fraction of wafer F is quite high.

In run 3969, wafer E has the highest intensity among others and lowest FWHM value was also for the same wafer in this run indicating the best crystalline quality.

Figure 3-2 (d) shows in run 3971 wafer F has the highest intensity and it has the lowest FWHM value. In addition, p-fraction of wafer F is the lowest among other wafers in this run.

Looking at Figure 3-2 (e) in run 3979 wafer F has the highest intensity and wafer U has the second highest intensity. These two wafers have the same FWHM value, which is 468 arcsec, but p-fraction of wafer F which is 10% is higher that of wafer U, which is 6%.

Looking at HRXRD characterization of different wafers in each growth run, wafer F in all the growth runs and wafer U from run 3979 shows better crystalline quality among the Si substrate wafers.

3.2.1.2 Comparin different growth runs

FWHM values of wafers from different growth runs are reported in Table 3.5 to make it easier for comparison and results of Omega scan are plotted in logarithmic scale shown in Figure 3-3.

FWHM value Comparison (arcsec)					
Run number	Wafer E	Wafer F	Wafer T	Wafer n+ GaAs	Wafer MBE
3957	576	468	576	342	-
3963	576	540	612	396	-
3969	432	828	756	288	648
3971	612	504	936	288	1081
3979	540	468	684	396	-

Table 3.5: FWHM values for different wafers of different runs.

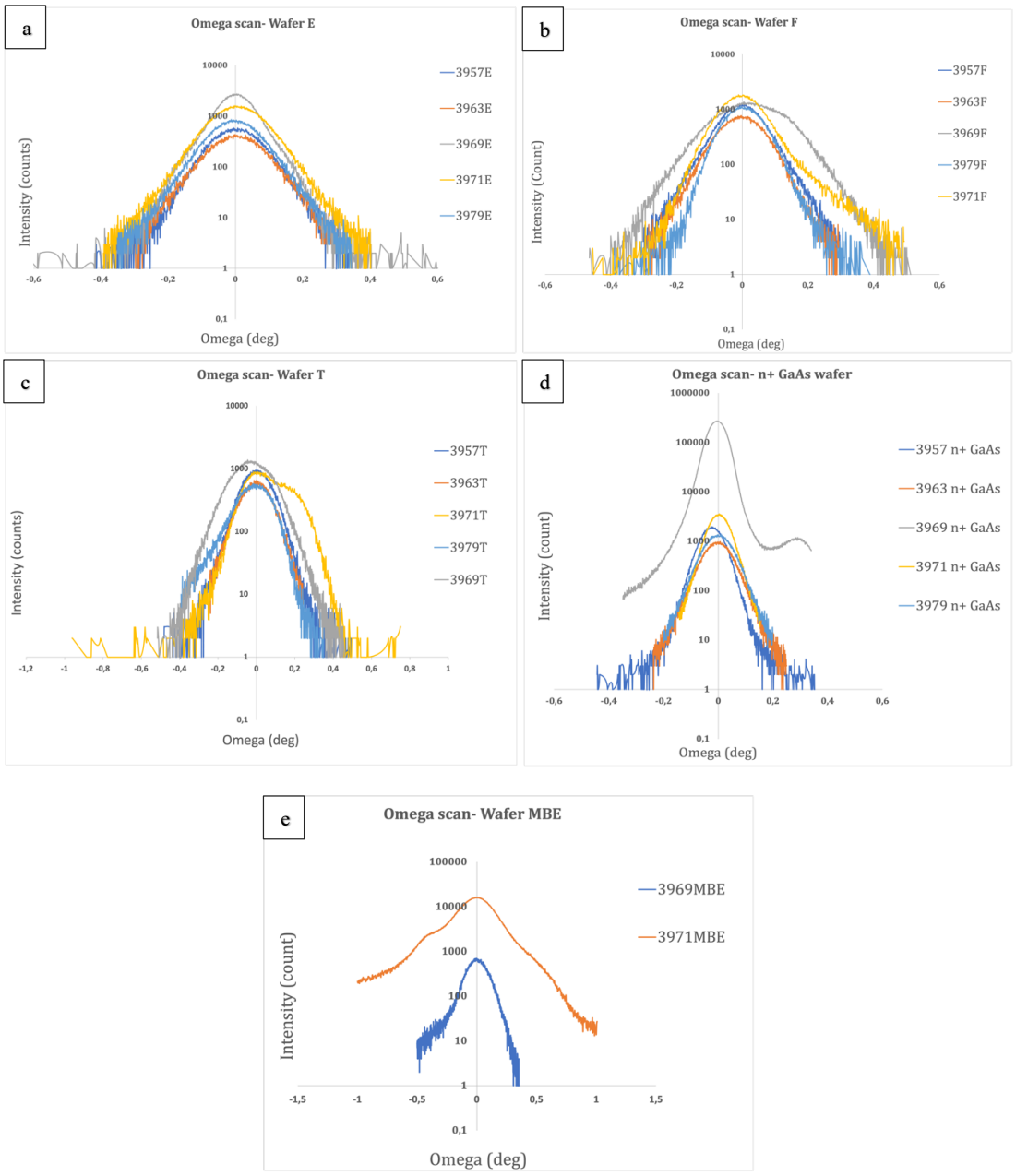


Figure 3-3: **Omega scan plots of a) wafer E, b) wafer F, c) Wafer T, d) n+ GaAs wafer and e) wafer MBE of different growth runs.**

Figure 3-3 (a) shows among all wafer E from different runs, wafer E in run 3969 has the lowest FWHM value indicating the best crystalline quality.

Comparing wafer F from different growth runs shows wafer F from run 3979 has the lowest FWHM value and wafer F from run 3969 has the highest FWHM value indicating the worse crystalline quality as Figure 3-3 (b) shows.

Figure 3-3 (c) shows wafer T from run 3957 has the lowest FWHM value and run 3971 has the highest FWHM value among other growth runs.

Results of Omega-2theta scans in double axis for different runs are plotted in logarithmic scale in Figure 3-4. Crystalline quality and composition of the epi-layer are information which can be deduced from Omega-2theta scan.

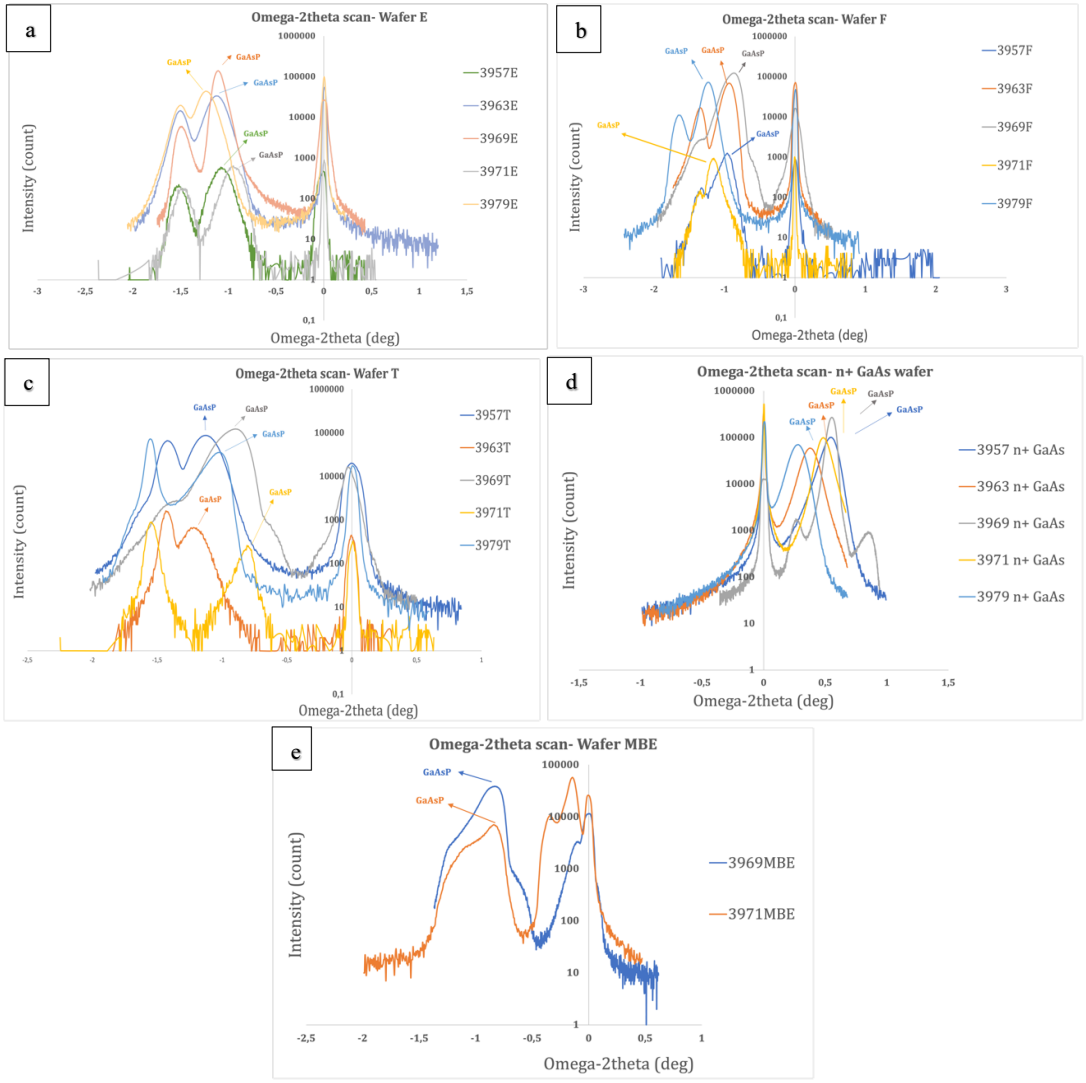


Figure 3-4: **Omega-2theta plots of a) wafer E, b) wafer F, c) wafer T d) wafer n+ GaAs and e) wafer MBE of different runs.**

Figure 3-4 (a) shows wafer E from run 3969 has the highest intensity among other runs which indicates a good crystalline quality, and the same wafer had the lowest FWHM value which shows the same results.

As it is shown in Figure 3-4 (b), wafer F from run 3969 has the highest intensity and the second highest intensity belongs to run 3979.

Wafer F from run 3969 has a high FWHM value, which is 828 arcsec and looking at Table 3.5 its p-fraction is 58%. Wafer F from run 3979 has the lowest FWHM value which indicates the best crystalline quality. Looking at Table 3.4, the P-fraction of this sample is 10%, so one can conclude by decreasing the flow of PH_3 , from 85 sccm in run 3969 to 75 sccm in run 3979 the crystalline quality is improved.

Figure 3-4 (c) shows wafer T from run 3969 has the highest intensity while it has a high FWHM value and 32% P-fraction. The second highest intensity belongs to wafer T from run 3957, with the lowest FWHM value among other runs. Temperature in runs 3969 and 3957 is 710 ℃ and 660 ℃, respectively, so it seems decreasing the temperature will increase the crystalline quality of the epi-layer.
For n+ GaAs substrate samples, the highest intensity is for run 3969 and FWHM value of this sample is the lowest, so among n+ GaAs substrate samples run 3969 gives the best crystalline quality.
Figure 3-4 (e) shows run 3963 has the higher intensity and has lower FWHM value compared to run 3971 which indicates the better crystalline quality.

3.2.2 Surface morphology

Surface morphology of the sample reflects the crystalline quality to some extent. Basically, large number of pits and hillocks could affect the performance of the device in a negative way. So, a smoother surface with less roughness is desired for device fabrication.
The morphology of all samples is studied with an optical microscope and the results are shown below.

3.2.2.1 Comparing Si substrate samples in each growth run

First, Si substrate samples from each run are investigated and compared with each other to figure out the best substrate.

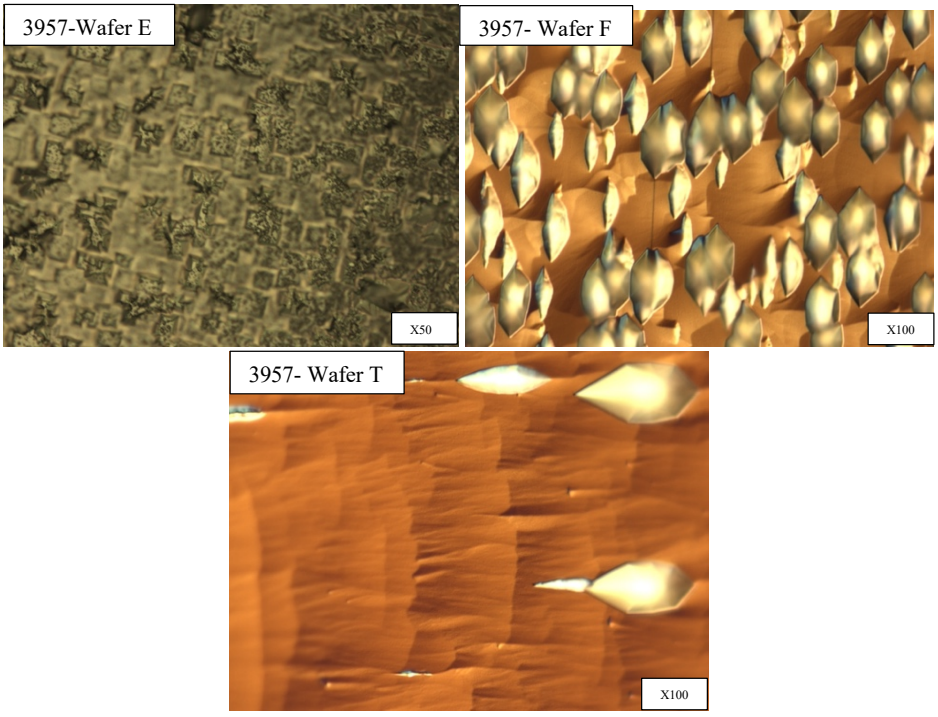


Figure 3-5: Top view of Si substrate wafers in run 3957.

It seems in run 3957, wafer E shows anti phase domain (APD) which is a crystallographic defect that happens during heteroepitaxial growth of a polar layer on a non-polar substrate. When a polar compound semiconductor such as GaAs is deposited on a non-polar semiconductor such as Si, APD is formed. GaAs has zinc blend structure with two elements (Ga and As) and Si has diamond structure

with one element (Si). When GaAs is placed on top of the Si two configuration could be formed. It can be either Ga or As atoms occupying the first layer on top of the Si that makes two configuration. These two configurations are opposite to each other, and this defect is known as APD.
Wafer F has large pits that are dense and wafer T also is covered by pits in smaller size but still dense.

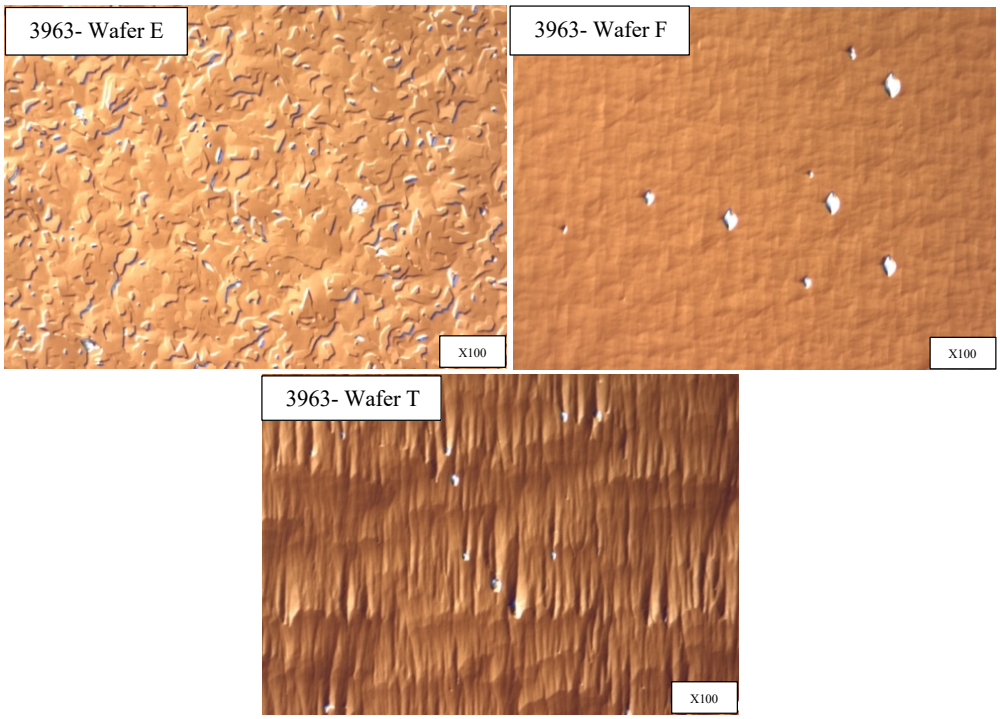
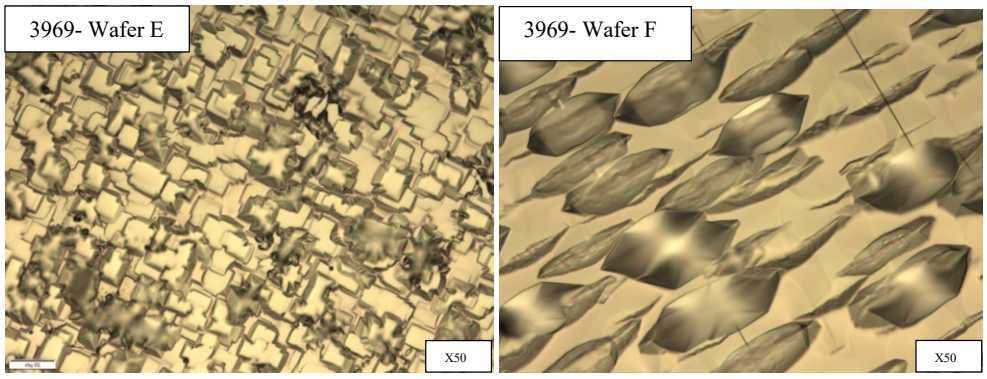


Figure 3-6: Top view of Si substrate wafers in run 3963.

In growth run 3963, wafer E again shows anti-phase domain and top view of wafer F shows a few pits which are not dense whereas wafer T has no pits and has a smoother surface.



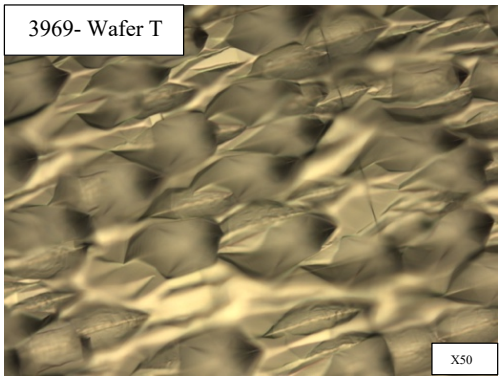


Figure 3-7: Top view of Si substrate wafers in run 3969.

In run 3969, again wafer E shows anti phase domain whereas wafer F has lots of pits close to each other and wafer T has larger pits but less dense than wafer F.

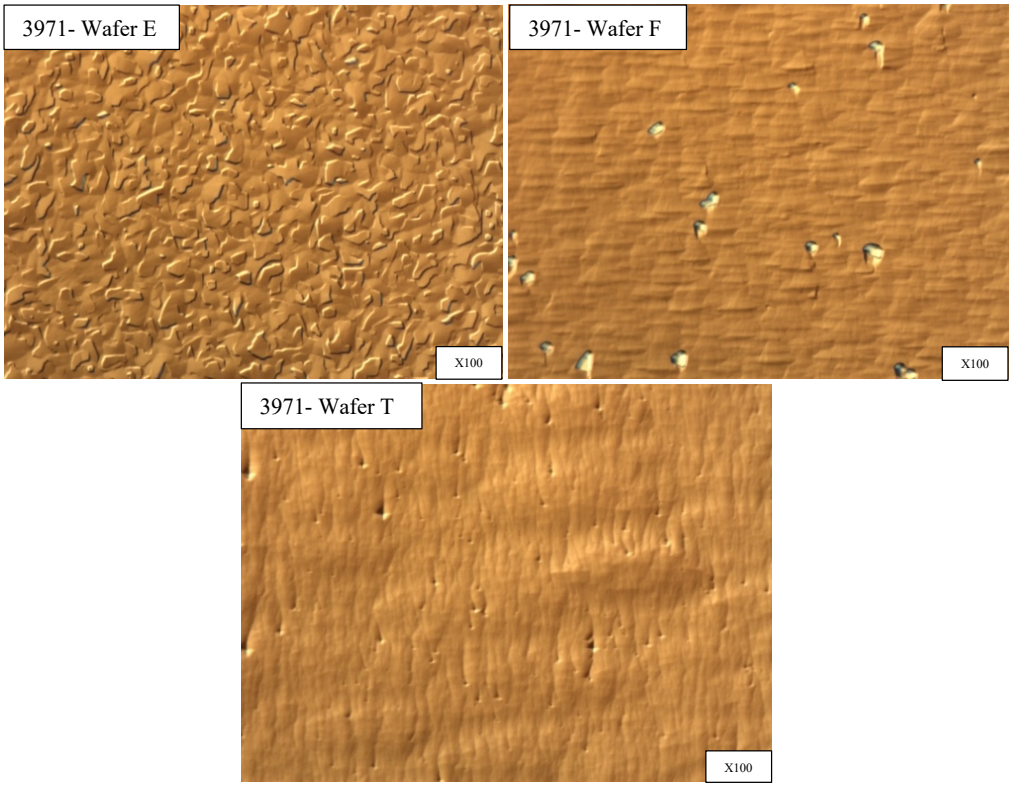


Figure 3-8: Top view of Si substrate wafers in run 3971.

In 3971, wafer E shows anti phase domain the same as other growth runs and wafer F surface is quite smooth without large pits which is a positive factor in device fabrication. Wafer T is also smooth but less smooth than wafer F.

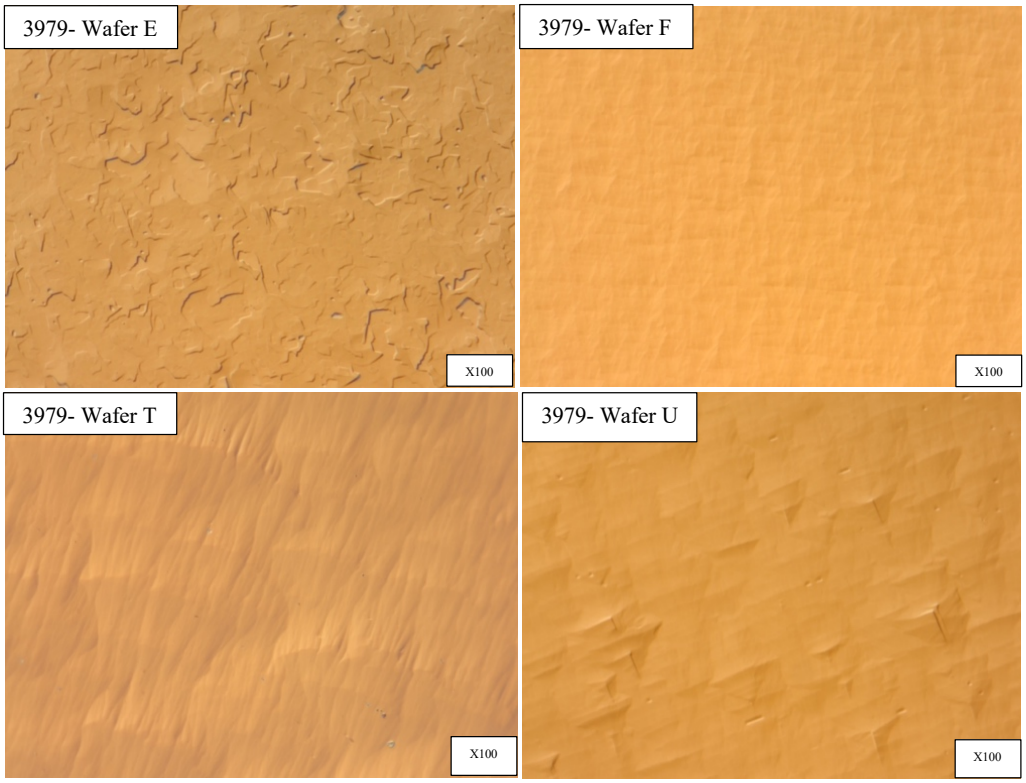


Figure 3-9: Top view of Si substrate wafers in run 3979.

In run 3979 wafer F has a very smooth surface the same as wafer T and U, but in wafer E anti phase domain still exists.
In conclusion, it seems in each run on on-axis GaAs/Si substrate wafers exhibit anti phase domain which is not desired and could affect the device functionality in a negative way. Off-cut GaAs/Si substrate wafers have a few pits, but the number of pits has decreased from run 3957 to 3979 due to growth conditions that will be discussed in 3.2.2.2. To sum up, it seems off-cut samples have a better crystalline quality in terms of morphology.

3.2.2.2 Comparing different growth runs

Figure 3-10 represents top view of On-axis GaAs/Si substrate wafers from different growth runs.

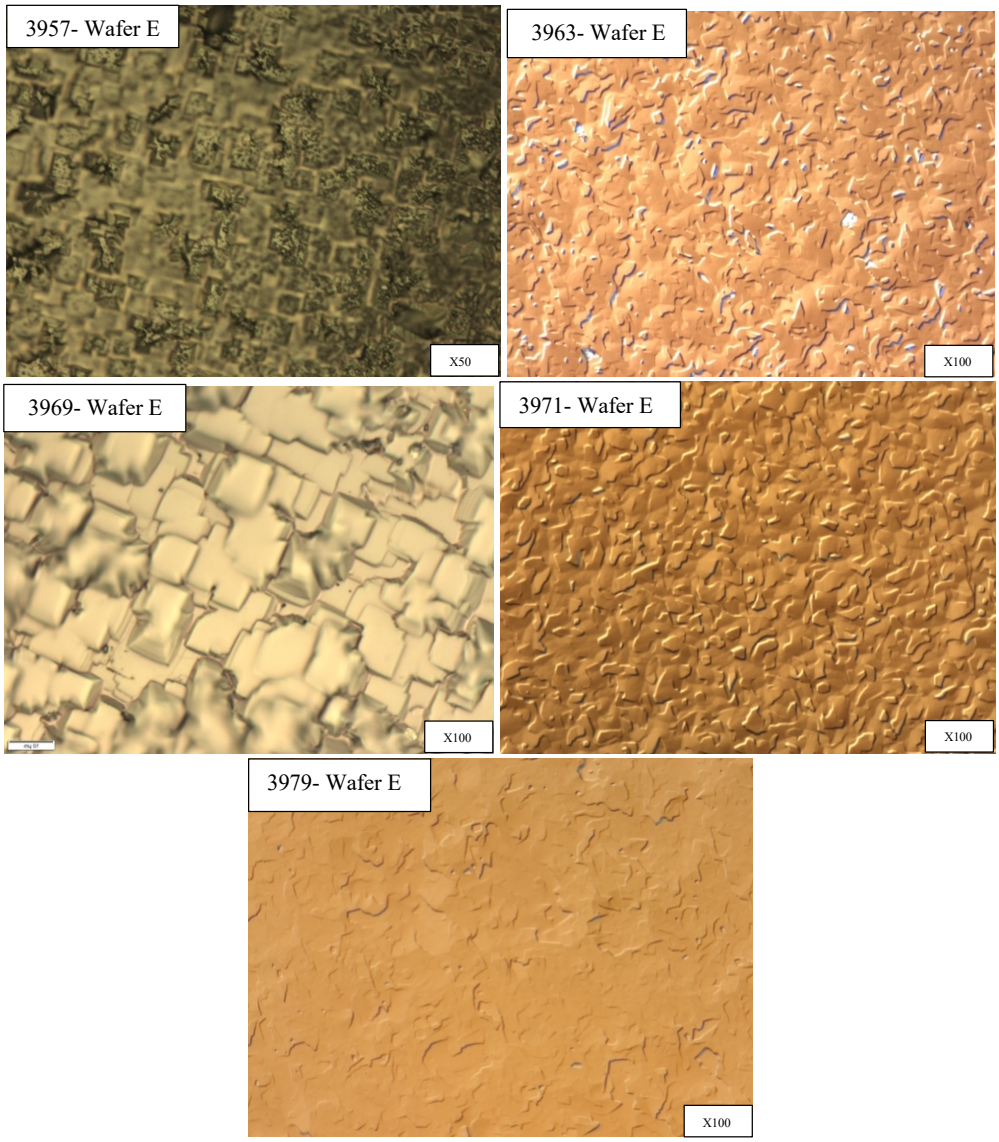


Figure 3-10: Top view of wafer E from different growth runs.

Wafer E in all runs shows anti phase domain, however the density of this defect is not the same in all the growth runs. Temperature in runs 3957 and 3969 are 660 ℃ and 710 ℃, respectively, which is higher than that in other runs, which is 610 ℃. Therefore, it seems lower temperature will produce smoother surface. Moreover, surface of wafer E from run 3979 is significantly smoother than that of wafer E from other runs. Looking at Table 3.3 one can infer increasing flow of AsH_3 from 15 sccm to 25 sccm and decreasing flow of PH_3 from 85 sccm to 75 sccm could improve the crystalline quality of the samples.

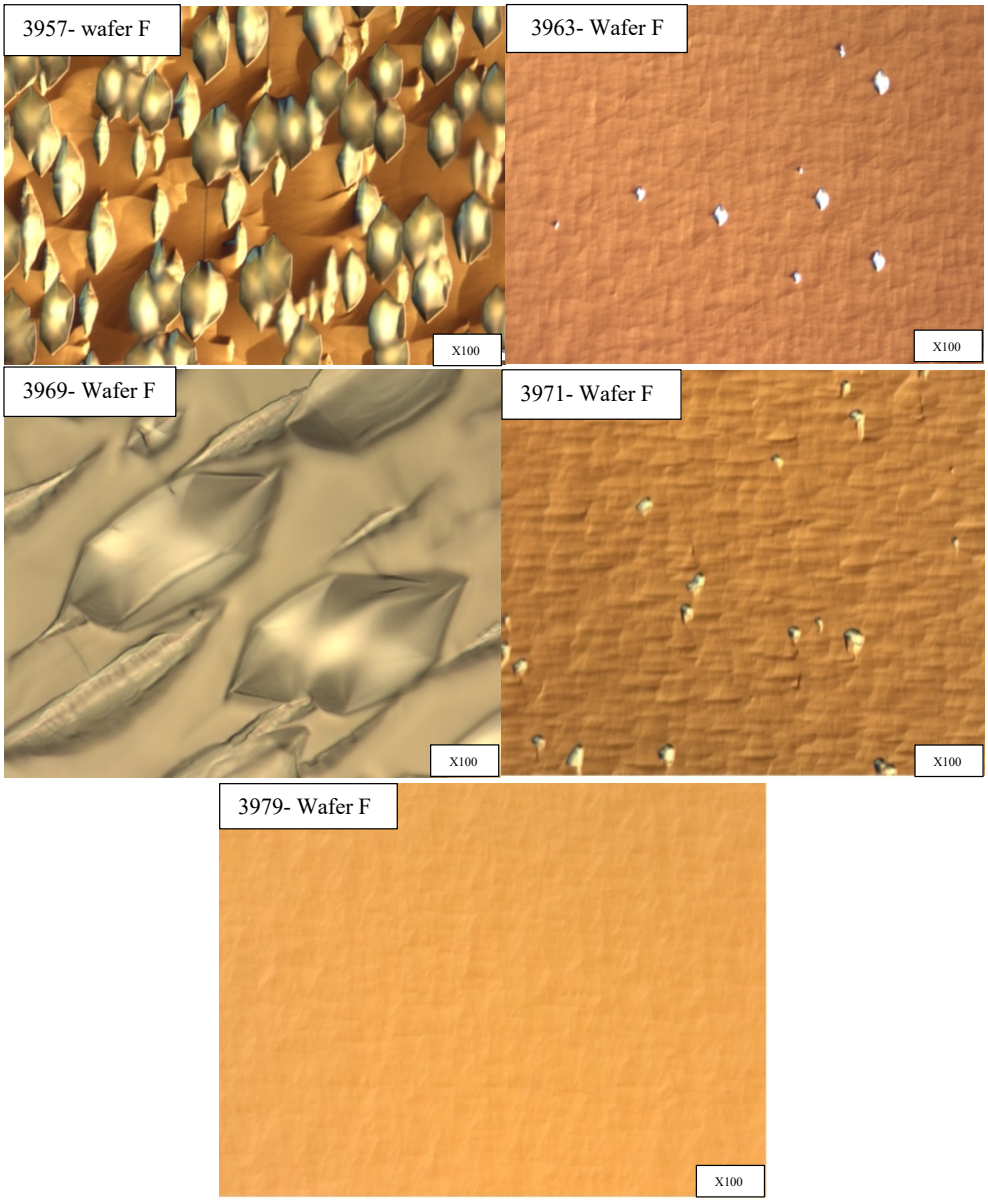


Figure 3-11: Top view of Wafer F from different growth runs.

As Figure 3-11 shows, among off-axis GaAs/Si substrate samples, runs 3957 and 3969 show more of large pits and pits of wafer F from run 3969 is larger than those from run 3957 indicating higher temperature will cause larger pits. Comparing runs 3963, 3971 and 3979, run 3971 and 3979 have smoother surface without pits and in these two runs GaCl flow has been increased from 15 sccm to 25 sccm. To be more precise, wafer F from run 3979 is even smoother than wafer F from run 3971 and the differences in the growth conditions of these two runs are AsH_3 and PH_3 flows. It seems by increasing the AsH_3 flow from 15 sccm to 25 sccm and decreasing the PH_3 flow from 85 sccm to 75 sccm, crystalline quality gets improved.

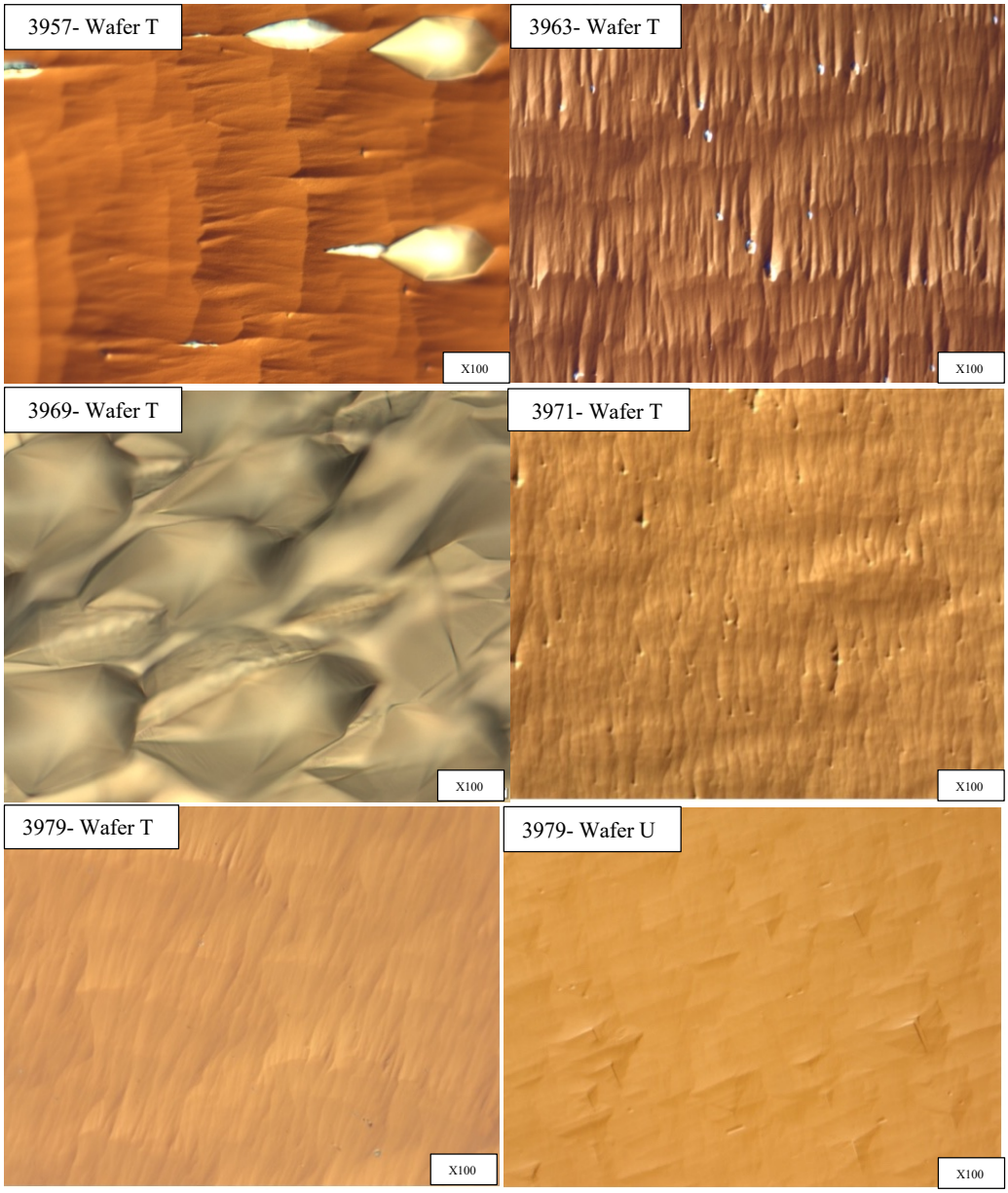


Figure 3-12: Top view of Wafer T from different runs and wafer U from run 3979.

Among the off-cut thickened GaAs/Si substrate wafers, runs 3957 and 3969 produce epi-layer with large pits due to high growth temperature. Wafer T from run 3979 has the smoother surface because of higher flow of AsH_3 and lower flow of PH_3.

Figure 3-13 shows the same result for n+ GaAs substrate samples: run 3979 produces a smoother surface which is desired for device fabrication.

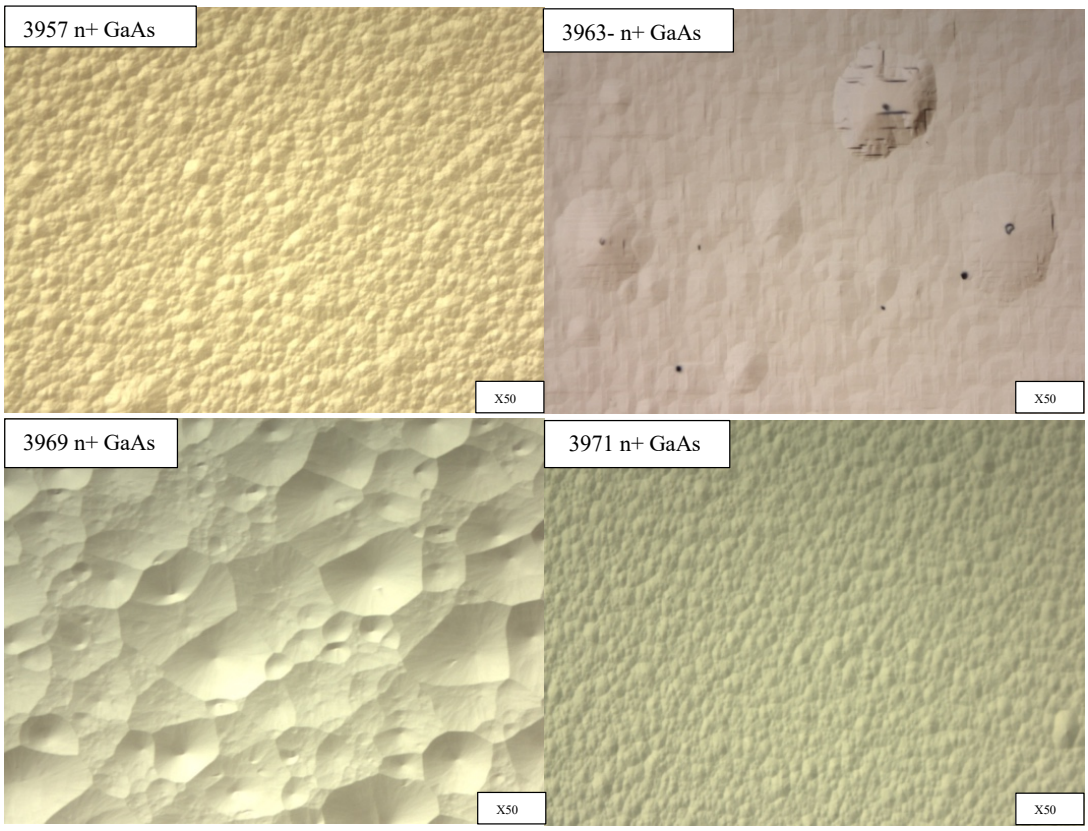


Figure 3-13: Top view of wafer n+ GaAs from different growth runs.

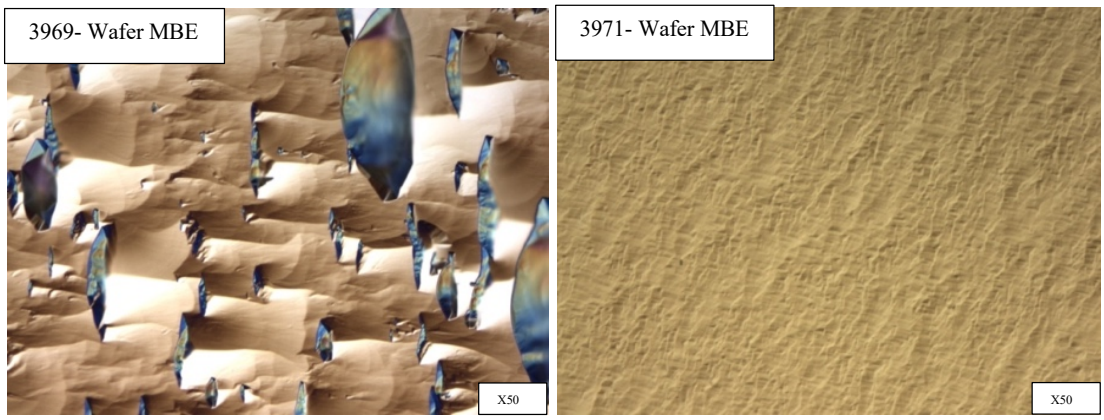


Figure 3-14: Top view of wafer MBE from different growth runs.

The top view of the wafer MBE from run 3969 shows large pits, but the surface of the wafer MBE from run 3971 has less roughness.

As a conclusion, the n+ GaAs substrate samples have smoother surface compared to Si substrate samples and among the Si substrate samples, off-cut GaAs/Si substrate (wafer F) and $GaAs_xP_{1-x}$/ Off-cut thickened $GaAs_xP_{1-x}$/ Si polished Seed (wafer U) show higher crystalline quality.

Considering the growth conditions, lower temperature leads to a better crystalline quality and also increasing the flow of AsH_3 and GaCl as well as decreasing the flow of PH_3 could improve the crystalline quality of the samples.
It can be said, the growth conditions for run 3979 are the best optimized growth conditions of all the others and are shown in Table 3.6; besides, off-cut GaAs/Si seed and $GaAs_xP_{1-x}$/ Off-cut thickened GaAs on polished Si substrate would be the best substrate for growing $GaAs_xP_{1-x}$ epitaxial layer.

Optimized growth conditions			
Temperature (°C)	Precursor flow (sccm)		
	AsH_3.source	GaCl	PH_3.source
610	25	25	75

Table 3.6: Optimized growth conditions.

4 Characterization of sharp solar cell samples

Since the size of the designed solar cell device is 1cm × 1cm, those samples that are large enough are used for device fabrication. Also, three more large samples are grown under the optimized growth conditions shown in Table 4.1, in run numbers 3999, 4001 and 4041.
Samples that are considered for solar cell fabrication, the so-called sharp samples, should be characterized by HRXRD and optical microscope to investigate the crystalline quality and composition as well as surface morphology.

4.1 Crystal quality and composition

Omega scan on $GaAs_xP_{1-x}$ layer in triple axis has been done for the sharp samples to obtain the FWHM value to assess the crystalline quality. In addition, Omega-2theta scan in double axis is done to get crystalline quality and also composition of samples.
Information deduced from HRXRD measurements of the sharp solar cell samples is presented in Table 4.1.

	HRXRD results of sharp solar cell samples			
Run number	Sample	Name of the sharp sample	GaAsP layer FWHM (arcsec)	Composition
3957	Wafer E	3957E	576	$GaAs_{0.63}P_{0.37}$
3957	Wafer F	3957F	468	$GaAs_{0.48}P_{0.52}$
3957	Wafer T	3957T	576	$GaAs_{0.58}P_{0.42}$
3963	Wafer F	3963F	540	$GaAs_{0.46}P_{0.54}$
3963	Wafer T	3963T	612	$GaAs_{0.63}P_{0.37}$
3999	$GaAs_xP_{1-x}$/ Thickened GaAs/Off-cut Si substrate- Wafer CD	3999CD	612	$GaAs_{0.68}P_{0.32}$
4001	$GaAs_xP_{1-x}$/ Thickened and CMPed GaAs/ On-axis Si substrate- Wafer S	4001S	720	$GaAs_{0.72}P_{0.28}$
4041	$GaAs_xP_{1-x}$/ GaAs grown on Off-cut Si substrate via MOVPE- Wafer DV	4041DV	468	$GaAs_{0.74}P_{0.26}$

Table 4.1: Information deduced from HRXRD measurement for the sharp solar cell samples.

Omega scan in triple axis on $GaAs_xP_{1-x}$ layer has been done for the sharp solar cell samples and plots in logarithmic scale are presented in Figure 4-1.

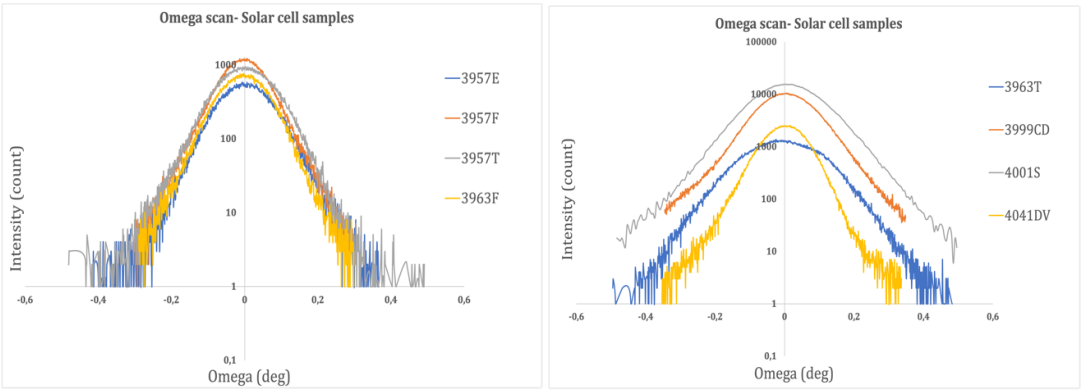


Figure 4-1: Omega plots of solar cell samples.

Looking at Table 4.1 and also Figure 4-1 it can be seen that samples 3957F and 4041DV have the lowest FWHM values which is 468 arcsec representing the highest crystalline quality whereas FWHM value of sample 4001S is 720 arcsec which is the highest FWHM value among the sharp solar cell samples. Omega-2theta scans in double axis presented in linear form in Figure 4-2.

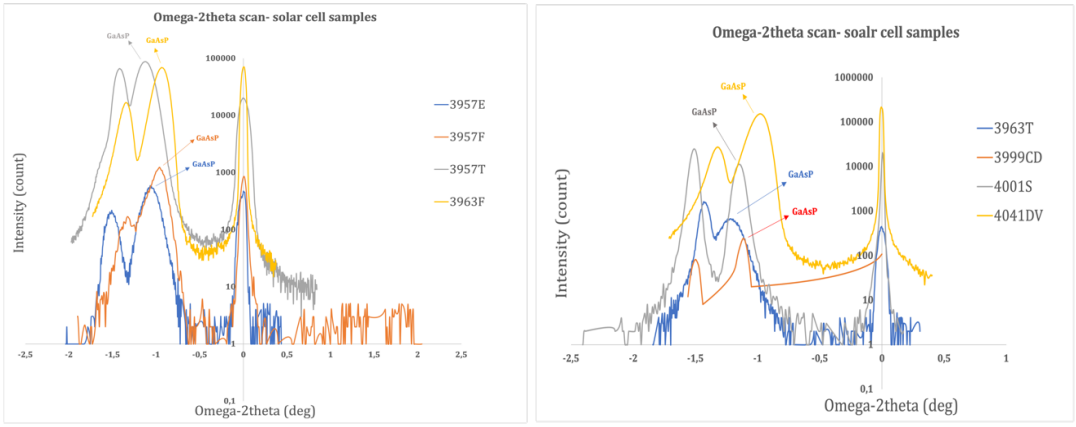


Figure 4-2: Omega -2theta plots of sharp solar cell samples.

Figure 4-2 shows 3957T and 4041DV have the highest intensity among other sharp samples and 4041 DV has the lowest FWHM value indicating the best crystalline quality. The lowest intensity belongs to sample 3999CD, and this sample had the second highest FWHM value which shows the second worst crystalline quality.
So, sample 4041DV in both omega and omega-2theta scan represents the best crystalline quality, but this result should be confirmed by morphology investigation as well.

In this thesis HRXRD is used to investigate the composition of epi-layer, but as it was mentioned before PL measurement also provides information about composition of the epitaxial layer and similarity in results from HRXRD and PL indicates that characterizations are done correctly. So, PL characterization has been done on sample 4041DV during the fabrication process, before dry III-V etching (shown in Figure 5-1) and PL spectra is presented in Figure 4-3.

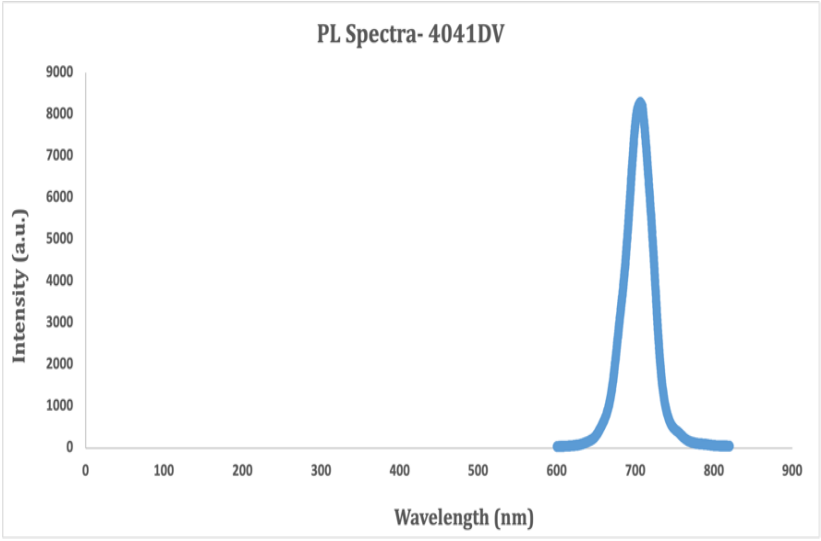


Figure 4-3: Photoluminescence spectra of sample 4041DV, at middle of the sample, before dry III-V etching.

The most important information of PL spectra is the bandgap energy which can be obtained by knowing the wavelength of peak. For sample 4041DV, the wavelength of the peak is 709.04 nm, so bandgap energy can be calculated by using the following equation:

$$E_g = h\upsilon = \frac{hc}{\lambda} = \frac{(6.63 \times 10^{-34})[j.s] \times (3 \times 10^{8})[\frac{m}{s}]}{709{,}04 \times 10^{-9}[m]} = 1.7\ [ev]$$

Where, h is Planck's constant and c is the light speed. The bandgap of the material is calculated as $E_g = 1.7$ eV. Composition of the epi-layer can be calculated by Vegard's law **[19]**:

$$E_{gGaAs_xP_{1-x}} = 2.75 - 1.54x + 0.21x2 \text{ eV},$$

$$x = 0.75$$

Data obtained by PL characterization on sample 4041DV is summarized in Table 4.2.

Information from PL spectra – Sample 4041DV		
Wavelength (nm)	Bandgap (eV)	Composition
709.04	1.7	$GaAs_{0.75}P_{0.25}$

Table 4.2: Information about PL characterization.

Composition of $GaAs_xP_{1-x}$ epi-layer for sample 4041DV obtained by PL characterization is $GaAs_{0.75}P_{0.25}$ that confirms the $GaAs_{0.74}P_{0.26}$ obtained from HRXRD characterization.

4.2 Surface morphology

Optical microscope images from the top view of solar cell samples are represented in Figure 4-3.

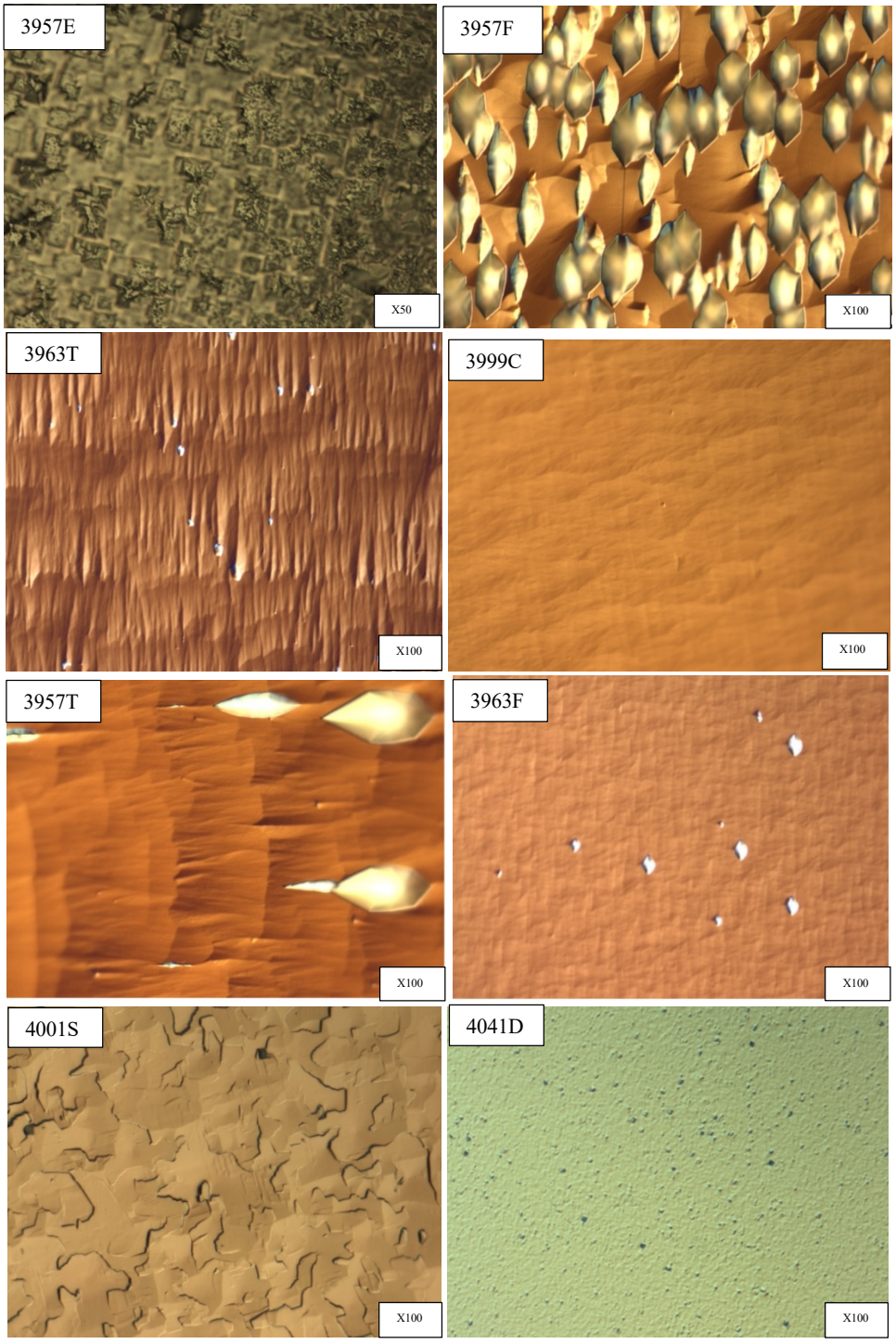


Figure 4-4: Top view of solar cell samples.

Figure 4-4 shows that sample 3957E and 4001S have anti phase domain, and as it was mentioned before on-axis samples exhibit this defect more. However, this defect in 4001S is less dense compared to 3957 probably because of lower growth temperature. Samples 3957F and 3963T have large pits as

mentioned before. Sample 3999CD has a few pits which are not dense and 4041DV has a smooth surface which is desired for device fabrication.
Sample 3999CD, 4001S and 4041DV are grown under the same conditions, but the crystalline quality is quite different due to their substrates. It seems $GaAs_xP_{1-x}$ epitaxial layer which is grown by MOVPE on off-cut GaAs/Si substrate shows smoother surface and better crystalline quality.

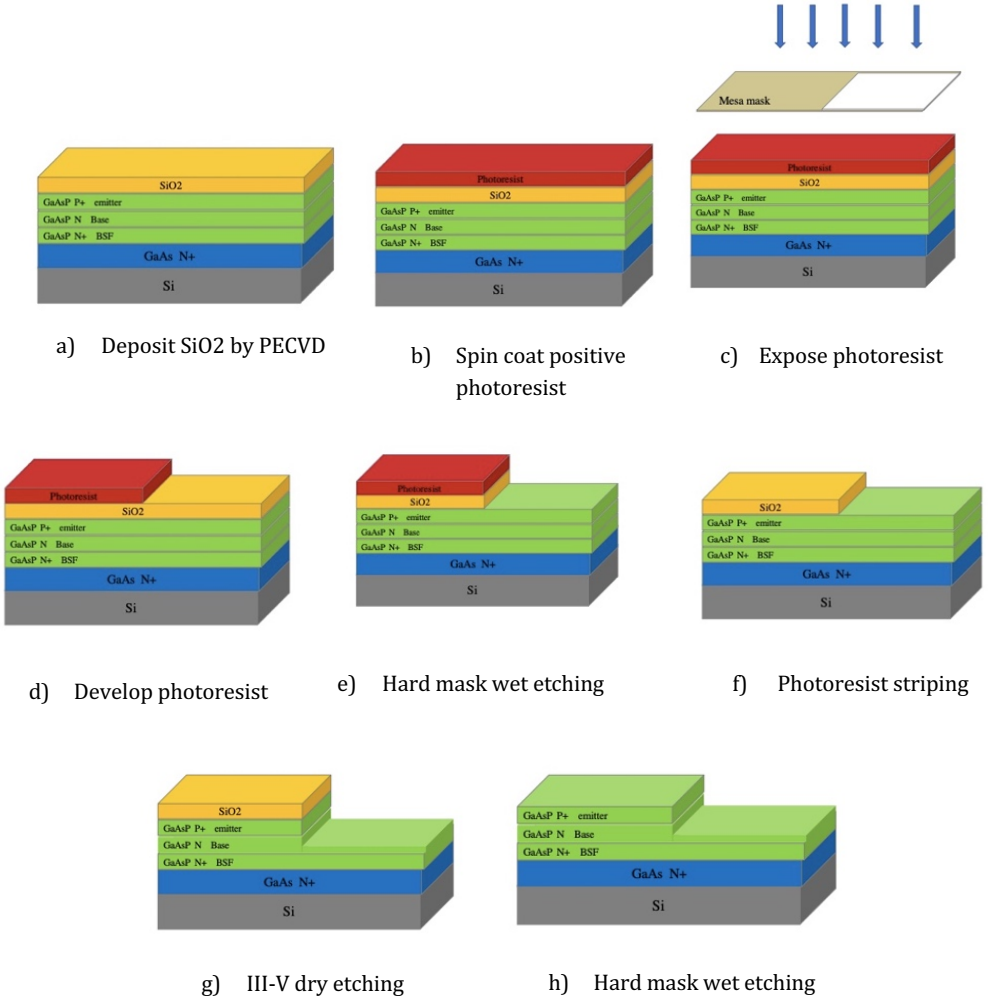
5 Solar cell fabrication

In previous chapters the process of choosing samples for solar cell fabrication as well as characterization of the chosen samples were studied.
The base of solar cell structure which is pn-junction is formed on $GaAs_xP_{1-x}$ layer consisting of emitter, base, and back surface field (BSF) on substrate grown by HVPE. In this thesis a single-junction solar cell is fabricated and in this chapter the process of formation top metal contact on p-side and middle metal contact on n-side of the pn-junction will be studied and described.
Since there are many steps in fabrication process of solar cell, to make it easier to follow, in this thesis steps are categorized in 3 sections as below.

- Dry etching process for III-V semiconductors
- P-contact formation
- N-contact formation.

5.1 Dry etching process for III-V semiconductors

The schematic form of different steps to process samples for dry etching is shown in Figure 5-1.



a) Deposit SiO2 by PECVD

b) Spin coat positive photoresist

c) Expose photoresist

d) Develop photoresist

e) Hard mask wet etching

f) Photoresist striping

g) III-V dry etching

h) Hard mask wet etching

Figure 5-1: Dry etching process flow for III-V semiconductors in the sharp samples.

As it is shown in Figure 5-1 (a), a thin layer of SiO_2 is deposited on sample as hard mask by PECVD at 300°C. Before running the recipe, preconditioning must be done and then solar cell samples with a Si reference sample are put in PECVD chamber and recipe "YS OXID STD 4KA" is run for 6 minutes and 30 seconds. After deposition session, the thickness of the oxide layer is measured by interferometer for Si reference sample. Since the deposition of SiO_2 is not performed for all the samples in one session, hard mask thickness is slightly different from one sample to another. Table 5.1 shows the thickness of the hard mask for different samples.

Sample	3957E	3957F	3957T	3963F	3963T	3999CD	4001S	4041DV
SiO_2thickness (nm)	483.6	483.6	483.6	483.6	483.6	476.2	476.2	483

Table 5.1: Thickness of SiO_2 layer deposited on samples.

After oxide deposition, samples should be coated by a positive photoresist in a spin coater illustrated in schematic form in Figure 5-1(b). To do so first adhesion coating is done on samples in tool HMDS, with the recipe "HMDS2" for 16 minutes. And then positive resist S1813 is coated on sample surface in spin coater with recipe "4000rpm" and then the resist is baked in hotplate for 90 seconds. For some sample the baking temperature was 100℃, but since in lithography step there were some damages on the pattern after exposure for these samples, we decided to increase the baking temperature to 115 ℃ which was a successful decision. Table 5.2 shows the baking temperature for all the sharp solar cell samples.

Sample	3957E	3957F	3957T	3963F	3963T	3999CD	4001S	4041DV
Baking temperature (℃)	100	100	100	100	100	115	115	115

Table 5.2: Thickness of SiO_2 layer deposited on samples.

After baking the samples in hotplate, "mesa etch photo mask," which was designed for this project is used to pattern the photoresist with mask aligner for 7.5 seconds as Figure 5-1(c) shows.
First, vacuum contact mode with alignment gap of 30 μm was used for some samples but since resist was stuck to the mask and contaminated it and we had to remove photoresist and repeat the process again, we decided to change the mode to hard contact and increased alignment gap. Sample 3963T broke after lithography step and it seems vacuum contact is not a good choice for small samples.
After this calibration, checking the pattern on microscope in yellow room showed that pattern was still not perfectly transferred onto the samples and for sample 4041DV we decided to increase alignment gap even more and use soft contact mode.
In soft contact the wafer and photomask are just brough into contact without any force, whereas in vacuum contact and hard contact a force is applied to press them towards each other. So, soft contact is the best option to avoid breaking the wafer and contaminating the mask which makes the pattern imperfect. In addition, increasing the alignment gap would also avoid sticking of the resist to the photomask which would improve the quality of the transferred pattern.
Table 5.3 shows information on the lithography procedure.

Sample	3957E	3957F	3957T	3963F	3963T	3999CD	4001S	4041DV
Exposure mode	Vacuum contact	Vacuum contact	Vacuum contact	Vacuum contact	Vacuum contact	Hard contact	Hard contact	Soft contact
Alignment gap (μm)	30	30	30	30	30	100	100	200

Table 5.3: Exposure information on lithography procedure adopted for the sharp solar cell samples.

After exposure, the desired pattern will be transferred after using a suitable developer, which is CD-26 for resist S1813, in two steps one for 30 seconds and then for 15 seconds. For the positive photoresist, the exposed part of the resist is removed by using the developer which is shown schematically in Figure 5-1 (d). After using the developer, the possible residual photoresist is removed with plasma treatment in Tepla with recipe "program 10- with cage".
Then the uncovered hard mask is removed with wet etching using Buffered oxide etchant (BOE) that is an etchant to removing SiO_2 and Si_3N_4 thin films.shown in Figure 5-1 (e)for a desired time. To calculate the etch rate, Si reference wafer with SiO_2 layer on it has been etched with buffered oxide etchant for 1 minute and 10 seconds and then the thickness of SiO_2 after etching is measured by interferometer. Target etch depth is also calculated by the sum of SiO_2 thickness and 50% of it (over etch). Etch rate and target etch depth as well as etch time for the sharp solar cell samples are summarized in Table 5.4.

Sample	3957E	3957F	3957T	3963F	3999CD	4001S	4041DV
Etch rate (nm/min)	373.2	373.2	373.2	373.2	292.4	292.4	373.2
Target etch depth	725.4	725.4	725.4	725.4	714.4	714.4	725.4
Etch time (s)	110	110	110	110	127	127	110

Table 5.4: Information about wet etching of the SiO_2 hard mask.

After wet etching the hard mask, remaining photoresist is striped by solvents such as acetone and iso propanol and also with plasma treatment with recipe "Program 4- without cage" as shown in Figure 5-1 (f).
III-V dry etching is performed on $GaAs_xP_{1-x}$ layer on samples by ICP with recipe "YS GaAs etch" for a desired time. First cleaning is performed with recipe "SF6 clean" for 20 minutes and then conditioning is run with dummy wafer for 15 minutes with recipe "GaAs Condition".
First, the etch rate should be calculated and to do so the thickness of SiO2 layer of a reference sample (undoped GaAsP 3887) is measured in Tencor. After that we put the reference sample in ICP for 10 minutes, and the depth is measured in Tencor after etching as well. This depth is the sum of SiO_2 thickness and etched $GaAs_xP_{1-x}$ layer and since we know the thickness of SiO_2 layer, the etched depth of $GaAs_xP_{1-x}$ layer can be calculated. Therefore, etch rate can be obtained and since the target etch is determined, one can calculate the etch time. Information about III-V dry etching is presented in Table 5.5.

Sample	3957E	3957F	3957T	3963F	3999CD	4001S	4041DV
Etch rate (μm/min)	1.15	1.15	1.15	1.15	1.15	1.15	0.7
Target etch depth (μm)	3.5	3.5	3.5	3.5	3.5	3.5	2
Etch time (min)	3	3	3	3	3	3	2 min,50s

Table 5.5: Information about dry etching for III-V semiconductors.

After doing dry etching, samples should be characterized by SEM to check the etch depth more precisely.
SEM measurement has been done for sample 3957E and since the stage was tilted 42°, to calculate the real depth triangle shown in Figure 5-2 (b) should be considered.

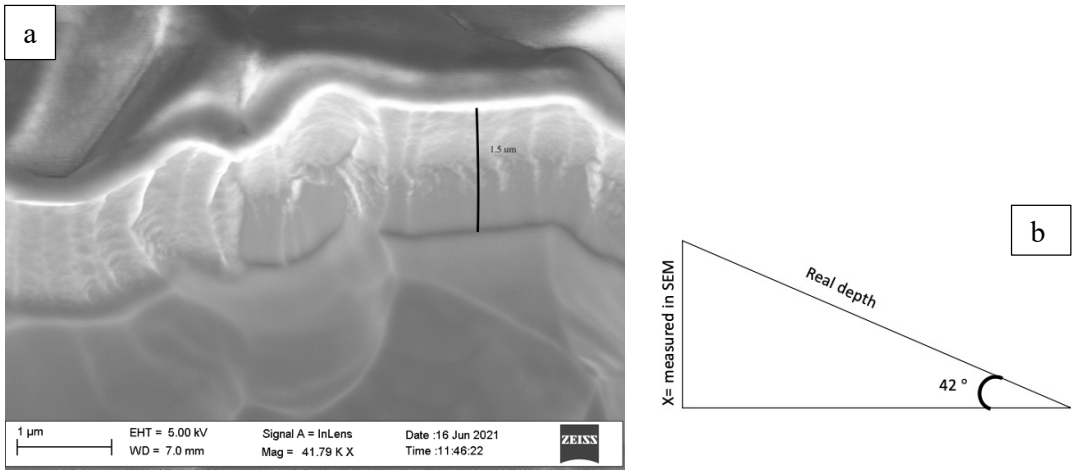


Figure 5-2: **a) SEM image of side wall of sample 3957E after dry III-V etching, b) real depth calculation.**

$$sin\,42 = \frac{x}{Real\ depth}$$

Therefore, real depth can be calculated as below:

$$Real\ depth = \frac{x}{sin\,42} = \frac{1.5\ \mu m}{0.67} = 2.08\ \mu m$$

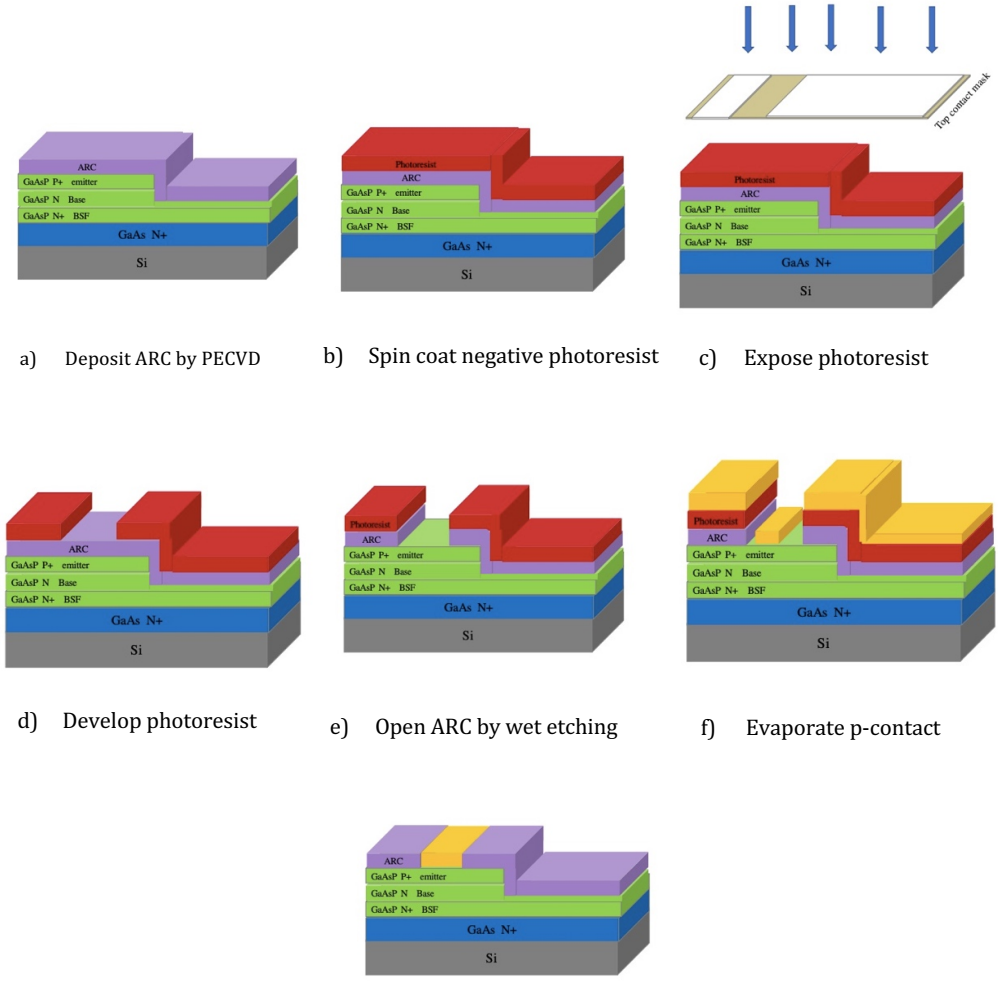
So, the real etch depth is 2.08 μm whereas the target etch depth was 3.5 μm.

After dry III-V etching for sample 4041DV, sample is cleaned with diluted nitric acid (69.5%) to remove any contamination caused by III-V dry etching. A 1:2 mixture of nitric acid and DI water is used that etches the sample very slightly. This procedure was found to be necessary as it was found that the device performance improved after this step.

Once dry etching is done and etch depth is checked with SEM, the oxide layer should be removed which is done by Buffered oxide etchant for 6 minutes and is shown in Figure 5-1 (h).
Sample 3957F broke after dry etching.

5.2 P-contact formation

Schematic form of different steps for p-contact formation is shown in Figure 5-3.



a) Deposit ARC by PECVD b) Spin coat negative photoresist c) Expose photoresist

d) Develop photoresist e) Open ARC by wet etching f) Evaporate p-contact

g) Pattern p-contact by lift off

Figure 5-3: P-contact formation.

P-contact of the solar cells consisting of Cr 40nm/ Au 180nm should be formed on p-side of the pn-junction but there are some steps that must be done before, and the first step is depositing a thin layer of anti-reflection coating (ARC).
When light shines on solar cell, incident beams are either reflected or absorbed and clearly absorbing more light creates more electrical current. Therefore, a thin layer of silicon nitride (Si_3N_4) is coated on the solar cell device to prevent reflection of incident beam.
In this work Si_3N_4 is deposited on top of the samples as ARC as well as hard mask for lithography process. The schematic form of the sample after ARC deposition in PECVD is shown in Figure 5-3 (a).

First cleaning must be done in PECVD with the recipe “P PLASMACLEAN” to avoid contamination of SiO_2 in chamber, and after that conditioning is done with recipe “NIT CONDITION 300” for 5 minutes. By conditioning we basically coat the chamber walls with the material which is Si_3N_4 here to make sure the deposition is done homogenously. The target thickness is 76 nm, but to calculate the

deposition rate and desired deposition we run the recipe “YS spacer 300C” for 10 minutes. Then thickness of Si_3N_4 is measured by interferometer and the deposition rate and the desired deposition time are calculated.
Finally, ARC is deposited on the sharp solar cell samples for calculated time and information about this deposition is summarized in Table 5.6.

Sample	3957E	3957T	3963F	3999CD	4001S	4041DV
Deposition rate (nm/min)	15.88	14.13	14.13	14,13	14,13	14,12
Deposition time	4 min, 50 sec	5 min, 22 sec	5 min, 22 sec	5 min, 22 sec	5 min, 22 sec	5 min, 22 sec
Measured ARC thickness (nm)	68.26	68.26	68.26	85.91	85.91	83.16

Table 5.6: Information about deposition ARC for p-contact.

Since ARC needs to be patterned to put the top contact metal inside it, first samples are adhesion coated in HMDS with recipe “HMDS2” for 16 minutes and then coated with negative resist ma-N 1420 with recipe “3000 rpm” in spin coater. Then all samples are baked in hotplate at 100 °C for 120 seconds, the schematic form of samples are shown in Figure 5-3 (b).
Top contact mask designed for this project is used to pattern the photoresist in mask aligner for 27.5 seconds with soft contact mode. Before exposure, alignment needs to be done to make sure that sample is placed in right position under the photomask and alignment gap is also set to 100 μm for all samples. Schematic form of the sample after exposure is shown in Figure 5-3 (c).
After exposure, developer ma-D 533 is used for 100 seconds to reveal the pattern and as negative photoresist is used, unexposed part of photoresist is removed. The residual photoresist is removed by plasma treatment in Tepla with recipe “program 10-with cage” for 1 minute. This procedure is shown schematically in Figure 5-3 (d).
In the next step ARC should be opened to enable depositing the top contact on the semiconductor which is done by etching with buffered oxide etchant for desired time as it is shown schematically in Figure 5-3 (e).
To calculate the etch time and etch rate, Si reference wafer with Si_3N_4 layer on it has been etched with buffered oxide etchant for 1 minute and 10 seconds and then the thickness of Si_3N_4 after etching is measured by interferometer from which the etch rate is calculated to be 98.88 nm/min for all the samples. Target etch depth is also calculated by from the sum of Si_3N_4 thickness and 50% of it (over etch). Target etch depth and etch time for the sharp solar cell samples are reported in Table 5.7.

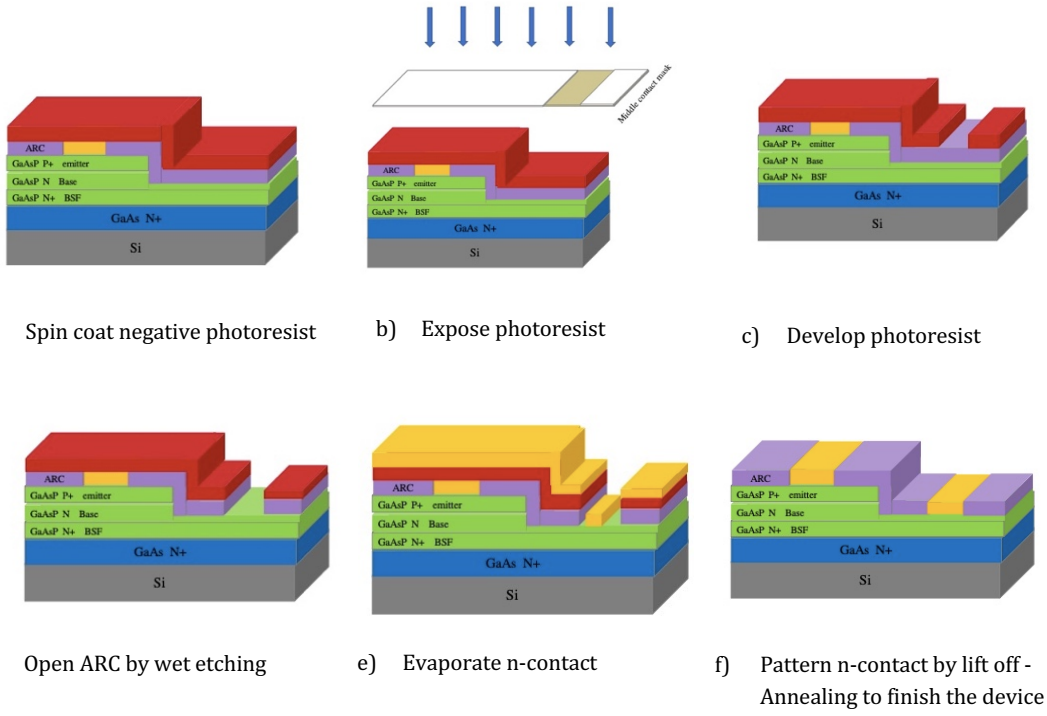
Sample	3957E	3957T	3963F	3999CD	4001S	4041DV
Target etch depth (nm)	128.9	102.4	102.4	128.9	128.9	124.7
Etch time	1 min, 3 sec	1 min, 3 sec	1 min, 3 sec	1 min, 19 sec	1 min, 19 sec	1 min, 15 sec

Table 5.7: Information about wet etching the ARC for p-contact.

In this step, Cr and Au are deposited on the p-side as top metal contact of the samples by metal evaporation with recipe “HMA-device 2- top contact-v1”. Cr is used as the adhesion layer deposited first on $GaAs_xP_{1-x}$ layer with the thickness of 40 nm and Au which is a good conductor for electricity is deposited on top of it with thickness of 180 nm. The schematic form of the sample is shown in Figure 5-3 (f). After depositing the top contact metal, lift-off process is used to remove the metal from the surface of the resist by keeping samples in acetone until all the metal on the resists removed. Sample after lift-off process is shown schematically in Figure 5-3 (g).

5.3 N- contact formation

Schematic form of different steps for n-contact formation is shown in Figure 5-4.



a) Spin coat negative photoresist

b) Expose photoresist

c) Develop photoresist

d) Open ARC by wet etching

e) Evaporate n-contact

f) Pattern n-contact by lift off - Annealing to finish the device

Figure 5-4: N- contact formation.

When the p-contact is formed, samples are prepared for depositing the middle metal contact on n-side of the pn-junction. N-contact contains Au 100nm (bottom layer)/ Ge 50nm/ Ni 50nm/ Au 100nm (top layer) for samples 3057E, 3957T, 3963F and 4001S but after characterizing these samples, we decided to increase the thickness of the top Au layer to 600 nm.
First of all, samples are adhesion coated in HMDS with recipe “HMDS2” for 16 minutes, and then are coated with negative photoresist ma-N 1420 with recipe “3000 rpm” in spin coater. Coated samples

need to be baked in hotplate at 100 ℃ for 120 seconds. This whole procedure is shown schematically in Figure 5-4 (a).
N-contact photomask designed for this project is used to pattern the samples in mask aligner with soft contact mode and 100 μm alignment gap is used for all the samples. Before exposure, alignment must be done to make sure that samples are in the right place under the photomask. Alignment marks and TLM patterns are used to align the samples and once the sample and the photomask are aligned, exposure is done for 27.5 seconds. This step is shown schematically in Figure 5-4 (b).
Developer ma-D 533 is used to develop and reveal the pattern of the mask on samples for 120 seconds and since negative photoresist is used, unexposed parts of the photoresist is removed by the developer as Figure 5-4 (c) shows.
Sample 3999CD broke during the lithography process.
In the next step, ARC should be opened with wet etching by buffered oxide etchant but etch rate and etch time need to be calculated in the same way as done for the top contact formation. So, etch rate is 98.88 nm/min for all the samples from which the etch time and the target etch depth are calculated. The results are summarized in Table 5.8.

Sample	3957E	3957T	3963F	4001S	4041DV
Target etch depth (nm)	102.39	102.39	102.39	128.86	124.78
Etch time	1 min, 3 sec	1 min, 3 sec	1 min, 3 sec	1 min, 19 sec	1 min, 16 sec

Table 5.8: Information about wet etching the ARC for n-contact.

Samples are ready for metallization, so Au 100nm (bottom layer) / Ge 50nm/ Ni 50nm/ Au 100nm are deposited as n-contact for samples 3957E, 3957T, 3963F and 4001S by e-beam metal evaporation with recipe “HMA-device2-middle contact-V1”. As it was mentioned before, after characterizing solar cell samples (except for 4041DV), we have decided to increase thickness of top Au layer, to 600nm, so for sample 4041DV thickness of the top Au layer is 600nm. Figure 5-4 (e) shows schematic of the metal evaporation step.
Lift-off must be done on samples to remove unwanted metal from the resist surface, so samples are put in baker full of Acetone. For sample 4041DV since Au thickness was so high, lift off process was quite difficult and time consuming.
To finish the devices, they need to be annealed at 380 ℃ for 1-minute and the schematic of final step in solar cell device fabrication is shown in Figure 5-4 (f).

6 Solar cell characterization

When solar cell devices are fabricated, they should be characterized to figure out their performance. Two kinds of characterization have been done on the solar cells, TLM measurements and IV measurement.
Top view of the fabricated devices is shown in Figure 6-1: samples 3957E, 3957T, 3963F and 4001S are at the left and the whole wafer 4041DV containing 8 solar cells are at right.

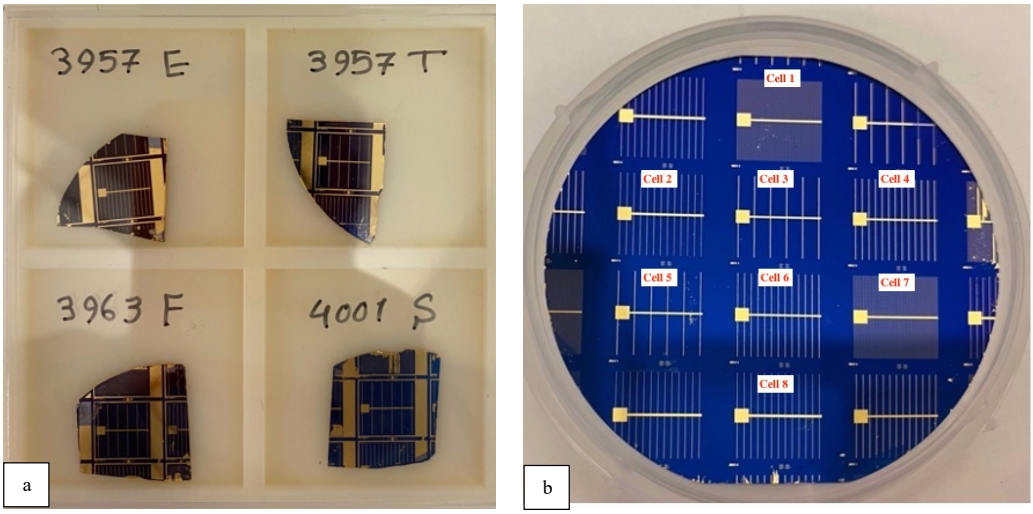


Figure 6-1: **Picture of fabricated Solar cell devices, b) picture of under processing solar cell device 4041DV (including Cell 1-Cell 8)**

6.1 TLM measurement

TLM measurement is performed to measure parameters such as specific contact resistance and sheet resistance.
This measurement is done for both the p-contact and the n-contact as well.
As it is mentioned in chapter 5, the p-contact of the solar cell includes Cr 40nm/ Au 180nm and the n-contact Au 100 nm/ Ge 50 nm/ Ni 50 nm/ Au 100 nm (top layer). For sample 4041DV the Au (top layer) thickness has been increased to 600 nm.
For some devices, measurement has been done using TLM pattern on top of the cell as well as TLM pattern on bottom of the cell. In this case the average value of parameters is reported.
TLM measurement for the top contact has been done for most of the devices and the results are presented in Table 6.1.

TLM measurement, p-contact				
Device	Contact resistance (Ω)	Specific contact resistance ($\Omega.cm^2$)	Sheet resistance (Ω/sq)	Transfer length (μm)
3957T	7.5	$2.4x10^{-5}$	924	1.6
3963F	-	$1.2x10^{-5}$	534	-
4001 S	7.6	$4.6x10^{-5}$	506.8	3
4041DV – Cell 1	1.9	$9.6x10^{-6}$	143.8	2.6
4041 DV– Cell 2	1.5	$7.1x10^{-6}$	128.4	2.4
4041 DV– Cell 3	2.4	$1.5x10^{-5}$	150	3.1

4041 DV– Cell 4	2.6	$1.8x10^{-5}$	145.9	3.5
4041 DV– Cell 5	0.2	$8.8x10^{-8}$	123.7	0.3
4041DV – Cell 6	-	$3.2x10^{-9}$	152.5	-
4041DV – Cell 7	0.3	$2.8x10^{-7}$	148.3	0.4
4041DV – Cell 8	0.1	$7.4x10^{-8}$	108.6	0.3

Table 6.1: p-contact TLM measurement of solar cells.

Obviously, when specific contact resistance and sheet resistance are low, electrical current would be able to flow through the device easily. By looking at Table 6.1, it can be seen before n-contact formation, Cell 5 and Cell 8 have the lowest specific contact resistance as well as lowest sheet resistance among other solar cells.
Since the thickness of the Au top layer of the n-contact had been increased for 4041 Wafer DV, the lift off process was not completely done. Therefore, it was not possible to do the TLM measurement for n-contact for device 4041DV.
Information on the TLM measurement for the n-contact for other solar cells is presented in Table 6.2.

TLM measurement, n-contact				
Device	Contact resistance (Ω)	Specific contact resistance ($\Omega.cm^2$)	Sheet resistance (Ω/sq)	Transfer length (μm)
3957E	-	5.4×10^{-6}	1766	-
3957T	22.4	6.5×10^{-3}	30.8	145.7
3963F	7.5	2.4×10^{-6}	93.7	15.9
4001S	7.8	1.03×10^{-3}	23.4	66.2

Table 6.2: n-contact TLM measurements of solar cells.

Among devices that TLM measurement of n-contact is done, 3957E has the lower specific contact resistance, but the sheet resistance value is quite high. On the other hand, sample 3957T has the highest specific contact resistance, but the sheet resistance is low.

6.2 Current-voltage (IV) characterization

Each fabricated solar cell has its own IV curve which shows the relation between voltage and current flowing through a solar cell device. Investigation of current-voltage relation gives information about the performance of the devices.
In this project two kinds of IV curves are produced, namely, dark curve (i.e., under dark conditions) which is useful to investigate the diode properties of the cell and light curve (i.e., under illumination) which shows the behavior of solar cell exposed to sunlight simulation spectrum (AM1.5). Properties such as efficiency, open circuit voltage, short circuit current and fill factor can be obtained from light curves.
Solar cell samples are categorized in two batches as below.

Batch1: 3957E, 3957T, 3963F, 4001S
Batch2: 4041DV (Cell 1- Cell 2- Cell 3 – Cell 4- Cell 5- Cell 6- Cell 7- Cell 8)

Solar cells in the dark acts like a diode, so its IV curve should be the same as IV curve of an ideal diode, but this is not always the case. The dark current curve of the solar cell sometimes shows deviation from an ideal diode IV curve and that could be due to series resistance, parallel resistance (shunt) or combination of both resistances.
To be more precise, a diode with a series resistance shows a deviation from the exponential behavior at higher current and a diode with shunt resistance shows a hump in log scale curve at lower currents. So, a diode with series and shunt resistances would show deviation from exponential behavior at high current as well as hump at low current.
Flowing electrical current through emitter and base and also high resistance of the metal contacts can cause series resistance.
Series resistance does not have effect on V_{oc} because the current flowing through solar cell and therefore through the series resistance is zero but will reduce the fill factor and very high series resistance will reduce I_{SC}.
The main cause of power loss due to shunt resistance is because of manufacturing defects.
A solar cell with a low shunt resistance produces lower power since current generated by light has an alternative path to flow.

The IV curves of the fabricated solar cells are presented below:

Figure 6-2 shows dark and light current curves of cell 3957E- batch1. Looking at the dark curve in linear scale at higher currents one observes that there is a deviation from an ideal diode IV curve which shows a series resistance. So, probably the metal- semiconductor contact is not ohmic and there is a high resistance.

In light curve in log scale, the minimum point of the curve shows V_{OC} which is 0.25 V and the intersection of the light curve with current axis shows I_{SC} which is 0.19 mA. The fill factor of the cell is also 37.

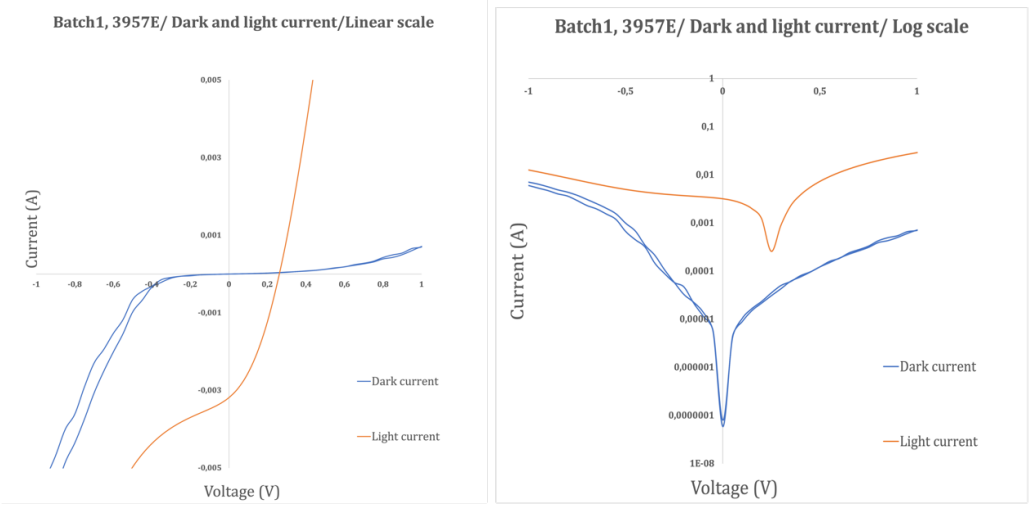


Figure 6-2: Dark and light current curves of cell 3957E- batch 1, in linear and logarithmic scale.

Figure 6-3 shows dark and light current curve of cell 3957T, batch 1. The value of fill factor (FF) extracted from light curve is zero which means the cell does not function at all.

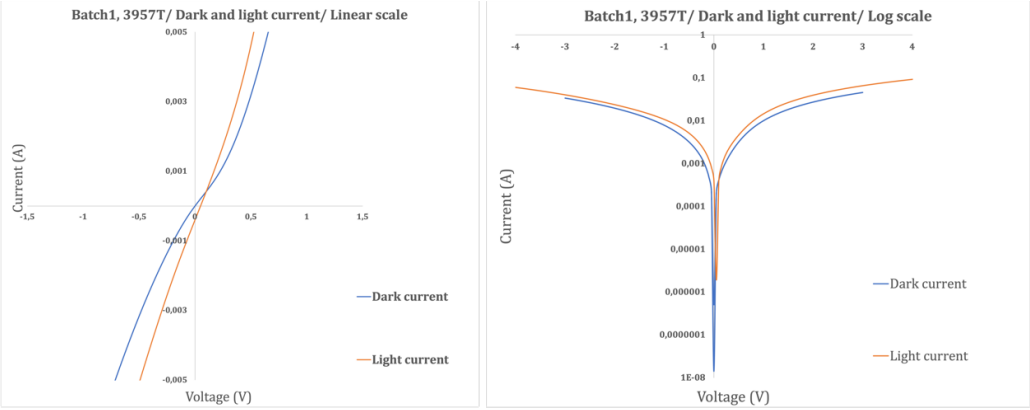


Figure 6-3: Dark and light current curves of cell 3957T- batch 1, in linear and logarithmic scale.

Figure 6-4 shows dark and light current curves of cell 3963F-batch1. Dark current curve in linear scale looks like an ideal diode, so the pn-junction probably works well.
Light curve in log scale shows value of V_{OC} and I_{SC} which are 0.35 V and 3.68 mA, respectively and fill factor value is 37.

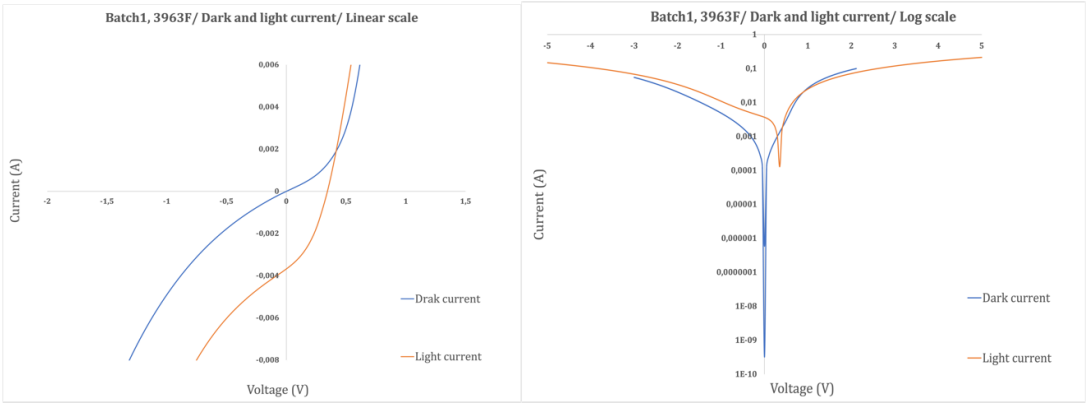


Figure 6-4: Dark and light current curves of cell 3963F- batch 1, in linear and logarithmic scale.

Figure 6-5 shows dark and light curves of cell 4001S, batch1. The dark curves look like an IV curve of a diode which shows that pn-junction works well. Looking at the light curves in both linear and log scale shows value of V_{OC} is 0.20 V and I_{SC} value is 1.41 mA. The fill factor of this cell is 27 which is lower than that of the cells 3957E and 3693F.

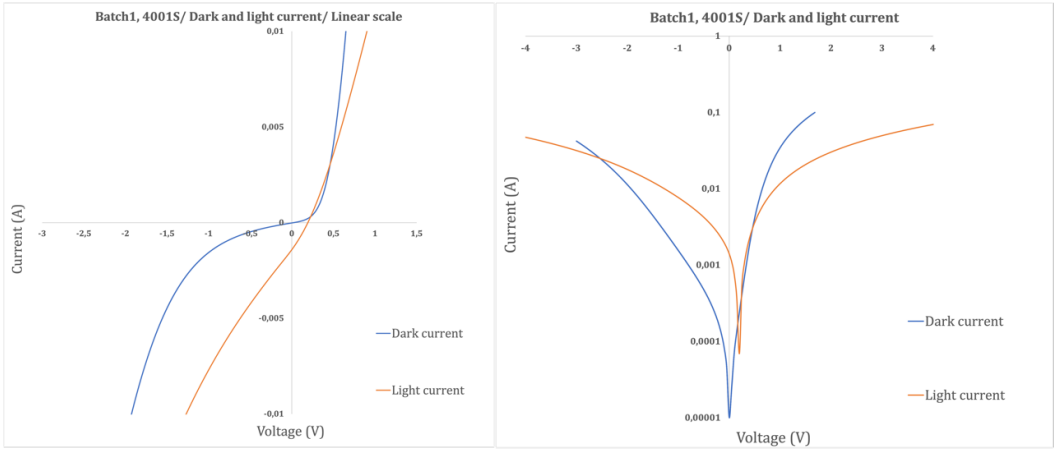


Figure 6-5: Dark and light current curves of cell 4001S- batch1, in linear and logarithmic scale.

As it was mentioned before, intersection of the light current curve with x-axis and y-axis shows V_{oc} and I_{SC}, respectively, which can be recognized in light current curves of devices.
Information obtained from light current curves for batch 1 solar cells is shown in Table 6.3.

Device	Efficiency (%)	V_{OC}(V)	I_{SC}(mA)	FF (%)
3957E	0.29	0.25	0.19	37
3957T	0.0001	0.05	0.40	0
3963F	0.48	0.35	3.68	37
4001S	0.07	0.20	1.41	27

Table 6.3: Information deducted from light current curves of batch1 solar cells.

The highest fill factor between batch 1 solar cells belong to device 3957E and 3963F and device 3957T does not operate and the efficiency and fill factor are extremely low.

Batch 2 solar cells are investigated as well and dark and light current curves of cell 2- cell 8 (cell 1 broke in previous step) in linear and log scale are presented below.

Figure 6-6 shows dark and light curve of cell2, batch 2. The dark curve in linear scale shows a deviation in high current which means a series resistance. Probably the metal-semiconductor junction is not ohmic junction with low resistance.

Light curves in both scales shows values of V_{oc} and I_{SC} , 0.69 V and 4.25 mA, respectively.

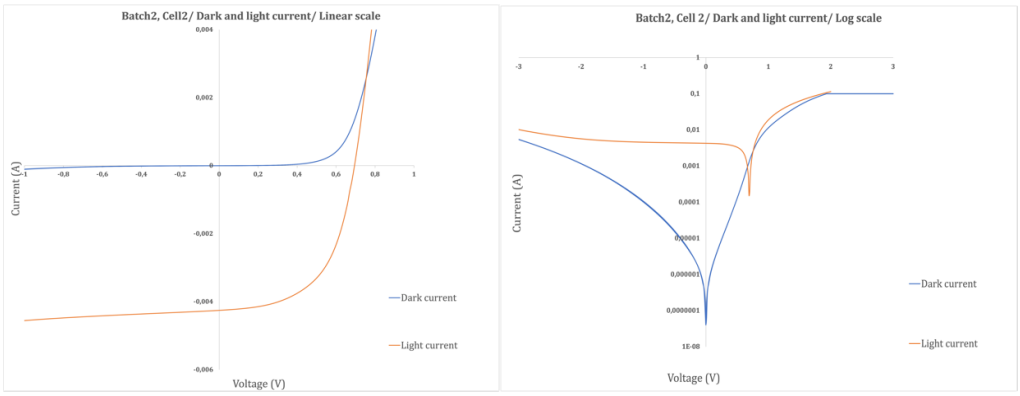


Figure 6-6: Dark and light current curves of cell2- batch2, in linear and logarithmic scale.

Figure 6-7 shows dark and light curve of cell3, batch 2. Deviation in high current and hump in low currents in dark curve indicates series and shunt resistance. Therefore, pn-junction is not working like an ideal diode.
Light curve shows values of 0.8 V and 3.85 mA values for V_{oc} and I_{SC}, respectively.

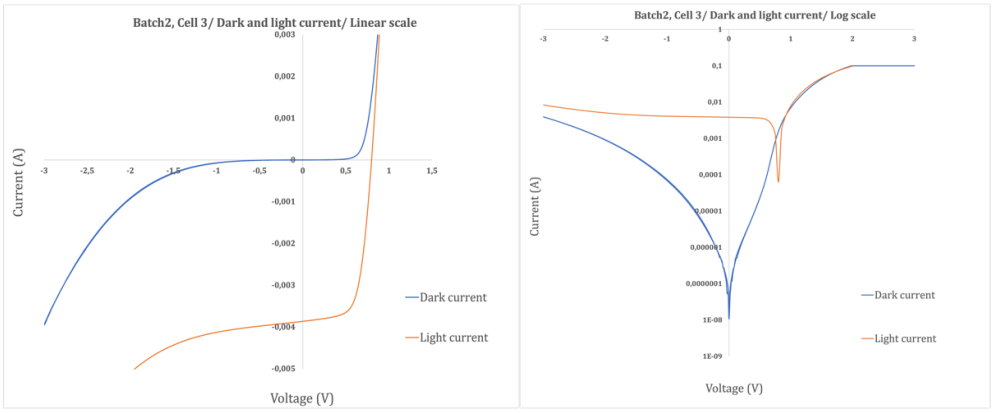


Figure 6-7: Dark and light current curves of cell3- batch2, in linear and logarithmic scale.

Figure 6-8 shows dark and light curve of cell 4, batch 2. The same as cell 3, dark curve shows a shunt and series resistance. So, pn-junction does not operate as an ideal diode because there is a series and parallel series with it.
Light curve shows values of o.67 V and 2.56 mA for V_{oc} and I_{SC}, respectively.

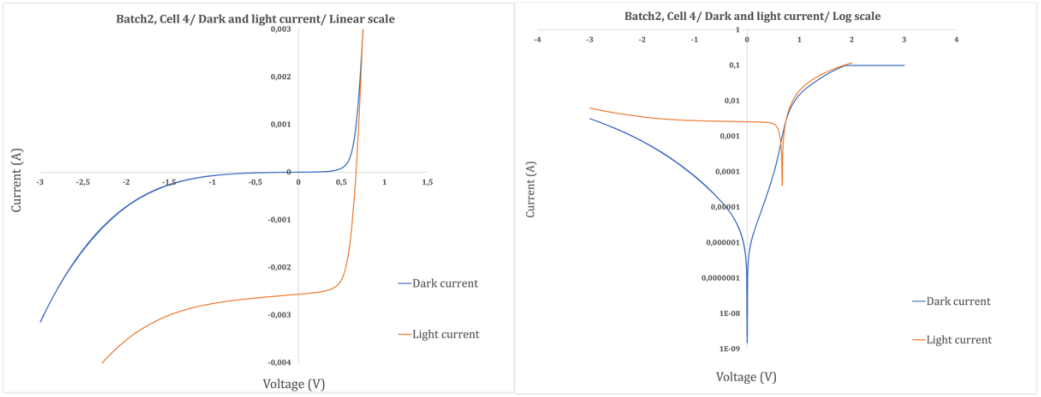


Figure 6-8: **Dark and light current curves of cell4- batch2, in linear and logarithmic scale.**

The dark current curve of cell 5 shows an exponential increase of current by increasing the voltage like an ideal diode which means the pn-junction works properly as Figure 6-9 shows.
Light curve shows values of o.61 V and 2.35 mA for V_{oc} and I_{SC}, respectively.

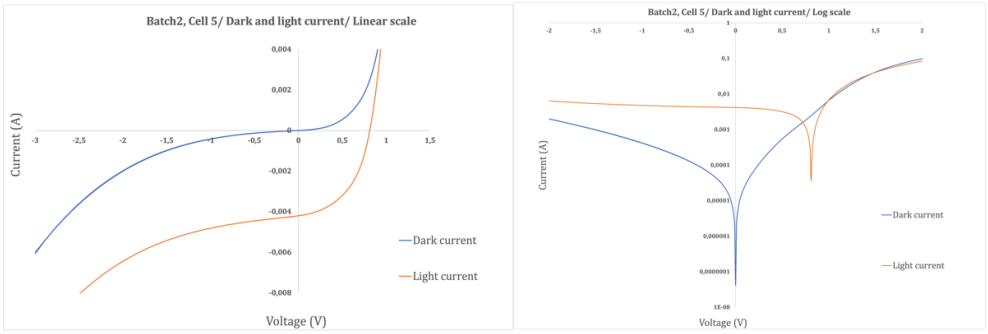


Figure 6-9: **Dark and light current curves of cell5- batch2, in linear and logarithmic scale.**

Figure 6-10 shows dark and light curve of cell6, batch 2. A dark curve shows a slight hump in lower current which indicates a low shunt resistance. Light curves show values of 0.20 V and 3.35 mA for V_{oc} and I_{SC}, respectively.

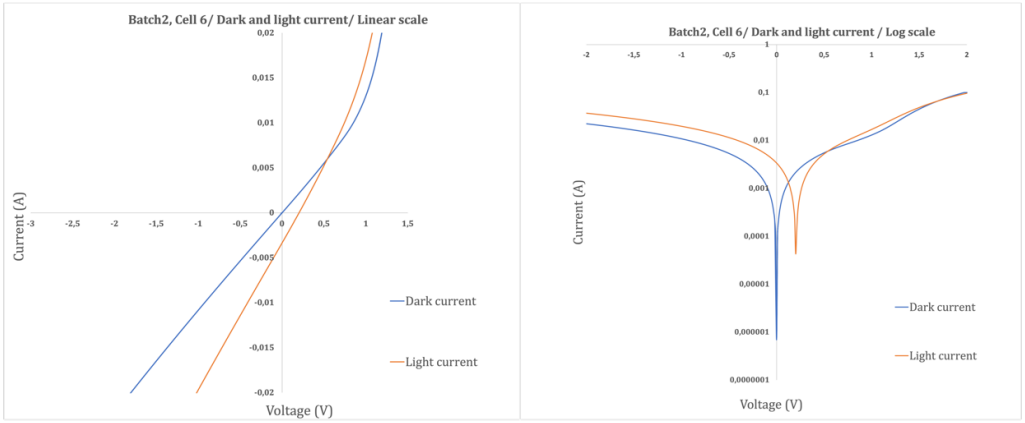


Figure 6-10: **Dark and light current curves of cell6- batch2, in linear and logarithmic scale.**

Figure 6-11 shows dark and light curve of cell7, batch 2. Deviation in high current and a hump in low current of dark curve shows a series and shunt resistance with a pn-junction (diode).
Values of 0.55 V and 2.91 mA can be deducted from light curves for V_{oc} and I_{SC}, respectively.

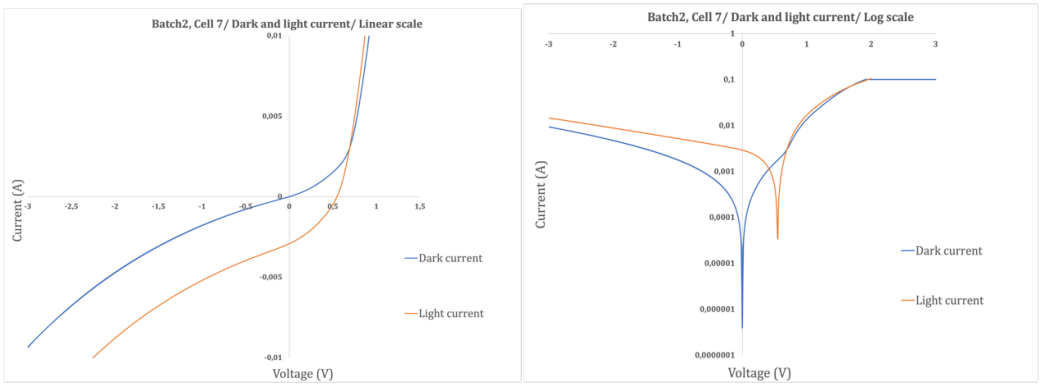


Figure 6-11: **Dark and light current curves of cell7- batch2, in linear and logarithmic scale.**

Figure 6-12 shows the dark and light curve of cell 8, batch 2. The same as cell 7, dark curve shows a series and a low shunt resistance with a pn-junction (diode).
Values of 0.49 V and 2.43 mA can be deducted from light curves for V_{oc} and I_{SC}, respectively.

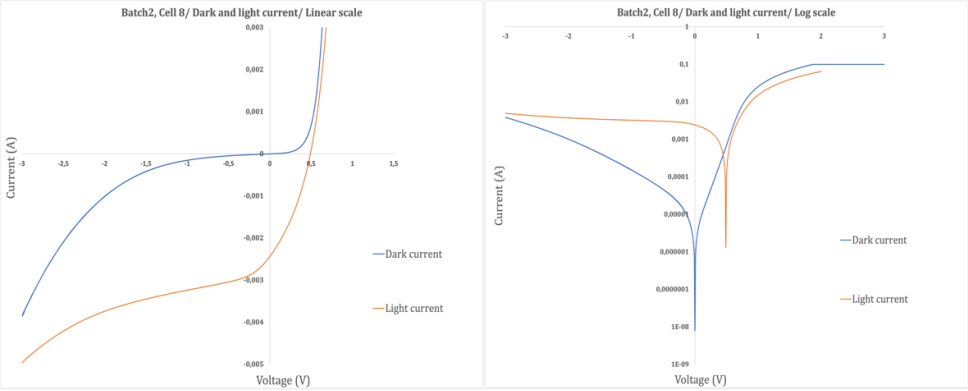


Figure 6-12: Dark and light current curves of cell8- batch2, in linear and logarithmic scale.

By looking at information obtained from light current curves of cells in batch 2, in Table 6.4, cell 3 and cell 4 have the highest FF value and also highest efficiencies.

Device	Efficiency (%)	V_{OC}(V)	I_{SC}(mA)	FF (%)
Cell 2	1.64	0.69	4.25	56
Cell 3	2	0.80	3.86	65
Cell 4	1.13	0.67	2.56	66
Cell 5	0.29	0.61	2.39	20
Cell 6	0.17	0.20	3.35	26
Cell 7	0.55	0.55	2.91	34
Cell 8	0.4	0.49	2.43	34

Table 6.4: Information obtained from light curve of batch2 solar cells.

It would be easier to compare the functionality of the pn-junction of batch 2 cells with one another by looking at Figure 6-13.
Cell 3 and cell 4 show series resistance and a high shunt resistance and dark IV curve of cell 2 and cell 8 have deviation in low current indicating shunt resistance. Cell 5, cell 6 and cell 7 behave like a diode however cell 7 has a small shunt resistance.

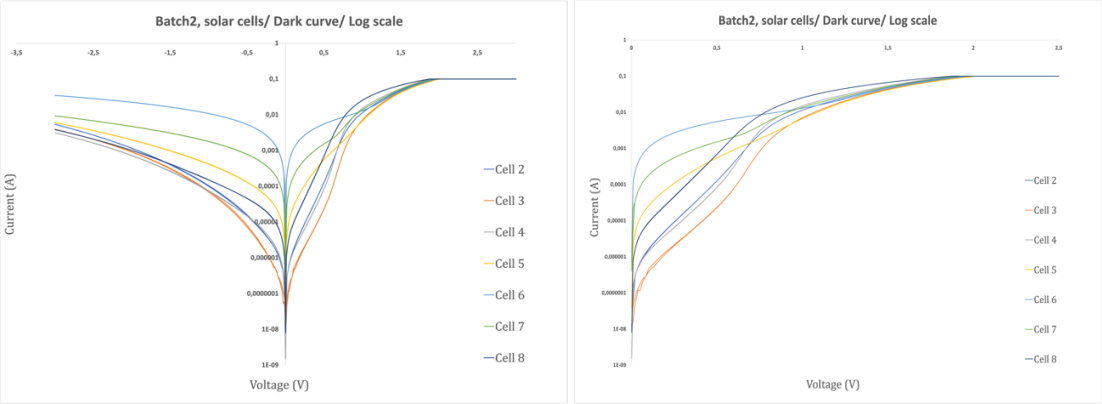


Figure 6-13: Dark curves of batch2 solar cells in logarithmic scale.

Figure 6-14 represents light curve of all fabricated solar cells in batch 2. Since the power of fabricated solar cell is $P = I_{SC} \times V_{OC}$, open circuit voltage and short circuit current values of cells will be observed. In Figure 6-14, light current curve of cell5 shows the highest V_{OC} (the far right), but Table 6-4 shows V_{OC} value for cell5 is 0.61V which is not the highest value. Moreover, I_{SC} value for cell 5 is the lowest according to Table 6-4.

In Figure 6-14, cell3 has the second highest V_{OC} whereas, Table 6.4 shows the highest V_{OC} value for cell3 that is 0.80 V and also the I_{SC} value for cell 3 is the second highest according to Table 6-4.

Table 6-4 also shows the efficiency of cell3 is 2% which is the highest efficiency among other cells.

On the other hand, looking at light curves in Figure 6-14, one can see cell6 has the lowest V_{OC} compared to other cells (the far left). Table 6-4 also confirms that the lowest V_{OC} value belong to cell6 which is 0.20 V.

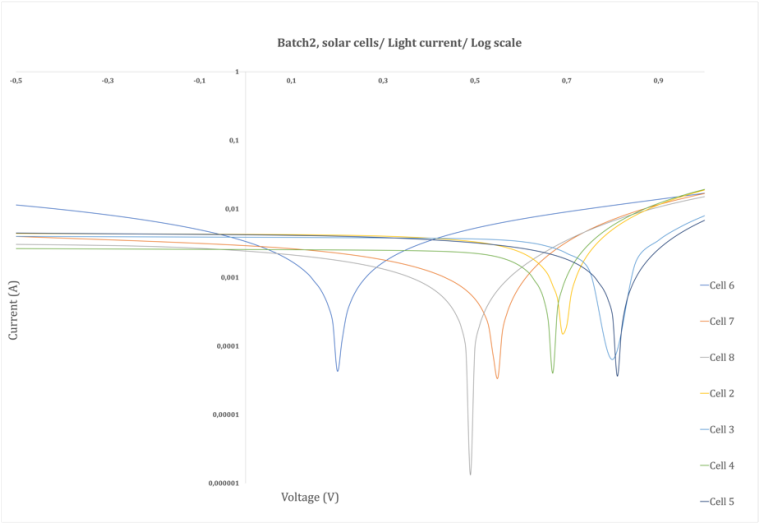


Figure 6-14: Light curves of batch2 solar cells in logarithmic scale.

Table 6.5 shows power values of batch2 solar cells. The highest and lowest electrical power values are 3.1 mW and 0.7 mW corresponding to cell 3 and cell 6, respectively.

Device	Power [mW]
Cell 2	2.9
Cell 3	3.1
Cell 4	1.7
Cell 5	1.5
Cell 6	0.7
Cell 7	1.6
Cell 8	1.2

Table 6.5: Power value for batch2 solar cells.

7 Conclusions and future work

In this thesis fabrication and characterization of $GaAs_xP_{1-x}$ single junction solar cell on GaAs/Si are presented. Firstly, crystalline quality of some samples was investigated via optical microscope and HRXRD to find the optimized growth conditions of $GaAs_xP_{1-x}$ epitaxial layer in HPVE. Then the fabrication process has been done on chosen samples and at the end device characterizations such as TLM and IV measurement have been done to see the performance of the devices.
The crystalline quality of the samples improved during the optimization process and the number of pits decreased. Using metal organic vapor phase epitaxy (MOVPE) to grow GaAs layer on Si substrate and also using chemical mechanical polishing (CMP) on thickened GaAs on off-axis Si substrate before growing $GaAs_xP_{1-x}$ layer improves the crystalline quality of samples.
During the fabrication process, for batch 2 solar cells some changes have been done in recipes such as baking time after spin coating or cleaning the sample after III-V dry etching by nitric acid, target etching depth in III-V dry etching etc. and the results showed improvement in solar cell performance.
Therefore, one can conclude device results improved because of improving the material by changing the growth conditions as well as improving the fabrication process by changing a few recipes as mentioned above.
The work in this thesis can be continued in future and there are still some features that need to be changed to improve solar cell operation. For instance, in growing $GaAs_xP_{1-x}$ layer, a thicker back surface filed (BSF) could improve the device functionality. Since we expect GaAs seed to have defect, a thicker BSF can prevent minority carriers reaching to GaAs seed to avoid recombination. In addition, a thin p-doped GaP window layer can be integrated on top surface of the emitter. The purpose of this window layer is a high bandgap material that can reduce the number of surface states to avoid recombination and the window layer should be transparent to let light through the rest of the solar cell.

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