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A Low-Distortion Current-Mode Signal Generator for Wide-Range Bioimpedance Spectroscopy

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Abstract—This paper presents a low-distortion current-mode sinusoidal signal generator for bioimpedance spectroscopy measurements. The proposed full current-mode operation enables linearity enhancement and potential savings in silicon area and power consumption. Programmability in the low-pass filter and current driver enables impedance measurements from 0.2 Ω to 10 kΩ over a wide frequency range from 1 kHz to 1 MHz. The current generator, designed in a 0.18 μm CMOS process, consumes between 736 μW at the lowest frequency and gain, and 1.70 mW at the highest frequency and gain, and occupies 1.76 mm² silicon area. Post-layout simulation results show a spurious-free dynamic range larger than 40 dBc over the entire frequency range, which enables bioimpedance measurements with errors below 1%, as it is required for wearable devices evaluating neuromuscular disorders.

Index Terms—bioimpedance spectroscopy, sinusoidal signal generator, current-mode, programmable gain, programmable low-pass filter, low-distortion.

I. INTRODUCTION

Bioimpedance spectroscopy (BIS) has received significant attention in biomedical contexts due to its means of providing low-cost and valuable physiological information in a wide range of clinical and point-of-care applications. For instance, BIS has been used in Electrical Impedance Tomography [1], as an evaluation tool for neuromuscular disorders [2], [3], detection of cancerous tissue [4], [5], and body composition analysis [6], [7]. In most of these applications, the impedance is measured by injecting a small amplitude sinusoidal current [8] in the kHz to MHz frequency range, and sensing changes of the bioimpedance through the voltage response from tissues. The bioimpedance of human tissues has typical baseline values from a few Ω up to several kΩ, which may dynamically change by a few mΩ over time due to physiological processes [9]. Consequently, bioimpedance spectroscopy systems require programmable sinusoidal signal generators (SSGs) which can cover a wide range of frequencies and output currents. Moreover, the aforementioned applications also impose accurate impedance measurements (typically, errors below 1%), which can only be achieved by minimizing the SSG’s distortions [10].

State-of-the-art low-distortion SSGs for bioimpedance spectroscopy and single-frequency bioimpedance generally comprise waveform generation, linearity enhancement, and current injection stages [10]. For instance, in [11]–[15], sinusoids are generated by using a digital-to-analog converter (DAC) and a digital control. These waveforms are known as DAC-based sinusoids [10], and have better distortion performance compared to square waves, thus relaxing requirements for the linearity enhancement stage. In [11], [13], resistive DACs (RDACs), which are limited in resolution and require power hungry buffering stages, are employed. In [14], [15], capacitive DACs (CDACs) are used to improve power efficiency and resolution. However, for high frequency operation, CDACs require a power hungry voltage buffer to drive the RC filters in the following stage. In [15], a Gm-C filter is used to circumvent the voltage buffer issue, but the SSG still requires a power hungry (relative to the rest of the system) V/I conversion stage to drive the bioimpedance with low distortion. Current steering DACs (IDACs) have been widely used in SSG generators [12], [16]–[18], due to their area efficiency, potential high resolution, high speed, and ability to drive resistive loads. However, most of the linearity enhancement circuits work in voltage domain, thus the IDAC needs to drive directly the bioimpedance, degrading the distortion performance.

To address the aforementioned challenges, this paper proposes a full current-mode SSG, employing IDAC-based sinusoidal waveform generation, and signal conditioning in current domain. The benefits of this approach are twofold: (i) we make use of the IDAC advantages while avoiding conversion of the IDAC waveform to voltage domain through a transimpedance amplifier. The IDAC is able to directly drive any linearity enhancement circuit, thus improving distortion performance and potentially saving area and power. (ii) operating the SSG in current domain allows the use of current amplifiers, which can operate at higher speeds, and have better linearity and dynamic range than their voltage domain counterparts [19]–[21]. This paper is organized as follows: Section II presents the proposed architecture of the current signal generator. Section III describes the circuit implementation of the key building blocks and Section IV shows post-layout simulation results. Finally, Section V concludes the paper.

II. PROPOSED CURRENT SIGNAL GENERATOR

The proposed current signal generator should enable evaluating neuromuscular disorders [2], [3] by measuring bioimpedances from 1 Ω to 10 kΩ in the 1 kHz–1 MHz frequency range, with maximum impedance errors of 1%. To fulfill these requirements, the SSG should achieve a spurious free dynamic range (SFDR) larger than 40 dBc.

A. Signal Generation Analysis

In a DAC-based SSG, the signal at the output of the DAC has unwanted harmonics caused by sampling and nonlin-
earities in the waveform generation [22]. These harmonics are attenuated by the linearity enhancement stage, typically implemented with a low-pass filter (LPF).

The harmonic distortions due to sampling are at $kf_s \pm f_{SG}$, where $k$ is an integer, $f_s$ is the sampling frequency, and $f_{SG}$ is the frequency of the SSG output signal [10]. The magnitude of these harmonics is given by [22]:

$$|H_{Sinc}(f)| = \frac{\sin(\pi f / f_s)}{\pi f / f_s}$$  \hspace{1cm} (1)

which shows that the dominant harmonic is at OSR$\cdot f_{SG}$, where OSR = $f_s / f_{SG}$ is the oversampling ratio. This tone determines the SFDR and has the highest influence on the total harmonic distortion (THD). It can also be noticed that increasing the OSR moves the dominant harmonic towards higher frequencies. Consequently, the order of the required LPF can be reduced and its cutoff frequency, $f_c$, can be chosen to fulfill the distortion requirements.

The DAC’s signal-to-noise ratio (SNR) is given by [22]:

$$\text{SNR[dB]} = 1.76 + 6.02N_{DAC} + 10\log(\text{OSR})$$  \hspace{1cm} (2)

where $N_{DAC}$ is the DAC resolution in bits. It can be seen that increasing the OSR and $N_{DAC}$ results in higher SNR, thus extended range of bioimpedances that can be measured.

Considering that the maximum frequency of interest for the BIS application is 1 MHz, an OSR of 64 is chosen. A larger OSR implies higher power consumption and design complexity. An appropriate approach to achieve the desired impedance range and accuracy is to trade OSR for $N_{DAC}$, and then choose the filter order and cutoff frequency for mitigating distortions. By choosing OSR = 64 and $N_{DAC} = 6$, an SFD $= 20\log(H_{Sinc}(f_{SG})/H_{Sinc}(63f_{SG})) = 36$ dBc and an SNR $= 55.94$ dB can be achieved, theoretically. Therefore, a 3rd order LPF with a cutoff frequency at $2f_{SG}$ is sufficient to reduce distortions up to the 63rd harmonic ($f_s - f_{SG}$) and to fulfill the application requirements with some margin.

B. Proposed Architecture

The block diagram of the proposed current-mode signal generator is shown in Fig. 1. The SSG consists of the following stages: (i) waveform generation, comprising a clock divider, a DAC control and a 6-bit thermometer-encoded IDAC, (ii) linearity enhancement, comprising a tunable current-mode 3rd order LPF, and (iii) current injection, comprising a current driver with variable gain. The clock divider generates 11 logarithmically spaced frequencies in the 62.5 kHz–64 MHz frequency range, from a 128 MHz clock reference. A 16:1 multiplexer selects the desired clock frequency, $f_{DAC}$, to run the DAC control. Therefore, the SSG frequency, given by $f_{SG} = f_{DAC} / 64$, can be tuned from 1 kHz to 1 MHz. The phase accumulator block uses a 6-bit counter to accumulate up to 64 cycles of the DAC control clock, thus effectively dividing a period of the DAC-based sinusoid into 64 phase values. The value of the 6-bit counter is then transferred to the amplitude mapping block. This counter is used to search in a look-up table (LUT) for the 6-bit binary equivalent DAC input, which maps the sinusoidal waveform to the corresponding phase value. Then, the determined LUT value is thermometer-encoded and shuffled by a butterfly network of the dynamic element matching (DEM) block for improving the DAC’s linearity. The clock divider and DAC control circuits and layout were implemented by synthesizing their respective register transfer level (RTL) code using a standard digital flow, and are not covered in the following section. The 6-bit thermometer-encoded IDAC consists of 64 complementary unit current sources, thus generating positive and negative rectified DAC-based sinusoidal current waveforms. These waveforms are chopped with a clock at $2f_{SG}$ (from the clock divider) to generate a differential waveform. The 3rd order current-mode LPF, with a tunable cutoff frequency over the entire frequency range, removes the spurs from the differential DAC-based sinusoid. The current driver amplifies the differential filtered current signal with a variable gain from 0 dB to 40 dB.

III. CIRCUIT IMPLEMENTATION

A. Current-Steering DAC

The 6-bit thermometer IDAC is shown in Fig. 2. Only a single side of the complementary IDAC is shown for simplicity. Each unit current source supplies 125 nA when is turned on, thus, at peak amplitude, each side of the IDAC supplies a total current of 8 $\mu$A. The unit current sources are implemented with cascodes to improve linearity. To enhance speed, the PMOS and NMOS unit current sources are steered to ground or supply, respectively, when they are not applying current for waveform generation (See green traces in Fig. 2). A complementary wide-swing cascode current mirror applies the sum of unit current sources to the following stage (See red traces in Fig. 2), thus overcoming the limited voltage swing of the unit current sources and decoupling them from the common-mode feedback (CMFB) of the LPF. The wide-swing cascode current mirror attenuates the amplitude of the DAC-based sinusoid to 2 $\mu$A, to relax the linearity requirements and power consumption of the following LPF.

B. Programmable Current-Mode Low-Pass Filter

Fig. 3 shows the current-mode LPF block diagram. The 3rd order Butterworth filter has been implemented with a GaN-C topology, with identical $G_m$-C topology. Double output $G_m$ cells decouple the filter’s feedback and feedforward paths, and simplifies the design of the CMFB circuits. To fulfill the required
distortion performance, the LPF should suppress harmonics over the entire frequency range. Therefore, a widely tunable cutoff frequency, given by $f_c = 2f_{SG}$ (2 kHz–2 MHz), has been chosen, to enable rejection of the 3rd harmonic by 8.5 dB, and the 63rd harmonic by 85 dB, sufficient to fulfill the SFDR requirements. Nonetheless, this introduces a constant phase shift of $-59.22^\circ$ across the supported frequency range, which can be corrected by software. The tunable cutoff frequency, $f_c$, is realized with programmable $C_1-C_3$ and $G_m$ cells. The programmable capacitors are implemented with a 7-bit binary weighted matrix with 250 fF unit capacitances. Moreover, a switch-controlled capacitor divider (100 fF unit capacitance) with biasing pseudoresistors is placed at the input of each $G_m$ cell, as it is shown in Fig. 3, to linearize the cells and extend the tunability of $f_c$ by a factor $k_{div} = 11$, towards the lower end of the frequency range.

The programmable $G_m$ cell, shown in Fig. 4, consists of a $G_m$ core and 3-bit binary-weighted programmable current mirrors. The $G_m$ core, inspired from [25], is based on a flipped voltage follower (FVF) with a common-gate gain stage and degeneration resistor. This architecture improves linearity and robustness to PVT variations due to a higher loop gain as compared to traditional FVF [26] and super source follower [11] topologies. The current flowing through the degeneration resistor, $R_{DEG}$, is attenuated by the programmable current mirrors to adjust the effective $G_m$. The $G_m$ tuning range is determined by the programmable current mirror aspect ratios as:

$$G_{m,max} = \frac{1}{\sum_{i=0}^{3} \left( \frac{W_i}{L_i} \right)_{mirror}}$$

where $i$ represents the branch number in the programmable current mirror. $i=0$ represents the default branch, which is not controlled by switches, and $i=1,2,3$ represent the branches controlled by $b_0, b_1, b_2$. Therefore, the $G_m$ tuning range is $G_{m,max}/G_{m,min}=4.5$. The total cutoff frequency tuning range is given by $f_{c,max}/f_{c,min}=2^{i_{div}}(G_{m,max}/G_{m,min})=6336$.

C. Current Driver

The current driver, shown in Fig. 5, is based on a two-stage current amplifier with current feedback, inspired from [21]. In our design, the linearity is enhanced by using cascode current mirrors in the first and feedback stage, and wide-swing cascode current mirrors in the output stage. Moreover, to cover the required bioimpedance range, programmable current mirrors were employed in the output stage, which enable variable gain. Therefore, the gain can vary in three steps: 0 dB, 20 dB, and 40 dB, and its controlled by $b_0, b_1, b_2$, as shown in Fig. 5, each bit controlling a single gain step. The current feedback reduces the input impedance, increases bandwidth, and minimizes the effects of PVT variations on the amplifying current mirrors. The combination of programmable gain, wide voltage swing compliance and high output resistance enables bioimpedance measurements from 0.2 $\Omega$ up to 10 k$\Omega$.

IV. POST-LAYOUT SIMULATIONS RESULTS

The layout of the current signal generator is shown in Fig. 6. It has been implemented in a 180 nm CMOS process, occupies an area of 1.76 mm$^2$, and it is intended to be embedded into a fully-integrated bioimpedance spectrometer. Post-layout simulations show that the power consumption depends on the output signal frequency and current driver gain, and it varies from 0.736 mW to 1.70 mW, when powered from a 1.8 V supply. Fig. 7 shows the transient waveforms of the IDAC and SSG outputs and their respective spectrum for $f_{SG}=1$ kHz and $f_{SG}=1$ MHz at maximum amplitude. The spectra were computed for 16384 FFT bins with a sampling frequency of 256$f_{SG}$. It can be seen that at $f_{SG}=1$ kHz, the 63rd harmonic is fully attenuated and only the low harmonics ($3^{rd}$, $5^{th}$ and $7^{th}$), caused by IDAC nonlinearities, limit the overall distortion performance to 51.43 dBc. At $f_{SG}=1$ MHz, the harmonics
TABLE I: Comparison with state-of-the-art SSGs.

<table>
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<tbody>
<tr>
<td>[11]</td>
<td>180</td>
<td>1.8</td>
<td>976–2 M</td>
<td>2</td>
<td>1652</td>
<td>0.13–10</td>
<td>&gt;40</td>
<td>&lt;0.7</td>
<td>0.75 m</td>
<td>1.62</td>
</tr>
<tr>
<td>[13]</td>
<td>180</td>
<td>1.8</td>
<td>1 k–2 M</td>
<td>3</td>
<td>16</td>
<td>(140 mV–720 mV)³</td>
<td>&gt;47</td>
<td>&lt;0.7</td>
<td>5.1 m</td>
<td>0.72</td>
</tr>
<tr>
<td>[14]</td>
<td>130</td>
<td>1</td>
<td>15 k–125 k</td>
<td>8</td>
<td>N.R.</td>
<td>20–200</td>
<td>&gt;58</td>
<td>N.R.</td>
<td>1.08 m</td>
<td>N.R.</td>
</tr>
<tr>
<td>[15]</td>
<td>65</td>
<td>0.5</td>
<td>20 k</td>
<td>6</td>
<td>64</td>
<td>2</td>
<td>44.6 0.66</td>
<td>4.62 µ µ</td>
<td>N.R.</td>
<td>3.0 m</td>
</tr>
<tr>
<td>[24]</td>
<td>65</td>
<td>0.5</td>
<td>20 k</td>
<td>6</td>
<td>64</td>
<td>2</td>
<td>44.6 0.66</td>
<td>4.62 µ µ</td>
<td>N.R.</td>
<td>3.0 m</td>
</tr>
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</table>

a Only post-layout simulations  
b Voltage output, i.e. SSG excludes current driver  
c Multi-frequency sigma-delta modulator SSG with recursive signal oscillator  
d Single-frequency SSG

![SG Layout](image)

*Fig. 6: SSG Layout*

caused by IDAC nonlinearity dominate over sampling distortions. Additionally, at high frequencies, the low biasing current of Gm cells cause also nonlinearity that further degrade the overall SFDR to 40.24 dBc, as compared to fSG=1 kHz. Monte Carlo simulations (see Fig. 8), performed for 100 runs, computed only from 1024 FFT bins at fSG=1 kHz and fSG=1 MHz, demonstrate the robustness of the proposed solution against PVT variations. Table I summarizes the proposed SSG performance and comparison with state-of-the-art SSGs. It can be seen that our solution achieves similar distortion performance and power consumption as compared to other solutions targeting wide-frequency range bioimpedance spectroscopy.

V. CONCLUSIONS

A full current-mode SSG for bioimpedance spectroscopy measurements was presented. Accurate measurements with errors below 1%, over a wide frequency range of 1 kHz - 1 MHz, and wide bioimpedance range of 0.2 Ω - 10 kΩ corresponding to a 2–200 µA injected current, are achieved by employing current-mode operation and programmability. Post-layout simulations show low-distortion performance, while dynamically consuming between 736 µW and 1.70 mW from 1.8 V supply and occupying 1.76 mm² silicon area. These key characteristics make the proposed SSG a potential candidate for wearable applications targeting muscle monitoring and diagnosis of neuromuscular disorders.

REFERENCES
