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Analogue Circuit for Detection of Ageing Phenomena in Electric Drives

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Abstract

This master thesis presents an analogue peak holder circuit design aimed at facilitating the non-invasive inspection of the ageing process in electric drives. The ageing process of electric drives is a crucial aspect that demands accurate monitoring to ensure their long-term performance and reliability.

The proposed peak holder circuit is specifically designed to detect fast and narrow-width pulses of ringing current present in the PWM drive current. By capturing and measuring the peak values of these pulses, the circuit provides valuable insights into the ageing characteristics of electric drives.

Experimental results demonstrate the remarkable efficiency of the peak holder circuit in accurately detecting and quantifying the peak values of the ringing current pulses. The circuit exhibits a stable output swing within a specified effective input swing range, with low mean-squared error (MSE) values. This signifies a strong linear correlation between the input and output signals, enhancing the reliability of the ageing detection process.

The ability of the peak holder circuit to effectively detect and analyze the ageing process of electric drives offers numerous advantages. By focusing on peak detection, which captures the highest values of the ringing current, the circuit provides a more efficient and targeted approach to inspecting the ageing process. This enables engineers and maintenance personnel to gain crucial insights into the degradation and performance of electric drives, allowing for timely interventions and proactive maintenance.

Keywords

Electric Drives, Ageing Process, Pulse-Width Modulation, Ringing Current, Peak Holder, Analogue Circuits
Sammanfattning

Detta examensarbete presenterar en nyutvecklad kretslösning för toppvärdesdetektering hos elektriska drivsystem, med målet att underlätta icke-invasiv övervakning av åldrandesprocessen hos eld drivsystem. Åldrandet hos eld drivsystem är en avgörande faktor som kräver noggrann övervakning för att säkerställa deras långsiktiga prestanda och tillförlitlighet.

Den föreslagna kretsen för att detektera toppvärdena är specifikt utformad för att detektera snabba och kortvariga ringningar i PWM-modulerade strömmar. Genom att mäta toppvärdena ger kretsen värdefull information om åldrandekarakteren hos eld drivsystemen.


Krestsens förmåga att effektivt detektera och analysera åldrandeprocessen hos eld drivsystem erbjuder flera fördelar. Genom att fokusera på toppvärdesdetektering, som fångar de högsta värdena av ringströmmen, ger kretsen ett mer effektivt och riktat tillvägagångssätt för att inspektera åldrantedet. Det möjliggör för ingenjörer och underhållspersonal att få viktig information om nedbrytning och prestanda hos eld drivsystem, vilket möjliggör tidiga insatser och proaktivt underhåll.

Nyckelord

Elektriska drivsystem, Åldringsprocess, Pulsbreddsmodulering, Ringningar i strömmen, Toppvärdesdetektor, Analog krets
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Stockholm, November 2023
Yudong Lin
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<td>AC</td>
<td>alternating current</td>
</tr>
<tr>
<td>ADS</td>
<td>Advanced Design System</td>
</tr>
<tr>
<td>BJT</td>
<td>bipolar junction transistor</td>
</tr>
<tr>
<td>CMOS</td>
<td>complementary metal-oxide-semiconductor</td>
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<tr>
<td>DC</td>
<td>direct current</td>
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<tr>
<td>EMI</td>
<td>electromagnetic interference</td>
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<tr>
<td>ESR</td>
<td>equivalent series resistance</td>
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<tr>
<td>FE</td>
<td>finite element</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field-programmable gate array</td>
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<tr>
<td>IC</td>
<td>integrated circuit</td>
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<tr>
<td>IM</td>
<td>induction motor</td>
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<tr>
<td>ITSC</td>
<td>inter-turn short circuit</td>
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<tr>
<td>MSE</td>
<td>mean-squared error</td>
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<tr>
<td>op-amp</td>
<td>operational amplifier</td>
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<tr>
<td>PCB</td>
<td>printed circuit board</td>
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<tr>
<td>PWM</td>
<td>pulse-width modulation</td>
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<tr>
<td>RSH</td>
<td>rotor slot harmonics</td>
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<tr>
<td>SRF</td>
<td>high self-resonant frequency</td>
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<tr>
<td>VHDL</td>
<td>Very High-Speed Integrated Circuit Hardware Description Language</td>
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Introduction

The ageing process of electric drives is a critical aspect that significantly impacts industrial systems’ reliability, performance, and safety. Detecting and monitoring the ageing process of electric drives is essential for ensuring optimal operation, predicting failures, and implementing timely maintenance strategies. By understanding the ageing characteristics, it becomes possible to take proactive measures and prevent unexpected downtime or costly repairs.

In recent years, extensive research has been conducted to develop effective methods for detecting and assessing the ageing process of electric drives. These researches aim to identify key indicators or parameters that correlate with the ageing phenomena and provide valuable insights into the health and condition of the drive system. By accurately monitoring these indicators, it becomes possible to estimate the remaining useful life, identify potential faults, and implement condition-based maintenance strategies.

In this thesis, we will examine a possible design and way of implementation of ageing process detection for electric drives. We will mainly focus on evaluating the peak value of ringing current caused by the pulse-width modulation (PWM) drive voltage.

1.1 Background

Electric drives play a crucial role in various industries, providing power to critical machinery and systems. Ensuring their reliable operation is vital to avoid costly breakdowns, downtime, and potential hazards. Among the factors that can compromise motor performance, faults in motor insulation present a significant challenge. The advent of the Industry 4.0 initiative has prompted the reevaluation of electric drives’ roles and functionalities, challenging
traditional hierarchical communication architectures. Consequently, the development of condition monitoring techniques for early fault detection and preventive maintenance has become crucial.

Stator winding insulation faults are a prevalent cause of failures, necessitating the development of fault detection techniques that are independent of operating conditions. Traditionally, detecting insulation faults in electric motors has relied on invasive techniques involving physical contact with motor windings or the use of external monitoring systems. Previous literature discussed the different behavior of electric drives by observing the high overshoot in PWM drive voltage [1]. However, these methods are associated with limitations such as high cost, complexity, and an inability to detect certain types of faults.

To overcome these limitations, there is an increasing demand for non-intrusive and effective techniques for insulation fault detection in electric motors. These techniques should be capable of capturing and analyzing the fast pulse signals characteristic of insulation faults. By accurately detecting such faults, timely maintenance actions can be undertaken to prevent further deterioration and ensure uninterrupted motor operation.

Recent research proposed an active ageing control model, making use of voltage waveforms at the inverter and motor sides and phase current showing the high-frequency transient [2]. Reference [3] presents a method of insulation detection by observing the stimulated electromagnetic interference (EMI) of an electric drive in the frequency domain. [4] describes a work focusing on the correlation between the long and short axis of the Park vector trajectory ellipse and the positive and negative sequence components of the stator current. Though this work lifts the precision up to a certain level, the complex mathematical model still poses a barrier to economic and real-time applications. Reference [5] proposed a model that describes insulation faults as resulting in a change in stray capacitance between the stator windings and the ground as the degradation of insulation is observed. This model is the foundation for developing a circuit capable of detecting and quantifying these faults. The circuit is specifically designed to capture the ringing current generated by the PWM voltage in the windings, which exhibits frequencies ranging from ones to tens of kilohertz and duty cycles of approximately 0.3 microseconds, as indicated by the experimental results in [5]. By measuring the amplitude of these ringing currents, we can determine whether the degradation happens before the fault occurs. Reference [6] proposes an architecture of peak sample detection and hold implemented using 180nm complementary metal-oxide-semiconductor (CMOS) technology, yielding a
good performance in high-speed applications. In fact, research on voltage sag detection has a close relationship with peak detection, as [7] and [8] have discussed, despite the fact that these outcomes are for high-voltage applications. Reference [9] analyses several peak detection methods for AC voltage, including analogue circuits and some other implementations using Very High-Speed Integrated Circuit Hardware Description Language (VHDL).

Therefore, the objective of this study is to design a circuit for inductive sensing of motor insulation faults. By leveraging the proposed model in [5], our aim is to develop a non-intrusive method capable of accurately detecting ringing currents in electric drives. This research holds the potential to enhance the reliability and maintenance strategies of electric drives.

1.2 Problem

Insulation fault detection in electric motors presents several challenges, including noise interference, low-speed response, and limited precision in traditional peak holder designs. While noise interference is a common issue across various inductive sensor designs, traditional peak holder circuits face specific limitations in capturing precise voltage levels due to the short duty cycles of incoming signals.

One of the challenges is the presence of noise signals that can significantly affect the accuracy of insulation fault detection systems. Inductive sensors used in these systems are vulnerable to electromagnetic interference, power supply fluctuations, and environmental factors, leading to the introduction of unwanted noise into the measured signals. Consequently, this noise interference can result in false positives or false negatives, impairing the reliability and effectiveness of insulation fault detection methods. Addressing noise-related issues is crucial to ensure accurate fault detection and enable timely maintenance actions.

Furthermore, the low-speed response of traditional peak holder designs hampers their ability to capture and analyze fast pulse signals associated with insulation faults. These faults often manifest as short-duration voltage spikes or ringing currents characterized by high-frequency components. However, traditional peak holder circuits, due to their design limitations, struggle to capture and track these rapid changes with sufficient speed and precision. As a consequence, the voltage amplitude of such short-duration signals may not be accurately captured and stored in the peak holder capacitors. This limitation compromises the precision of fault detection, potentially leading to undetected
or misinterpreted insulation faults.

Thus, in addition to noise interference and low-speed response, limited precision in traditional peak holder designs represents a critical challenge. The short duration of incoming signals prevents the capacitors in peak holder circuits from being adequately “filled” with electric charge, resulting in reduced precision in measuring the amplitude of the fault signals. Overcoming this limitation is essential to ensure precise and reliable detection of insulation faults, enabling effective maintenance strategies.

Addressing these challenges requires the development of advanced peak holder circuitry capable of effectively mitigating noise interference, capturing fast pulse signals with improved speed and precision, and ensuring accurate measurements of fault amplitudes. By overcoming these limitations, the reliability and performance of insulation fault detection in electric motors can be significantly enhanced.

1.3 Purpose

The purpose of this study is to design a circuit for inductive sensing of motor insulation faults, focusing on the analysis of signals and the development of an improved fault detection solution. The key objectives of this research are as follows:

- Mitigating Noise Interference: One important objective of this study is to address the challenge of noise interference in insulation fault detection. The proposed circuit should incorporate advanced noise cancellation techniques and filtering mechanisms to minimize the impact of unwanted noise signals on the accuracy of fault detection. By effectively mitigating noise interference, the circuit will improve the reliability and robustness of the insulation fault detection system.

- Improving Speed, Responsiveness, and Precision: A primary objective of this research is to enhance the speed, responsiveness, and precision of the circuit for insulation fault detection. The proposed circuit will be designed to capture and analyze fast pulse signals, such as short-duration voltage spikes and ringing currents, with improved accuracy and speed. By optimizing the signal processing circuit and leveraging advanced design techniques, this design will enable timely and precise fault detection, facilitating proactive maintenance strategies.
By fulfilling these objectives, this research aims to advance the state-of-the-art in motor insulation fault detection, offering an improved circuit design that can effectively analyze signals and provide accurate fault detection outputs.

1.4 Goals

The main goal of this project is to design a high-speed, low-noise peak holder circuit for motor insulation fault detection. The specific subgoals include:

1. Circuit design: Develop a comprehensive circuit design for the peak holder that accurately captures and tracks voltage spikes and ringing currents associated with insulation faults.

2. Simulations and verification: Perform simulations and verification to validate the circuit’s functionality and performance, ensuring accurate detection and measurement of fault signals.

3. Printed circuit board (PCB) layout design: Create an optimized PCB layout that considers signal integrity, noise reduction, and efficient component placement.

4. Usability verification: Verify the usability of the circuit with proper simulation setups.

By achieving these goals and subgoals, this project aims to deliver a high-speed, low-noise peak holder circuit that provides reliable detection of motor insulation faults. The successful completion of these objectives will advance motor fault detection techniques and support proactive maintenance strategies in various industries.

1.5 Research Method

The research methodology for this project follows a systematic approach to achieve the desired outcomes. The key components of the methodology are as follows:

- Literature Review: A comprehensive review of relevant research papers, theses, and technical articles in the field of motor insulation fault detection and peak holder designs was conducted. This step helped
identify the existing techniques, challenges, and potential areas of improvement in the field.

- Circuit Design and Simulation: Based on the insights gained from the literature review, a circuit schematic for the high-speed, low-noise peak holder was developed. Simulations were performed to validate the circuit’s functionality and performance under various operating conditions.

- PCB Layout Design: The circuit schematic was translated into a PCB layout design using industry-standard software KiCad. Attention was given to component placement, trace routing, and grounding techniques to ensure optimal performance and noise reduction.

- Prototype Construction and Testing: A prototype of the designed circuit was constructed using the PCB layout. Rigorous testing was conducted to verify the circuit’s ability to accurately capture and analyze the ringing currents associated with motor insulation faults.

- Data Analysis and Validation: The captured data from the prototype was analyzed using appropriate algorithms and signal processing techniques. The performance of the peak holder circuit was evaluated based on the accuracy and reliability of the insulation fault detection results.

By following this research methodology, the aim is to develop a robust and effective circuit for inductive sensing of motor insulation faults, contributing to the advancement of fault detection techniques in electric drives.

1.6 Delimitations

This design primarily emphasizes the post-processing of the detected signal, excluding the design and implementation aspects of the probe, which serves as the input for this module. However, it is important to note that a constraint will be imposed on the input signal to ensure the proper functioning of this design.

1.7 Ethics and sustainability

Since this project is focused on fault detection of electric drives, the precision of the design plays a crucial role in ensuring both labour protection and energy-
saving measures. By developing an accurate and reliable fault detection system, potential risks and hazards associated with faulty electric drives can be identified in a timely manner, thus safeguarding the well-being and safety of personnel working in industrial environments.

Meanwhile, precise fault detection enables proactive maintenance and repairs, preventing costly downtime and reducing overall energy consumption. A highly precise design ensures that the fault detection system can effectively differentiate between regular operation and potential faults, minimizing false alarms and unnecessary interventions. Consequently, the precision of the design directly contributes to the optimization of labour resources, enhances operational efficiency, and promotes sustainable energy practices within the industrial sector.

1.8 Structure of the thesis

Chapter 2 presents relevant background information about insulation fault detection and previous relevant work on high-speed pulse peak holder design. Chapter 3 presents the methodology and method used to design this peak holder. Chapter 4 provides a comprehensive explanation of the processes involved in designing the circuit schematic, conducting simulations, and creating the PCB layout. In Chapter 5, the results of simulations and experimental circuit test results are demonstrated, together with thorough analysis and discussions. Chapter 6 gives conclusions and foresight of the work in this project.
8 | Introduction
Chapter 2

Background

This chapter serves as a foundational background for the subsequent discussions in this thesis. It provides essential background information on fault detection methods for induction motors with inter-turn short circuit faults, as well as an exploration of high-speed peak holder circuit design. Additionally, this chapter delves into related work that has been conducted in these areas, setting the stage for the research and development presented in this thesis.

2.1 Fault detection methods for induction motors with inter-turn short circuit faults

[5] discusses two methods for detecting the ageing process of electric drives are proposed, offering a more precise and theoretical understanding of the phenomenon.

2.1.1 Fault detection based on rotor-slot harmonics

The first method involves observing the frequency characteristic, specifically focusing on the harmonic distribution of the phase current of the electric drive. Insulation problems within the drive system can lead to changes in the harmonic distribution in a specific manner. This method is based on rotor slot harmonics (RSHs) analysis. Analyzing the changes in the harmonic makes it possible to identify and diagnose insulation faults, providing valuable insights into the ageing process of the drive.

This subsection explores the utilization of RSHs as a fault detection method for inter-turn short circuit (ITSC) faults in induction motors (IMs).
RSHs are frequencies generated by the influence of rotor bars on the air-gap permeance.

By analyzing the RSH frequencies, potential fault signatures can be identified. Take experiment results from [5] as an example. Notably, frequencies such as 727 Hz 1303 Hz exhibit significant variations in the presence of ITSC faults as shown in Fig 2.1.

![Figure 2.1: FE model results of the phase-b magnitude current spectrum in two conditions for the IM prototype: (a) healthy and (b) with an ITSC fault. Note that the y-axis is limited, to highlight the RSHs. A blue arrow indicates a RSH present in both healthy and faulty cases; a red arrow indicates a RSH present in only the faulty case. [5]](image)

Experimental and finite element (FE) model results validate the behaviour of these RSHs, providing insights into their consistent responses across different stator currents. The asymmetries observed in the responses can potentially aid in identifying the phase containing the ITSC fault.

However, it should be acknowledged that frequency analysis, which involves complex mathematical techniques, can pose challenges in practical implementation due to the intricate nature of the method. It is also important to note that this method heavily relies on the specific characteristics and
specifications of the motor being analyzed. Adapting frequency analysis to different types of electric drives, which exhibit inherent variances, may further complicate the application of this method.

In summary, this subsection delves into the utilization of rotor-slot harmonics as potential fault signatures for ITSC fault detection in induction motors. It acknowledges the complexities involved in frequency analysis and emphasizes the challenges associated with applying this method to diverse electric drive systems.

2.1.2 Insulation health monitoring with current ringing measurements

The second method proposed in [5] involves examining the ringing phenomenon in the PWM drive current. This method utilizes kHz-range current ringings, which can produce harmonics up to several MHz, that occur after a switching transition of the converter, eliminating the need for additional sensors or equipment. These ringings are influenced by the presence of parasitic capacitance in the stator windings, which are closely tied to the insulation state.

[5] reveals an interesting finding that insulation faults can be equivalent to an added capacitance between one phase terminal and the motor ground point. This added capacitance alters the electrical characteristics of the electric drive, resulting in changes in the ringing metrics of the current waveform. As described in [5], several experiments were conducted to test a motor with ageing insulation to evaluate the current ringing metrics. The metrics exhibited different behaviour compared to the experiments with emulated insulation change. $\Delta_{RMS}$ and $\Delta_{peak}$ showed quasi-linear trends, as demonstrated in Figure 2.2, reflecting the decrease in parasitic capacitances, which indicates faster insulation deterioration after 400 hours of testing.

By comparing the initial state’s ringing current metrics with those of the current state, it becomes possible to assess the extent of ageing or insulation degradation in the drive system. This approach offers a precise and theoretical framework for ageing process detection, enabling proactive maintenance strategies and facilitating the safe and efficient operation of electric drives in industrial applications.

The implementation of the proposed method for fault detection involved the use of an Field-programmable gate array (FPGA) to implement the entire analysis system. While the FPGA offers flexibility and high processing capabilities, it also raises the cost of detection.
Figure 2.2: $\Delta_{\text{peak}}$ of ringing currents in three stators during motor accelerated ageing, considering thermal-steady state only. The ringings are measured when the currents are at $i = +15$ A. [5]

Additionally, it’s worth noting that measuring the parasitic capacitance in the stator windings still presents challenges. It typically requires opening the motor to access the windings and perform the measurements. This adds complexity and time to the inspection process. Opening the motor and accessing the windings may not be a straightforward task, especially in industrial settings where downtime must be minimized. Therefore, the practicality and feasibility of incorporating capacitance measurements into routine inspection procedures deserve to be carefully considered.

Considering both the cost implications of FPGA-based implementation and the challenges associated with capacitance measurements, it becomes evident that further research and development efforts are necessary. Alternative approaches that offer cost-effective solutions and minimize the need for invasive measurements should be explored. These could include the development of simpler analogue circuits or the integration of non-intrusive monitoring techniques to assess the insulation state of the stator winding. By
addressing these practical concerns, the proposed method can be made more accessible and applicable for widespread adoption in industrial settings.

2.2 Peak holder design

In this section, we will briefly discuss the theories about analogue peak holder circuit design.

2.2.1 Definition

In the context of circuit design, a peak holder refers to a device or circuit that captures and holds the maximum value of an input signal. Its purpose is to preserve and provide a stable representation of the peak voltage or current level, even after the original signal has passed. Peak holders are commonly used in various applications where it is essential to track and analyze peak values, such as in signal processing, measurement systems, audio applications, and control systems.

The operation of a peak holder involves detecting and storing the highest instantaneous value of the input signal. Once the peak value is captured, it remains constant until a new peak value exceeds it. This mechanism ensures that the peak holder retains the highest amplitude reached by the signal, allowing for subsequent analysis or processing.

Peak holders can be implemented using different circuit configurations, including analogue and digital designs. Analogue peak holders typically utilize capacitors and diodes to capture and hold the peak voltage, while digital peak holders employ digital sampling and storage techniques. The choice of peak holder implementation depends on the specific application requirements, signal characteristics, accuracy, and response time considerations.

In this project, we mainly discuss the analogue peak holder design.

2.2.2 Traditional peak holder design

Figure 2.3 demonstrates a basic traditional peak holder design. This design consists of an operational amplifier (op-amp), a diode and a capacitor. A transistor switch functions as a drainer to reset the circuit, that is, set the stored voltage level to zero. The voltage input is connected to the non-inverting input of the op-amp.

The circuit works as follows:
Charging Phase: When the input signal exceeds the voltage across the capacitor, the diode conducts and allows the capacitor to charge to the peak voltage level. The capacitor captures and holds this peak voltage as long as the input signal remains above the stored value.

Holding Phase: Once the peak voltage is captured, the diode blocks further charging, thus preserving the peak value. The capacitor acts as a reservoir, maintaining the stored voltage level even if the input signal decreases.

The basic peak holder circuit is relatively simple in its design and can be implemented using commonly available electronic components. Its analogue nature enables real-time peak tracking without the need for complex digital processing. However, there are important considerations to ensure accurate and reliable peak detection:

- Capacitor Selection: The choice of capacitor value is critical to strike a balance between response time and signal fidelity. A larger capacitor provides a longer hold time but may result in a slower response to rapid signal changes.

- Hold Time: The hold time is the duration for which the peak voltage is maintained by the circuit after the input signal drops below the stored value. It depends on the discharge characteristics of the capacitor and the leakage current of the diode.

- Circuit Limitations: The basic peak holder circuit has limitations that should be taken into account. Factors such as temperature variations,
component tolerances, and input impedance can affect its performance. Rapid changes in the input signal during the hold time can introduce inaccuracies.

This basic peak holder circuit has a few drawbacks. One drawback is the discharge time of the capacitor, which can be relatively slow. This slow discharge occurs through leakage currents and can lead to a delay in accurately tracking subsequent peaks. As a result, the circuit may not be able to respond quickly to rapid changes in the input signal, which is intolerable when tracking the amplitude of the high-speed pulses.

Another drawback is the accuracy of the hold time. The duration for which the peak voltage is maintained depends on the discharge characteristics of the capacitor and the leakage current of the diode. Variations in these factors can introduce inconsistencies in the hold time, potentially resulting in inaccuracies in peak detection.

The basic peak holder circuit does not account for signal variations during the hold time. If the input signal undergoes rapid changes or exhibits high-frequency components, the captured peak value may not accurately represent the true maximum value of the signal. This can introduce signal distortion and compromise the accuracy of peak detection.

Additionally, the performance of the primary peak holder circuit can be sensitive to component tolerances. Small variations in the diode and capacitor used can lead to inconsistencies in peak detection and introduce measurement errors. Therefore, careful component selection and calibration are necessary for accurate peak detection.

Lastly, the basic peak holder circuit has a limited dynamic range. It can accurately capture peaks within a certain voltage range, but if the input signal exceeds this range, the circuit may fail to accurately capture the true peak value. Instead, it may saturate or clip the signal, leading to inaccurate measurements.

These drawbacks highlight the need for more advanced peak holder designs that address these limitations and provide improved accuracy, faster response times, enhanced dynamic range, and better immunity to signal variations.

2.2.3 Improved peak holder for high-speed application

In order to address the limitations of the basic peak holder circuit, various improvements have been introduced to meet specific requirements in different
application scenarios.

In the circuit depicted in Figure 2.4, two op-amps are utilized, with an additional op-amp inserted between the capacitance and the load, functioning as a unity-gain buffer. This modification aims to address some of the limitations of the basic peak holder circuit. When the input voltage surpasses the charge stored on the capacitor, a larger input signal value will be “refreshed”. Conversely, when the input has a smaller value, a diode connected to the output of the leftmost op-amp $A_1$ in Figure 2.4 prevents $A_1$ from becoming negatively saturated. As a result, the capacitor retains its previous value for a longer duration, thereby extending the recovery time of this peak holder circuit.

![Figure 2.4: Improved peak holder with reference voltage buffer.](image)

Reference [10] proposes two ways of further improvement using LTC6244 op-amps to implement a high-speed peak detector.

The circuit in Figure 2.5 improves upon the speed and accuracy of the circuit in Figure 2.4 by addressing the limitations of the classic peak detector’s architecture. By using a Schottky barrier diode instead of a rectifying diode, the forward voltage drop is reduced, leading to increased initial charging current and faster recovery time. The circuit compensates for the diode drop by balancing it with a matching Schottky diode in the local feedback loop. The left-most diode clamps the input voltage to protect the circuit.

Figure 2.6 presents an alternative improvement method by incorporating matched NPN bipolar junction transistors (BJTs) as current boosters to enhance the charging speed of the reservoir capacitor. This circuit operates similarly to the one shown in Figure 2.5, since the P-N node across the base and emitter of BJTs, namely functions almost the same as a diode, but with the addition of a current pump. By connecting the emitter node of the current pump to the reservoir, the charging speed is significantly increased,
and the bandwidth is extended due to the low source impedance to the capacitor. The primary speed limitation of this circuit lies in the output buffer section, specifically, the unity-gain amplifier implemented using the rightmost amplifier depicted in Figure 2.6.

2.3 Other related circuit design

In this section, some other circuit theories that have been touched on in this project are briefly introduced.

2.3.1 Active low-pass filter design

Active low-pass filters are fundamental components in electronic circuits that allow low-frequency signals to pass through while attenuating high-frequency
signals. Among the various filter configurations, the first-order active low-pass filter stands out as a simple yet effective design for many applications. An example of a non-inverting first-order active low-pass filter is shown in Figure 2.7.

![First-order active low-pass amplifier](image)

**Figure 2.7:** An example of the first-order active low-pass filter.

The first-order active low-pass filter utilizes an op-amp and a combination of resistors and capacitors to achieve its frequency response characteristics. This configuration offers a single-pole rolloff, resulting in a gradual attenuation (-20 dB/decade of slope and -3.01 dB of attenuation at the cutoff frequency) of higher frequencies beyond the cutoff frequency. The cutoff frequency can be calculated using

\[
f_c = \frac{1}{2\pi RC}.
\]

One key advantage of the first-order active low-pass filter is its straightforward design and ease of implementation. By selecting appropriate resistor and capacitor values, the cutoff frequency can be precisely determined according to the desired application requirements. Moreover, the gain of the filter can be adjusted by incorporating feedback resistors, allowing for signal amplification if needed.

Another benefit of the first-order active low-pass filter is its minimal component count. With just a single op-amp and a few passive components, it offers a cost-effective solution for filtering applications. Furthermore, the simplicity of the circuit enables easy troubleshooting and modification if necessary.
2.3.2 Differential Operational Amplifier Configuration

The differential amplifier is a circuit that performs voltage subtraction. It takes two input signals and produces an output voltage that is proportional to the voltage difference between these two inputs. The differential amplifier commonly utilizes the inverting and non-inverting terminals of an operational amplifier to achieve this functionality. A common structure of a differential amplifier using an op-amp is depicted as Figure 2.8.

![Figure 2.8: An example of a differential amplifier using an op-amp.](image)

Suppose the voltages of two input nodes are $V_1$ and $V_2$ respectively, we have

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_f = \frac{V_a - V_{out}}{R_3}.$$  

Considering an ideal op-amp, since $V_a = V_b$ and

$$V_b = V_2 \cdot \frac{R_4}{R_2 + R_4},$$  

(2.1)

From $I_1 = I_f$, we can deduce

$$\frac{V_1 - V_a}{R_1} = \frac{V_a - V_{out}}{R_3} \Rightarrow V_{out} = \frac{(R_1 + R_3) V_a - R_3 V_1}{R_1}.$$  

(2.2)
Substitute \( V_b \) with 2.1, we have

\[
V_{out} = \frac{(R_1 + R_3) \cdot \frac{R_4}{R_2+R_4} \cdot V_2 - R_3 V_1}{R_1}.
\]  

(2.3)

Suppose both of the input paths are symmetrical, we have \( R_1 = R_3, R_2 = R_4 \), thus

\[
V_{out} = \frac{R_3}{R_1} \cdot (V_2 - V_1).
\]  

(2.4)

Let \( V_{in} = V_2 - V_1 \), we have the voltage gain of this differential amplifier

\[
A_v = \frac{V_{out}}{V_{in}} = \frac{R_3}{R_1}.
\]  

(2.5)

### 2.3.3 Non-inverting Operational Amplifier Configuration

This type of configuration does not invert the phase of the input while amplifying. A common structure of a non-inverting operational amplifier is shown in Figure 2.9.

![Non-inverting Operational Amplifier](image)

Figure 2.9: An example of a non-inverting amplifier using an op-amp.

Considering the ideal summing point \( V_{in} = V_1 \), and

\[
V_1 = \frac{R_2}{R_2 + R_f} \cdot V_{out},
\]  

(2.6)
we have

\[ A_v = \frac{V_{out}}{V_{in}} = \frac{R_2 + R_f}{R_2}. \]  \hspace{1cm} (2.7)

## 2.4 Summary

This chapter explores two important topics: insulation fault detection and the peak holder circuit. The chapter begins by discussing insulation fault detection, which involves identifying faults or breaks in electrical insulation and discusses possible methods to implement the detection system. The principles and techniques for insulation fault detection are explained, highlighting their significance in ensuring electrical safety.

Next, the chapter dives into the peak holder circuit, providing an introduction to its basic design and discussing its limitations. Various improvements to the circuit are presented, including the use of a unity-gain buffer, Schottky diodes or BJTs as current boosters, which enhance its performance in terms of recovery time, voltage drop and charging speed.

By covering these topics, the chapter equips readers with knowledge of insulation fault detection techniques and design considerations for peak holder circuits. This knowledge is the basis of the peak holder design targeted at inductive sensing for insulation fault detection, which is further discussed in the coming chapters.
Chapter 3
Research Methodology and Validation Design

The purpose of this chapter is to provide an overview of the design objectives and validation process of this project. Section 3.1 introduces the expected outcome and specifications for the circuit design. Section 3.2 describes the experiment design for simulation and validation. Finally, Section 3.3 briefly discussed the software and hardware used in this project.

3.1 Design Objective and Specifications

Figure 2.2 illustrates the variation of $\Delta I_{\text{peak}}$, which represents the difference in peak values of the ringing current, across three stators of an electric drive. Notably, the figure showcases a linear increase in $\Delta I_{\text{peak}}$ over time, reflecting the accelerated ageing process. To accommodate diverse probe configurations, it is recommended to integrate a gain-adjustable pre-amplifier into the input stage, ensuring improved adaptability and system flexibility. Therefore, rather than absolute precision, this project primarily focuses on achieving a substantial linear correlation between the input and output. Furthermore, given the gradual nature of the ageing process, the speed requirements for the circuit system can be moderately relaxed.

Figure 3.1 shows the overall structure of the circuit design. The pulse input from the inductive probe undergoes a two-stage amplification process. Initially, it is amplified using a differential amplifier with a relatively low voltage gain, and subsequently, re-amplified by an adjustable gain amplifier.
Following this, one side of the amplified input is eliminated by a rectifier prior to reaching the peak holder stage. In order to achieve a smoother output response, a low-pass filter is employed to attenuate the additional harmonics introduced by potential spikes generated during switching operations within the peak holder.

![Figure 3.1: System schematic](image)

### 3.2 Simulation Setup and Validation Design

To validate the circuit’s performance at the schematic level, a simulation environment is necessary. Figure 3.2 demonstrates a characteristic feature of a single ringing current induced by a pulse drive current as observed in [5], and 3.3 analyzes the frequency components in ringing currents.

The experimental results provide confirmation that the width of a single pulse in the ringing currents is approximately 0.25 microseconds. Considering the typical frequency range of PWM drive currents in commercial electric drives, which spans from 2 to 20 kHz, and accounting for the presence of three phases in electric drives, each period encompasses three events.

In order to accurately simulate these conditions, the simulation environment in Advanced Design System (ADS) is configured as depicted in Figure 3.4 where two different setups are demonstrated. A "ladder-shaped" input approximation, as depicted in 3.4a, prioritizes the envelope of the actual input signal, with a primary focus on its peak voltage. This configuration generates pulses with rise time, hold time, and fall time of 0.1 microseconds, while their amplitudes exhibit a slow variation at a rate of 4 Hz, following a triangle wave envelope. 3.4b depicts a more precise design of the input approximation, which consists of a pulse generator (zero rise time and fall time, 0.25 microseconds of pulse width), a lowpass filter and an equalizer.
Figure 3.2: Current ringing for (a) positive and (b) negative currents, measured with two different current sensors. [5]

Figure 3.3: Spectrum of harmonics in ringing current. [5]

matrix made up of five bandpass filters and voltage multipliers. Ideal op-amps named from “AMP1” to “AMP6” are voltage buffers while “AMP7” and “AMP8” add up all different components and adjust the peak of the simulated signal. The equalizer matrix focuses on relatively dominant harmonics in ringing tails as shown in 3.2, which are 1.2 MHz, 2.8 MHz, 5 MHz and 7 MHz.

The results of approximated input stimuli are shown in 3.5. Figure 3.5(a)
compares different ways of input approximation, namely ideal pulses, ladder-shaped pulses, and tuned harmonics in ringing tails. To better replicate the stimuli in the real world, the distribution of harmonics in ringing tails is tuned to resemble the one being demonstrated in 3.3, as displayed in Figure 3.5(b).

![Diagram of input approximation](image)

(a) "Ladder-shaped” input approximation.

(b) Input approximation with ringing tail harmonics tuning.

Figure 3.4: Simulation setups of input stimuli in ADS. (a) demonstrates a "ladder-shaped” approximated input signal, where "Vf_Pulse” generates pulse voltage while "Vf_Triangle” denotes the slow envelope of pulses. (b) shows a more complex way of input signal approximation with harmonics calibrated in ringing tails which better mimics the real ringing effect in drive current.

To validate the performance of the circuit with the main concern about the linear correlation between the input signal from the probe and the output of
Figure 3.5: Simulation results of various ways of input stimuli approximation. (a) Waveform of different ways of approximation, the blue trace for ideal pulses, the magenta trace of the ladder-shaped, and the red trace for which has ringing tails with tuned harmonics. (b) Spectrum of stimuli with ringing tails tuned in harmonics.

In this design, we apply the mean-squared error (MSE) to do the analysis, that is, we can measure the average of the square of the errors between the normalised input (expected outcome) and the normalised output.

Suppose that $\hat{Y}$ is the normalised output values and $Y$ is the normalised...
input, we have

\[
MSE = \frac{1}{n} \sum_{i=1}^{n} (Y_i - \hat{Y}_i)^2,
\]

(3.1)

where \( n \) means the number of samples.
Usually, a smaller value of MSE means a better precision.

### 3.3 Used Hardware and Software

During the design phase, the ADS software is utilized to facilitate the schematic design and simulation setup. Furthermore, KiCad, a tool for printed circuit board (PCB) layout design, is employed to ensure efficient and accurate PCB layout. MATLAB is applied in simulation data analysis.

The high bandwidth op-amp model selected for this design is the TSV772IYST, manufactured by ST Microelectronics. This op-amp integrated circuit (IC) features a gain bandwidth product of 20 MHz and a low offset voltage of 200 \( \mu \)V [11]. In conjunction with the op-amp, the design incorporates paired BJTs employing the BCM847DS model from Nexperia [12].

To convert the direct current (DC) power supply, the design incorporates the L7805CV by ST Microelectronics and the MC7905BTG by Onsemi as voltage regulator ICs [13][14]. These regulators perform DC-DC conversion, effectively transforming the 12V DC input into ±5V DC power rails, ensuring stable and reliable operation of the circuit.

### 3.4 Summary

This chapter delves into the design methodology for the circuit detecting ringing currents in electric drives. It emphasizes the linear increase of \( \Delta I_{peak} \) over time as a reflection of the accelerated ageing process. The chapter highlights the importance of an adjustable gain pre-amplifier for adaptability and system flexibility, prioritizing a significant linear correlation over absolute precision. The simulation setup and validation design are discussed, including the use of ADS and function generators for performance assessment. The chapter also gives an overview of the hardware and software utilized.
Chapter 4

Design and Implementation

In this chapter, the focus is on the detailed design and implementation of the circuit. Section 4.1 covers the schematic design, which is divided into three subsections: power supply, preamplifier, and peak holder. The power supply section addresses the design considerations and selection of components for providing stable and regulated power to the circuit. The preamplifier section discusses the design and configuration of the input stage, including amplification and signal conditioning. The peak holder, being the core component, is explored in-depth, considering its design principles, components, and performance requirements.

Following the schematic design, Section 4.2 focuses on the PCB design. This section highlights the process of transforming the schematic into a physical layout on a PCB. It covers aspects such as component placement, routing, and considerations for signal integrity and noise reduction. The PCB layout is crucial for ensuring the proper functionality, reliability, and manufacturability of the circuit.

4.1 Schematic Design

In this section, we delve into the comprehensive schematics of various components of the circuit. The schematic of the entire circuit can be found in Appendix 4.1.

4.1.1 Power Supply

The power conversion circuit (Figure 4.1) is designed to efficiently convert a 12V DC power input into a desired ±5V power output. To facilitate the power
conversion, the ICs L7805 and MC7905 are employed, providing reliable +5V and -5V DC outputs, respectively. The circuit incorporates several capacitors (C₃, C₄, C₆, C₇, and C₈) to absorb the ripple in the output voltage, ensuring a stable power supply. Additionally, resistors (R₂₇, R₂₈, R₂₉, and R₃₀) are implemented to divide the ±5V power output into ±2.5V for optimal compatibility with the subsequent amplification stage, where op-amps are utilized.

![Figure 4.1: Power conversion module](image)

### 4.1.2 Preamplifier

In the pre-amplification stage, two cascaded operational amplifiers (op-amps) are employed to amplify the input signal, as described in Chapter 3.

U1A serves as a differential amplifier, utilizing resistors R₆ and R₇ as the input matching resistors, both set to 1kΩ. The feedback resistors R₁₃ and R₁₀ are chosen as 20kΩ, considering the assumption that the normal maximum input voltage swing is 10mV. According to equation (2.5), the voltage gain of this differential amplifier is calculated as $A_v = \frac{R_{13}}{R_6} = \frac{R_{10}}{R_7} = 20$, corresponding to a gain of 26dB.

U1B functions as a non-inverting single-ended amplifier. It utilizes resistors R₁₄ and R₁₅ as the input matching resistors, both set to 1kΩ. The resistor R₁₉ in the feedback loop is adjustable and is initially set to the standard value of 20kΩ. However, it is important to note that R₁₉ should be calibrated according to the frequency of the input signal to ensure optimal performance and accurate amplification.
4.1.3 Peak Holder

According to the theories in Chapter 2 and the specification requirements, the peak holder can be divided into three parts:

- Rectifier module, which clips out the negative side of the amplified signal,
- Current-boosted comparator module, derived from Hassan Kelley and Gabino Alonso with extended dynamic range,
- Active low-pass filter for removing added harmonics from the output.

Figure 4.3 provides a comprehensive schematic of the peak holder section, offering a detailed representation of its internal components and their connections. Within this configuration, U2A functions as a non-inverting buffer stage amplifier, while D1 acts as a high-speed switch diode responsible for rectifying the input signal. To slightly lower the input voltage, the combination of $R_8$ and $R_{12}$ is employed as a voltage divider. U3 and U4 are paired BJT ICs, with the left half of U3 supplying current to the inverting input of U2B. Moreover, all base nodes of U3 are interconnected with the output of U2B, forming a comparator loop. U5A operates as a non-inverting buffer, while U5B serves as an active low-pass filter with a cutoff frequency ($f_c$) calculated as $\frac{1}{2\pi R_{26}C_5} = 338.6$Hz.

In the original design by Hassan Kelley and Gabino Alonso, the charge reservoir capacitor $C_2$ and the protective draining resistor $R_{23}$ were connected to the ground. However, to extend the dynamic range, which was slightly restricted by the rectifier diode $D_1$, these two components are now connected to a negatively biased voltage source generated by another pair of BJT ICs.
By setting \( R_4 \) and \( R_5 \), the DC bias of U4 is established at -1.8V. Considering the typical base-emitter voltage drop \( V_{BE} \) of the BCM847DS BJT at 0.7V, the voltage output from the emitter node of U4 is determined as \( V_{ref} = (V_B - V_{BE}) - V_EE = -2.5V \). Consequently, the current flowing through \( R_{18} \) and \( R_{22} \) can be calculated as \( I_E = \frac{V_{ref}}{R_{18}} = \frac{(-1.8 - 0.7) - (-5)\text{V}}{47\text{Ω}} = 53.2\text{mA} \), providing an efficient charging current for \( C_2 \) without causing voltage bouncing. Additionally, this voltage serves as the reference for the inverted input of U5A.

Figure 4.3: Peak holder

### 4.2 Printed Circuit Board Layout Design

Figure 4.4 depicts a two-layer PCB layout design of the entire circuit, showcasing the arrangement of components and their interconnections. The J1 connector, located on the PCB, features pins that are arranged from top to bottom as follows: 12V DC input, negative input terminal, positive input terminal, and external ground.

In order to effectively suppress voltage ripples and maintain stable operation, capacitors are strategically placed in close proximity to the rectifier ICs. These capacitors serve to absorb and filter out any unwanted fluctuations in the voltage, providing enhanced protection to the sensitive input circuitry against potential interference originating from the DC-DC conversion process.

Additionally, all layers of the PCB have undergone the copper filling process, which involves covering the ground areas with a continuous layer of copper. This technique improves the circuit’s immunity to external EMI by creating a shielding effect. Figure 4.5 provides a 3D-rendered preview of the PCB, offering a visual representation of the physical layout of this two-layer PCB.
To better counter the EMI, a four-layer PCB is a better choice for its better shielding effect with two DC power layers covering the inner circuit and the power components being split from the signal process components. Figure 4.6 and 4.7 show the layout using a four-layer design and a 3D-rendered preview.
Layer-by-layer graphs of both PCB designs are demonstrated in Appendix C and D.
Figure 4.7: Preview of the four-layer PCB with components mounted. (a) Front side with power supply components. (b) Back side with signal process components.
Chapter 5

Results and Analysis

In this chapter, we present the simulation results from experiments and give a brief analysis.

5.1 Simulation results

The simulation uses two types of stimuli mentioned in Section 3.2 respectively as the input into the designed circuit. Table 5.1 presents a compilation of typical output swing corresponding to various input pulse frequencies and the MSE results using "ladder-shaped" input stimuli, while Table 5.2 demonstrates the simulation with a more precise input simulation, whose frequency characteristics of the ringing tails are tuned to resemble the drive current ringing as demonstrated in Section 3.2.

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>Effective Input Swing (mV)</th>
<th>Output Swing (V)</th>
<th>MSE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>0.680 - 10.0</td>
<td>0.95 - 3.70</td>
<td>0.19</td>
</tr>
<tr>
<td>24</td>
<td>0.699 - 10.0</td>
<td>0.98 - 3.91</td>
<td>0.058</td>
</tr>
<tr>
<td>60</td>
<td>0.707 - 10.0</td>
<td>1.01 - 3.96</td>
<td>0.051</td>
</tr>
</tbody>
</table>

Table 5.1: Simulation result of typical performance using ladder-shaped input approximation with certain input frequencies
<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>Effective Input Swing (mV)</th>
<th>Output Swing (V)</th>
<th>MSE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>0.879 - 11.0</td>
<td>0.97 - 4.12</td>
<td>0.22</td>
</tr>
<tr>
<td>24</td>
<td>0.931 - 10.0</td>
<td>1.02 - 4.47</td>
<td>0.15</td>
</tr>
<tr>
<td>60</td>
<td>0.898 - 11.0</td>
<td>1.04 - 4.54</td>
<td>0.12</td>
</tr>
</tbody>
</table>

Table 5.2: Simulation result of typical performance using harmonic-tuning input approximation with certain input frequencies

It is important to note that the input pulse frequency is set to three times the PWM drive current frequency of the electric drive being measured (considering the common electric drives are powered with three-phase alternating current (AC)), and a minor adjustment in input DC bias may be required to make full use of the input dynamic range. All values are measured under the circumstances where $R_{19} = 20\,\Omega$.

Figure 5.2 and 5.1 demonstrate the simulation results using two different input stimuli under different frequencies. All blue curves in the upper half of subgraphs are the output waveforms, while the red curves which are denser are the input waveforms. Since the harmonic-tuned ringing tail input stimuli behaves way more complex, the input waveforms in Figure 5.1 are not as well triangularly-formed as that in Figure 5.2. Again, the frequency of input is three times the base frequency as labeled to imitate the three phase PWM drive current. For example, the input stimuli is set to 6kHz to simulate under a 2kHz of PWM current.
Figure 5.1: Simulation results with laddered-shaped input stimuli at different frequencies. The blue curve indicates the output and the red curve for input voltage. (a) 2kHz PWM drive current. (b) 8kHz PWM drive current. (c) 20kHz PWM drive current.
Figure 5.2: Simulation results with harmonic-tuned ringing tail input stimuli at different frequencies. The blue curve indicates the output and the red curve for input voltage. (a) 2kHz PWM drive current. (b) 8kHz PWM drive current. (c) 20kHz PWM drive current.
5.2 Result Analysis

The performance of the circuit was evaluated using three sets of data, which were recorded at different frequencies of the detected ringing current events. The data is formatted as follows: frequency (kHz), effective input swing (mV), output swing (V), and MSE (%). The frequency represents the frequency of the detected ringing current events, while the effective input swing indicates the voltage range within which the input produces a linearly casted output. The output swing represents the range of the output voltage resulting from the input within the effective input swing. The MSE is the mean-squared error calculated using the normalized voltage values, providing a measure of the linear correlation between the input and output signals.

The ringing current, characterized by a set of short-width pulses, carries varying power depending on its frequency. Higher frequency results in denser pulses and consequently higher power. It should be noted that the input swing is limited to a lower boundary of 0.7V due to the presence of the rectifying diode.

The results reveal that the output swing remains relatively stable across different frequencies, with only a slight reduction observed at lower input frequencies. The simulation using input stimuli with harmonic-tuned ringing tail shows a slight reduction in precision due to a more complex waveform, but the error is still low with a worst case MSE of 0.22%, which is measured under the almost lowest frequency of PWM current that a commercial electric drive could use nowadays. This reduction can be attributed to slower charge actions occurring in the charge reservoir capacitance within the peak holder. At lower frequencies, the longer time between consecutive pulses leads to slower charging of the charge reservoir capacitance. As a result, the capacitance may not accumulate sufficient charge between pulses, causing a slight voltage drop in the circuit.

Figure 5.2 and 5.1 demonstrate the simulation result in time domain, each figure having subgraphs showing the result under the circumstances of 2kHz, 8kHz and 20kHz PWM drive current respectively. Despite the reduction in output swing at lower frequencies, all MSE results are significantly low, indicating a strong linear correlation between the input and output signals. This suggests that the circuit maintains good linearity even with the presence of slower charge actions and slight voltage drops at lower frequencies.

The analysis demonstrates the stable performance of the circuit across different frequencies of the ringing current events. The observed reduction in output swing at lower frequencies can be attributed to slower charge actions.
in the charge reservoir capacitance. However, the low MSE values indicate a strong linear correlation between the input and output signals, highlighting the effectiveness of the circuit design.
Chapter 6

Conclusions and Future work

6.1 Conclusions

To sum up, the results obtained from the investigation of the peak holder design for the detection of fast narrow-width pulses in PWM drive current for electric drives are highly encouraging. The comprehensive analysis of the circuit’s performance reveals its capability to accurately capture and detect the ringing current pulses. The consistent behaviour across different frequencies demonstrates its robustness in handling varying power levels associated with denser pulse patterns.

Throughout the study, careful attention was given to the design parameters and circuit components, resulting in a stable output swing within the expected operating range. The observed reduction in output swing at lower input frequencies, attributed to the slower charge actions of the reservoir capacitance, did not significantly impact the circuit’s overall effectiveness.

The low mean-squared error values indicate a strong linear correlation between the input and output signals, highlighting the circuit’s reliability in capturing and faithfully reproducing the pulse events. However, it is important to acknowledge the limitations of the study and recognize potential areas for further enhancement.

Future investigations could explore alternative component configurations to address the reduction in output swing at lower frequencies and assess the circuit’s performance under different operating conditions. Additionally, evaluating its compatibility with diverse electric drive systems would expand its applicability in real-world scenarios.

The findings from this study demonstrate the promising potential of the peak holder design for accurate pulse detection in PWM drive current. These
results contribute valuable insights to the field and pave the way for further advancements and refinements. Continued rigorous testing and analysis will be crucial to fully unlock the circuit’s capabilities and optimize its design parameters for practical deployment in electric drive systems and pulse signal analysis.

6.2 Limitations

One limitation of the current peak holder design is its performance at the extreme ends of the input frequency range. While the circuit demonstrates relatively good performance within the tested frequencies, it may encounter challenges when confronted with significantly higher or lower input frequencies. At lower frequencies, the slower charge actions to the reservoir capacitance may result in a reduced output swing, potentially affecting the accuracy and stability of the output swing. Moreover, the operating temperature is considered with an assumption that the power supply components on the PCB are not heat-productive, which could lead to some potential decrease in output precision.

To address these limitations, further optimization is required to enhance the circuit’s adaptability to a wider input frequency range while maintaining a stable output range. This may involve fine-tuning the values of critical components, such as the capacitance and resistance elements, to improve the circuit’s response time and charge/discharge characteristics. Additionally, exploring advanced capacitor technologies or utilizing frequency-dependent compensation techniques could offer potential solutions to mitigate the frequency-dependent variations in the output swing, and a more detailed heat sink design will address the problem of temperature change.

6.3 Future work

There are opportunities to optimize the peak holder design to reduce the size and complexity of the PCB while maintaining its performance. One avenue for improvement is the bipolar power supply design. Simplifying the power supply section by exploring alternative voltage regulation schemes or integrated power management solutions could lead to a more compact and efficient design. By reducing the number of discrete components and optimizing power routing, the overall PCB footprint can be significantly reduced.

To address the limitations regarding the circuit’s adaptability to a wider
input frequency range while keeping the output range stable, several methods can be pursued. Firstly, fine-tuning the values of critical components, such as the capacitance and resistance elements, can improve the circuit’s response time and charge/discharge characteristics. This can be achieved through systematic analysis and experimentation to determine the optimal component values for different input frequency ranges.

Additionally, exploring advanced capacitor technologies, such as low equivalent series resistance (ESR) and high self-resonant frequency (SRF) capacitors, can help improve the circuit’s performance at higher frequencies. These capacitors offer faster charging and discharging characteristics, enabling the peak holder to handle rapid pulse events more effectively.

Furthermore, employing frequency-dependent compensation techniques can be beneficial in mitigating the frequency-dependent variations in the output swing. This involves designing circuitry that dynamically adjusts the amplifier gain or other relevant parameters based on the input frequency. Adaptive filtering or gain control mechanisms can be implemented to ensure consistent and stable output characteristics across a wide range of input frequencies.

Moreover, integrating advanced simulation and modelling tools into the design process can aid in identifying optimal component values, evaluating different compensation techniques, and optimizing PCB layout. Computer-aided design software, electromagnetic simulation tools, and thermal analysis tools can provide valuable insights into signal integrity, power distribution, and thermal management aspects. This enables designers to make informed decisions on component placement, interconnect design, and power management, leading to a more efficient and compact design.

By incorporating these methods into future work, the peak holder can be further optimized to overcome the limitations related to input frequency range adaptability and PCB size. These advancements will enhance the peak holder’s performance and enable its seamless integration into a wide range of applications requiring accurate and stable detection of fast narrow-width pulses in PWM drive currents for electric drives.
Conclusions and Future work
References


Appendix A

Circuit Schematic

In this chapter, the schematic for the whole circuit of the peak holder design is demonstrated in A.1. This schematic is plotted using KiCad.
Figure A.1: Full schematic of the peak holder circuit.
Appendix B

Program Codes used in Analysis

This appendix illustrates the MATLAB codes used in analyzing the linear correlation between the input and output in the simulation.

```matlab
function [voltage] = INPUT_SIG_EMULATOR(time)
%INPUT_SIG_EMULATOR Voltage of input
% Calculate the input voltage at the given time
if time <= 0.126
    voltage = (0.01/0.125)*(time-0.001);
else
    voltage = 0.01 - (0.01/0.125)*(time-0.126);
end
end
clc;
%
% Calculate the MSE of the 2kHz test data
% Remove the first and last 10ms of data, whose
% voltage data lie in the
% cutoff region.
clear;
DATA_2kHz = readmatrix("TEST_2kHz.txt","OutputType ","double");
time = DATA_2kHz(:, 1);
truncated_data = DATA_2kHz(find(time>=0.01,1):find(time>=0.240,1),1:2);
```
% Renew the time axis
time = truncated_data(:, 1);
% Generate the input voltage
input_ref = zeros(length(time), 1);
for i = 1:length(time)
    input_ref(i) = INPUT_SIG_EMULATOR(time(i));
end
% Normalize the output and input
norm_output = normalize(truncated_data(:, 2));
norm_input = normalize(input_ref(:));
% Calculate the MSE of voltage values within the time span
% [0.01, 0.240]s
err_2kHz = immse(norm_input, norm_output);
disp('2kHz Test: The MSE between the normalised input and output is:');
disp(err_2kHz);

% Calculate the MSE of the 8kHz test data
% Remove the first and last 10ms of data, whose voltage data lie in the cutoff region.
clear;
DATA_8kHz = readmatrix('TEST_8kHz.txt', 'OutputType', 'double');
time = DATA_8kHz(:, 1);
truncated_data = DATA_8kHz(find(time>=0.01, 1):find(time>=0.240, 1), 1:2);
% Renew the time axis
time = truncated_data(:, 1);
% Generate the input voltage
input_ref = zeros(length(time), 1);
for i = 1:length(time)
    input_ref(i) = INPUT_SIG_EMULATOR(time(i));
end
% Normalize the output and input
norm_output = normalize(truncated_data(:, 2));
norm_input = normalize(input_ref(:, :));
% Calculate the MSE of voltage values within the time span
% [0.01, 0.240]s
err_8kHz = immse(norm_input, norm_output);
disp("8kHz Test: The MSE between the normalised input and output is:");
disp(err_8kHz);

% Calculate the MSE of the 8kHz test data
% Remove the first and last 10ms of data, whose voltage data lie in the
cutoff region.
clear;
DATA_20kHz = readmatrix("TEST_20kHz.txt","OutputType","double");
time = DATA_20kHz(:, 1);
truncated_data = DATA_20kHz(find(time>=0.01,1):find(time>=0.240,1),1:2);
% Renew the time axis
time = truncated_data(:, 1);
% Generate the input voltage
input_ref = zeros(length(time),1);
for i = 1:length(time)
    input_ref(i) = INPUT_SIG_EMULATOR(time(i));
end
% Normalize the output and input
norm_output = normalize(truncated_data(:,2));
norm_input = normalize(input_ref(1:end));
% Calculate the MSE of voltage values within the time span
% [0.01, 0.240]s
err_20kHz = immse(norm_input, norm_output);
disp("20kHz Test: The MSE between the normalised input and output is:");
disp(err_20kHz);
Appendix B: Program Codes used in Analysis
Appendix C

Double-layer PCB Layout

This appendix demonstrates all layers of the single-layer PCB layout design. The pictures are of the front copper layer, the back copper layer, the front paste layer, the back paste layer, the front silkscreen layer, the back silkscreen layer and the edge cuts layer respectively.
Appendix D

Four-layer PCB Layout

This appendix demonstrates all layers of the four-layer PCB layout design. The pictures are of the front copper layer, the first inner copper layer, the second inner copper layer, the back copper layer, the front paste layer, the back paste layer, the front silkscreen layer, the back silkscreen layer and the edge cuts layer respectively.
Appendix E

Bill of Materials

Here demonstrates the bill of materials used in the PCB design.
## Appendix E: Bill of Materials

<table>
<thead>
<tr>
<th>Ref</th>
<th>Qty</th>
<th>Value</th>
<th>Cmp name</th>
<th>Footprint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1,</td>
<td>1</td>
<td>1u</td>
<td>CAP</td>
<td>Capacitor_THT:CP_Radial_D5.0mm_P2.00mm</td>
<td>Capacitor symbol for simulation only</td>
</tr>
<tr>
<td>C2,</td>
<td>2</td>
<td>47n</td>
<td>C</td>
<td>Capacitor_SMD:C_0603_1608Metric</td>
<td>Unpolarized capacitor</td>
</tr>
<tr>
<td>C3,</td>
<td>5</td>
<td>10u</td>
<td>CAP</td>
<td>Capacitor_THT:CP_Radial_D5.0mm_P2.00mm</td>
<td>Capacitor symbol for simulation only</td>
</tr>
<tr>
<td>J1,</td>
<td>1</td>
<td></td>
<td>Conn_01x04</td>
<td>Connector_PinSocket_1.27mm:PinSocket_1x04_P1.27mm_Vertical</td>
<td>Generic connector, single row, 01x04</td>
</tr>
<tr>
<td>R1, R3, R11, R20,</td>
<td>5</td>
<td>1k</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R4,</td>
<td>1</td>
<td>8.2k</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R5,</td>
<td>1</td>
<td>4.7k</td>
<td>R</td>
<td>Resistor_THT:Axial_DIN0204_L3.6mm_D1.6mm_P5.08mm_Horizontal</td>
<td>Resistor</td>
</tr>
<tr>
<td>R6, R7, R12, R14, R5,</td>
<td>5</td>
<td>3k</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R10, R12, R16, R24,</td>
<td>4</td>
<td>20k</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R16, R17, R20, R21,</td>
<td>4</td>
<td>200</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R18, R22,</td>
<td>2</td>
<td>47</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R3,</td>
<td>1</td>
<td>1M</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>R25,</td>
<td>1</td>
<td>2.2k</td>
<td>R</td>
<td>Resistor_SMD:R_0603_1608Metric</td>
<td>Resistor</td>
</tr>
<tr>
<td>U1, U2, U3, U4,</td>
<td>3</td>
<td>TSV772IYST</td>
<td>TSV772IYST</td>
<td>Dual rail-to-rail input high bandwidth 20 MHz low offset operational amplifiers, MiniSO-8</td>
<td></td>
</tr>
<tr>
<td>U5,</td>
<td>1</td>
<td>L7805</td>
<td>L7805 Package_TO_SOT:TO-220-3_Horizontal_TabUp</td>
<td>Positive 1.5A 35V Linear Regulator, Fixed Output 5V, TO-220</td>
<td></td>
</tr>
<tr>
<td>U6,</td>
<td>1</td>
<td>MC7905</td>
<td>MC7905 Package_TO_SOT:TO-220-3_Horizontal_TabUp</td>
<td>Negative 1.5A 35V Linear Regulator, Fixed Output -5V, TO-220</td>
<td></td>
</tr>
</tbody>
</table>

**Figure E.1:** Bill of materials.
This master thesis presents an analogue peak holder circuit design aimed at facilitating the non-invasive inspection of the ageing process in electric drives. The ageing process of electric drives is a crucial aspect that demands accurate monitoring to ensure their long-term performance and reliability.

The proposed peak holder circuit is specifically designed to detect fast and narrow-width pulses of ringing current present in the PWM drive current. By capturing and measuring the peak values of these pulses, the circuit provides valuable insights into the ageing characteristics of electric drives. Experimental results demonstrate the remarkable efficiency of the peak holder circuit in accurately detecting and quantifying the peak values of the ringing current pulses. The circuit exhibits a stable output swing within a specified effective input swing range, with low mean-squared error (MSE) values. This signifies a strong linear correlation between the input and output signals, enhancing the reliability of the ageing detection process.

The ability of the peak holder circuit to effectively detect and analyze the ageing process of electric drives offers numerous advantages. By focusing on peak detection, which captures the highest values of the ringing current, the circuit provides a more efficient and targeted approach to inspecting the ageing process. This enables engineers and maintenance personnel to gain crucial insights into the degradation and performance of electric drives, allowing for timely interventions and proactive maintenance.

Keywords: Electric Drives, Ageing Process, Pulse-Width Modulation, Ringing Current, Peak-Holder, Analogue Circuits.
Detta examensarbete presenterar en nyutvecklad kretslösning för toppvärdesdetektering hos elektriska drivsystem, med målet att underlätta icke-invasiv övervakning av åldrandesprocessen hos eldrivsystem. Åldrandet hos eldrivsystem är en avgörande faktor som kräver noggrann övervakning för att säkerställa deras långsiktiga prestanda och tillförlitlighet.

Den föreslagna kretsen för att detektera toppvärden är specifikt utformad för att detektera snabba och kortvariga ringningar i PWM-modulerade strömmar. Genom att mäta toppvärdena ger kretsen värdefull information om åldrandekaraktären hos eldrivsystemen.

Experimentella resultat visar på den enastående effektiviteten hos spetsdetekteringskretsen för att noggrant detektera och kvantifiera toppvärdena hos ringningarna i strömmen. Kretsen uppvisar en stabil utsignal inom ett specifiserat ingångsintervall, med låga medelkvadratiska felvärden (MSE). Detta indikerar en stark linjär korrelation mellan ingångs- och utgångssignalerna, vilket förbättrar tillförlitligheten hos åldersdetektionsprocessen.

Krestsens förmåga att effektivt detektera och analysera åldrandeprocessen hos eldrivsystem erbjuder flera fördelar. Genom att fokusera på toppvärdesdetektering, som fångar de högsta värdena av ringströmmen, ger kretsen ett mer effektivt och riktat tillvägagångssätt för att inspektera åldrandet. Det möjliggör för ingenjörer och underhållspersonal att få viktig information om nedbrytning och prestanda hos eldrivsystem, vilket möjliggör tidiga insatser och proaktivt underhåll.

**Keywords**: Elektriska drivsystem, Åldringsprocess, Pulsbreddsmodulering, Ringningar i strömmen, Toppvärdesdetektor, Analog krets.
Local Variables:
mode: Latex
TeX-master: t

The following command is used with glossaries-extra
\setabbreviationstyle{long-short}
The form of the entries in this file is \newacronym\label{acronym}{phrase}
or \newacronym\options\label{acronym}{phrase}
see "User Manual for glossaries.sty" for the details about the options, one example is shown below
\newacronym\longplural={Debugging Information Entities} {DIE} {DIE} {Debugging Information Entity}

\begin{itemize}
\item The following example also uses options
\newacronym\shortplural={OSes}, firstplural={operating systems (OSes)} {OS} {OS} {operating system}
\end{itemize}

\begin{itemize}
\item note the use of a non-breaking dash in long text for the following acronym
\newacronym{KTH}{KTH}{KTH Royal Institute of Technology}
\newacronym{MSE}{MSE}{mean-squared error}
\newacronym{ESR}{ESR}{equivalent series resistance}
\newacronym{SRF}{SRF}{self-resonant frequency}
\newacronym{PWM}{PWM}{pulse-width modulation}
\newacronym{RMS}{RMS}{root mean squared}
\newacronym{RSH}{RSH}{rotor slot harmonics}
\newacronym{ISI}{ISI}{isolation state indicator}
\newacronym{ITSC}{ITSC}{inter-turn short circuit}
\newacronym{EMI}{EMI}{electromagnetic interference}
\newacronym{FPGA}{FPGA}{Field-programmable gate array}
\newacronym{BJT}{BJT}{bipolar junction transistor}
\newacronym{op-amp}{op-amp}{operational amplifier}
\newacronym{IC}{IC}{integrated circuit}
\newacronym{PCB}{PCB}{printed circuit board}
\newacronym{ADS}{ADS}{Advanced Design System}
\newacronym{DC}{DC}{direct current}
\newacronym{AC}{AC}{alternating current}
\newacronym{CMOS}{CMOS}{complementary metal-oxide-semiconductor}
\newacronym{VHDL}{VHDL}{Very High-Speed Integrated Circuit Hardware Description Language}