On Power-system Benefits, Main-circuit Design, and Control of StatComs with Energy Storage

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Preface

The work presented in this thesis was carried out at the Division of Electrical Machines and Power Electronics, School of Electrical Engineering, Royal Institute of Technology (KTH). The first part of this project was financed from the Competence Center in Electric Power Engineering (EKC$^2$) at KTH. The second part is financed from the ELEKTRA research program, which is administered by ELFORSK AB, SE-101 53 Stockholm, Sweden.

The main contributions of this work are:

- A novel flux modulation scheme combined with a deadbeat current control strategy has been developed for two-level voltage source converters (VSC). Both the positive and negative sequence components of the converter current and bus voltage can be controlled (Paper VII). A comparison between flux modulation and conventional voltage modulation has been made regarding the saturation problem of the transformers connected at the same bus as the VSC. The result shows that utilization of flux modulation tends to mitigate the saturation problem (Paper II).

- Effective active power compensation schemes have been proposed for improvement of the power quality at the point of common coupling (PCC) in power systems and for performance enhancement of certain phase sensitive applications (Paper VI). It has been shown that a static synchronous compensator (StatCom) with energy storage (ES) can significantly reduce phase jumps and magnitude deviations of the bus voltage under load disturbances (Paper I).
The impact of energy storage on the performance of a heavily loaded radial transmission system under fault conditions has been investigated. The results show that for a weak system with induction motor loads, a StatCom with certain energy storage capacity will effectively help with the fault recovery of the system (Paper V).

The possible use of a StatCom with ES to improve the power quality at the PCC of a system with cyclic loads has been studied (Paper IV).

A thyristor converter topology has been proposed as the interface between an ES and the dc link of a VSC. With the proposed interface, the VSC can operate at a constant dc-side voltage. It has been shown that the rating and cost of the VSC can be reduced using the proposed interface topology (Paper III).

A cost estimation for systems with the proposed interface topology has been performed, showing potential cost savings by utilization of the proposed interface topology. A cost comparison between different types of ES (capacitors, supercapacitors, and batteries) has been made, providing a guideline for the choice of ES in this kind of applications (Paper VIII).

The dynamics of the proposed system have been investigated. Control strategies are proposed and compared (Paper IX), (Paper X).

The study has resulted in the following publications:


VIII Hailian Xie, Lennart Ångquist and Hans-Peter Nee, ”Design Study of a Converter Interface Interconnecting an Energy Storage with the dc-link of a VSC,” submitted to IEEE Transactions on Industrial Electronics.

IX Hailian Xie, Lennart Ångquist and Hans-Peter Nee, ”Design and Analysis of a Controller for a Converter Interface Interconnecting an Energy Storage with the dc Link of a VSC,” submitted to IEEE Transactions on Power Systems.

X Hailian Xie, Lennart Ångquist and Hans-Peter Nee, ”Investigation of the control of a Converter Topology Interfacing an Energy Storage with the dc-link of a VSC,” to be published in Proceedings of EPE
2009, the 13th International European Power Electronics Conference and Exhibition.

Abstract

Static synchronous compensation (StatCom) is an application that utilizes a voltage source converter (VSC) to provide instantaneous reactive power support to the connected power system. Conventionally, StatComs are employed for reactive power support only. However, with the integration of energy storage (ES) into a StatCom, it can provide active power support in addition to the reactive power support. This thesis deals with the integration of ES into StatComs. The investigation involves the following aspects: possible benefits for power systems, main circuit design, and control strategies.

As the basis of the investigation, a control scheme is proposed for two-level VSCs. It is a novel flux modulation scheme combined with the well-known deadbeat current control. The current controller is capable of controlling the positive sequence, the negative sequence, and the offset components of the converter current. With flux modulation, all the three above-mentioned components of the bus flux are controllable. This differs from the conventional voltage modulation scheme, in which only the positive and negative sequence components of the bus voltage are controllable. The difference between the proposed flux modulation scheme and the voltage modulation scheme is investigated regarding saturation of transformers in the connected system during fault recovery. The investigation shows that by controlling the offset component of the bus flux, the transformer saturation problem can be mitigated to a certain extent.

The possible benefits of the additional active power support of StatComs are investigated through several case studies. Different active power compensation schemes are proposed. First, active power compensation for sudden load changes in weak systems is investigated. The proposed
control strategies are verified through computer simulations and through experiments in a real-time simulator. It is shown that with active power compensation, both the phase jumps and magnitude variations in the voltage at the PCC can be reduced significantly. Secondly, the power compensation of cyclic loads is investigated. The results show that the power quality at the connection point can be improved regarding both phase jumps and magnitude variations. In the third case study, the fault-recovery performance of an example system is investigated, showing that improved performance can be achieved by the additional active power support.

ES devices such as capacitors, supercapacitors, and batteries exhibit considerable variation in the terminal voltage during a charging/discharging cycle. A direct connection of ES devices to the dc side of a VSC requires a higher voltage rating of the VSC. Thus, the cost of the VSC has to be increased. In this thesis, a dual thyristor converter topology is proposed to interface ES devices with the dc side of the VSC. First, a cost comparison is performed to compare the total cost of the whole system with and without the proposed interface topology. A cost comparison between various types of ES is also presented, providing a guideline for the choice of ES at energy levels where several alternatives exist. Then, the dynamics of systems with the proposed interface topology are investigated. Control strategies are proposed and verified by computer simulations. Two different control methods for the dual-thyristor converter are compared.

Keywords

- Energy storage
- Voltage source converter
- VSC
- Static synchronous compensation
- StatCom
• Active power compensation
• Phase jump
• Voltage dip
• Weak network
• Flux modulation
• Deadbeat current control
• Transformer saturation
• Dual thyristor converter
• dc interface
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1 Introduction

1.1 Background

Electrical power is often generated in remote areas and has to be transmitted to end users through transmission and distribution systems. During the transmission, a certain part of the electrical power will be lost. Moreover, transmission of electrical power through overhead lines consumes a certain amount of reactive power, and transmission of the reactive power further increases the power losses. In order to reduce the transmission of reactive power, it should be generated locally. Various reactive power compensation technologies have been in use. Generically, these technologies are termed as flexible ac transmission systems (FACTS). By providing fast reactive power compensation, FACTS devices can help to enhance the stability and reliability of an existing transmission system, improve the power quality, and increase the transmission capacity. Compared to building new transmission lines, utilization of FACTS devices is an effective solution to increase transmission capacity with a low cost and a short project delivery time.

There are two technologies in the FACTS family: series compensation and shunt compensation. Normally, fixed capacitors are used in series compensation. The effect of series compensation is that the transmission distance is shortened electrically. Later, thyristor-controlled series compensator (TCSC) have been developed for certain applications. Thyristor-based shunt compensation technology - static var compensation (SVC) - has been around since the 1970’s. It can be implemented as a thyristor-switched capacitor (TSC) or as a thyristor-controlled reactor (TCR).

With the advance of semiconductor technology, insulated gate bipolar tran-
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Sistor (IGBT) based technology has come into application. Voltage source converters (VSC) are utilized both in series - static synchronous series compensation (SSSC) - and in shunt - static synchronous compensation (StatCom).

Conventionally, a StatCom is utilized for reactive power compensation only, either in a transmission system or in a distribution system. StatComs are also used to compensate for certain specific loads, such as arc furnaces. By providing instantaneous reactive power support, the voltage at the connecting point can be maintained at a desired level even when the network or load conditions vary. Therefore, improved power quality, enhanced system stability, and increased power transfer capacity can be achieved.

A StatCom provides power support by producing a three-phase voltage \( u_v \) at the VSC terminal. The magnitude and the phase angle of the generated voltage are both controllable. The magnitude and the phase angle of the produced voltage relative to the voltage at the point of common coupling (PCC) determine the power flow between the VSC and the PCC. This can be illustrated by a simplified system as shown in Fig. 1.1, in which only a StatCom is connected to the PCC. The possible power flow patterns between the PCC and the VSC are illustrated by the phasor diagrams in Fig. 1.2.

By producing a voltage with a magnitude higher than that of the voltage \( u_{PCC} \) at the PCC, the VSC provides reactive power to the power system, as shown in Fig. 1.2(a). As a result, the voltage level at the PCC will be raised (higher than \( u_{inf} \)). If instead the magnitude of \( u_v \) is lower than that of \( u_{PCC} \) as shown in Fig. 1.2(b), the VSC absorbs reactive power from the PCC and consequently it will reduce the voltage level at the PCC (lower than \( u_{inf} \)).

The active power flow is determined by the relative phase shift between \( u_v \) and \( u_{PCC} \). If \( u_v \) is leading \( u_{PCC} \) as in Fig. 1.2(c), the VSC provides active power to the PCC. Otherwise if \( u_v \) is lagging as in Fig. 1.2(d), the VSC draws active power from the PCC.

During normal operation of a conventional StatCom, the power exchange between the VSC and the network is mainly reactive, although there is also a small amount of active power exchange to cover the losses in the converter and to keep the dc-side voltage constant. If the StatCom is installed solely
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for reactive power support, the dc-side capacitor of the VSC is usually dimensioned with a time constant of 10 ms to 15 ms. The time constant of the capacitor is defined as the ratio of the stored electrostatic energy to the rated power of the StatCom. With this capacitor size, there cannot be any significant active power exchange. However, if energy storage (ES) devices are connected on the dc side of the VSC, the StatCom is capable of providing active power as well as reactive power support. The possible benefit of the additional active power support can be power oscillation damping capability, improved power quality, and enhanced system reliability, etc.
This project deals with StatComs with energy storage. The investigations include power system benefits, main-circuit design, and the control issues. The main objectives are summarized in the next section.

1.2 Project Objectives

- Develop proper control strategies for grid-connected VSCs.
- Investigate the possible benefits of integrating ES into a StatCom.
- Investigate interface topologies between an ES and the dc link of a VSC.

The investigations have been carried out through computer simulations with the power system simulation software PSCAD and partly through an analogue real-time simulator in the laboratory at the division of Electrical Machines and Power Electronics, Royal Institute of Technology (KTH). A brief description of the real-time simulator is provided in Appendix A.

1.3 Outline of the Thesis

Chapter 2 describes the converter control system, including the inner current control, the flux modulation scheme, and the outer power control loop.

Chapter 3 compares flux-based modulation with a voltage-based modulation scheme regrading transformer saturation.

Chapter 4 presents the possible benefits of the integration of ES into a StatCom.
Chapter 5 investigates a converter topology interfacing an ES with the dc link of a VSC. A cost estimation is presented and the dynamics of the system are investigated.

Chapter 6 concludes the investigations.

Chapter 7 gives suggestions for future work.
2 Converter Control

When a VSC is connected to a grid as a StatCom without energy storage, the power flow between the converter and the grid should be controlled such that the voltage at the connection point is maintained at a certain level and at the same time the converter dc-side voltage is kept at a reasonable and relatively constant value to ensure a successful converter operation. The power control of a three-phase pulse-width modulated (PWM) converter can be achieved either with or without an inner current control loop. Power control without the inner current control loop is usually called direct power control (DPC) [1]. However, current control has been broadly applied in the control of three-phase PWM VSCs due to its capability to provide fast and accurate converter output control as well as peak current protection. Among all the current control strategies, deadbeat control is one of the most effective ones and is widely used. Therefore, an inner current deadbeat control loop is employed in the converter control in this project. In addition, a novel flux modulation scheme is utilized for the control of the switching actions of the converter bridge. This chapter provides a detailed description of the flux modulation scheme combined with deadbeat current control and the power control of voltage source converters.

2.1 Overview of the Converter Control System

Fig. 2.1 shows the converter control system, which consists of an outer voltage control loop and an inner deadbeat current control loop. The VSC is connected to the PCC through a transformer and phase reactors, which have an inductance $L_v$ and a resistance $R_v$. The bus flux is measured and resolved into a positive sequence, a negative sequence, and an offset component using
the low-pass filter method described in [2], with a phase-locked loop (PLL) operating on the positive sequence component. The zero-sequence component is ignored in the study as the systems investigated are three-phase three-wire systems. The PLL operates in such a way that the d axis aligns with the bus flux vector in the rotating dq plane. The converter current is also separated into the same three components using the angle from the PLL. A brief description of the sequence separation method and the PLL are provided in Appendix B.

The deadbeat current control loop calculates the flux change for next sampling interval that is required to obtain the desired current. In calculation of the flux change, the bus flux with all components is used as a feed-forward signal. Then, the flux-modulator block generates the switching patterns that deliver the required flux change in the upcoming sampling interval. The inner current control is implemented in the rotating dq reference frame (defined by the PLL). As all the controlled current components are dc quantities at steady state, there will be no steady-state tracking errors.

The references for the converter current components are given by the outer control loop, where the dc-side voltage of the converter and the flux at the PCC (referred to as the bus flux) are controlled.

A detailed description of the inner and outer control loops will be given in the following sections.

2.2 Inner Loop - Flux Modulation and Deadbeat Current Control

The essence of deadbeat control is to control the converter current to follow the reference value with one sampling period delay disregarding the computational delay introduced by the digital control system. This control technique has been extensively investigated [3–6], with the current vector oriented with respect to the line voltage vector.
Conventionally, the current vector is oriented with respect to the network voltage vector and the PWM system works with the converter reference voltages. However, by considering the utility grid as a virtual electrical machine, the current vector can be oriented with respect to the virtual flux of the grid, which is constructed by integrating the grid voltage [7]. The original idea to control the machine flux directly in order to control the torque (or power) was first presented by Depenbrock in 1985 [8, 9]. Later Takahashi and Ohmori presented a modified version [10], in which the preferred flux path was a circle instead of the hexagon used in [8]. Both of these methods were based on hysteresis control. The virtual flux concept has also been reported in other works. A current control scheme based on virtual-flux orientation was proposed in [1], in which the estimated virtual flux vector provided the angle used in the coordinate transformation by both the line current and the reference voltage for the converter. The Direct Power Control method uses the estimated virtual flux to estimate instantaneous power flow in the system [11]. In [12], the converter virtual
flux magnitude is controlled, which, together with the angular difference between the virtual fluxes of the grid and the converter, determines the switching state of the converter by using a look-up table. A flux modulation approach is proposed in [13], which examines the movement of the converter flux and selects the corresponding switch action according to a set of switching rules. Another flux vector modulation strategy proposed in [14] takes the desired motor stator flux vector as reference and calculates the switching times such that the output flux vector can follow the reference.

In this project, a new control scheme combining flux modulation and deadbeat current control has been developed. Additionally, the current controller is capable of controlling positive and negative sequence current components as well as offset. The flux of the grid is obtained by numerical integration of the measured voltage or by directly measuring the output signal from a (passive) low-pass filter driven by the measured bus-voltage signal. The VSC is controlled to generate the virtual flux needed to drive the desired current flowing between the converter and the grid.

### 2.2.1 The Converter Virtual Flux

For a two-level voltage source converter shown in Fig. 2.2, the coupling function associated with phase $x$ ($x$ represents a, b and c when phase quantities are concerned throughout this work) can be defined as

\[
K_x = 0 \text{ when terminal } x \text{ is connected to the lower dc rail}
\]

\[
K_x = 1 \text{ when terminal } x \text{ is connected to the upper dc rail}
\]
With this definition, the alternating voltage generated by the converter can be described as a space vector in the $\alpha\beta$ plane:

$$\bar{u}^{\alpha\beta}_v(t) = \frac{2}{3} \left\{ K_a(t) + e^{j\frac{2\pi}{3}} K_b(t) + e^{-j\frac{2\pi}{3}} K_c(t) \right\} u_d \quad (2.1)$$

All the quantities used in the equation and the equations hereafter are in physical units unless otherwise stated.

It is obvious that the voltage vector adopts one of the seven different values corresponding to eight different combinations of the coupling functions $K_a$, $K_b$, and $K_c$ (both 111 and 000 give a zero vector).

The converter virtual flux is defined by

$$\frac{d\bar{\psi}^{\alpha\beta}_v(t)}{dt} = \bar{u}^{\alpha\beta}_v(t) = \frac{2}{3} \left\{ K_a(t) + e^{j\frac{2\pi}{3}} K_b(t) + e^{-j\frac{2\pi}{3}} K_c(t) \right\} u_d \quad (2.2)$$

Integrating (2.2) during one switching period $<t_k, t_{k+1}>$ yields

$$\Delta \bar{\psi}^{\alpha\beta}_v,_{k} = \bar{\psi}^{\alpha\beta}_v(t_{k+1}) - \bar{\psi}^{\alpha\beta}_v(t_k) = \frac{2}{3} \int_{t_k}^{t_{k+1}} \left\{ K_a(t) + e^{j\frac{2\pi}{3}} K_b(t) + e^{-j\frac{2\pi}{3}} K_c(t) \right\} u_d dt \quad (2.3)$$

This means that the switching state can be determined by the flux change during one sampling interval.

In the $\alpha\beta$ plane, tracing of the converter voltage vector always results in seven dots as shown in Fig. 2.3. On the other hand, the converter virtual flux, ideally, moves along a circle with a number of steps depending on the switching frequency. The higher the switching frequency, the closer the locus resembles a circle.

In the next section, the current control, which gives the reference value of the converter flux change, will be described.
2 Converter Control

2.2.2 Deadbeat Current Control

The converter is assumed to be connected to the PCC in the grid via phase inductors with certain inductance $L_v$ and resistance $R_v$, as shown in Fig. 2.1. This point is referred to as the ‘bus-bar’ in this work and the virtual bus-bar flux $\bar{\psi}_B$ represents the grid flux.

The bus-bar flux can be represented by a space vector with a positive sequence component and a negative sequence component of the fundamental component, and an offset component, i.e., it has the following form

\[
\bar{\psi}^{\alpha\beta}_B(t) = \bar{\psi}^{\alpha\beta}_{B,ofs} + \bar{\psi}^{dq}_{B,p} e^{j\theta(t)} + \bar{\psi}^{dq\ast}_{B,n} e^{-j\theta(t)}
\]

\[
\dot{\theta}(t) = \omega(t) \quad (2.4)
\]

Equation (2.4) also shows that the concept of positive and negative sequence components inherently relies on the existence of a time function, $\theta(t)$, which defines a coordinate system that rotates with the speed of the fundamental frequency ($\omega$) component. A Phase-Locked-Loop (PLL) operating on the positive sequence component of the bus-bar flux is utilized to provide such a coordinate system reference.

The current controller operates with a fixed sampling interval $T_s$, corresponding to twice the frequency $f_{tri}$ of the triangular wave used in the
"carrier-based" PWM modulation scheme.

\[ T_s = \frac{1}{2f_{tri}} \]  

(2.5)

The target for the current controller is to control the positive and negative sequence components of the fundamental frequency component of the converter current, plus the offset component of the converter current. This means that the current reference has the following form

\[ \bar{i}_{v,ref}^{\alpha \beta} (t) = \bar{i}_{v,o,ref}^{\alpha \beta} + \bar{i}_{v,p,ref}^{dq} e^{j\theta(t)} + \bar{i}_{v,n,ref}^{dq*} e^{-j\theta(t)} \]  

(2.6)

The deadbeat current control in the virtual flux modulation system was based on the strategy described in detail in [3]. In deducing the control algorithm it is assumed that the desired flux change in the preceding sampling interval has been delivered. Accordingly, the desired converter current will be obtained at the end of the preceding sampling interval. This means that the essence of the dead-beat control is to calculate the estimated converter flux change for interval \( < t_k, t_{k+1} > \) such that no additional error will be created.

With the indicated current direction the following formula applies

\[ \bar{\psi}_{v,ref}^{\alpha \beta} (t) = \bar{\psi}_{v,ref}^{\alpha \beta} (t) + x_v \bar{i}_{v,ref}^{\alpha \beta} (t) + R_v \int_{-\infty}^{t} \bar{i}_{v,ref}^{\alpha \beta} (\xi) d\xi \]  

(2.7)

where \( x_v \) is the reactance of the phase reactors. It can be seen that when (2.7) is transformed into the dq reference frame, there is no cross-coupling between the d and q components associated with \( x_v \). Although these two components are still coupled through \( R_v \), which is usually one order of magnitude smaller than \( x_v \), the cross-coupling effect is significantly reduced.

The flux change during one switching period \( < t_k, t_{k+1} > \) is easily estimated by calculating the difference between the fluxes at the start and the end of the interval:

\[ \Delta \hat{\psi}_{v}^{\alpha \beta} (k) = \Delta \hat{\psi}_{v,ref}^{\alpha \beta} (k) + x_v \Delta \bar{i}_{v,ref}^{\alpha \beta} (k) + R_v \int_{t_k}^{t_{k+1}} \hat{i}_{v,ref}^{\alpha \beta} (\xi) d\xi \]  

(2.8)

where the symbols with the ‘hat’ indicator on top, e.g. \( \Delta \hat{\psi}_{v}^{\alpha \beta} \), denote the estimated values.
The three terms on the right-hand side of (2.8) are easily identified as:

- The flux change necessary to balance the bus-bar flux change.
- The flux change necessary to obtain the desired current at $t_{k+1}$.
- The flux change necessary to compensate for the resistive voltage drop.

To eliminate the steady-state current errors, a PI controller is employed. This gives the fourth term of the converter flux change:

- Corrective flux change provided by the current controller.

Due to the computational time needed by any digital control system, the flux change in the interval $< t_k, t_{k+1} >$ will be calculated using the current reference values and other measured values available up to the time instant $t_{k-1}$.

At the sampling instant $t_{k-1}$, the vectors in (2.8) can be obtained together with the measured converter current and the actual value of the coordinate system angle and frequency. These values at $t = t_{k-1}$ are denoted $\vec{I}_{v,ofs,ref,k-1}$, $\vec{I}_{v,p,ref,k-1}$, $\vec{I}_{v,n,ref,k-1}$, $\vec{\psi}_{B,ofs,k-1}$, $\vec{\psi}_{B,p,k-1}$, $\vec{\psi}_{B,n,k-1}$, $\vec{i}_{v,k-1}$, $\theta_{k-1}$, and $\omega_{k-1}$.

The four terms of the converter flux change can be calculated respectively as shown below.

### 2.2.2.1 Required Flux Change to Balance the Bus-bar Flux Change

At the time instant $t_{k-1}$ the bus-bar flux vectors $\vec{\psi}_{B,ofs,k-1}$, $\vec{\psi}_{B,p,k-1}$, $\vec{\psi}_{B,n,k-1}$, the coordinate system angle $\theta_{k-1}$ and the frequency $\omega_{k-1}$ are known. Then, it is possible to estimate the flux at the start and the end of
the sampling interval \(< t_k, t_{k+1} >\) as

\[
\hat{\theta}_{k|k-1} = \theta_{k-1} + T_s \omega_{k-1}
\]

\[
\hat{\psi}^{\alpha\beta}_{B,k|k-1} = \hat{\psi}^{\alpha\beta}_{B,ofs,k-1} + \hat{\psi}^{dq}_{B,p,k-1} e^{j\hat{\theta}_{k|k-1}} + \hat{\psi}^{dq*}_{B,n,k-1} e^{-j\hat{\theta}_{k|k-1}}
\] (2.9)

and

\[
\hat{\theta}_{k+1|k-1} = \theta_{k-1} + 2T_s \omega_{k-1}
\]

\[
\hat{\psi}^{\alpha\beta}_{B,k+1|k-1} = \hat{\psi}^{\alpha\beta}_{B,ofs,k-1} + \hat{\psi}^{dq}_{B,p,k-1} e^{j\hat{\theta}_{k+1|k-1}} + \hat{\psi}^{dq*}_{B,n,k-1} e^{-j\hat{\theta}_{k+1|k-1}}
\] (2.10)

where the estimated values with double subscripts, e.g. \(\hat{\psi}^{\alpha\beta}_{B,k+1|k-1}\), denote estimations of the values of the complex vector \(\hat{\psi}^{\alpha\beta}_{B}\) at time \(t_{k+1}\) based on the information available at time \(t_{k-1}\).

Thus, the required flux change to balance the bus-bar flux change is:

\[
\Delta \hat{\psi}^{\alpha\beta}_{B,k|k-1} = \hat{\psi}^{\alpha\beta}_{B,k+1|k-1} - \hat{\psi}^{\alpha\beta}_{B,k|k-1}
\] (2.11)

### 2.2.2.2 Required Flux Change to Drive Converter Current through the Phase Inductor

It is assumed that the phase inductor reactance is \(x_v\). At the time instant \(t_{k-1}\) the current references are given in the rotating coordinate system as \(\tilde{i}^{\alpha\beta}_{v,ofs,ref,k-1}\), \(\tilde{i}^{dq}_{v,p,ref,k-1}\), \(\tilde{i}^{dq*}_{v,n,ref,k-1}\). Due to the one-sample control delay and one-sample computational delay in a digital control system, a successful deadbeat control ensures that the current follows the reference value with a two-sample delay. Hence, the desired currents at the instants \(t_k\) and \(t_{k+1}\) are estimated based on the current references at the instants \(t_{k-2}\) and \(t_{k-1}\). Accordingly,

\[
\hat{\tilde{i}}^{\alpha\beta}_{v,k|k-2} = \hat{\tilde{i}}^{\alpha\beta}_{v,ofs,ref,k-1} + \hat{\tilde{i}}^{dq}_{v,p,ref,k-2} e^{j\hat{\theta}_{k|k-2}} + \hat{\tilde{i}}^{dq*}_{v,n,ref,k-2} e^{-j\hat{\theta}_{k|k-2}}
\]

\[
\hat{\tilde{i}}^{\alpha\beta}_{v,k+1|k-1} = \hat{\tilde{i}}^{\alpha\beta}_{v,ofs,ref,k-1} + \hat{\tilde{i}}^{dq}_{v,p,ref,k-1} e^{j\hat{\theta}_{k+1|k-1}} + \hat{\tilde{i}}^{dq*}_{v,n,ref,k-1} e^{-j\hat{\theta}_{k+1|k-1}}
\] (2.12)
where $\hat{\theta}_{k|k-2} = \theta_{k-2} + 2T_s \omega_{k-2}$.

The converter flux contribution required to force the desired current at time instant $t_{k+1}$ is given by

$$\hat{\psi}_{Iref,k+1|k-1} = x_v \hat{i}_{v,k+1|k-1}$$  \hspace{1cm} (2.13)

Therefore, the estimated flux change is given by

$$\Delta \hat{\psi}_{Iref,k|k-1} = x_v \left[ \hat{z}_{\alpha\beta} - \hat{i}_{v,k|k-2} \right]$$  \hspace{1cm} (2.14)

### 2.2.2.3 Required Flux Change to Cover Resistive Voltage Drop

The resistive voltage drop causes a loss of flux as given by the following expression

$$\bar{\psi}_{IR}(t) = \int_{-\infty}^{t} R_v \bar{i}_{\alpha\beta}(\xi) d\xi$$  \hspace{1cm} (2.15)

Thus, the corresponding estimated flux change in the interval $< t_k, t_{k+1} >$ is given by

$$\Delta \hat{\psi}_{IR,k|k-1} = R_v \int_{t_k}^{t_{k+1}} \hat{i}_{v,\alpha\beta}(\xi) d\xi$$

$$= \frac{R_v T_s}{2} \left[ \hat{z}_{\alpha\beta} + \hat{i}_{v,k|k-2} \right]$$  \hspace{1cm} (2.16)

### 2.2.2.4 Corrective Flux Change Given by the Current Controller

At the instant $t_{k-1}$ the converter current $\bar{i}_{v,k-1}$ is measured and resolved into a dc offset, a positive sequence, and a negative sequence components; and the positive and the negative sequence components are further resolved into current components in the rotating coordinate systems. These components are: $\tilde{I}_{v,ofs,k-1}$, $\tilde{I}_{v,p,k-1}$, $\tilde{I}_{v,n,k-1}$. Because of the two-sample delay, the obtained converter current components at the instant $t_{k-1}$ are compared with
the reference components from time instant $t_{k-3}$.

\[
\begin{align*}
\Delta \tilde{I}_{v,p,k-1}^{dq} &= \tilde{I}_{v,p,ref,k-3}^{dq} - \tilde{I}_{v,p,k-1}^{dq} \\
\Delta \tilde{I}_{v,n,k-1}^{dq*} &= \tilde{I}_{v,n,ref,k-3}^{dq*} - \tilde{I}_{v,n,k-1}^{dq*} \\
\Delta \tilde{I}_{v,ofs,k-1}^{\alpha\beta} &= \tilde{I}_{v,ofs,ref,k-3}^{\alpha\beta} - \tilde{I}_{v,ofs,k-1}^{\alpha\beta}
\end{align*}
\] (2.17)

The current PI controllers operate according to

\[
\Delta \hat{\bar{i}}_{\text{reg},k+1|k-1}^{\alpha\beta} = \left( k_{p,ofs} \Delta \hat{\bar{i}}_{v,ofs,k-1}^{\alpha\beta} + \frac{T_s}{\tau_{ofs}} \sum_{m=0}^{k-1} \Delta \hat{\bar{i}}_{v,ofs,m}^{\alpha\beta} \right)
\]
\[+ \left( k_{p,p} \Delta \hat{\bar{i}}_{v,p,k-1}^{dq} + \frac{T_s}{\tau_{p}} \sum_{m=0}^{k-1} \Delta \hat{\bar{i}}_{v,p,m}^{dq} \right) e^{j\hat{\theta}_{k+1|k-1}}
\]
\[+ \left( k_{p,n} \Delta \hat{\bar{i}}_{v,n,k-1}^{dq*} + \frac{T_s}{\tau_{n}} \sum_{m=0}^{k-1} \Delta \hat{\bar{i}}_{v,n,m}^{dq*} \right) e^{-j\hat{\theta}_{k+1|k-1}}
\] (2.18)

This gives the corrective flux change:

\[
\Delta \hat{\psi}_{\text{reg},k-1}^{\alpha\beta} = x_v \Delta \hat{\bar{i}}_{\text{reg},k+1|k-1}^{\alpha\beta}
\] (2.19)

Then the total flux change required for the time interval $< t_k, t_{k+1} >$ is:

\[
\Delta \hat{\psi}_{k-1|k-1}^{\alpha\beta} = \Delta \hat{\psi}_{B,k-1|k-1}^{\alpha\beta} + \Delta \hat{\psi}_{I,k-1|k-1}^{\alpha\beta}
\] (2.20)

where

\[
\Delta \hat{\psi}_{I,k-1|k-1}^{\alpha\beta} = \Delta \hat{\psi}_{IR,k-1|k-1}^{\alpha\beta} + \Delta \hat{\psi}_{Iref,k-1|k-1}^{\alpha\beta} + \Delta \hat{\psi}_{Ireg,k-1|k-1}^{\alpha\beta}
\] (2.21)

In (2.20), and in the description hereafter, the subscript ‘$v$’ in the flux change of the VSC is omitted.

### 2.2.3 Flux Modulation

The modulation scheme takes the space vector of the converter flux change $\Delta \hat{\psi}_{k-1|k-1}^{\alpha\beta}$ as the input reference. The switching instants in the sampling interval $< t_k, t_{k+1} >$ that produce this desired change of the flux will be
The flux change in each phase can be obtained by transforming the flux-change vector into phase quantities according to (2.22):

\[
\begin{align*}
\Delta \hat{\psi}_{a,k|k-1} &= \text{Re}\left\{ \Delta \hat{\psi}_{k|k-1}^{\alpha\beta} \right\} \\
\Delta \hat{\psi}_{b,k|k-1} &= \text{Re}\left\{ \Delta \hat{\psi}_{k|k-1}^{\alpha\beta} e^{-j\frac{2\pi}{3}} \right\} \\
\Delta \hat{\psi}_{c,k|k-1} &= \text{Re}\left\{ \Delta \hat{\psi}_{k|k-1}^{\alpha\beta} e^{j\frac{2\pi}{3}} \right\}
\end{align*}
\]

With a certain dc side voltage \( u_d \), the flux change in phase \( x \) in the sampling interval \( < t_k, t_{k+1} > \) is related to the coupling function \( K_x \) by (2.23), from which the switching time can be calculated.

\[
\Delta \hat{\psi}_{x,k|k-1} = \int_{t_k}^{t_{k+1}} u_d K_x(t) \, dt
\]  

(2.23)

In the classical PWM modulation each of the three phases in the converter switches once in each sampling interval. Accordingly, all coupling functions are equal, alternating 000 and 111, at the start of each sampling interval. The formulas used to calculate the switching times should be developed respectively for the case switching from 000 to 111 and the case switching from 111 to 000, as shown in Fig. 2.4.

### 2.2.3.1 Switching from 000 to 111 in the Sampling Interval \( < t_k, t_{k+1} > \)

In this case the integral for phase \( x \) contributes to the flux component only from the switching instant to the end of the sampling interval.

\[
\begin{align*}
\Delta \hat{\psi}_{x,k} &= \int_{t_{x,k}}^{t_{k+1}} u_d K_x(t) \, dt \\
&= u_d \left( t_{k+1} - t_{x,k} \right)
\end{align*}
\]

(2.24)

The formal solution is given by

\[
t_{x,k} = t_{k+1} - \frac{\Delta \hat{\psi}_{x,k}}{u_d}
\]

(2.25)
2.2 Inner Loop - Flux Modulation and Deadbeat Current Control

This is a solution for the standard sub-oscillation PWM method, with which the maximum voltage vector that can be realized by the converter is limited to the circle with a radius of $\frac{1}{2} u_d$ as shown in Fig. 2.5.

A well-known method to increase the modulation index, called symmetrical sub-oscillation PWM, is to add a zero-sequence component to the
Figure 2.5: Converter voltage vector limit in standard sub-oscillation PWM method

Converter reference voltages (e.g., [3]). This method is also applicable in the case of flux modulation. If all switching actions are displaced by the same amount of time the active voltage pulse remains the same. Therefore, the displacement $\Delta t_0$ of the switching times can be arbitrarily selected, resulting in:

$$t_{x,k} = t_{k+1} + \Delta t_0 - \frac{\Delta \hat{\psi}_{x,k}}{u_d}$$

(2.26)

One option is to choose $\Delta t_0$ such that the midpoint of the active pulse occurs in the middle of the sampling interval, i.e. at $\frac{t_{k} + t_{k+1}}{2}$, as shown in Fig. 2.6(a). The active voltage pulse starts at the minimum of the three switching times, which is denoted $\min (t_{a,k}, t_{b,k}, t_{c,k})$; and it lasts to the maximum of the switching times, $\max (t_{a,k}, t_{b,k}, t_{c,k})$. Hence,

$$\frac{t_{k} + t_{k+1}}{2} = t_{k+1} + \Delta t_0 - \frac{\min x (\Delta \hat{\psi}_{x,k}) + \max x (\Delta \hat{\psi}_{x,k})}{2u_d}$$

(2.27)

Solving for $t_{k+1} + \Delta t_0$ yields

$$t_{k+1} + \Delta t_0 = \frac{t_{k} + t_{k+1}}{2} + \frac{\min x (\Delta \hat{\psi}_{x,k}) + \max x (\Delta \hat{\psi}_{x,k})}{2u_d}$$

(2.28)
Finally, the switching time for each phase $x$ is given by

$$t_{x,k} = \frac{t_k + t_{k+1}}{2} + \frac{\min x \left( \Delta \hat{\psi}_{x,k} \right) + \max x \left( \Delta \hat{\psi}_{x,k} \right) - 2 \Delta \hat{\psi}_{x,k}}{2u_d} \quad (2.29)$$

### 2.2.3.2 Switching from 111 to 000 in the Sampling Interval $< t_k, t_{k+1} >$

In this case the integral for phase $x$ contributes to the flux component only from the start of the sampling interval to the switching instant.

$$\Delta \hat{\psi}_{x,k} = \int_{t_k}^{t_{x,k}} u_d K_x(t)\,dt$$

$$= u_d (t_{x,k} - t_k) \quad (2.30)$$

The formal solution is

$$t_{x,k} = t_k + \frac{\Delta \hat{\psi}_{x,k}}{u_d} \quad (2.31)$$

As in the case when switching from 000 to 111, the symmetrical sub-oscillation PWM method is used. Thus, all the switching times are displaced by $\Delta t_0$ such that the midpoint of the active pulse occurs in the middle of the sampling interval, i.e. at $\frac{t_k + t_{k+1}}{2}$. Accordingly,

$$t_{x,k} = t_k + \Delta t_0 + \frac{\Delta \hat{\psi}_{x,k}}{u_d} \quad (2.32)$$

The active voltage pulse starts at $\min (t_{a,k}, t_{b,k}, t_{c,k})$ and it lasts to $\max (t_{a,k}, t_{b,k}, t_{c,k})$, which means:

$$\frac{t_k + t_{k+1}}{2} = t_k + \Delta t_0 + \frac{\min x \left( \Delta \hat{\psi}_{x,k} \right) + \max x \left( \Delta \hat{\psi}_{x,k} \right)}{2u_d} \quad (2.33)$$

Solving for $t_k + \Delta t_0$ yields

$$t_k + \Delta t_0 = \frac{t_k + t_{k+1}}{2} - \frac{\min x \left( \Delta \hat{\psi}_{x,k} \right) + \max x \left( \Delta \hat{\psi}_{x,k} \right)}{2u_d} \quad (2.34)$$

Finally, the switching time formulas are obtained as

$$t_{x,k} = \frac{t_k + t_{k+1}}{2} - \frac{\min x \left( \Delta \hat{\psi}_{x,k} \right) + \max x \left( \Delta \hat{\psi}_{x,k} \right) - 2 \Delta \hat{\psi}_{x,k}}{2u_d} \quad (2.35)$$
Figure 2.6: Modified flux change during one switching period

(a) switching from 000 to 111

(b) switching from 111 to 000
2.2.4 Limitation of the Flux Change

With a certain dc-side voltage, the flux-change vector in the $\alpha\beta$ reference frame during each switching period is confined in a hexagon with the side length $\frac{2}{3}u_d T_s$, as shown in Fig. 2.7. However, during transients, the reference of the flux change delivered by the inner current control loop might exceed the flux-change hexagon, which is usually referred to as saturation or over-voltage of the modulation. When saturation occurs, on the one hand the integration of the current PI controller should be stopped in order to avoid wind-up of the integrator. On the other hand, the reference of the flux change should be limited according to the instantaneous dc-side voltage. A limitation method called Minimum Amplitude Error Limit method as proposed in [4] is adopted for limitation of saturated flux modulation reference. By this limitation method, the reference for the flux-change vector exceeding the hexagon is replaced with a vector on the hexagon boundary that is closest to the reference and has the minimum amplitude error, as shown in Fig 2.7.
### Table 2.1: Specifications for the Simulation System

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>8 VA</td>
</tr>
<tr>
<td>Rated current</td>
<td>0.267 A; rms</td>
</tr>
<tr>
<td>Grid voltage</td>
<td>$10\sqrt{3}$ V; line-to-line, rms</td>
</tr>
<tr>
<td>Line impedance</td>
<td>0; e.g. a strong network; for the step response simulation</td>
</tr>
<tr>
<td></td>
<td>72 mH (0.5pu); for the unsymmetrical load simulation</td>
</tr>
<tr>
<td>Phase reactor</td>
<td>17.9 mH (0.15pu)</td>
</tr>
<tr>
<td>Dc side capacitor</td>
<td>345 µF (<a href="mailto:0.2J@33.9V">0.2J@33.9V</a>)</td>
</tr>
<tr>
<td>Dc-side voltage (controlled)</td>
<td>33.9 V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>1350 Hz (‘triangular frequency’)</td>
</tr>
</tbody>
</table>

#### 2.2.5 Simulation and Experimental Result

In this section, results from both computer simulations and the real-time simulator will be presented to verify the validity of the deadbeat current control and the flux modulation system. The computer simulations were carried out by means of the power system simulation software PSCAD. The system parameters used in PSCAD and in the real-time simulator were identical and are listed in Table 2.1.

Fig. 2.8 and Fig. 2.9 depict the step response of the reactive current, from computer simulations and the real-time simulator respectively. The figures show a successful deadbeat control, where the reactive current follows the reference value with a two-sample delay (0.74 ms). It also can be seen that the active current was almost unaffected by the step change in the reactive current.

Fig. 2.10 and 2.11 show the converter flux response to the reactive current step change, from the simulation and the real-time simulator respectively. When the converter is commanded to provide reactive power to the network, it generates a flux with a larger magnitude.
2.2 Inner Loop - Flux Modulation and Deadbeat Current Control

Figure 2.8: Simulated step response of the reactive current

Figure 2.9: Measured step response of the reactive current
2 Converter Control

Figure 2.10: Simulated converter flux response to a step change in the reactive current

Figure 2.11: Measured converter flux response to a step change in the reactive current
2.3 Outer Loop - Power Control of Voltage Source Converters

The converter response to an unsymmetrical load condition (only phase A and phase B are loaded) has also been investigated. In this case, a relatively weak network is assumed with a line impedance of 72 mH (0.5 pu). When the control system detects the negative sequence component of the bus voltage caused by the unsymmetrical load, it commands the converter to produce flux with negative sequence, as shown by the elliptic flux loci in Fig. 2.12 and Fig. 2.13, which are recorded from the simulation and the real-time simulator respectively. In these figures, the circular flux loci under normal operation conditions are also plotted with dashed lines as a comparison. The three-phase converter current and line current recorded from the PSCAD simulation are depicted Fig. 2.16. The converter provides a negative sequence current to symmetrize the unbalanced load. As a result, the line current (current drawn from the source) is well balanced. With the help of the VSC, the bus voltage is kept balanced even under extremely unbalanced load conditions, which can be seen from Fig. 2.14 (simulated) and 2.15 (measured).

2.3 Outer Loop - Power Control of Voltage Source Converters

The outer power control loop (or the outer voltage control loop) provides the reference values of the reactive and active current components to the inner control loop, as depicted in Fig. 2.1. The controllability of positive, negative, and offset components of the converter current makes it possible to control both the positive and negative sequence components of the bus voltage.

Due to the integral relation between the bus voltage and bus flux, the latter is less sensitive to disturbances that might occur in the network. Therefore, it is advantageous to control the bus flux, instead of the bus voltage. Moreover, since the offset component of the bus flux is accessible, it is also possible to control the offset component of the bus flux if necessary.
2.3.1 Bus Flux Control

In the outer control loop, PI controllers are utilized to control the bus flux. The controller working on the magnitude of the positive sequence component of the bus flux commands the reference value of the positive sequence reactive converter current ($i_{v,p,ref}^d$). The negative sequence $d$ and $q$ components of the reference current ($i_{v,n,ref}^d$ and $i_{v,n,ref}^q$) are given respectively by the two controllers working on the negative sequence $d$ and $q$ components of the bus flux. The offset components of the reference current ($i_{v,ofs,ref}^α$ and $i_{v,ofs,ref}^β$) can either be set to zero or be provided by the two PI controllers operating on the offset components of the bus flux. In the latter case, the offset components of the bus flux are controllable, which can mitigate the saturation problem of the transformers connected at
2.3 Outer Loop - Power Control of Voltage Source Converters

![Diagram of measured converter flux under normal conditions and with unsymmetrical load](image)

Figure 2.13: Measured converter flux under normal conditions and with unsymmetrical load

the same point of the VSC. The mitigation of the saturation problem will be demonstrated in chapter 3.

All the PI controllers utilized in the outer control loop have the form:

\[ y = (k_p + \frac{1}{s\tau_i})u, \]  

(2.36)

where \( k_p \) is the proportional gain, \( \tau_i \) is the integration time constant, \( s \) is the Laplace variable, \( y \) is the controller output, and \( u \) is the input, which is the error signal.

### 2.3.2 Dc-side Voltage Control

Charging and discharging the capacitor involves active power exchange and thus energy exchange between the converter and the grid as indicated by
where $W_C$ is the energy stored in the dc-side capacitor, $u_d$ is the dc-side voltage and $P_d$ is the active power flowing into the dc side of the converter.

If the power loss in the converter bridge is neglected, the active power flowing into the dc side of the converter equals the power flowing from the network into the ac side of the converter, which is given by:

$$P_{ac} = -\frac{3}{2} \omega (\psi_{B,p}^d i_{v,p}^q - \psi_{B,p}^q i_{v,p}^d)$$  \hspace{1cm} (2.38)$$

where $\psi_{B,p}^d$ and $\psi_{B,p}^q$ are positive sequence dq components of the bus flux, $i_{v,p}^d$ and $i_{v,p}^q$ are the positive sequence components of the converter current, and $\omega$ is the angular frequency of the bus flux. In (2.38), the negative sequence flux
and current are neglected since they normally do not present simultaneously. Since the PLL locks on the positive sequence of the bus flux, $\psi_{B,p}^q$ is very close to zero so that the active power can be approximated as:

$$P_{ac} = -\frac{3}{2} \omega \psi_{B,p}^d i_{v,p}^q = -ai_{v,p}^q$$  \hspace{1cm} (2.39)

where $a = \frac{3}{2} \omega \psi_{B,p}^d$.

Combining (2.37) and (2.39) results in

$$\frac{d(W_C)}{dt} = -ai_{v,p}^q$$  \hspace{1cm} (2.40)

The linearity between the derivative of $W_C$ and $i_{v,p}^q$ shown in (2.40) suggests that it is advantageous to control the energy stored in the capacitor instead of the dc-side voltage. The plant model can be written as:

$$G_p(s) = \frac{W_c(s)}{-i_{v,p}(s)} = a/s$$  \hspace{1cm} (2.41)
In addition, since only a capacitor is connected on the dc side, it is advantageous to introduce a virtual resistor $R_{\text{virt}}$ in parallel to the capacitor, as shown in Fig. 2.17, in order to increase the system damping when designing the energy controller. The value of the virtual resistance can be chosen such that the virtual power consumption in steady state will be a few percent of the VSC rated power. The introduction of the virtual resistance is equivalent to the active damping as suggested in [15].
To derive the modified plant model, the power $P_{\text{virt}}$ consumed by the virtual resistor can be added to both sides of (2.40). $P_{\text{virt}}$ is given by:

$$P_{\text{virt}} = \frac{u_d^2}{R_{\text{virt}}} = \frac{2W_C}{R_{\text{virt}}C} = p_{ad}W_C \quad (2.42)$$

where $p_{ad} = 2/(R_{\text{virt}}C)$.

Then, (2.40) can be modified as:

$$\frac{d(W_C)}{dt} + p_{ad}W_C = -ai_{v,p}^q + p_{ad}W_C$$

$$= -ai_{v,p}^{q'} \quad (2.43)$$

where $i_{v,p}^{q'} = i_{v,p}^q - (p_{ad}/a)W_C$.

The linear relation in (2.43) is represented by the plant model given in (2.44):

$$G'_{p}(s) = \frac{W_c(s)}{i_{v,p}^{q'}(s)}$$

$$= a/(s + p_{ad}) \quad (2.44)$$

The modification of the plant model can be illustrated by Fig. 2.18.

According to the IMC (internal model control) design method [16], in order
to make the closed-loop transfer function a first order system, i.e., $G_c(s) = 1/(1 + \tau_c s)$, the controller should have the following form:

$$G_k(s) = \frac{1}{a\tau_c} + \frac{p_{ad}}{(a\tau_c)s} \quad (2.45)$$

where $1/\tau_c$ is the cut-off frequency or the bandwidth of the closed-loop system.

This is a PI controller of form (2.36) with the proportional gain and the integration time constant given by:

$$k_p = \frac{1}{a\tau_c} \quad , \quad \tau_i = \frac{a\tau_c}{p_{ad}} \quad (2.46)$$

### 2.4 Design of Converter Filter

Fast switching of the converter bridge creates high-frequency harmonics in the converter output voltage. In order to prevent these harmonics from getting into the network, a properly designed filter must be utilized.

In [17], a filter configuration as shown in Fig. 2.19 is recommended specially for PWM inverters.

In the figure, $u_v$ stands for the converter output voltage and $u_b$ for the network bus voltage at the converter connection point.
In case the converter is connected to the network through a phase reactor $L_v$, the phase reactor can be used as the series filter inductor.

The filter consists of two parts. The right parts, the combination of the series inductor $L_v$ and the filter capacitor $C_f$, gives a high reduction of the high-frequency component and low reduction of the fundamental frequency. However, a resonance occurs at a certain frequency $f_{01}$. In order to avoid the amplification of any harmonic components, this resonance frequency should be chosen lower than the lowest harmonic frequency that might appear in the output voltage. Moreover, a parallel branch with the same capacitance is added as the left part of the filter to damp out this resonance. The resonance frequency $f_{02}$ of the parallel branch is empirically chosen as half the series resonance frequency $f_{01}$ and the resistance as

$$R_f = \frac{x_{01}}{0.442} = \frac{w_{01}L_v}{0.442} \quad (2.47)$$

where $x_{01}$ represents the reactance of the phase reactor at the frequency $f_{01}$ and $w_{01} = 2\pi f_{01}$.

According to the above design procedure, the capacitance $C_f$ and the inductance $L_f$ of the filter are determined by

$$C_f = \frac{1}{\omega_{01}^2 L_v} \quad (2.48)$$

$$L_f = 4L_v$$

It can be seen that the characteristic of the filter is determined by $f_{01}$ and $L_v$.

A typical value of 0.15 pu (see the per-unit system in the next section) is chosen for the reactance $L_v$ of the phase reactors and is used throughout the thesis. From the view point of converter voltage utilization, the phase reactors should be chosen as small as possible. However, the phase reactors are also used as a part of the converter filter circuit. A reduction of the phase reactor inductance, therefore, results in a higher current ripple. Based on the overall consideration of the above factors, a moderate value of 0.15 pu is chosen.

For a switching frequency of 1350 Hz (‘triangular frequency’), which
is always used in the simulations and the real-time simulator throughout this project, the first set of harmonics generated by the converter has the orders of \( n = p \pm 2m, m = 1,2,3, \ldots \), where \( p = 1350/50 = 27 \) is the frequency modulation ratio. In order to obtain an adequate reduction of the lower-order harmonics, a series resonance frequency \( f_{01} \) of 350Hz is chosen.

The frequency response of the filter designed for this switching frequency is depicted in Fig 2.20. The gains at fundamental frequency and at the switching frequency are 1.03 and 0.08 respectively.

It should be mentioned that the capacitor banks are utilized on one hand to filter out the harmonics, on the other hand to offset the operation range of the StatCom. As a result, the losses of the VSC in steady state operation are reduced. The reactive power provided by the filter capacitor will be estimated in the next section.
2.4 Design of Converter Filter

2.4.1 Reactive Power Provided by the Filter Capacitors

In the per-unit system used in this thesis, the peak values of the rated phase voltage and current are taken as the base voltage $U_{\text{base}}$ and base current $I_{\text{base}}$, respectively. Accordingly, the base power $S_{\text{base}}$ and base impedance $Z_{\text{base}}$ are given by

$$S_{\text{base}} = \frac{3}{2} U_{\text{base}} I_{\text{base}}$$

$$Z_{\text{base}} = \frac{U_{\text{base}}}{I_{\text{base}}}$$  \hspace{1cm} (2.49)

Assume the reactance of the phase reactor at line frequency $\omega_N$ is $x$ pu, i.e.,

$$\omega_N L_v = x Z_{\text{base}}$$  \hspace{1cm} (2.50)

The capacitance $C_f$ of the filter capacitors is given by:

$$C_f = \frac{1}{\omega_0^2 L_v} = \frac{\omega_N}{\omega_0^2 x Z_{\text{base}}}$$  \hspace{1cm} (2.51)

The reactive power provided by the capacitor in the right branch of the filter is

$$Q_{C_f} = \frac{3}{2} U_{\text{base}}^2 \omega_N C_f$$

$$= S_{\text{base}} \left( \frac{\omega_N}{\omega_0} \right)^2 \frac{1}{x}$$  \hspace{1cm} (2.52)

The total reactive power provided by the filter is approximately two times $Q_{C_f}$, i.e.,

$$Q_{F} \approx 2 Q_{C_f} = S_{\text{base}} \left( \frac{\omega_N}{\omega_0} \right)^2 \frac{2}{x}$$  \hspace{1cm} (2.53)

For the filter designed in the previous section ($x = 0.15$ pu, $f_{01} = 350$ Hz), the reactive power provided is approximately 27% of the rated VSC power. The percentage will be increased to 37% if the resonance frequency $f_{01}$ is reduced to 300 Hz.
3 Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation

When a short circuit occurs, it is usually observed as a voltage sag in the surrounding part of the electric power system. Once the fault has been cleared, for instance, by a disconnection of the faulty line, the voltage returns to its pre-fault value. However, when the voltage returns, the transformers in the system may be driven into saturation due to a combination of the remaining flux in the core and the inception instant of the fault clearance [18]. The saturation is a result of an offset component in the transformer flux [19] [20]. Due to the nonlinear relation between flux density and magnetic field intensity of transformer core material, transformers draw high non-sinusoidal excitation current if they are driven into saturation. The consequences are for instance malfunction of protection systems, harmonic over-voltages [21], electromagnetic noise, and HVDC-converter transformer core saturation instability [22]. In [23] it is shown that the converter performance is affected by the saturation characteristics of the series connected transformer under single line-ground faults.

For cost reasons transformers are usually designed such that saturation occurs already when the flux slightly exceeds the steady-state value. Therefore, the transformer may be forced into saturation also due to other reasons than voltage sags (as discussed above). Over-voltages, dc components in the load current [24], and geomagnetically induced currents (GIC) may also result in transformer core saturation [25]. It has also been shown that inrush currents due to transformer saturation during energizing might drive other transformers in the system into saturation [26].
In a transmission system with a StatCom connected at the PCC, the voltage at the PCC can be influenced by the VSC to a certain extent. The weaker the system is, the stronger the influence will be. Depending on the modulation scheme and the control strategy employed, the VSC can influence the bus voltage in different ways.

The normally adopted control method for StatComs is to control the voltage in the converter connection point (referred to as the bus voltage in this work) by using conventional PWM. The reference voltage to the PWM modulator is calculated from the measured voltage at the converter connection point and the output from the current controllers. The switching time for each switch in the converter bridge is then calculated based on the reference voltage and the dc-side voltage of the VSC. This PWM technique is called voltage modulation in this work. The objective of the flux modulation, as described in section 2.2, is to control the time-integral of the voltage rather than the voltage itself. In steady state operation the flux modulation results in the same modulation pattern as the corresponding voltage modulation scheme. However, under disturbed conditions the measured bus flux signal provides information about the offset of the bus flux in addition to the positive and negative sequence components. The components in the network mainly have inductive characteristics and accordingly the flux offset component disturbs the normal operation of components like transformers, inductors, motors etc. As the measured information of the offset flux is available, it is possible to control the offset component of the bus flux. An interesting question then is what influence the StatCom has on the saturation problem of the transformers connected at the PCC during fault recovery.

In this chapter, the influence of the converter modulation scheme on transformer saturation during fault recovery is investigated. The system setup is identical for two cases that utilize different approaches for modulation and control. The comparison is made through simulations using the power system simulation software PSCAD. A brief description of these two schemes and the transformer model will be presented first.
3.1 Flux Modulation and Deadbeat Current Control

The converter control system with flux modulation and deadbeat current control, as shown in Fig. 2.1, will be employed. As mentioned in Section 2.3.1, the offset components of the reference current ($i_{v,ofs,ref}^\alpha$ and $i_{v,ofs,ref}^\beta$) can either be set to zero or be provided by the two PI controllers operating on the offset components of the bus flux. For the purpose of mitigation of the transformer saturation problem, the offset components of the bus flux should be controlled. Therefore, the control system is re-drawn in Fig. 3.1 Another modification made in the figures is that the magnitude of the voltage at the PCC is controlled instead of the magnitude of the bus flux. The reason is to make the two control systems (with flux and voltage modulation) as similar as possible such that the comparison will focus on the effect of the two modulation schemes.
3 Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation

3.2 Voltage Modulation and Deadbeat Current Control

The voltage modulation and deadbeat current control scheme is depicted in Fig. 3.2. The bus voltage is measured and split into a positive sequence, a negative sequence, and an offset component with a PLL operating on the positive sequence component such that the q axis aligns with the positive sequence voltage vector in the dq reference frame. Similarly, the converter current is measured and separated into the same three components using the angle from the PLL.

The inner deadbeat current control loop calculates the reference value of the converter voltage. From the reference value, the modulation block cal-
3.2 Voltage Modulation and Deadbeat Current Control

<table>
<thead>
<tr>
<th>Controller</th>
<th>Proportional gain (pu/pu)</th>
<th>Integration time constant (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCC voltage magnitude controller</td>
<td>5.9</td>
<td>7.4</td>
</tr>
<tr>
<td>Negative sequence bus flux/voltage controller</td>
<td>5.9</td>
<td>7.4</td>
</tr>
<tr>
<td>Offset bus flux controller</td>
<td>5.9</td>
<td>7.4</td>
</tr>
</tbody>
</table>

Calculates the switching times using the standard sinusoidal pulse-width modulation (SPWM) method. The deadbeat current control with SPWM is implemented based on [3] with some modifications. The equations used are described in the next section. The current controller gains are the same as those used in the flux modulation scheme and are listed in Table 3.2.

In the outer loop, the PCC voltage magnitude, the converter dc-side voltage, and the negative sequence of the bus voltage are controlled to command the references of the converter current components. The dc-side voltage controller gives the reference for the active current (q component) of the positive sequence component and the PCC voltage magnitude controller provides the reference for the reactive current (d component) of the positive sequence component. The references of the negative sequence current components (d and q) are determined by the two negative sequence bus voltage controllers respectively. The references of the offset components are set to zero. This differs from the method used in the flux modulation case, in which the offset references are determined by the bus flux offset component controllers. All the outer loop controllers are PI type with the same gains as those used in the flux modulation scheme and listed in Table 3.1.
3 Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation

Table 3.2: Inner Loop Current Controller Gains

<table>
<thead>
<tr>
<th>Current controller</th>
<th>Proportional gain (pu/pu)</th>
<th>Integration time constant (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive sequence</td>
<td>0.3</td>
<td>370</td>
</tr>
<tr>
<td>Negative sequence</td>
<td>0.03</td>
<td>740</td>
</tr>
<tr>
<td>Offset</td>
<td>0.03</td>
<td>740</td>
</tr>
</tbody>
</table>

3.3 Formulas Used for Deadbeat Current Control and the Voltage Modulation

3.3.1 Calculation of Converter Voltage Reference

The bus voltage $\bar{u}_B$ and the converter current $\bar{i}_v$ are measured and resolved into dc offset, positive, and negative sequence components. The positive and the negative sequences are further resolved into d and q components in the rotating coordinate system. A PLL operates on the positive sequence bus voltage. The following data are sampled at the time instant $t_{k-1}$:

- Converter current reference (positive, negative sequence, and offset): $\vec{I}_{dq,v,p,ref,k-1}$, $\vec{I}_{dq,v,n,ref,k-1}$, $\vec{I}_{\alpha\beta,v,ofs,ref,k-1}$.

- Converter current (positive, negative sequence, and offset): $\vec{I}_{dq,v,p,k-1}$, $\vec{I}_{dq,v,n,k-1}$, $\vec{I}_{\alpha\beta,v,ofs,k-1}$.

- Bus voltage (positive, negative sequence, and offset): $\vec{u}_{dq,B,p,k-1}$, $\vec{u}_{dq,B,n,k-1}$, $\vec{u}_{\alpha\beta,B,ofs,k-1}$.

- Angle and frequency from PLL: $\theta_{k-1}$, $\omega_{k-1}$.

During the time period $< t_{k-1}, t_k >$ the converter reference voltage vector $\vec{u}_{\alpha\beta,v,k|k-1}$ for the switching period $< t_k, t_{k+1} >$ is calculated based on the data
3.3 Formulas Used for Deadbeat Current Control and the Voltage Modulation

sampled at the time instant \( t_{k-1} \). Accordingly,

\[
\hat{u}_{v,k|k-1}^{\alpha\beta} = \hat{u}_{v,B,k|k-1}^{\alpha\beta} + \hat{u}_{IL,k|k-1}^{\alpha\beta} + \hat{u}_{IR,k|k-1}^{\alpha\beta} + \hat{u}_{I_{reg},k|k-1}^{\alpha\beta}.
\]  
(3.1)

The four terms on the right-hand side are identified as follows.

1. Feed-forward from the bus voltage

\[
\hat{u}_{v,B,k|k-1}^{\alpha\beta} = \vec{u}_{B,ofs,k-1}^{\alpha\beta} + \vec{u}_{B,pk-1}^{\alpha\beta} e^{j\hat{\theta}_{k|k-1}} + \vec{u}_{B,nk-1}^{\alpha\beta} e^{-j\hat{\theta}_{k|k-1}}
\]  
(3.2)

where \( \hat{\theta}_{k|k-1} = \theta_{k-1} + 1.5T_s \omega_{k-1} \) and \( T_s \) is the sample period. The estimated phase angle corresponds to the time instant in the middle of the switching period \( <t_k,t_{k+1}> \).

2. Voltage to drive the desired current through the phase reactor \( L_v \)

\[
\hat{u}_{IL,k|k-1}^{\alpha\beta} = L_v \frac{\vec{I}_{v,ofs,ref,k-1}^{\alpha\beta} - \vec{I}_{v,ofs,ref,k-2}^{\alpha\beta}}{T_s} + e^{j\hat{\theta}_{k|k-1}} \left( L_v \frac{\vec{I}_{v,p,ref,k-1}^{dlq} - \vec{I}_{v,p,ref,k-2}^{dlq}}{T_s} + j\omega_{k-1} L_v \frac{\vec{I}_{v,p,ref,k-1}^{dlq} + \vec{I}_{v,p,ref,k-2}^{dlq}}{2} \right) + e^{-j\hat{\theta}_{k|k-1}} \left( L_v \frac{\vec{I}_{v,n,ref,k-1}^{dlq} - \vec{I}_{v,n,ref,k-2}^{dlq}}{T_s} - j\omega_{k-1} L_v \frac{\vec{I}_{v,n,ref,k-1}^{dlq} + \vec{I}_{v,n,ref,k-2}^{dlq}}{2} \right).
\]  
(3.3)

3. Voltage to cover the resistive voltage drop across \( R_v \)

\[
\hat{u}_{IR,k|k-1}^{\alpha\beta} = R_v \left( \frac{\vec{I}_{v,ofs,ref,k-1}^{\alpha\beta} + \vec{I}_{v,ofs,ref,k-2}^{\alpha\beta}}{2} + \frac{\vec{I}_{v,n,ref,k-1}^{dlq} + \vec{I}_{v,n,ref,k-2}^{dlq}}{2} e^{-j\hat{\theta}_{k|k-1}} + \frac{\vec{I}_{v,p,ref,k-1}^{dlq} + \vec{I}_{v,p,ref,k-2}^{dlq}}{2} e^{j\hat{\theta}_{k|k-1}} \right).
\]  
(3.4)
4. Corrective voltage given by the current controller

Because of the two-sample delay common to digital control systems, the converter current components obtained at the time instant \( t_{k-1} \) are compared with the reference components from the time instant \( t_{k-3} \).

\[
\begin{align*}
\Delta \mathbf{I}_{v,ofs,k-1}^\beta & = \mathbf{I}_{v,ofs,ref,k-3}^\beta - \mathbf{I}_{v,ofs,k-1}^\beta \\
\Delta \mathbf{I}_{v,p,k-1}^{dq} & = \mathbf{I}_{v,p,ref,k-3}^{dq} - \mathbf{I}_{v,p,k-1}^{dq} \\
\Delta \mathbf{I}_{v,n,k-1}^{dq*} & = \mathbf{I}_{v,n,ref,k-3}^{dq*} - \mathbf{I}_{v,n,k-1}^{dq*}.
\end{align*}
\]

(3.5)

The PI controllers for the current operate as given by

\[
\begin{align*}
\Delta \hat{\mathbf{i}}_{\alpha\beta}^{reg,k|k-1} & = (k_{p,oofs} \Delta \mathbf{I}_{v,oofs,k-1}^\beta \\
& + \frac{T_s}{\tau_{oofs}} \sum_{m=0}^{k-1} \Delta \mathbf{I}_{v,oofs,m}^\beta ) \\
& + e^{j\hat{\theta}_{k|k-1}} (k_{p,p} \Delta \mathbf{I}_{v,p,k-1}^{dq} \\
& + \frac{T_s}{\tau_{p}} \sum_{m=0}^{k-1} \Delta \mathbf{I}_{v,p,m}^{dq} ) \\
& + e^{-j\hat{\theta}_{k|k-1}} (k_{p,n} \Delta \mathbf{I}_{v,n,k-1}^{dq*} \\
& + \frac{T_s}{\tau_{n}} \sum_{m=0}^{k-1} \Delta \mathbf{I}_{v,n,m}^{dq*} ).
\end{align*}
\]

(3.6)

This gives the corrective voltage:

\[
\hat{\mathbf{u}}_{\alpha\beta}^{reg,k|k-1} = \frac{L_v}{T_s} \Delta \hat{\mathbf{i}}_{\alpha\beta}^{reg,k|k-1}.
\]

(3.7)

\subsection*{3.3.2 Calculation of Switching Time}

After the reference voltage vector \( \hat{\mathbf{u}}_{\alpha\beta}^{v,k|k-1} \) is calculated, It is transformed into phase quantities \( \hat{\mathbf{u}}_{v,x,k|k-1} \). From the reference values for the three phase-voltages, the switching time for each phase is obtained as

\[
t_{x,k} = t_k + \frac{T_s}{2} \left( 1 \pm \frac{\hat{\mathbf{u}}_{x,k|k-1}}{1/2 ud} \right)
\]

(3.8)
3.4 Transformer Model

The PSCAD transformer model used in the simulation will be described briefly in this section. It is a 3-phase 2-winding transformer model based on the classical modeling approach with a current injection routine to model magnetizing characteristics [27]. The positive sequence leakage inductance, the winding (copper) losses, and the core losses (no load losses) are represented in the model. The saturation is represented with a compensating current source across the winding wound closest to the core [28], as shown in Fig. 3.3. The transformer flux is determined as a function of the integral of the terminal voltage. The saturation characteristic then determines the magnetizing current. Fig. 3.4 shows the core saturation characteristic, which is determined by the air core reactance, knee point flux, and the magnetizing current at nominal flux.

This method of modeling transformer saturation has been verified to be successful in several study cases, e.g., core saturation instability studies where the model results agreed closely to actual system responses [27] [29]. Since the purpose of the investigation is to qualitatively compare the difference in saturation with two types of converter modulation schemes, it is believed by the author that the representation of the transformer is sufficiently accurate.
3 Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation

![Graph showing transformer core saturation characteristic](image)

Figure 3.4: Transformer core saturation characteristic

![Diagram of simulation system](image)

Figure 3.5: Diagram of the simulation system

### 3.5 Simulation Results

Simulations have been performed to compare the influence of flux and voltage modulation on transformer saturation during fault recovery. The system simulated is depicted in Fig. 3.5. The converter is connected to the network at the PCC via a phase reactor and transformer T1. Transmission line L2 is loaded at bus A. Load 1 is fed from the PCC via transformer T2. The system parameters and the specifications of the transformers are listed in Table 3.3 and Table 3.4 respectively. The knee point for T1 is set to be higher than that of T2 since T1 is designed to be used with a StatCom, which shall be capable of delivering reactive power to the network.

Three-phase-to-ground faults were applied at bus A in this study. Although different types of faults have different characteristics, the three-phase-to-
3.5 Simulation Results

Table 3.3: Specifications of the Simulation System

<table>
<thead>
<tr>
<th>Transmission Line</th>
<th>L1: 138 kV/150 km; L2: 138 kV/65 km</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSC rating</td>
<td>80 MVA; 22 kV line-to-line, rms</td>
</tr>
<tr>
<td>Phase reactor</td>
<td>$L_v$: 2.89 mH (0.15 pu); $R_v$: 0</td>
</tr>
<tr>
<td>DC side</td>
<td>Voltage: 43 kV; Capacitor: 861 µF</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>1350 Hz (‘triangular frequency’)</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>2700 Hz</td>
</tr>
<tr>
<td>Load 1</td>
<td>Normal load condition: 64 MW; 22 MVar</td>
</tr>
<tr>
<td></td>
<td>low-load condition: 7.6 MW; 2.6 MVar</td>
</tr>
<tr>
<td>Load 2</td>
<td>45 MW; 16 MVar</td>
</tr>
</tbody>
</table>

Table 3.4: Specifications of the Transformers

<table>
<thead>
<tr>
<th>Rated voltage</th>
<th>138 kV/22 kV; line-to-line, rms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>T1: 100 MVA; T2: 80 MVA</td>
</tr>
<tr>
<td>Positive sequence leakage reactance</td>
<td>0.1 pu</td>
</tr>
<tr>
<td>No load losses</td>
<td>0.005 pu</td>
</tr>
<tr>
<td>Copper losses</td>
<td>0.005 pu</td>
</tr>
<tr>
<td>Saturation property</td>
<td>Secondary winding</td>
</tr>
<tr>
<td>(current injection</td>
<td>Saturation placed on</td>
</tr>
<tr>
<td>approach)</td>
<td>Air core reactance</td>
</tr>
<tr>
<td></td>
<td>0.2 pu</td>
</tr>
<tr>
<td></td>
<td>Knee point</td>
</tr>
<tr>
<td></td>
<td>T1: 1.2 pu; T2: 1.1 pu</td>
</tr>
<tr>
<td></td>
<td>Magnetizing current</td>
</tr>
<tr>
<td></td>
<td>2% of the rated primary current</td>
</tr>
</tbody>
</table>

ground faults produce the most severe situations in a system. It should be pointed out that due to the controllability of the negative sequence of both the bus voltage/flux and the converter current, the converter is capable of riding through any unsymmetrical voltage dips caused by unsymmetrical faults such as single-phase-to-ground faults or phase-to-phase faults. With the system specifications, the faults caused a voltage drop of 70% at the PCC (30% remaining voltage) if there was no VSC connected. The three-phase-to-ground faults with different fault inception times (ranging from 2.0 s to 2.0034 s with an increment of 0.0002 s) and different fault
durations (ranging from 0.10 s to 0.12 s with an increment of 0.001 s) were applied. The faults were cleared by opening breaker B1. The range of the fault inception time is set from 2.0 s to 2.0034 s due to the fact that the fault condition repeats with a period of one sixth of a cycle in a three-phase system. With the chosen ranges for fault inception time and fault duration, all the possible fault conditions were represented.

Transformers behave differently with different load conditions. The presence of the copper losses and core losses helps with the damping of the offset component of the transformer flux. The damping effect becomes more pronounced with heavier load. Therefore, it is necessary to study the saturation problem under both the normal-load condition and low-load condition. Furthermore, similar behavior regarding saturation has been observed from transformer T1 and T2. This is due to the fact that they are connected at the same bus - the PCC. Therefore, only the saturation problem of T2 will be presented and studied.

3.5.1 Normal-Load Condition

A load of 90% of the nominal power is considered for normal-load condition of transformer T1 and T2. For all the 378 fault conditions, the peak values of the magnetizing current of transformer T2 were recorded and plotted in Fig. 3.6(a) for voltage modulation and Fig. 3.6(b) for flux modulation. The peak of the magnetizing current with flux modulation is generally smaller than with voltage modulation. It varies from 0.38 pu to 0.92 pu with voltage modulation and from 0.09 pu to 0.38 pu with flux modulation. The worst case is the fault applied at 2.0016 s with voltage modulation and 2.0014 s with flux modulation. In both these two cases, the fault duration is 0.107 s.

Simulation results for the worst case with the two modulation schemes are plotted in Fig. 3.7 and Fig. 3.8 showing the following quantities: three-phase transformer flux linkage, three-phase transformer magnetizing current, three-phase PCC voltage, and three-phase converter current.
Examining the transformer flux shows that not only the peak is smaller with flux modulation (1.17 pu compared to 1.28 pu), but also the offset component is eliminated much faster. This is due to the different control strategies employed. With voltage modulation, there is no control over the bus flux offset component. Hence, the elimination of the offset flux component depends on the system damping characteristics only. However, with flux modulation, the VSC also contributes to the offset suppression by controlling the bus flux offset component (see Fig. 3.10 for the low-load condition).
3 Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation

![Diagram of Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation]

Figure 3.7: Three-phase transformer flux linkage, transformer magnetizing current, and PCC voltage. (a) Voltage modulation, (b) Flux modulation
Figure 3.8: Three-phase VSC current (a) Voltage modulation, (b) Flux modulation
The higher flux peak obtained with voltage modulation results in a higher transformer magnetizing current peak (0.92 pu compared to 0.38 pu), which in turn creates greater distortion in the voltage at the PCC. In addition, the period with transformer saturation is longer.

It can also be noted that the voltage level at the PCC is slightly lower during the fault with flux modulation (0.339 pu compared to 0.367 pu). This can be explained as follows. During the fault, the converter is commanded to deliver the rated current (1 pu) for both voltage modulation and flux modulation. With flux modulation there is a certain amount of offset component in the converter current as is clearly shown in Fig. 3.8(b). The presence of the offset component means a reduction in the reactive power support (due to limitation of the output current) and a lower PCC voltage is obtained.

A higher converter transient current with flux modulation can also be observed immediately after the fault occurrence (2.01 pu compared to 1.7 pu). The reason is that the detection of the fault disturbance is slower with flux modulation due to the integral relation between the bus flux and the bus voltage. However, the high transient current lasts only for a very short period. To summarize, utilization of flux modulation tends to mitigate the transformer saturation problem. Both the saturation degree and the saturation period are reduced. However, this is achieved at a price of slightly lower PCC voltage during the fault and a higher transient peak current in the converter.

3.5.2 Low-load Condition

Simulations have also been performed with transformer T1 and T2 loaded with approximately 10% of their nominal power. The peak values of the magnetizing current of transformer T2 under different fault conditions are depicted in Fig. 3.9(a) for voltage modulation and Fig. 3.9(b) for flux modulation.
3.5 Simulation Results

Figure 3.9: Transformer magnetizing current peak values under different fault conditions (low-load) (a) Voltage modulation, (b) Flux modulation

It can be seen that the transformer gets more saturated under the low-load condition compared to the normal-load condition. However, the peak of the magnetizing current with flux modulation is till generally smaller than with voltage modulation (0.26-0.77 pu compared to 0.68-1.33 pu). The worst fault is the one applied at 2.001 s with voltage modulation and 2.0034 s with flux modulation. In both these two cases, the fault duration is 0.108 s.

The worst-case simulation results with these two modulation schemes are summarized in Table 3.5. Similar to the situation for the normal-load condition, a higher flux peak, higher magnetizing current peak, longer
saturation period, slightly higher PCC voltage magnitude during the fault, and a lower VSC current peak can be observed from the case with voltage modulation compared to the case with flux modulation.

The flux linkage vector loci are plotted in Fig. 3.10. It shows clearly that the flux is brought back to the pre-fault condition more quickly with flux modulation.

Simulations with other fault types have also been performed. The peak value of the magnetizing current of T2 for the worst case of each fault type is listed in Table 3.6, which shows that the three-phase-to-ground fault saturates the transformers the most.

Table 3.7 lists the magnetizing current peak of T2 with three-phase-ground faults applied at different locations along line 2. It shows that T2 gets more saturated if the fault is closer to the PCC.

Table 3.6 and 3.7 show that with different fault types and fault locations, the transformer saturation is always less severe with flux modulation.

Since the effect of the StatCom is related to the system configuration and the strength of the network, simulations have also been performed with different strength of the network. The system setup is the same as shown in Fig. 3.5 which is typical in power systems. Three-phase-to-ground faults were applied at bus A. By changing the length of Line 1 and Line 2 proportionally, the network strength was changed whereas the remaining voltage during the fault was kept unchanged. The peak values of the magnetizing current of T2 for the worst cases are listed in Table 3.8. The results show that the mitigation effect on the transformer saturation becomes more pronounced in weaker systems.
3.5 Simulation Results

Figure 3.10: Transformer flux linkage vector: pre-fault (dashed), during fault (solid), and post-fault (bold solid). (a) Voltage modulation, (b) Flux modulation

Table 3.5: Summary of the Simulation Results

<table>
<thead>
<tr>
<th>Variable</th>
<th>Voltage modulation</th>
<th>Flux modulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2 magnetizing current peak range under different fault conditions</td>
<td>0.68 pu - 1.33 pu</td>
<td>0.26 pu - 0.77 pu</td>
</tr>
<tr>
<td>T2 flux peak with the worst fault</td>
<td>1.36 pu</td>
<td>1.25 pu</td>
</tr>
<tr>
<td>Voltage magnitude at PCC during the worst fault</td>
<td>0.385 pu</td>
<td>0.348 pu</td>
</tr>
<tr>
<td>VSC transient current peak with the worst fault</td>
<td>1.52 pu</td>
<td>1.81 pu</td>
</tr>
</tbody>
</table>
3 Comparison of Flux Modulation and Voltage Modulation Regarding Transformer Saturation

Table 3.6: Magnetizing Current Peak with Different Fault Types

<table>
<thead>
<tr>
<th></th>
<th>Single-line-ground</th>
<th>Line-line</th>
<th>Line-line-ground</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flux modulation</td>
<td>0.38 pu</td>
<td>0.76 pu</td>
<td>0.73 pu</td>
</tr>
<tr>
<td>Voltage modulation</td>
<td>1.04 pu</td>
<td>1.16 pu</td>
<td>1.19 pu</td>
</tr>
</tbody>
</table>

Table 3.7: Magnetizing Current Peak with Different Fault Locations

<table>
<thead>
<tr>
<th>Distance to the PCC</th>
<th>15 km</th>
<th>30 km</th>
<th>65 km</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flux modulation</td>
<td>1.23 pu</td>
<td>1.03 pu</td>
<td>0.77 pu</td>
</tr>
<tr>
<td>Voltage modulation</td>
<td>1.65 pu</td>
<td>1.54 pu</td>
<td>1.33 pu</td>
</tr>
</tbody>
</table>

3.6 Conclusion

In a transmission system with a StatCom connected at the PCC, different modulation schemes and control strategies utilized by the VSC have different influence on the flux of the transformers connected at the PCC. During fault recovery, transformers in the system might be driven into saturation due to the presence of the offset components in the transformer flux. The transformer saturation problem during fault recovery has been studied with two alternative modulation schemes: voltage modulation and flux modulation. With voltage modulation, there is no control over the bus flux offset component. Hence, the elimination of the offset flux component depends on the system damping characteristics only. However, with flux modulation, the VSC also contributes to the offset suppression by controlling the bus flux offset component.

Table 3.8: Magnetizing Current Peak with Different Network Strength

<table>
<thead>
<tr>
<th></th>
<th>L1: 100 km</th>
<th>L1: 150 km</th>
<th>L1: 225 km</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L2: 43.3 km</td>
<td>L2: 65 km</td>
<td>L2: 97.5 km</td>
</tr>
<tr>
<td>Flux modulation</td>
<td>1.05 pu</td>
<td>0.77 pu</td>
<td>0.58 pu</td>
</tr>
<tr>
<td>Voltage modulation</td>
<td>1.50 pu</td>
<td>1.33 pu</td>
<td>1.24 pu</td>
</tr>
</tbody>
</table>
3.6 Conclusion

The comparison shows that the saturation problem during fault recovery can be mitigated to a certain extent by utilization of flux modulation due to the controllability of the offset component of the bus flux. Both the saturation degree and the saturation period are reduced. However, the bus voltage during the fault is slightly lower in the case with flux modulation since the presence of the offset component in the converter current reduces the reactive power support during the fault. Meanwhile, the VSC transient current peak is higher with flux modulation.

Transformer saturation may not be a major problem in most applications. However, as saturation has to be taken into account during the design process and may be a cost-driving factor, any means to reduce the saturation effect without additional cost should be considered. The study illustrates that the use of flux modulation may contribute in this respect and it further can be assumed that it can be implemented without additional cost. In a system in which transformer saturation is a concern, the flux modulation scheme is preferable.
4 Possible Benefits of Integrating an ES into a StatCom

Conventionally, StatComs are deployed to provide reactive power support to the connected power systems. With the integration of ES, a StatCom is able to provide active power support in addition to the reactive power support. Possible benefits have been studied regarding power oscillation damping, power quality, and system stability, etc.

Power oscillation occurs when there is a trip of transmission lines, loss of generation, or large changes in electric load. Previous works have shown that enhanced performance in power oscillation damping can be achieved with the additional active power support from StatComs [30–34]. Due to the long active power delivery period, the energy level is relatively high. Therefore, batteries are considered as the energy storage in these studies.

Voltage sags, usually caused by faults in the electrical system, are the most common disturbances in power systems and thus cause very much concern. Voltage sags can also occur during the start-up of large motor loads or during the operation of electrical equipments such as welders, arc furnaces, smelters, etc. It has been shown in [35] that by injecting a certain amount of active power into the grid in addition to the reactive power, the voltage sag mitigation effect of the StatCom can be improved.

In the literature, it has also been investigated how energy storage can be used for the improvement of power quality and reliability. It has been shown that a StatCom with ES can reduce the power fluctuation in a wind farm and improve its fault ride-through capability [36]. Studies show that voltage flicker can be compensated by active power compensation [37]. Improvement of
power quality and stability has also been reported in [38–40].

The possible benefits of integrating an energy storage into a StatCom have also been investigated in this project. The investigations cover the following three aspects:

- compensation of sudden active load changes for the reduction of voltage phase jumps in weak networks
- compensation of a cyclic load for the improvement of the power quality at the PCC
- active power compensation for the enhancement of the performance of a weak system under fault conditions

The results of these investigations will be presented in the following sections.

4.1 Reduction of Voltage Phase Jumps in Weak Networks

Large time-variable and cyclic loads in weak points of the grid give rise to undesirable fluctuations in the voltage at the PCC. Not only fluctuations in magnitude are observed, but also in phase. There may be phase-sensitive loads which trip occasionally despite the fact that the monitoring systems tell that the voltage magnitude is flawless. The impacts of phase jumps on ac motors and their drives are described in detail in [41] and [42] respectively. For thyristor-controlled drives in for instance paper mills, a phase jump may be as severe as a magnitude fluctuation in certain cases [43]. Repeated trippings of vital motor drives in paper mills may cause devastating problems, and the corresponding production loss may be very costly. The same statement holds for steel mills and several other industrial processes.

The common remedy to substantial voltage-magnitude fluctuations is to install SVCs or StatComs [44–46], depending mainly (but not only) on the frequency of the load variation. However, concentrating only on magnitude
4.1 Reduction of Voltage Phase Jumps in Weak Networks

variations may not always be very fruitful as pointed out above. In order to cope with phase jumps, the active power drawn at the PCC, must vary slowly or at a controlled rate. If the load cannot be controlled to meet the demands on the phase of the voltage, an external device must provide the power which is necessary to limit the variation of the phase. This can be achieved comparably easily by connecting for instance a large capacitor bank to the dc side of a StatCom. In this way the StatCom could control not only the magnitude of the voltage at the PCC by means of reactive power. It could also limit the variation in phase of the voltage at the PCC by means of active power. In a typical case the rated active power may only be a fraction of the rated reactive power of the StatCom. This means that the total apparent power rating of the StatCom is almost unchanged due to the fact that the active and reactive currents are orthogonal. It must, however, be kept in mind that the capacitance of the dc-link of a typical StatCom is far too low to make any difference if power variations with durations of the order of several seconds are considered. The additional capacitance which is necessary may be several orders of magnitude higher. Obviously, this has a dramatic influence on the total initial cost of the StatCom, but if the potential benefits are considered it might still be an attractive solution.

In previous works, utilization of series-voltage injection techniques, e.g., dynamic voltage restorers, to mitigate voltage sags with phase jumps has been investigated extensively in, e.g., [47–52]. The studies show that keeping the load voltage as the pre-sag condition by injecting required voltage in series can protect the load from both magnitude sags and phase jumps. These voltage sag mitigation techniques aim to reduce the impact of voltage sags on certain particularly protected loads. This section will instead describe control strategies for a StatCom with capacitor energy storage to reduce the voltage phase jump and magnitude fluctuation at the PCC, with the focus on the reduction of phase jumps in the PCC voltage.

In order to show the potential benefit of adding a capacitor bank to the dc-side of a StatCom, and to show how the StatCom could be controlled, computer simulations with PSCAD and analog real-time simulations describing the dynamics of the modified StatCom and the associated power system have been performed.
A simplified schematic diagram of the system under investigation is depicted in Fig. 4.1. Assume a weak network with a resistive load connected and disconnected occasionally. The connection and disconnection of the resistive load may represent the switching of large loads or large time-varying loads such as steel mills, arc furnaces, or railway-feeding systems, etc. A VSC is connected at the same bus where the resistive load is connected. Due to the weakness of the power system, a sudden active load change in the PCC will cause bus voltage magnitude deviations as well as phase jumps.

A condensed block diagram of the control system is also depicted in Fig. 4.1 in the lower part. The inner current control, the outer flux control, and the energy control have been described in Chapter 2. In the following section, active power compensation schemes will be proposed.
4.1 Reduction of Voltage Phase Jumps in Weak Networks

4.1.1 Active Power Compensation

The converter can keep the voltage magnitude deviation within a certain range by reactive power support, but before the controller takes any action, it must first detect a voltage deviation at the connection point. Next, it takes some time for the controller to respond, because the alternating voltage controller is in an outer control loop. However, with an energy storage capacitor bank connected on the dc side, the converter can also provide a certain amount of energy to compensate for the active power change under load disturbances. The active power compensation takes the active load as a feed-forward signal and can be quite fast because of the deadbeat control scheme utilized in the inner current control loop. By means of active power compensation, it is possible to reduce the phase jump and the bus voltage magnitude deviation.

In order for the VSC to compensate for the active load, load power or load current measurement is necessary. In case the active load is 3-phase symmetric, load current measurement is more straightforward (and preferred) than load power measurement due to the utilization of deadbeat current control in the inner loop. The current signal in some loads might be unaccessible. However, for the dedicated compensation for large time-varying loads or cyclic loads, the current signal may be obtained by, e.g., reconstruction of the measurements in the network. The measured load current is transformed into the dq plane using the angle from the PLL, and the active current (q component) is taken as the reference for the active power compensation.

As stated above, the cause to the bus voltage phase jump and magnitude deviation, especially the phase jump, is the sudden change in the active load. To mitigate this problem, initial compensation after the sudden change is essential whereas the compensation afterwards is dispensable.

4.1.1.1 Compensation Scheme I

The compensation scheme is depicted in Fig. 4.2. A high-pass (HP) filter (washout filter) is applied to the measured active load current such that the
4 Possible Benefits of Integrating an ES into a StatCom

![Diagram of Active Power Compensation Scheme I](image_url)

Figure 4.2: Active power compensation scheme I

The converter provides full active power support only at the initial stage after the load change, and then the load current is handed over to the network gradually. Since the energy that can be provided or absorbed by the capacitor bank is limited to a certain range, limitations must also be set on the filtered active load current before it is taken as the feed-forward active current reference for the converter.

When the feed-forward control commands active current from the converter, the energy stored in the capacitor bank will change accordingly, which in turn will cause the energy controller to react in a way counteracting the feed-forward control. For example, the feed-forward control commands a positive converter current (flowing out of the converter) when there is a step-up change in the active load. The converter then starts supplying active power immediately, which results in a drop in the stored energy. As soon as the energy controller detects the energy drop, a negative active converter current is ordered in order to keep the energy at the reference value. It should be noted that the feed-forward control is much faster than the energy controller because of the deadbeat control in the inner current control loop. The conflict between these two controls may be settled in favor of the feed-forward control since active power compensation is desired. The higher priority of the feed-forward control is kept by modifying the energy controller reference. Detailed description of each block is given below.
4.1 Reduction of Voltage Phase Jumps in Weak Networks

**HP Filter**  Assume a step change $\Delta i_{Ld}^q$ in the active load at time 0.

By means of the HP filter, the reference of the active converter current commanded by the feed-forward controller is given by:

$$i_{v,p,ref,ff}^q = \Delta i_{Ld}^q e^{-\frac{t}{\tau}}$$  \hspace{1cm} (4.1)

where $\tau$ is the time constant of the HP filter.

A simple way to select the time constant for the HP filter is to set it to a fixed value. This value should be the time constant $\tau_{\text{max}}$, with which the dc-side energy can be maintained in the safe operation range under all possible active load conditions. Calculation of this value should then be based on the worst case, i.e., with maximum possible load $\Delta i_{Ld,\text{max}}^q$ and minimum energy $\Delta W_{C,\text{min}}$ that can be provided or absorbed in steady state. $\Delta W_{C,\text{min}}$ is determined by:

$$\Delta W_{C,\text{min}} = \min \{(W_{C,st} - W_{C,\text{min}}), (W_{C,\text{max}} - W_{C,st})\}$$  \hspace{1cm} (4.2)

where $W_{C,st}$ is the energy stored in the dc-side capacitor bank in steady state, and $W_{C,\text{min}}$ and $W_{C,\text{max}}$ are the minimum and maximum stored energies respectively.

The energy required by the feed-forward control can be estimated as:

$$\hat{W}_{ff,\text{max}} = \int_0^\infty \frac{3}{2} \omega \psi_{B,p}^d i_{v,p,ref,ff}^q dt|_{\text{max}}$$

$$= \frac{3}{2} \omega \psi_{B,p}^d \Delta i_{Ld,\text{max}}^q \int_0^\infty e^{-\frac{t}{\tau_{\text{max}}}} dt$$

$$= \frac{3}{2} \omega \psi_{B,p}^d \Delta i_{Ld,\text{max}}^q \tau_{\text{max}}$$  \hspace{1cm} (4.3)

Setting $\Delta W_{C,\text{min}} = \hat{W}_{ff,\text{max}}$ yields:

$$\tau_{\text{max}} = \frac{\Delta W_{C,\text{min}}}{\frac{3}{2} \omega \psi_{B,p}^d \Delta i_{Ld,\text{max}}^q}$$  \hspace{1cm} (4.4)

**Limitation on the Feed-Forward Current**  The converter can provide or absorb active power only when the dc-side voltage is within the safe operation
Possible Benefits of Integrating an ES into a StatCom

4 Possible Benefits of Integrating an ES into a StatCom

range. Therefore, the feed-forward reference current should be modified into \( i'_{v,p,ref,ff} \) based on the energy stored on the dc side. A comparator can be employed to set the feed-forward reference to zero when the energy stored on the dc side is outside the safe operation range.

Modification of the Energy Reference

As stated above, a PI energy controller is utilized to control the dc-side voltage and thus to control the energy for general purpose Var compensation. In case active power compensation is desired, a relatively large energy variation is inevitable. The reference for the energy controller should then be modified as shown in (4.5) and in Fig. 4.3:

\[
W'_C,ref(t) = W_{C,ref} - \dot{W}_{ff}(t)
\]

where \( \dot{W}_{ff}(t) = \int_0^t \frac{3}{2} \omega \psi_{B,p}^d i'_{v,p,ref,ff} dt \) is the estimated energy that the feed-forward control will take from the converter.

The modified energy reference must be taken back to the steady-state value after the compensation process is finished, i.e., to bring \( \dot{W}_{ff} \) back to zero in steady state. A PI controller can be employed to fulfill this. The PI controller is active only when the feed-forward reference current is within a tolerance band of \( \pm \epsilon \). Here \( \epsilon \) is the threshold value to enable the active power compensation. As long as the active power compensation is in force, the input to this PI controller is zero.
4.1 Reduction of Voltage Phase Jumps in Weak Networks

4.1.1.2 Compensation Scheme II

In the compensation scheme shown in Fig. 4.2, the time constant of the HP filter is a fixed value based on the worst case calculation. In order to fully utilize the energy stored on the dc side and thus to minimize the disturbances introduced by the load change to the grid, the filter constant can be calculated individually for each load disturbance as shown in Fig. 4.4.

When a sudden change in the active load is detected, the time constant of the feed-forward HP filter is updated based on the actual load and energy condition. For detecting sudden load changes, a HP filter with time constant $\tau_1$ in the range of milliseconds can be employed. Whenever the output from this HP filter exceeds a predefined threshold value, e.g., 0.2 pu, a sample pulse is sent out such that the dc-side energy and the load current change at that instant are sampled for calculation of the feed-forward HP filter time constant.

Let the sampled energy and active load current change be $W_{C,S}$ and $\Delta i_{Ld,S}^q$. 

Figure 4.4: Active power compensation scheme II
The energy that can be provided or absorbed by the capacitor bank is:

\[ \Delta W_C = \begin{cases} W_{C,\text{max}} - W_{C,S}, & \text{for step-down changes} \\ W_{C,S} - W_{C,\text{min}}, & \text{for step-up changes} \end{cases} \]  

(4.6)

The energy that the feed-forward control will take can be estimated as:

\[
\hat{W}_{ff} = \int_0^\infty \frac{3}{2}\omega \psi_B^d p i_{v,p,ref,ff}^q \, dt = \frac{3}{2}\omega \psi_B^d \Delta i_{Ld,S}^q \int_0^\infty e^{-\frac{t}{\tau}} \, dt = \frac{3}{2}\omega \psi_B^d \Delta i_{Ld,S}^q \tau
\]

(4.7)

Setting \( \Delta W_C = \hat{W}_{ff} \) gives:

\[
\tau = \frac{\Delta W_C}{\frac{3}{2}\omega \psi_B^d |\Delta i_{Ld,S}^q|}
\]

(4.8)

### 4.1.2 Simulation and Experimental Result

The bus voltage magnitude and phase angle in response to sudden active load changes were investigated both in the power system simulation software PSCAD and in a real-time simulator.

The main circuit and the control system are as shown in Fig. [4.1] but without any sensitive load connected. The transmission line and the phase reactor are represented by their corresponding impedance, and a large capacitor on the dc side of the converter is used as the energy storage device. A resistive load is switched on and off occasionally. The three-phase bus voltage is measured and its magnitude and phase angle with respect to the infinite bus are derived. The specifications of the simulation system are listed in Table [4.1].

The experimental set up has the same numerical values as the simulation system but in V and W instead of kV and MW. It should be mentioned that the dc-side voltage rating and capacitor size are chosen without any optimization in this work. Active power compensation scheme II is employed in all the simulations and experiments.
Table 4.1: Specifications of the Simulation System

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid voltage</td>
<td>17.32 kV; line-line, rms</td>
</tr>
<tr>
<td>Converter rating</td>
<td>8 MVA</td>
</tr>
<tr>
<td>Rated current</td>
<td>0.267 kA; rms</td>
</tr>
<tr>
<td>Resistive load</td>
<td>6.4 MW</td>
</tr>
<tr>
<td>Line impedance</td>
<td>84.5 mH (0.7pu)</td>
</tr>
<tr>
<td>Phase reactor</td>
<td>18 mH (0.15pu)</td>
</tr>
<tr>
<td>dc-side capacitor</td>
<td>3645 μF</td>
</tr>
<tr>
<td>dc-side voltage</td>
<td>Maximum: 70.7 kV (5 pu)</td>
</tr>
<tr>
<td></td>
<td>Steady state: 56.6 kV (4 pu)</td>
</tr>
<tr>
<td></td>
<td>Minimum: 33.9 kV (2.4 pu)</td>
</tr>
<tr>
<td>VSC switching frequency</td>
<td>1350 HZ</td>
</tr>
</tbody>
</table>

Figure 4.5: Simulated bus voltage magnitude under load disturbance

4.1.2.1 Bus Voltage Response when the Resistive Load is Switched on

The voltage response was studied for three conditions: with both active power compensation and reactive power support, with only reactive power support, and without any external support. In the following figures presenting the simulation and experimental results, these three conditions are marked respectively as ‘with PQ supp.’, ‘with Q supp.’ and ‘without supp.’. The simulation results are plotted in Fig. 4.5 and Fig. 4.6 Fig. 4.7 shows the zoomed initial response of the voltage magnitude.
It can be seen that in case no power support was employed, the bus voltage dropped permanently with the accompaniment of a phase jump of $32^\circ$. With reactive power support, the voltage magnitude dropped down by 11.6%. However, with active power compensation added, the magnitude just went down by 4.8% and came back much faster. A dramatic improvement has been achieved. More noticeable is the improvement of the phase angle jump. Without any power support, the phase angle shifted to the new angle almost instantly. The reactive power support did not help with the phase jump reduction. On the contrary, the phase jump was accentuated. The phase angle jumped from $0^\circ$ to approximately $-52^\circ$ in 38 ms and then fluctuated around
4.1 Reduction of Voltage Phase Jumps in Weak Networks

![Graph showing bus voltage magnitude under load disturbance.](image)

Figure 4.8: Measured bus voltage magnitude under load disturbance

The steady-state value (-42°) for 200 ms. In the case with active power compensation, the initial jump was only 6° for 7 ms and then the angle changed gradually towards the steady-state value. This gradual change of the phase angle is of great significance to phase sensitive loads. For instance, it gives enough time for the rotor flux of an induction motor to adapt to the stator flux and thus large torque and current transients can be avoided. For a load with its own PLL, the smooth transition of the supply voltage phase angle reduces the error in the load PLL that will be much larger without active power compensation.

The experimental results plotted in Fig. 4.8 and Fig. 4.9 show good agreement with the simulation results.

4.1.2.2 Bus Voltage Response when the Resistive Load is Switched off

Fig. 4.10 and Fig. 4.11 provide a comparison of the simulated bus voltage response for the three conditions. The initial response of the voltage magnitude is zoomed into Fig. 4.12. In the case with only reactive power support, the bus voltage magnitude fluctuated with a maximum of 21%. Active power compensation reduced the amplitude fluctuation to 1.9% and with a much shorter period, which is a dramatic improvement. With only reactive power support, the phase angle jumped from -42° to 18° in 36 ms and then fluctuated for 300 ms around the steady-state value of 0°. The active power
4 Possible Benefits of Integrating an ES into a StatCom

Figure 4.9: Measured bus voltage phase angle under load disturbance

Figure 4.10: Simulated bus voltage magnitude under load disturbance

compensation again made a smooth transition of the phase angle from -42° to 0° and the initial fluctuation was only 6° for 7 ms.

Fig. 4.13 and Fig. 4.14 present the experimental results of the bus voltage responses. They are in good agreement with the simulation results.
4.1 Reduction of Voltage Phase Jumps in Weak Networks

Figure 4.11: Simulated bus voltage phase angle under load disturbance

Figure 4.12: Simulated bus voltage magnitude under load disturbance (zoomed)

4.1.3 Remarks on Accentuated Phase Jumps due to Reactive Power Support

In Fig. 4.6 and Fig. 4.9 it is shown that the phase jump becomes larger with fast reactive support than without. As a matter of fact this holds generally. It is shown below that fast reactive support inevitably will accentuate the problem with phase jumps in weak grids with large time-varying resistive loads. The consequence of this is that when a StatCom is installed in a weak network with phase-sensitive loads, active compensation should also be considered.
Consider the equivalent circuit shown in the Fig. 4.15. Here $u_{inf}$ is the voltage of the strong grid, $X_L$ and $R_L$ are the reactance and resistance of combined lines connecting the weak part of the grid to the strong grid, $R$ is the variable resistance of the time-varying load, $X_C$ is the equivalent variable reactance of the fast reactive compensator, and $u_b$ is the voltage across the load.

The load is considered to be passive, which means that the power is reduced if the voltage is reduced. Moreover, it is assumed that the tap-changers of the transformers in the system are too slow to compensate for voltage drops.
4.1 Reduction of Voltage Phase Jumps in Weak Networks

![Equivalent circuit of a system with a StatCom](image)

Figure 4.15: Equivalent circuit of a system with a StatCom

![Phasor diagram without reactive power support](image)

Figure 4.16: Phasor diagram without reactive power support

during the transients considered below. The voltage \( u_{inf} \) of the strong grid is assumed to be constant all the time. For proper operation of the load \( R \), it is assumed that \( |u_b| = |u_{inf}| \). In order to achieve this \( X_C \) has to provide a certain amount of reactive power.

4.1.3.1 Phase Lag of \( u_b \) without Reactive Power Support

Now, an example is considered where the load \( R \) is switched on and that \( R \) is constant with \( R = R_0 \). Before this it is assumed that no current was flowing through either \( R \) or \( X_C \) and that the voltage \( u_b \) was equal to \( u_{inf} \) with respect to both magnitude and phase.

The case with \( R \) being switched on can be described by a simple phasor diagram as shown in Fig. 4.16.

From the figure it is obvious that the magnitude of \( u_b \) is decreased and that
4 Possible Benefits of Integrating an ES into a StatCom

![Phasor diagram with reactive power support]

Figure 4.17: Phasor diagram with reactive power support

the bus voltage experiences a rapid change in phase. Now \( u_b \) lags \( u_{inf} \) with the angle \( \varphi_0 \). Thus,

\[
\tan(\varphi_0) = \frac{X_L}{R_L + R_0}
\]  
(4.9)

and

\[
\varphi_0 = \arctan\left(\frac{X_L}{R_L + R_0}\right)
\]  
(4.10)

4.1.3.2 Phase Lag of \( u_b \) with Reactive Power Support

In this case the magnitude of \( u_b \) is kept constant by means of the fast reactive power compensation. For the magnitude of the voltage this means that \( |u_b| = |u_{inf}| \). To determine the phase of the voltage, the phasor diagram in Fig. 4.17 is considered.

Let the phase angle of the bus voltage be \( \varphi_Q \) in this case. From the figure it can be seen that as long as there is a reactive current from the converter, the phase angle will increase by \( \Delta \varphi \) compared to the case without reactive power support, i.e., \( \varphi_Q = \varphi_0 + \Delta \varphi \).

The phase angle is given by:

\[
\varphi_Q = \arcsin\left(\frac{X_L}{R_0} + \frac{R_L X_L i_{v,Q}}{X_L R_0 i_{Ld,Q}}\right)
\]  
(4.11)
4.1 Reduction of Voltage Phase Jumps in Weak Networks

where $i_{v,Q}$ is the magnitude of the capacitive current $\vec{i}_{v,Q}$ from the VSC and $i_{Ld,Q}$ is the magnitude of the load current $\vec{i}_{Ld,Q}$. The ratio $i_{v,Q}/i_{Ld,Q}$ is determined by:

$$\sqrt{[(R_0 + R_L)i_{Ld,Q} - X_Li_{v,Q}]^2 + (X_Li_{Ld,Q} + R_Li_{v,Q})^2} = i_{Ld,Q}R_0$$  \hspace{1cm} (4.12)

4.1.3.3 Comparison of Uncompensated and Compensated Phase Jump

In order to make a realistic comparison of the two cases, the quantities $X_L/R$ and $X_L/R_L$ must be studied. In distribution systems $X_L/R_L$ might be of the order of 8. In a weak grid $X_L$ might be of the order of 0.5 pu and a large load $R$ may be of the order of 0.8 pu. The quantity $X_L/R$ is therefore approximately 0.63. It is therefore reasonable to study this quantity between 0.4 and 0.85 for different network strengths. In Fig. 4.18 and Fig. 4.19 the phase jumps of the two considered cases and the ratio of them are shown as functions of the quantity $X_L/R$.

As can be seen from the figures, $\varphi_Q$, which corresponds to the case with fast reactive power support, is always considerably larger than $\varphi_0$. The relative difference increases with $X_L/R$, i.e., as the grid gets weaker. This indicates that energy storage should be considered when installing a StatCom in a
4 Possible Benefits of Integrating an ES into a StatCom

Figure 4.19: Ratio of phase jumps as a function of $X_L/R$

weak grid with large time-varying loads, especially if phase-sensitive loads are installed in the same grid.

4.1.4 Conclusion

Effective active power compensation schemes for StatComs with capacitive energy storage have been proposed in this section and verified by both computer simulations and experiments with a real-time simulator. It has been shown that phase jumps and magnitude fluctuations of the voltage at the PCC can be reduced significantly with the additional active power support of the StatCom.

4.2 Compensation of Cyclic Loads

The power consumption of cyclic loads varies with certain periods. A particle accelerator is a typical cyclic load consuming pulsating reactive and active power with varying power factor. Fast magnetization and demagnetization of the main magnets require short rise and fall times of the power during each power cycle. The pulsating load power creates large fluctuations in the bus voltage at the connection point if there is no external voltage support device connected. In order to mitigate the voltage fluctuation, fast reactive
power compensation is required. Studies in [53] have shown that, as a possibility, an SVC can serve this purpose. The reactive power can be almost fully compensated by the SVC, whereas the pulsating active power will be supplied by the network.

This section investigates the possible use of a StatCom with energy storage to improve the power quality at the PCC where the cyclic load is connected. A control strategy for StatComs with capacitive energy storage is proposed. Simulations have been performed with the power system simulation software PSCAD. The investigation shows that the phase jump and magnitude fluctuation in the PCC voltage can be reduced significantly by compensation of both the active and the reactive power.

A similar study has been carried out by Dragan Jovcic and Karsten Kahle [54]. A different control strategy is, however, proposed for compensation of a particle accelerator load. In that study, the measured load power is taken as a feed-forward for the alternating voltage control, which in turn gives the d component of the converter reference voltage. Meanwhile, the active power of the load is controlled in an outer loop, delivering the reference of the dc-side voltage for the inner direct voltage control loop, which gives the q component of the converter reference voltage. Although different control approaches are utilized in these two studies, the results are in good agreement.

### 4.2.1 Load Model in PSCAD

The cyclic load simulated in PSCAD is a model of a particle accelerator main magnet supplied from a 12-pulse thyristor converter, as shown in Fig. 4.20. The accelerator consumes cyclic active and reactive power with a period of 2 seconds as shown in Fig. 4.21. Fast magnetization of the main magnet requires a short rise time of the load current (e.g., 650 ms). When the acceleration is finished, the main magnet should be demagnetized quickly, requiring a short fall time of the current (e.g., 550 ms). The load current is depicted in Fig 4.22.
4 Possible Benefits of Integrating an ES into a StatCom

![Load model](image)

**Figure 4.20: Load model**

![Pulsating load power](image)

**Figure 4.21: Pulsating load power**

![Load current](image)

**Figure 4.22: Load current**
4.2 Compensation of Cyclic Loads

The control system of the cyclic load implemented in PSCAD is shown in Fig. 4.23. The outer loop controls the load current and gives the reference for the output direct voltage of the thyristor converter. An inner loop controls the output voltage of the thyristor converter and delivers the command of the firing angle $\alpha$.

### 4.2.2 Converter Control

The VSC is connected to the PCC via a phase reactor as shown in Fig. 4.24. The control system, which is depicted in the lower part of Fig. 4.24, consists of two loops. The inner current control, the outer flux control, and the energy control have been described in Chapter 2. The load power compensation scheme will be described in the next section.

### 4.2.3 Compensation of the Cyclic Load

#### 4.2.3.1 Reactive Power Compensation

The aim of reactive power compensation is to achieve a fast voltage control. For the general function of the StatCom, i.e., providing reactive power to the network to maintain the bus voltage level, the converter can be controlled only by the bus-flux controller. However, the bus-flux PI controller takes action only when bus-flux deviations have been detected; and its control speed is limited. Meanwhile, the reactive power of the load keeps changing during each load cycle. Hence, even though the bus voltage deviation can be
controlled within a small range, the duration of the deviation can be quite long (85% of the load cycle as observed from the simulations). In order to obtain a faster voltage control, the pulsating reactive power should be compensated directly. The measured reactive power $Q_{Ld}$ of the load can be taken as a feed-forward to command the required current and thus reactive power $Q_v$ from the converter.

The reactive power provided by the converter is related to the converter current as given by

$$Q_v = \frac{3}{2} \omega (\psi_{B,p}^d v_{v,p}^d + \psi_{B,p}^q i_{v,p}^q)$$  \hspace{1cm} (4.13)$$

where $\psi_{B,p}^d$ and $\psi_{B,p}^q$ are positive sequence dq components of the bus flux, $i_{v,p}^d$ and $i_{v,p}^q$ are the positive sequence components of the converter reactive and active current, and $\omega$ is the angular frequency of the bus flux.

Since the PLL locks on the positive sequence of the bus flux, $\psi_{B,p}^q$ is very close to zero such that the reactive power of the converter can be approximated.
4.2 Compensation of Cyclic Loads

Figure 4.25: Reactive power compensation and flux control

\[
Q_v = \frac{3}{2} \frac{\omega \psi^{d}_{B,p}}{\psi^{d}_{B,p}} i^{d}_{v,p,ref,ff}
\]

(4.14)

Therefore, to directly compensate for the reactive power of the load, the required reactive current \(i^{d}_{v,p,ref,ff}\), given in (4.15), should be added into the reference of the converter positive sequence reactive current.

\[
i^{d}_{v,p,ref,ff} = \frac{2Q_{Ld}}{3\omega \psi^{d}_{B,p}}
\]

(4.15)

Fig. 4.25 shows the reactive compensation and positive-sequence flux-magnitude control scheme.

4.2.3.2 Active Power Compensation

Although the voltage magnitude disturbance at the PCC is mainly caused by the pulsating reactive power, the active load power also plays a role. In addition to the magnitude disturbance, the pulsating active power also creates phase jumps in the voltage at the PCC, which might degrade the performance of other loads, especially phase sensitive loads, connected at the same point.

In order to mitigate the disturbances introduced by the pulsating active load, active power compensation can be utilized if energy storage devices are connected on the dc side of the converter. In this study, the energy storage device is supposed to be a large capacitor bank. The pulsating active
power will be mainly exchanged between the cyclic load and the converter, while the network only needs to supply the average active power to the load. The active power compensation and energy control scheme is depicted in Fig. 4.26.

![Figure 4.26: Active power compensation and energy control](image)

The active power that flows from the converter to the network is determined by

$$P_v = \frac{3}{2} \omega (\psi^d_{B,p} i^q_{v,p} - \psi^q_{B,p} i^d_{v,p})$$

(4.16)

Since the PLL locks on the positive sequence component of the bus flux, $\psi^q_{B,p}$ is very close to zero. Hence, the converter active power can be approximated as:

$$P_v = \frac{3}{2} \omega \psi^d_{B,p} i^q_{v,p}$$

(4.17)

To compensate for the pulsating part of the active power $P_{Ld}$ of the load, the feed-forward reference for the active converter current must fulfill

$$i^q_{v,p,ref,ff} = \frac{2(P_{Ld} - P_{Ld,av})}{3\omega \psi^d_{B,p}}$$

(4.18)

where $P_{Ld,av}$ is the average active power of the load.

Since the energy that can be provided or absorbed by the capacitor bank is
limited within a certain range, limitations must also be set on this calculated feed-forward reference for the active current of the converter. As stated in Section 4.1.1.1, due to the conflict between the feed-forward control and the energy control, the reference for the energy control should be modified in order to achieve fast active power compensation. A detailed description of the blocks ‘Limitation’ and ‘Energy reference modification’ can be found in Section 4.1.1.1.

4.2.4 Simulation Results

Simulations have been performed in PSCAD to verify the proposed compensation strategy. The simulation system configuration is as shown in the upper part of Fig. 4.24. The specifications of the system are listed in Table 4.2. The converter rating used is 50 MVA and the capacitors used for the converter filter provide additional 19 MVar reactive power.

Since the power quality at the PCC is of great concern, the bus voltage was recorded and the amplitude and the phase angle with respect to the infinite bus were extracted.

To see the impact of the active and reactive power compensation, the bus voltage magnitude and phase angle were recorded with different simulation conditions: general control without feed-forward active and reactive power compensation, with only reactive power compensation, with both active and reactive power compensation.

Fig. 4.27 shows the bus voltage magnitude during one load cycle under different compensation conditions. From the upper plot it can be seen that even without feed-forward active and reactive power compensation, the bus voltage could be kept within the range of 0.98-1.02 pu except two spikes that occurred when the active power of the load changed abruptly. Although the voltage deviation was not very large, the duration was quite long (85% of the load cycle). The bus voltage magnitude was improved when the reactive

---

1 The specification of dc-side voltage rating and dc capacitor size in this table is just an example. No optimization has been done in this work.
Table 4.2: Specifications of the Simulation System

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer primary-side voltage</td>
<td>400 kV; line-line, rms</td>
</tr>
<tr>
<td>Transformer secondary-side voltage</td>
<td>17.32 kV; line-line, rms</td>
</tr>
<tr>
<td>Converter rating</td>
<td>50 MVA</td>
</tr>
<tr>
<td>Filter capacitors</td>
<td>19 MVar</td>
</tr>
<tr>
<td>Lumped line impedance</td>
<td>5.5 mH (0.7 pu)</td>
</tr>
<tr>
<td>Phase reactor</td>
<td>2.4 mH (0.15 pu)</td>
</tr>
<tr>
<td>dc-side capacitor</td>
<td>9376 μF</td>
</tr>
<tr>
<td>dc-side voltage</td>
<td>Maximum: 66 kV (4.7 pu)</td>
</tr>
<tr>
<td></td>
<td>Steady state: 33.9 kV (2.4 pu)</td>
</tr>
<tr>
<td></td>
<td>Minimum: 33.9 kV (2.4 pu)</td>
</tr>
<tr>
<td>dc-side energy</td>
<td>Maximum: 20.4 MJ, τ = 0.408 s</td>
</tr>
<tr>
<td></td>
<td>Steady state: 5.4 MJ, τ = 0.108 s</td>
</tr>
<tr>
<td></td>
<td>Minimum: 5.4 MJ, τ = 0.108 s</td>
</tr>
<tr>
<td>VSC switching frequency</td>
<td>1350 HZ</td>
</tr>
</tbody>
</table>

power of the load was compensated directly by taking it as a feed-forward to the converter reactive power control, as shown in the middle plot. With feed-forward reactive power compensation, the reactive load power was almost completely provided by the StatCom (including the 19 MVar filter capacitor reactive power). As shown in Fig. 4.28, the reactive power supply from the network was almost zero for the whole load power cycle.

Even though the overall voltage magnitude was improved, the reactive power feed-forward control had hardly any impact on the voltage spikes. Moreover, the two upper plots in Fig. 4.29 show two phase jumps in the bus voltage. A large phase jump means big disturbance to other loads, especially phase-sensitive loads such as ac motors, line-commutated converters, etc.
When the converter had energy storage capability and the pulsating load active power was compensated by feed-forward active power control as described above, both the magnitude and the phase angle of the bus voltage were well controlled, as indicated by the lower plots of Fig. 4.27 and Fig. 4.29.

By utilization of load power feed-forward control, the pulsating part of the active power of the load was almost fully provided by the VSC, while the network only had to supply the average value of the active power. This
can be seen from Fig. 4.30, in which the load power, the power taken from the network, and the power taken from the StatCom are plotted. Since the network only had to supply the average value of the active power of the load, there was almost no phase shift in the bus voltage. Although there were two spikes accompanied by the phase jump occurring when the active power of the load changed abruptly, the magnitude variation was kept at a fairly low level of 3.2%. The phase jump was also reduced significantly due to the utilization of the active power compensation, which means reduced disturbance to phase-sensitive loads.

Fig. 4.31 shows the variation of the dc-side voltage and its reference value during one load cycle.

4.2.5 Conclusion

Cyclic loads may create severe disturbances in the network. Simulations have shown that a StatCom can provide fast reactive power support and thus can stabilize the bus voltage. Integration of energy storage with a StatCom can further mitigate the magnitude disturbance of the bus voltage. Additionally, the phase jumps of the bus voltage caused by the pulsating active power of the load can be reduced significantly.
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Studies in the previous chapters have shown that with additional active power support, a StatCom can mitigate voltage disturbances regarding phase jumps as well as magnitude fluctuations. Reduced phase jumps can be beneficial for phase-sensitive loads such as ac motors and thyristor-controlled drives. It is, therefore, valuable to investigate the impact of the
energy storage on the performance of weak systems under fault conditions. The investigation has been performed by studying an example system. The system model was established based on a real system, in which a number of induction motors driving pumps along a pipeline are fed from a radial transmission line. To facilitate the investigation, modifications to the real system were made.

The system under investigation consists of two sources and a long radial voltage-constrained transmission line, as shown in Fig. [4.32] Along the line are eight lumped loads and six induction motors. In addition to the shunt capacitor banks that are connected along with the loads and motors (not shown in the figure), two more 20 MVar capacitor banks are installed
at bus 5 and bus 10, respectively, to compensate for the reactive power consumption in the system. Moreover, 40 MVar reactive power is required to maintain the voltage level at bus 10. This portion of reactive power will be provided either by a capacitor bank (at the absence of StatCom) or by a StatCom and its filter.

All the motors are assumed to have the same inertia constant of 2 MJ/MVA, although other parameters differs slightly. The parameters of motor 6 are listed in Appendix C for an example. Although the mechanical torques of the motors will reduce with the drop of the motor speeds, they are assumed to be constant during the fault for simplicity. This approximation makes the recovery of the motor speeds more difficult. The target is to prevent the motors from slipping away and desirably to prevent the motors from slipping out of a certain speed, e.g., 0.95 pu, when faults occur in the system.

The critical fault will be the one close to the source, which in this system is the fault at bus 3. The fault was assumed to occur at the bus-3-end of the line connecting bus 3 and bus 2 in this study. After 103 ms of the fault inception, the breaker at the bus-3-end opened and 33 ms later the breaker at the bus-2-end opened. The faults applied in the simulations were phase-phase-ground faults.

Since the system is vulnerable to faults close to the sources, additional reactive power support is necessary to improve the fault ride-through capability of the system and the performance of the motors. As a possibility, the reactive power support can be provided by mechanically switched capacitor banks. However, due to the constraints of the breakers, the capacitor banks can only be switched on with a certain delay with respect to the inception of the faults, usually after the faults are cleared. Alternatively, a StatCom can be installed to provide fast and dynamic power support to the system.
Figure 4.32: System diagram
4.3 Impact of Energy Storage on System Performance under Fault Conditions

4.3.1 Fault-recovery Performance without Additional Reactive Power Support

During a fault, the terminal voltage of the motors is extremely low and the motors are demagnetized. The unbalance between the electrical torque and the mechanical torque decelerates the motors. After the fault is cleared, the motors start to accelerate if the electrical torque generated is larger than the mechanical torque. In order to produce the required torque, the motors have to be magnetized and thus they consume much more reactive power than under normal conditions. If the reactive power support is not sufficient, the motors will keep decelerating until they stop. For this system, under the fault condition specified previously, some motors will stop if no additional reactive power support is available. As indicated by the simulation results shown in Fig. 4.33, this occurred to motor 3, 4, 5 and 6, which were far away from the sources.

4.3.2 Fault-recovery Performance with Two Mechanically Switched Capacitor Banks

Additional capacitor banks might be utilized to provide reactive power support under fault conditions. In order to maintain the voltage level at
bus 10, a fixed 40 MVar capacitor bank was connected. The faulty line was disconnected from bus 2 and bus 3 at 103 ms and 136 ms respectively after the fault inception. The two additional banks A1 and A2 were supposed to be switched on at 135 ms and 144 ms respectively. They stayed on for 600 ms and then were disconnected.

Simulations show that a minimum total capacitor bank rating of 90 MVar (2x45 MVar) was required for successful motor speed recovery. The motor speeds were depicted in Fig. 4.34(a). Even though the additional capacitor bank could help the system to restore, it created an over-voltage problem during the period after the motor speeds had recovered and before the capacitors were switched off. This can be seen from Fig. 4.35(a), which shows the three phase voltages at bus 10. The bus voltage was about 20% higher than the nominal voltage, which is unacceptable for the system.

It is quite straightforward that the more reactive power provided, the faster the motor speeds get restored. However, the over-voltage problem is more severe. The simulation result with a 100 MVar capacitor bank were plotted in Fig. 4.34(b) and 4.35(b). A faster recovery was achieved, but the over-voltage at the connection bus was 8% higher than that with the 90 MVar capacitor banks.

### 4.3.3 Fault-recovery Performance with StatCom

Capacitor banks can help the motor to get back to the normal speed after the fault is cleared. However, the capacitor banks are usually switched on after the fault is cleared. A StatCom, in contrast, can provide power support immediately after the fault inception. This power support includes both active and reactive power. Although the StatCom is usually supposed to provide reactive power support, the fault will cause an active power flow from the converter to the network. In the converter control system, a PLL works on the positive-sequence component of the ac-side bus flux. In case of a fault, there is a phase shift in the bus flux, which generates a difference between the real phase angle of the bus flux and the phase angle seen by the converter control system before the PLL follows the real angle. As long as
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.34: Motor speed with capacitor banks

(a) With 90 MVA capacitor bank

(b) With 100 MVA capacitor bank

Figure 4.34: Motor speed with capacitor banks
the difference exists, the output voltage of the converter is phase advanced relative to the real bus voltage and the converter is forced to provide active power resulting in a drop in the dc-side voltage. Of course, the active power support is possible only if there is some kind of energy source, e.g., the energy stored in the dc-side capacitor of the converter.

Moreover, by control of the bus voltage through the StatCom, the over-voltage problem is avoided.
Simulations have been carried out to study the impact of the converter rating, dc-side capacitor size, and the energy stored in the dc-side capacitor on the motor performance. The additional two capacitor banks A1 and A2 were replaced by a StatCom. As shown in Fig. 4.36, the VSC is connected to bus 10 through a 138 kV/33 kV transformer and phase reactors with a reactance of 0.15 pu. The rating of the StatCom is varied in this study to investigate the impact of the rating on the fault-recovery performance. However, the ac-side voltage is always 33 kV (line-to-line, rms). Meanwhile, the 40 MVar capacitor bank at bus 10 was removed as this portion of the reactive power was provided by the StatCom and its filter capacitors.

The suitable location of the StatCom is bus 10 due to two factors. One is that the critical fault is the one occurring at bus 3; the StatCom should keep a certain distance from the fault in order to function effectively. The other reason is that the StatCom should be in the middle of the motor string in order to support all the six motors.

During the fault, the motor speeds keep dropping due to the unbalance between the developed electrical torque and the mechanical torque of the load. Meanwhile, the motors are being demagnetized and pushing reactive power into the network. After the fault is cleared, the motors try to restore the set speeds. Since the speeds are low, a large amount of reactive power is needed for magnetization of the motors and thus indirectly for the speed restoration. The lower the speeds are, the more reactive power is required. Therefore, if the speed drops during the fault can be reduced, it will be easier for the motors to restore their speeds after the fault. This can be achieved by providing active power support and thus increasing
the developed electrical torque in the motors. Conventionally, the reactive power flow between a StatCom and the network is controlled to maintain the ac-voltage level at the connection point, whereas the active power is controlled to keep a constant dc-side voltage. Under such a control strategy, there is only a small amount of active power exchange between the VSC and the network. Therefore, the speed drop of the motors during the fault is mainly determined by the network configuration. However, if an active power compensation mechanism is employed such that the electrical torque developed by the motors can be increased during the fault, the speed drops will be reduced. This makes the speed restoration afterwards easier. In the section below, the system performance with these two different control strategies is analyzed.

4.3.3.1 Converter with Reactive Power Control but without Active Power Compensation

This control strategy has been described in Chapter 2. Simulations have been carried out in PSCAD to study the impact of the rating of the VSC and the size of the dc-side capacitor on the system performance.

The rating of the VSC It has to be pointed out that the power rating of the VSC in this study refers to the ac-side power rating and the variation on the dc-side voltage is not taken into account when the ac-side power rating is concerned.

With the StatCom at bus 10, a minimum rating of 75 MVA (voltage: 33 kV line-to-line rms; current: 1.86 kA phase peak value) was needed for a successful system recovery. Fig. 4.37(a) shows the motor speed with a 75 MVA StatCom. Increasing the converter rating from 75 MVA to 90 MVA (voltage: 33 kV line-to-line rms; current: 2.23 kA phase peak value) made the motor speed recovery faster, which can be seen from Fig. 4.37(b). The voltage at bus 10 was depicted in Fig. 4.38, which shows that no significant over-voltage occurred after the fault was cleared.
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.37: Motor speed with StatCom
Comparing the output power of the StatCom with 75 MVA and 90 MVA ratings plotted in Fig. 4.39(a) explains why the speed restoration is faster with higher StatCom rating. As mentioned previously, the active power exchange is caused by the phase jump due to the fault occurrence and clearance. With higher converter rating, more reactive power was pushed into the network; hence the bus voltage at the converter connection bus 10 was higher during the fault, as shown in Fig. 4.39(b). Therefore, the same phase jump caused by the fault occurrence took more active power from the converter. During the fault, the motors were being demagnetized, pushing reactive power to the network. The higher converter rating slowed down the demagnetization of the motors. However, the differences were too small to make any big difference in the speed drop of the motors during the fault. The speed of motor 6 was taken as an example in Fig. 4.39(c) since it is the far most motor and the speed restoration situation is most severe. After the fault was cleared, the reactive power provided by the StatCom was larger with higher rating, making the speed restoration faster.

The size of the dc-side capacitor In previous section, it was assumed that the dc-side voltage of the VSC is always above a reasonable level such that the converter can always deliver the required power to the system. Bigger capacitors and higher dc-side voltages were employed for those simulations
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.39: Performance comparison with the 75 MVA and 90 MVA StatCom
to fulfill this assumption.

As stated above, the converter is forced to provide active power into the network during the fault transients. Hence, the rating of the dc-side energy is a concern in this study.

If the converter is not supposed to provide additional active power support to the network, a dc-side voltage of 2.4 pu (with the peak value of the phase voltage as the base voltage, i.e., $u_{\text{base}} = 26.9$ kV) might be reasonable. In the flux modulation scheme utilized for the converter control, the reference flux change is limited according to the dc-side voltage of the VSC. In case the dc-side voltage drops below a certain level, the saturation in the flux modulation occurs and the converter may not deliver the required power. The threshold value of the dc-side voltage is not fixed, but depends on the ac-side voltage level. During the fault, the alternating voltage level becomes lower. Therefore, the minimum dc-side voltage without saturation of the flux modulation is also lower than during normal operation conditions.

Simulations have been performed with a 90 MVA StatCom. To compare the performance with different capacitor sizes, the capacitors are dimensioned in terms of their time constants. The time constant $\tau_C$ is the time that it takes for the capacitor to be charged to nominal voltage with nominal power, i.e.,

$$\tau_C = \frac{1}{2} \frac{C U_N^2}{P_N} \quad (4.19)$$

Here $U_N = 64.7$ kV(2.4 pu) and $P_N = 90$ MW.

Fig. 4.40 shows the speeds of the motors for dc-side capacitors with time constants of 25 ms, 55 ms, and 100 ms, respectively. It can be seen that the speed of motor 6 could not be restored with a 25 ms capacitor.

With a capacitor of 25 ms time constant, the dc-side voltage dropped down to 1.27 pu at 0.22 s, i.e., 120 ms after the fault inception (see Fig. 4.41(a)). The signal monitoring the saturation of the flux modulation is plotted in Fig. 4.42 showing that for a 25 ms capacitor, the flux saturation
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.40: Motor speeds with different dc capacitor size

(a) Capacitor time constant: 25 ms

(b) Capacitor time constant: 55 ms

(c) Capacitor time constant: 100 ms
occurred during the time period from 0.158 s to 0.249 s, whereas no satu-
ration occurred for the 100 ms case except for a very short period (0.207 s - 0.209 s) immediately after the fault was cleared. The saturation is also
reflected in the power output from the converter. From 0.158 s, the active
and reactive power outputs were both reduced compared to the simulation
result with a 100 ms capacitor (see Fig. 4.41(b) and 4.41(c)), resulting in a
steeper speed drop. Although the saturation ended at 0.249 s, the output
power was still low because of the low ac-side voltage as indicated by the
bus flux level in Fig. 4.41(d). The speed kept dropping steeply until 0.35 s
when the alternating voltage catches up with the voltage level of the 100 ms
case. At this time, the dc-side voltage had reached a level of 2.7 pu. The
fast rise of the dc-side voltage was due to the phase jump created by the
fault clearance. Even though the converter could provide as much power
as in the 100 ms case, the magnetization of the motors at lower speeds
consumed much more reactive power, which was beyond the capacity of the
converter. The motor finally slipped away.

Similar observations can be made from the simulation results with a
capacitor of 55 ms time constant. However, the saturation occurred for a
shorter period (from 0.198 s to 0.22 s). The speed also dropped more than
in the 100 ms case, but could still be restored.

Simulations show that increasing the capacitor size further made the
speed restoration slightly faster but the improvement was not significant.

4.3.3.2 Converter Control with Active Power compensation

Studies in Section 4.1 have shown that active power compensation can mit-
igate phase-jump related disturbances in a weak transmission system. Be-
cause of the quadratic relation between active and reactive current, the con-
verter can provide a certain amount of active power with an insignificant
reduction of reactive power support. It is a particular concern whether the
active power compensation can assist the extremely weak system under in-
vestigation in fault conditions. In order to provide active power support, the
converter must store a certain amount of energy on the dc side. The energy
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.41: Performance comparison with different dc-side capacitances
4 Possible Benefits of Integrating an ES into a StatCom

Figure 4.42: Occurrence of flux modulation saturation

storage devices used in this study are large capacitor banks. The energy can be stored by increasing the capacitance of the dc capacitor or raising the dc-side steady-state voltage, or by a combination of them.

Compensation scheme The inner control loop utilizes flux modulation and deadbeat current control as stated in Section 2.2. In the outer control loop of the converter, the bus-flux control described in Section 2.3 is employed here, whereas the energy control (dc-side voltage control) will be modified into a scheme combining active compensation and energy control.

The phase error from the PLL of the converter control system is an indicator of phase jumps caused by large active load steps or faults, and hence can be taken as the reference for the active power compensation. The compensation scheme is depicted in Fig. 4.43. The proportional feed-forward controller takes the phase angle from the PLL as an input and gives the feed-forward reference value of the converter active current (positive sequence). This feed-forward reference is then limited through a ‘Limitation’ block as described in Section 4.1. The energy reference of the energy controller is then modified through the block ‘Energy reference modification’ as described in Section 4.1. The limited feed-forward reference and the reference from the energy controller are then added together providing the reference of the positive sequence active current of the converter.
4.3 Impact of Energy Storage on System Performance under Fault Conditions

The selection of the proportional gain $K_p$ depends on two factors. One is the energy storage capacity of the dc-side capacitor and the other one is the optimal division of the converter output power into the active and reactive power for a certain converter rating. The former is quite straightforward. In steady state, the dc-side voltage is controlled at an intermediate level between the maximum voltage rating of the capacitor and the minimum voltage ensuring effective converter operation. Therefore, the maximum energy that the capacitor can absorb or provide is limited. As for dividing the converter output into active and reactive power, the proper ratio depends on the respective importance of the active and reactive power to the speed restoration of the motors.

**Simulations and Analysis** Simulations have been performed with a 35 MVA (voltage: 33 kV line-to-line rms; current: 0.86 kA phase peak value) StatCom using the above compensation scheme. The dc-side voltage reference was set to 64.7 kV (2.4 pu), 97 kV (3.6 pu), and 120 kV (4.5 pu) for the minimum, steady state, and maximum levels. The dc-side capacitor had a time constant of 55 ms. By varying $K_p$, the active power support was varied. The results reported here are from the simulations with $K_p =$ 1, 4, and 15 pu/rad respectively. The motor speeds plotted in Fig. 4.44 show that with the increase of the active power support, the motor speed restoration

---

2The specification of dc-side voltage rating and dc-capacitor size in this study is just an example. No optimization has been done in this work.
became faster and easier. In case the active power support was not enough (with $K_p = 1$), the speeds of motor 4, 5 and 6 could not be restored. This implies that the active power support is much more important than the reactive power to the system recovery under fault conditions. This can be explained by analyzing the simulation results.

The reactive power supply is important in the sense that the reactive power can help to keep the terminal voltage of the motor. The electrical torque developed is proportional to the square of the voltage, and the active power provided by the converter is also proportional to the ac-side voltage. However, during the fault, the motors could not absorb more reactive power even if there was more reactive power supply available from the converter. The reason was that the voltage level increased along the line from bus 3 to the end of the line. Thus, the reactive power flew in a reverse direction, from bus 14 to bus 3. All the motors were being demagnetized and pushing reactive power to the network, as shown in Fig. 4.45(a), in which motor 6 was taken as an example with $K_p =1$, 4, and 15 respectively. Although the reactive power output from the StatCom was 10 MVar higher in case $K_p = 1$ (see Fig. 4.45(b)), this portion of the reactive power was mainly transmitted from bus 10 to bus 9, as shown in Fig. 4.45(c) and 4.45(d). Therefore, the resulting difference in the motor input reactive power and the motor terminal voltage were hardly noticeable in Fig. 4.45(a) and 4.46.

In contrast, active power supply during the fault was critical to the system since the developed electrical torque helped to prevent the motor speed from dropping down. The active power outputs of the converter for $K_p =1$, 4, and 15 were plotted in Fig. 4.47(a), which show an increase by approximately 10 MW when $k_p$ changed from 1 to 15. Increase of the active power support reduced the backward phase jump at the connection bus 10, as shown in Fig. 4.48. Relative to bus 9 and bus 11, the phase angle of the voltage at bus 10 made a forward move. Therefore, the increased portion of the converter active power output was transmitted to bus 9 and bus 11 (see Fig. 4.47(b) and 4.47(c)) and was then absorbed by the motors, as shown in Fig. 4.47(d). The increased active power supply to the motor reduced the motor speed drop during the fault by 0.01 pu, as can be seen from Fig. 4.49. The reduction of the speed
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.44: Motor speeds with different $K_p$
Possible Benefits of Integrating an ES into a StatCom

(a) Reactive power supply to motor 6
(b) Reactive output power from the StatCom
(c) Reactive power flow from bus 10 to bus 9
(d) Reactive power flow from bus 10 to bus 11

Figure 4.45: Reactive power flow during the fault
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.46: Magnitude of the terminal voltage of motor 6

drop resulted in a decreased reactive power demand during the post-fault recovery. This explains why such a low converter rating was sufficient for the speed restoration when a proper active power compensation scheme was employed, whereas a minimum of 75 MVA was required for a successful restoration when no active power feed-forward control was involved.

When the fault was cleared, there was a forward phase jump at bus 10. The active power compensation scheme took additional active power from the network (see Fig. 4.50(a)). However, this did not reduce the active power supply to the motors. In contrast, as a consequence of the active power compensation, the forward phase jump at bus 10 was reduced (see Fig. 4.51), resulting in a larger amount of active power transmission from bus 9 to bus 10 (see Fig. 4.50(b)). Therefore, the active power transmitted from bus 10 to bus 11 was increased with the increase of active power support (see Fig. 4.50(c)). As a result, the active power supply to the motors was also increased (see Fig. 4.50(d), in which motor 6 was taken as an example). The combination of the reduced speed drop during the fault and the increased active power support after the fault clearance made the motor speed restore quickly with a small demand of reactive power, as shown in Fig. 4.52 and Fig. 4.53.

Based on the above analysis, the proportional gain $K_p$ should be selected in favor of the active power since active power supply during the fault is much more important and useful for preventing the speed drop of the
4 Possible Benefits of Integrating an ES into a StatCom

(a) Active output power from the StatCom

(b) Active power flow from bus 10 to bus 9

(c) Active power flow from bus 10 to bus 11

(d) Active power supply to motor 6

Figure 4.47: Active power flow during the fault
4.3 Impact of Energy Storage on System Performance under Fault Conditions

motor. A smaller speed drop during the fault and a continuing large active power support make the speed restoration faster and less demanding on the post-fault reactive power supply. However, the limitation imposed on $K_p$ by the capacitor voltage rating still exists. As can be seen from Fig. 4.54, with a $K_p$ of 15, the capacitor was operating close to its voltage rating limit (4.5 pu) and the converter minimum operation voltage limit (2.4 pu).
4 Possible Benefits of Integrating an ES into a StatCom

(a) Active output power from the StatCom

(b) Active power flow from bus 10 to bus 9

(c) Active power flow from bus 10 to bus 11

(d) Active power supply to motor 6

Figure 4.50: Active power flow after the fault is cleared
4.3 Impact of Energy Storage on System Performance under Fault Conditions

Figure 4.51: PLL phase angle after the fault is cleared

Figure 4.52: Motor 6 speed after the fault is cleared

Figure 4.53: Reactive power supply to motor 6
4 Possible Benefits of Integrating an ES into a StatCom

4.3.4 Conclusion

For a weak system with induction motor loads, a StatCom with certain energy storage capacity will effectively help with the system recovery from faults. Although this incurs extra cost for the increasing dc-side voltage rating and size of the dc-side capacitor, the overall rating of the converter can be reduced by utilization of the proposed active power compensation scheme. In case no active power compensation is employed, a larger StatCom rating together with a sufficiently large dc-side capacitor is necessary for a successful system recovery.

4.3.5 Discussion

The conclusion on the impact of the energy storage on system performance is quite promising. However, there are several points that might need more discussion.

The investigations were based on the simulations with the specific system configuration, motor model, and fault characteristic. Although it might not be adequate to draw a general conclusion about to what extent the energy storage can help the system, studies do show that energy storage is more helpful to weaker systems or the same system with more severe
The system performance depends on certain control system parameters to a considerable extent, for example, the speeds of the PLL and the energy controller. A slower PLL allows the network to take more active power from or push more active power into the StatCom during transients and thus helps the system more, but at a price of a worse overall control performance. So does a slower energy controller. In this study, the control parameters were kept unchanged for all the simulations in order to get fair comparisons.

The motor control in the simulations switched from constant-speed control to constant-torque control after the start-up transient died out. The faults were applied after the motors reached their steady states with constant-torque control. Simulations show that the pre-fault torque of the motors was slightly higher with a higher converter rating. For example, the pre-fault torque of motor 6 was 0.772 pu for a 35 MVA converter and 0.801 pu for a 75 MVA converter, which was 3.76% higher. This made the motor recovery situation with the 75 MVA converter slightly more severe. However, this difference was too small to have any great influence on the final conclusion.
5 Interface between the ES and the dc Link of the VSC

As discussed in Chapter 4, StatComs with ES can benefit power systems in different aspects. Depending on the power and energy level and the application requirements, the ES devices can be batteries, large conventional capacitor banks, or supercapacitors, etc.

These ES devices exhibit significant variations in the terminal voltage depending on the state of charge and on the magnitude and direction of the current. For instance, the variation of the terminal voltage for nickel-cadmium (Ni-Cd) batteries may be as high as 50% [55]. The voltage swing for capacitors and supercapacitors can be even larger since the energy stored in a capacitor/supercapacitor is proportional to the square of the terminal voltage. Direct connection of an ES device to the dc link of a StatCom implies that the dc-side voltage of the VSC will vary accordingly. For a StatCom to deliver reactive power to the connected system, the VSC must be able to produce an alternating voltage with a higher magnitude than the network voltage. Therefore, the dc-side voltage must be maintained above a certain level depending on the modulation scheme utilized for the VSC. This level is the minimum-required dc-side voltage. If the dc-side voltage varies with the terminal voltage of the ES device, the final discharging voltage of the ES should not be lower than the minimum-required dc-side voltage. Hence, the VSC has to handle a voltage level up to the charging voltage of the ES, which results in an increased voltage rating, and thus increased power rating of the VSC.

It, therefore, makes sense to consider an intermediate conversion stage between the ES and the dc-link of the VSC, especially if the rated active power
of the converter is only a fraction of the rated reactive power (e.g., 20%). If the dc-link voltage can be kept constant, substantial cost savings can be made since the voltage rating of the VSC does not have to be increased by adding the ES. Topologies for interfacing ES with the dc link of a VSC have been reported in literature. They are for low and medium voltage applications and are mainly IGBT based bi-directional dc/dc converters either with a single leg [56–59] or with three legs [60,61].

The cost of the additional conversion stage is, however, not insignificant even though this converter only has to have a rating corresponding to the rated active power of the VSC. This is especially the case in high-power high-voltage applications. Here, applications with the active-power rating of the StatCom lower than its reactive-power rating are considered. One way to reduce the rating of this converter is to have a converter which acts only on the difference in voltage between the ES and the dc-link of the VSC. The rating of such a converter would be substantially lower than the rated active power of the VSC, and typically approximately one order of magnitude lower than the total rating of the VSC. In order to reduce the additional cost even more, a thyristor-based technology may be chosen. In this chapter, such an interface topology will be proposed and analyzed.

Section 5.1 provides a description of the main properties of the proposed topology. In Section 5.2 the total cost of the system is compared with and without the proposed system. Meanwhile, comparisons regarding the total costs with three different types of ES are also presented. The control of the system with the proposed interface is investigated in Section 5.3.

5.1 The Proposed Topology and its Main Properties

5.1.1 The Proposed Topology

In the system shown in Fig. 5.1, a dual thyristor converter is proposed to interface the ES and the dc link of the VSC. The VSC is connected to the PCC through a transformer T1 and a phase reactor, which has an
5.1 The Proposed Topology and its Main Properties

inductance \( L_v \) and a resistance \( R_v \). The phase reactor is utilized on the one hand as the filter reactor. On the other hand, it reduces the steep front of the voltage of transformer T1. A two-level VSC is employed in this investigation. However, the proposed interface topology is also applicable to StatComs with other configurations as long as the ES is concentrated and is connected to the common dc link of a converter, e.g., three-level VSCs with ES. A capacitor bank implemented as a filter is employed to offset the operation range of the StatCom. Consequently, the losses in steady-state operation can be reduced. The configuration and characteristics of the filter are described in detail in Section 2.4.

In addition to the reactive power support, the VSC is supposed to deliver a certain amount (less than 25% of the VSC rating) of active power to the network for a certain period. The dual thyristor converter is connected via transformer T2 to the low-voltage side of the VSC transformer T1, both for voltage adaptation and for galvanic isolation. The dc side of the dual thyristor converter consists of an inductor and a capacitor \( C_2 \), which can be quite small. Capacitor \( C_2 \) is connected in series with the ES and the whole branch is then connected in parallel with the dc-side capacitor (\( C_1 \)) of the VSC.

The dual thyristor converter consists of two standard three-phase thyristor bridges, as shown in Fig. 5.2 connected in anti-parallel. The anti-parallel

Figure 5.1: Diagram of the system with the proposed interface topology.
connection of these two thyristor bridges enables a power flow in either direction and facilitates the charging and discharging of the ES device. The dual thyristor converter itself is not new. However, the application as an energy storage interface is a new concept.

5.1.2 Dc-side Voltage and Active Power Flow

The output voltage of the thyristor converter is controlled such that the dc-side voltage of the VSC is always kept constant. In other words, the thyristor converter should always provide a voltage across capacitor $C_2$ that is the difference between the constant dc-side voltage of the VSC and the varying terminal voltage of the ES. In this study, the constant voltage of the VSC is selected to be higher than the maximum voltage of the ES.

The power flow during a discharging process has the following pattern. When a power $P_{ES}$ is delivered from the ES device, the current passes through the thyristor converter. Meanwhile, if the terminal voltage of the ES drops, the thyristor converter has to charge capacitor $C_2$ to keep the dc-side voltage of the VSC. This requires a certain active power output from the thyristor converter. This power is provided by the VSC and is circulating through the VSC and the thyristor converter. The amount of the circulating power depends on the final discharging voltage of the ES devices and peaks at the instant when the voltage of the ES is the lowest. The peak value of the circulating power is determined by

$$P_{crl} = \frac{u_d - u_f}{u_f} P_{ES},$$

(5.1)
where $u_d$ is the dc-side voltage of the VSC and $u_f$ is the final discharging voltage of the ES.

A lower final discharging voltage requires a higher voltage boost across $C_2$ and a higher discharging current, resulting in a higher circulating power.

The active power flows with a similar pattern during the recharging process but with the opposite direction.

### 5.1.3 Comparison of Converter Rating with Different Solutions to Connect the ES

Even with the addition of the circulating active power, the VSC power rating does not increase proportionally since the circulating active current is in quadrature with the reactive current. However, with direct connection of the ES to the dc link, the power rating increases in proportion to the increase of the voltage rating. A rough comparison of the converter rating can be made through a simple example.

Consider a 100 MVA VSC which is supposed to provide additional 20 MW active power with the integration of energy storage on the dc side. The voltage swing of the ES device is 50%, i.e., the charging voltage $u_{ES,chg}$ is 50% higher than the final discharging voltage $u_{ES,f}$. The total converter rating will be compared for three cases: with direct connection (no interface in between the ES and the VSC), with the proposed interface, and with a bi-directional dc/dc converter interface.

#### 5.1.3.1 Total Converter Rating with Direct Connection

In order to interface the network, the dc-side voltage of the VSC must be higher than a certain level $U_{d,\text{min}}$. In case of direct connection, the final discharging voltage $u_{ES,f1}$, which is the same as the minimum terminal voltage $u_{ES,\text{min1}}$, of the ES must be no lower than $U_{d,\text{min}}$. In order to interface the ES, the VSC voltage rating $u_{d1}$ has to be increased by 50% and so does the
power rating, i.e.,

\[
\begin{align*}
    u_{ES,min} &= u_{ES,f1} = U_{d, min} \\
    u_{d1} &= u_{ES,chg1} = 1.5 U_{d, min} \\
    S_1 &= \frac{u_{d1}}{U_{d, min}} S_{base} = 150 \text{ MVA},
\end{align*}
\]

where \( S_{base} \) is the original VSC power rating.

### 5.1.3.2 Total Converter Rating with the Proposed Interface Topology

With the proposed topology, however, the following holds:

\[
\begin{align*}
    u_{ES,chg2} &= U_{d, min} \\
    u_{d2} &= u_{ES,chg2} = 1.5 u_{ES,f2} \\
    P_{crcl} &= 0.5 P_{ES}
\end{align*}
\]

The VSC power rating is determined by:

\[
S_2 = \sqrt{S_{base}^2 + (P_{ES} + P_{crcl})^2} = 104 \text{ MVA}
\]

The rating of the thyristor converter depends on the peak of the circulating power, which is 10 MVA in this example.

The VSC voltage ratings in relation to the ES voltage swing for the above two cases can be illustrated by Fig. 5.3.

### 5.1.3.3 Total Converter Rating with a Bi-directional dc/dc Converter Interface

If, instead, a buck-type bi-directional dc/dc-converter was used as interface, this converter had to have a rating of 1.5\(*20=30 \text{ MW}. Assuming that the per-unit cost of the bi-directional dc/dc-converter is the same as that of the StatCom, the total converter rating would in this case be 104+30=134 \text{ MVA}.

Thyristor technology is considerably cheaper than IGBT technology, especially in high-power high-voltage applications that the proposed topology
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

Having the freedom to let the voltage of the energy storage vary without affecting the voltage rating of the VSC, the question is which kind of energy storage to use, and what potential cost savings that can be obtained compared to the case without an interface between the energy storage and the dc-link of the VSC. This issue will be investigated in this section.

Section 5.2.1 describes the foundations of the investigation. The method for cost estimation is presented in Section 5.2.2. In Section 5.2.3, the total system cost is investigated with and without the converter interface between

Figure 5.3: VSC voltage rating in relation to the voltage swing of the energy storage.

The high voltage and current handling capability and low cost features of thyristors make this dual thyristor interface topology attractive for high-power applications. This topology is suitable for high-power high-voltage applications where a StatCom is required to deliver a moderate amount of active power (e.g., 20% of the rated power) in addition to the reactive power support.
the energy storage and the dc-link of the VSC. For each of the three types of energy storage, a cost comparison is made between the cases with and without the thyristor converter interface. A fixed energy-delivery period is considered. In Section 5.2.4, the total system cost is again investigated using the three different kinds of energy storage. Different discharging/charging cycles have been considered and the costs using different energy storages are compared. The choice of the type of energy storage depends mainly on the amount of energy which is required during a typical discharging/charging cycle. In some cases when several alternatives exist, the choice of the energy source must be made based on a cost estimation.

5.2.1 Foundations of the Investigation

5.2.1.1 System Specifications and Comparison Method

The system with the proposed interface topology is depicted in Fig. 5.1. In addition to the reactive power support, the VSC is supposed to deliver a certain amount of active power occasionally or periodically to the time-varying-load at the PCC. The total cost of the system will be estimated relative to the cost of a 100 MVA VSC including the dc capacitor $C_1$ and the phase inductors. The relative costs of the different parts in the apparatus are listed in Table 5.1.

The cost for the two transformers can be assumed to be constant for all the cases. However, the costs of the energy storage, the VSC, and the thyristor converter vary from case to case and are proportional to the energy/power ratings.

As mentioned in the previous section, there is a certain amount of active power circulating through the VSC and the dual thyristor converter. The circulating power causes a further reduction in the reactive power support capability of the VSC. Therefore, a fair comparison should be the comparison of the total cost required for a certain amount of energy delivery in addition to the original reactive power support.
Table 5.1: Relative cost of different parts

<table>
<thead>
<tr>
<th>Part</th>
<th>Symbol</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSC (100 MVA) with dc capacitor and phase inductor</td>
<td>(cst_V)</td>
<td>1 pu /100 MVA</td>
</tr>
<tr>
<td>Transformer T1(below 220 kV)</td>
<td>(CST_{T1})</td>
<td>0.5 pu</td>
</tr>
<tr>
<td>Transformer T2</td>
<td>(CST_{T2})</td>
<td>0.1 pu</td>
</tr>
<tr>
<td>Dual thyristor converter with dc inductor (VSC power)</td>
<td>(cst_{thy})</td>
<td>0.5 pu /100 MVA</td>
</tr>
<tr>
<td>DC capacitor energy storage (VSC power during 1 s)</td>
<td>(cst_C)</td>
<td>3.7 pu /100 MJ</td>
</tr>
<tr>
<td>Supercapacitor (VSC power during 10 s)</td>
<td>(cst_{SC})</td>
<td>1.1 pu /1000 MJ</td>
</tr>
<tr>
<td>Battery (4% of VSC power during 1 h)</td>
<td>(cst_{btr})</td>
<td>1.8 pu /14400 MJ</td>
</tr>
</tbody>
</table>

In the system shown in Fig. 5.1, the StatCom is supposed to provide a certain amount of active power \(P_{ES}\) for a certain duration \(t_{P_{ES}}\) in addition to the reactive power support. An active power support of 20\% of the nominal apparent power will be considered in this study, which corresponds to a reduction of approximately 2\% in the reactive power supply.

In the comparison in Section 5.2.3, the energy delivery periods for capacitors, supercapacitors, and batteries are set to 0.5 s, 30 s, and 15 minutes respectively based on the following consideration. Compared to supercapacitors, conventional capacitors have much lower capacitance and higher cost per energy unit. On the other hand, supercapacitors have a higher equivalent series resistance (ESR), which means low efficiency at fast charging/discharging. Therefore, conventional capacitors are suitable for power delivery with short durations, whereas supercapacitors can only reach a reasonably high efficiency when they are charged and discharged in at least tens of seconds. Batteries also have certain internal resistance, which limits the charging/discharging efficiency. However, the cost per energy unit is much lower than that of capacitors and supercapacitors. This makes them suitable
Table 5.2: Specifications of the system parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSC Rated power $S_{base}$</td>
<td>100 MVA</td>
</tr>
<tr>
<td>VSC Rated current $I_{base}$</td>
<td>1.5 kA (RMS)</td>
</tr>
<tr>
<td>Rated ac voltage $U_{base}$</td>
<td>38.5 kV (line-line, RMS)</td>
</tr>
<tr>
<td>Phase reactor inductance $x_{vn}$</td>
<td>0.15 pu</td>
</tr>
<tr>
<td>Active power to be delivered $P_{ES}$</td>
<td>20 MW (20% of the apparent power)</td>
</tr>
<tr>
<td>Active power delivery duration $t_{PES}$</td>
<td></td>
</tr>
<tr>
<td>Capacitors</td>
<td>0.5 s</td>
</tr>
<tr>
<td>Supercapacitors</td>
<td>30 s</td>
</tr>
<tr>
<td>Batteries</td>
<td>15 min.</td>
</tr>
</tbody>
</table>

for long-period energy delivery (from minutes to hours).

The specifications of the system parameters are listed in Table 5.2. The VSC phase reactors are 0.15 pu. From the viewpoint of converter voltage utilization, the phase reactors should be chosen as small as possible. However, the phase reactors are also used as a part of the converter filter circuit. A reduction of the phase reactor inductance, therefore, results in a higher current ripple. Based on the overall consideration of the above factors, a moderate value of 0.15 pu is chosen.

The minimum dc-side voltage level is calculated for the most demanding situation in which the converter is required to deliver the rated reactive power to keep the bus voltage at the nominal value. Hence, the magnitude (line-to-line, RMS) of the converter output alternating voltage should be:

$$U_v = U_b + I_{base}x_v = (1 + x_{vn})U_{base}$$  \(5.5\)

where $U_b = U_{base}$ is the RMS value of the line-to-line voltage at the bus, $x_v$ is the phase reactor reactance, and $x_{vn}$ is the pu value of $x_v$.

If Sinusoidal PWM with third harmonic injection is utilized, the minimum dc-side voltage is determined by:

$$U_{d,\text{min}} = \sqrt{2}(1 + x_{vn})U_{base}$$  \(5.6\)
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

5.2.2 Method of Cost Estimation

The total cost without interface consists of three parts: the cost of transformer $T_1$, the cost of the VSC, and the cost of the energy storage devices, i.e.,

$$c_{wo} = c_{ESwo} + c_{Vwo} + CST_{T_1} \quad (5.7)$$

The rating of the VSC has to be increased in proportion to the increase of the dc-side voltage, and so does the cost:

$$c_{Vwo} = cst_V \ast u_{ES,\text{max}} / U_{d,\text{min}} \quad (5.8)$$

where $u_{ES,\text{max}}$ is the highest voltage of the ES.

Introduction of the proposed dual thyristor converter interface incurs two additional parts of cost, the cost of the dual thyristor converter and the cost of the thyristor converter transformer $T_2$. The total cost including the interface is therefore given by

$$c_w = c_{ESw} + c_{thy} + c_{Vw} + CST_{T_1} + CST_{T_2} \quad (5.9)$$

The rating of the VSC and the thyristor converter can be estimated as follows.

In the case with the thyristor converter interface, the dc-side voltage of the VSC is supposed to be kept constant at the minimum required value, i.e., $u_d = U_{d,\text{min}}$.

The current from the ES is determined by the delivered power and the terminal voltage of the ES. Thus,

$$i_{ES} = -P_{ES} / u_{ES} \quad (5.10)$$

The current required to charge capacitor $C_2$ has to match the rate of change of $u_{ES}$. Accordingly,

$$i_{C_2} = C_2 \frac{d(u_d - u_{ES})}{dt} = -C_2 \frac{du_{ES}}{dt} \quad (5.11)$$
Therefore, the dc-side current of the thyristor converter is given by
\[
i_{thy} = i_{C2} - i_{ES} = -C_2 \frac{dU_{ES}}{dt} + \frac{P_{ES}}{U_{ES}}
\] (5.12)

The instantaneous power provided by the thyristor converter can now be expressed as
\[
P_{thy} = (u_d - u_{ES})i_{thy}
\] (5.13)

The power rating of the thyristor converter is basically determined by the maximum active power delivery by the converter since the converter should be designed such that the power factor is close to unity when the active power reaches its maximum. Hence, the rating of the thyristor converter is given by:
\[
S_{thy} = P_{thy, max}
\] (5.14)

Since the power provided by the thyristor converter will be circulating through the VSC and the thyristor converter, the VSC has to provide both the circulating power and the power from the energy storage. Accordingly,
\[
P_{V, max} = P_{thy, max} + P_{ES}
\] (5.15)

The required power rating of the VSC including the additional active power support is now obtained as
\[
S_{Vw} = \sqrt{S^2_{base} + P^2_{V, max}}
\] (5.16)

The costs of the dual thyristor converter and the VSC can be estimated as
\[
\begin{align*}
    c_{thy} &= S_{thy} * c_{st_{thy}} / S_{base} \\
    c_{Vw} &= S_{Vw} * c_{st_{V}} / S_{base}
\end{align*}
\] (5.17)

where \(c_{st_{thy}}\) and \(c_{st_{V}}\) are as given in Table 5.1

### 5.2.2.1 Capacitors as ES

**With thyristor converter interface** With capacitors as the ES, (5.13) can be rewritten as:
\[
P_{thy} = \left(\frac{u_d}{u_{ES}} - 1\right)(\frac{C_2}{C_{ES}} + 1)P_{ES}
\] (5.18)
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

For a certain power $P_{ES}$ with a delivery period $t_{ES}$ and a certain energy storage capacitance $C_{ES}$, the minimum ES voltage is determined by:

$$u_{ES,\min} = \sqrt{U_{d,\min}^2 - 2P_{EST}t_{ES}/C_{ES}} \quad (5.19)$$

The maximum power $P_{thy,\max}$ delivered through the thyristor converter is then determined by the minimum ES voltage.

$$P_{thy,\max} = \left(\frac{u_d}{u_{ES,\min}} - 1\right)\left(\frac{C_2}{C_{ES}} + 1\right)P_{ES} \quad (5.20)$$

The costs of the VSC and the thyristor converter can then be estimated from (5.14) through (5.17).

The cost of the ES capacitor can be calculated as:

$$c_{ESw} = \frac{1}{2}C_{ES}U_{d,\min}^2 \ast cst_C/E_{base,C} \quad (5.21)$$

where $E_{base,C} = 100$ MJ is the energy base for capacitors, and $cst_C$ is as given in Table 5.1.

Finally, the total cost with the thyristor converter interface can be obtained with (5.9).

**With direct connection** The cost of the VSC can be calculated from (5.8), with $u_{ES,\max}$ given by

$$u_{ES,\max} = \sqrt{U_{d,\min}^2 + 2P_{EST}t_{ES}/C_{ES}} \quad (5.22)$$

and the cost of the ES can be estimated as

$$c_{ESwo} = \frac{1}{2}C_{ES}u_{ES,\max}^2 \ast cst_C/E_{base,C} \quad (5.23)$$

Finally, the total cost is obtained from (5.7).

5.2.2.2 Supercapacitors as ES

Supercapacitors have a much larger capacitance per cell than conventional capacitors. However, the ESR is also high. A super capacitor can be represented by an internal capacitor and an ESR as shown in Fig. 5.4(a).
Figure 5.4: (a) Representation of a supercapacitor. (b) Supercapacitor terminal voltage (dashed) and internal capacitor voltage (solid) during a discharging/charging cycle.

Commercially available single-cell supercapacitors have a maximum voltage rating of $u_{N1,SC} = 2.7$ V and the capacitance can be as high as $C_{1,SC} = 5000$ F. The ESR of a 2.7 V/5000 F supercapacitor cell can be 0.4 mΩ [62]. Single-cell supercapacitors can be connected in series to reach higher voltage ratings and in parallel to increase the capacitance. With M strings of supercapacitors having N series connected cells in each, the total capacitance, the voltage rating, and the total resistance are given by

$$C_{SC} = \frac{M}{N}C_{1,SC}; \quad u_{N,SC} = N \times u_{N1,SC}; \quad R_{ES} = \frac{C_{1,SC}}{C_{SC}}ESR \quad (5.24)$$

With thyristor converter interface. Equation (5.20) can be used for estimation of the thyristor converter rating but with some modifications.

First, the term $C_2/C_{ES}$ can be neglected since $C_2$ has a much lower value than the supercapacitor capacitance. This simplification yields

$$P_{thy,\text{max}} = \left( \frac{u_d}{u_{ES,\text{min}}} - 1 \right)P_{ES} \quad (5.25)$$
Moreover, the power loss $P_R$ in the ESR should be taken into consideration in the determination of $u_{ES,\min}$.

The power loss $P_R$ varies with the drop of the supercapacitor voltage. To find out the average loss during the power delivery period, the whole period is divided into certain sub-periods with equal durations. The power loss $P_{Rs}$ during each sub-period can be approximated as the average of the losses at the start instant and the end instant of the sub-period and can be obtained as follows.

Start from the first sub-period. At the start instant, the internal voltage of the supercapacitor is $u_{SC1} = U_{d,\min}$ and the current $i_{ES1}$ into the ES is determined by

$$-(u_{SC1} + i_{ES1}R_{ES})i_{ES1} = P_{ES}$$

(5.26)

The current $i_{ES2}$, the internal voltage $u_{SC2}$, and the terminal voltage $u_{ES2}$ of the supercapacitor at the end instant of the sub-period can be obtained together with $P_R$ by numerically solving the equation set:

$$P_{Rs} = (P_{Rs1} + P_{Rs2})/2$$
$$= (i_{ES1}^2 + i_{ES2}^2)R_{ES}/2$$
$$u_{ES2} = u_{SC2} + i_{ES2}R_{ES}$$

(5.27)

$$u_{ES2}i_{ES2} = -P_{ES}$$

$$P_{ES} + P_{Rs})\Delta t = C_{SC}(u_{SC1}^2 - u_{SC2}^2)/2$$

where $\Delta t$ is the time step.

For the following sub-periods, the terminal voltage and the average loss can be obtained from (5.27) with $i_{ES1}$ and $u_{SC1}$ known from the end of the previous sub-period.

The mean value of all the average losses in all the sub-periods gives the overall average loss $P_R$. The terminal voltage $u_{ES,\min}$ at the end instant of the whole discharging process is obtained from the calculation for the last sub-period.
With $P_{\text{thy, max}}$ given by (5.25), the costs of the VSC and the thyristor converter can then be estimated with (5.14) through (5.17).

The cost of the ES is calculated as

$$c_{ESw} = \frac{1}{2} C_{ES} U_{d, \text{min}}^2 \frac{\text{cost}_{SC}}{E_{\text{base, SC}}}$$

(5.28)

where $E_{\text{base, SC}} = 1000 \text{ MJ}$ is the energy base for supercapacitors.

Finally, the total cost with the thyristor converter interface is obtained from (5.9).

Since the re-charging process after the energy delivery can always be controlled slower than the discharging process that is determined by the energy demand of the system, the rating calculations described here are based on the energy delivery process.

**With direct connection** At the end instant of the discharging process, the terminal voltage, internal voltage, and the current of the supercapacitor are determined by

$$u_{ES,f} = U_{d, \text{min}}$$

$$u_{SC,f} = u_{ES,f} - i_{ES,f} R_{ES}$$

$$i_{ES,f} = -\frac{P_{ES}}{u_{ES,f}}$$

(5.29)

To determine the maximum voltage across the supercapacitor, the losses should be taken into account. Similar to the method utilized in the previous sub-section, the whole energy delivery period is divided into equal sub-periods. Calculations are made from the end instant to the start instant of the discharging period with certain time steps. For the first sub-period, the current $i_{ES,f-1}$, the terminal voltage $u_{ES,f-1}$, and the internal $u_{SC,f-1}$ at the start instant $t_{f-1}$, together with the average loss $P_{Rs}$ in the sub-period
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

can be obtained by solving the equation set:

\[
P_{Rs} = \frac{(P_{Rs,f} + P_{Rs,f-1})}{2} = \frac{(i_{ES,f}^2 + i_{ES,f-1}^2)R_{ES}}{2}
\]

\[
u_{ES,f-1} = u_{SC,f-1} + i_{ES,f-1}R_{ES}
\]

\[
u_{ES,f-1}i_{ES,f-1} = -P_{ES}
\]

\[
(P_{ES} + P_{Rs})\Delta t = C_{SC}(u_{SC,f-1}^2 - u_{SC,f}^2)/2
\]

The maximum ES voltage \(u_{ES,\text{max}} = u_{SC,\text{max}}\) is then obtained from the calculation for the last sub-period.

The cost of the VSC can be calculated with (5.8). The cost of the ES can be estimated as

\[
c_{ES\text{wa}} = \frac{1}{2}C_{ES}u_{ES,\text{max}}^2 * c_{st\text{SC}}/E_{\text{base_SC}}\]

Finally, the total cost can be obtained from (5.7).

5.2.2.3 Batteries as ES

The battery voltage does not drop as rapidly as the capacitor voltage does during discharge. However, the final voltage can still be significantly lower than the nominal voltage. Due to the internal resistance, the charging voltage of a battery cell is higher than the nominal voltage. Table 5.3 lists the cell voltages of several battery technologies: sodium/nickel chloride or ZEBRA (zero emission battery research activities) batteries [63], sodium-sulfur (NaS) batteries [64], Ni-Cd batteries [55], lead-acid batteries [65], and lithium-ion (Li-Ion) batteries [66]. As can be seen, the voltage swing of batteries (from the final discharging voltage to the charging voltage) can be as high as 65% (e.g., ZEBRA batteries).

Assume that the charging voltage \(u_{b,chg}\) and the nominal voltage \(u_{b,N}\) are \(x\%\) and \(y\%\) higher than the final discharging voltage \(u_{b,f}\) respectively, i.e.,

\[
u_{b,chg} = (1 + x\%)u_{b,f}
\]

\[
u_{b,N} = (1 + y\%)u_{b,f}
\]
5 Interface between the ES and the dc Link of the VSC

Table 5.3: Cell voltages of different batteries

<table>
<thead>
<tr>
<th>Battery type</th>
<th>Nominal voltage ($u_{b,N}$) (V)</th>
<th>Final voltage ($u_{b,f}$) (V)</th>
<th>Charging voltage ($u_{b,chg}$) (V)</th>
<th>Voltage swing ($u_{b,chg}/u_{b,f} - 1$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZEBRA</td>
<td>2.58</td>
<td>1.72</td>
<td>2.85</td>
<td>65</td>
</tr>
<tr>
<td>NaS</td>
<td>2.08</td>
<td>1.82</td>
<td>2.3</td>
<td>26</td>
</tr>
<tr>
<td>Ni-Cd</td>
<td>1.2</td>
<td>1.0</td>
<td>1.5</td>
<td>50</td>
</tr>
<tr>
<td>Lead-Acid</td>
<td>1.94</td>
<td>1.79</td>
<td>2.3</td>
<td>28</td>
</tr>
<tr>
<td>Li-Ion</td>
<td>3.6</td>
<td>2.7</td>
<td>4.0</td>
<td>48</td>
</tr>
</tbody>
</table>

With the thyristor converter interface  The nominal voltage of the ES battery is designed to be the same as the dc-link voltage of the VSC in this case, i.e., $u_{b,N} = u_d = U_{d,\text{min}}$. When charging the battery, the dual-thyristor converter should be controlled to provide a negative voltage across capacitor $C_2$ such that the required charging voltage is supplied while the dc-side voltage of the VSC is kept constant. Correspondingly, the final discharging voltage should be:

$$u_{b,f,w} = U_{d,\text{min}}/(1 + y\%)$$ (5.33)

Since the voltage changing rate of the battery is moderate and $C_2$ is small, the charging current given in (5.11) is much smaller than the energy storage current in (5.12) and can thus be neglected in the thyristor converter rating calculation:

$$P_{\text{thy,max}} \approx \left( \frac{u_d}{u_{ES,\text{min}}} - 1 \right) P_{ES} = y\%P_{ES}$$ (5.34)

The costs of the thyristor converter and the VSC are then determined by (5.14) through (5.17).

The cost of the battery is determined by the energy level almost independently of the voltage level. Hence, this cost will remain unchanged no matter whether there is an interface or not and it is given by

$$c_{ES} = P_{ES} \times t_{PES} \times c_{st_{\text{btr}}} / E_{base,b}$$ (5.35)
where \( c_{st_{btr}} \) is as given in Table 5.1. \( P_{ES} \) and \( t_{PES} \) are in MW and minute, respectively.

Finally, the total cost with the thyristor converter interface can be obtained from (5.9).

### With direct connection

In case of direct connection, the battery voltage at the end of discharge should not be lower than the minimum VSC dc-link voltage required for reactive power delivery, i.e., \( u_{b,f} = U_{d,\text{min}} \).

The VSC rating has to be increased to:

\[
S_{Vw_0} = (1 + x\%)S_{\text{base}} \tag{5.36}
\]

and the cost of the VSC can be calculated as:

\[
c_{Vw_0} = 1 + x\% \tag{5.37}
\]

The total cost without interface is then obtained from (5.7).

### 5.2.3 Cost Comparison

#### 5.2.3.1 Capacitors as ES

The capacitors are supposed to deliver 20 MW for 0.5 s. The delivered energy is 10 MJ. In sizing the capacitors for energy storage, optimization must be done regarding the capacitance and the voltage variation since the stored energy can be increased either by increasing the capacitance or by raising the capacitor voltage. The total cost as a function of capacitance is plotted in Fig. 5.5a.

It can be seen that the optimum capacitance values are 5000 \( \mu \text{F} \) (at a voltage level of 89 kV, corresponding to an energy level of 19.8 MJ) without interface and 7000 \( \mu \text{F} \) (at a voltage level of 62.6 kV, corresponding to an energy level of 13.7 MJ) with interface. The optimum designs are marked with asterisks.
Figure 5.5: Total cost and voltage swing as functions of the capacitance of ES capacitor, with (solid) and without (dashed) interface.

The total cost can be reduced from 2.66 pu to 2.28 pu by utilization of the proposed interface, corresponding to a reduction of 38% of the cost of a 100 MVA VSC. With the optimum designs, the voltage swing (relative to $U_{d,min}$) is between 100% and 52% for the case with interface and between 100% and 142% for the case without interface, as shown in Fig. 5.5b. Fig. 5.6 shows the accumulated cost of the different parts for both the cases with and without interface.

5.2.3.2 Supercapacitors as ES

The supercapacitors are supposed to deliver 20 MW for 30 s. The corresponding energy is 600 MJ.

As can be seen from Fig. 5.7, the optimum design without interface is obtained with supercapacitor banks of 0.23 F and a voltage level of 110 kV (57% higher than $U_{d,min}$). With interface, the optimum capacitance is 0.4288 F.
with a voltage level equal to $U_{d,\text{min}}$. The voltage drops to 45% of $U_{d,\text{min}}$ at the end of the energy delivery period. The power losses in supercapacitors are depicted in Fig. 5.9, which shows higher losses with the thyristor converter interface. The total cost can be reduced from 3.29 pu to 2.74 pu by utilization of the thyristor converter interface. The accumulated cost of different parts is plotted in Fig. 5.8.
5 Interface between the ES and the dc Link of the VSC

Figure 5.7: Total cost and voltage swing as functions of the capacitance of ES supercapacitor, with (solid) and without (dashed) interface.

5.2.3.3 Batteries as ES

In order to plot the cost as a function of battery voltage swing $x\%$, the quantity $y\%$ has to be determined. As listed in Table 5.3, the difference between $x\%$ and $y\%$ does not vary very much for different batteries. It is in the range of 12% to 20%. Thus, by taking an intermediate value of 16%, $y\%$ can be approximated as $y\% = x\% - 16\%$.

The cost as a function of battery voltage swing $x\%$ is plotted in Fig. 5.10 for both the cases with and without interface.

The figure shows that when the voltage swing exceeds 12%, the total cost can be reduced by utilization of the proposed converter interface. The cost saving increases with the increase of the voltage swings. For NaS batteries that have a voltage swing of approximately 26%, the cost saving is 0.13 pu (4.01 pu vs. 3.88 pu). For ZEBRA batteries, however, the voltage swing is
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

![Diagram showing cost estimation with direct connection and proposed interface topology.](image)

(a) With interface

(b) Without interface

Figure 5.8: Accumulated cost with supercapacitors as ES.

![Diagram showing losses in supercapacitor.](image)

Figure 5.9: Losses in supercapacitor.
as high as 66% and the cost can be reduced from 4.41 pu to 3.94 pu.

Since the battery cost is common to both the two cases, a clear picture of the cost saving (as a result of utilization of the proposed interface topology) as a function of battery voltage swing can be obtained regardless the cost of batteries. This cost saving curve is depicted in Fig. 5.11.

The accumulated cost depicted in Fig. 5.12 shows that the battery cost becomes more dominating in the total cost for larger amounts of energy delivery. Therefore, the cost is the main hurdle to the application of batteries in large scales.
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

![Diagram showing cost estimation with direct connection and the proposed interface topology.](image)

(a) With interface

(b) Without interface

Figure 5.12: Accumulated cost with batteries as ES.

5.2.4 Cost Comparison with Capacitors, Supercapacitors, and Batteries in One Time Frame

This section presents a cost comparison for different types of energy storage with the same varying active power delivery period. For each active power delivery period, an optimization is made for capacitor and supercapacitor ES for both the cases with and without thyristor converter interface following the procedure described in Section 5.2.2.

One factor that has to be taken into consideration in making this comparison
is that the capacity of batteries reduces with the increase of the discharging speed. Batteries are usually designed for long-period power delivery. The nominal capacity of batteries is usually defined as the available ampere-hours (Ah) at 5 hours discharge to a certain end voltage. However, the capacity will reduce significantly if the batteries are discharged quickly. As an example, Fig. 5.13 shows the normalized capacity of a Ni-Cd battery as a function of discharging periods [55]. The capacities corresponding to different discharging periods are normalized with respect to the nominal capacity as defined above. It can be seen that the capacity reduces dramatically at discharges shorter than 25 minutes. In the following comparisons, the capacity reduction of batteries will be taken into account. The voltage swing is assumed to be 50%.

Another factor to be considered is the energy efficiency of supercapacitors. Fig. 5.14 depicts the energy efficiency as a function of the active power delivery period for the optimum cases. The efficiencies are calculated as the ratio of the delivered power to the sum of the delivered power and the losses in supercapacitors. It can be seen that in order to reach a reasonable efficiency, e.g., 95%, the power delivery period should be longer than 27 s with the interface and 10 s without the interface.

In the following comparisons, the cost with supercapacitors as the ES is estimated with an energy efficiency of 95%. Since the efficiency increases with the increase of the size of supercapacitors, the total cost might increase as a
5.2 Cost Estimation with Direct Connection and with the Proposed Interface Topology

result. Therefore, with the limitation on the energy efficiency, the solutions with supercapacitors might not be the cost-optimized cases.

The estimated costs for the two cases with three different energy storage types are depicted in Fig. 5.15(a) for periods ranging from 0.1 s to 1.5 min., and in Fig. 5.15(b) from 0.05 s to 0.4 s.

Due to the low cost per energy unit of battery energy storage, the solution with batteries becomes cheaper than that with supercapacitors for power delivery periods longer than 63 s with the interface and 45 s without the interface. The solution with capacitors is cheaper than that with supercapacitors only when the energy delivery period is shorter than 317 ms with the interface and 136 ms without the interface. If the requirement on the energy efficiency becomes stricter, e.g., 98%, these two intersections will be pushed rightward to 1 s and 500 ms, respectively.

As can be observed from the two lines for supercapacitor costs in Fig. 5.15, the solution with interface is not always cheaper than without interface. The reason is that the cost is estimated with an efficiency of 95% rather than for the cost-optimized case with a lower efficiency. The intersection of these two lines is at 3 s.

In this comparison, the life time of the ES and the losses in the ES have not been taken into account. Of the three types of ES, batteries have the

![Energy efficiency vs. power delivery period: with interface (solid) and without interface (dashed).](image)
shortest life time in terms of maximum number of charging-discharging cycles. Depending on the pattern of the active power delivery (occasionally or frequently), the choice of the type of ES should also take these factors into consideration. For instance, with optimum cases, the losses in supercapacitors become higher with the decrease of the discharging period. A trade-off must be made between the initial cost and the power loss afterwards. If a loss penalty and the cost for cooling are added to the total cost, the intersection in Fig. 5.15(b) would be pushed considerably rightward. Capacitors have the lowest losses and the least demand on maintenance. For frequent active power deliveries with very short period, the solution with capacitors might be the most attractive one.
5.3 Design of the Interface Control System

5.2.5 Conclusion

Integration of energy storage into a VSC involves connection of the energy storage on the dc side of the VSC. Charging and discharging processes of energy storage devices cause considerable voltage swings. As a result, the VSC rating has to be increased if the energy storage devices are connected directly to the dc-link. The study shows that the total cost can be reduced by introducing the proposed dual thyristor converter as the interface between the energy storage and the dc link of the VSC. The cost comparison between different types of ES, even considering the rough simplification and the uncertainty of cost figures, provides a guideline for the choice of ES at energy levels where several alternatives are available.

5.3 Design of the Interface Control System

In this section, the dynamics of the proposed interface topology are investigated. As already stated, the proposed topology is suitable for high-power high-voltage applications where a StatCom is required to deliver a moderate amount of active power (e.g., 20% of the rated power) in addition to the reactive power support. The investigation is performed with the system shown in Fig. 5.1. Control strategies are presented for a StatCom with ES and with the proposed dual thyristor converter as the interface. The focus is on active power compensation and the control of the dc-side voltage of the VSC.

Large capacitor banks are considered as the ES in this investigation. Capacitors are suitable ES devices that can be integrated into a StatCom for compensation of cyclic loads with cycle times in the range of seconds, e.g., the application investigated in Section 4.2 and in [54]. Furthermore, capacitors present the most demanding requirement for the control of the interface circuit. Simulation results are also presented to verify the proposed control strategies.

There are two control strategies in use for dual thyristor converters, namely
circulating-current control and circulating-current-free control [67,68]. With circulating-current-free control, the dc terminals of the two bridges are connected together directly, as shown in Fig. 5.1. Only one of the two thyristor bridges can be active at any time. With circulating current control, on the other hand, both of the two thyristor bridges are active all the time. The average output direct voltages of these two bridges have approximately the same amplitude but opposite polarity. The sum of the instantaneous terminal voltages of these two bridges creates a current that circulates in these two bridges. In order to limit the ripple in the circulating current, inductors are connected between two bridges. The system diagram with circulating-current control is depicted in Fig. 5.16. Both methods are investigated and a comparison is made in the end of the section.

5.3.1 System Control Using Circulating-current-free Control Method for the Dual Thyristor Converter

5.3.1.1 Overview of the Control System

The block diagram of the control system is depicted in Fig. 5.17. The VSC control system consists of two control loops: the inner current control loop...
and the outer voltage control loop. The inner control loop utilizes deadbeat current control combined with a flux modulation scheme as suggested in Section 2.2. The outer control loop controls the ac-side flux and the dc-side voltage and gives the references for the converter current components in the inner loop.

The magnitude of the positive sequence flux at the PCC is controlled close to the nominal value by a PI controller. The controller output provides the reference for the positive sequence reactive current \( (i^d_{v,p,ref}) \). Both the \( d \) and \( q \) component of the negative sequence bus flux are controlled to zero respectively by two PI controllers, which deliver the references for the \( d \) and \( q \) components of the negative sequence converter current \( (i^d_{v,n,ref} \) and \( i^q_{v,n,ref}) \). The references for the offset \( \alpha \) and \( \beta \) components of the converter current are set to zero as desired. All the three PI controllers utilized in the outer control loop have the form:

\[
G_k = k_p + \frac{1}{s\tau_i}
\]  

(5.38)

where \( k_p \) is the proportional gain, \( \tau_i \) is the integration time constant, and \( s \) is the Laplace variable.

The control of the dc-side voltage \( u_d \) is achieved by controlling the terminal voltage \( u_{ES} \) of the ES capacitor and the voltage \( u_{C2} \) across capacitor \( C_2 \) individually. The reference for \( u_{C2} \) is always set to the difference between the reference for \( u_d \) and for \( u_{ES} \). As a result, the dc-side voltage of the VSC will be kept constant.

The ES terminal voltage controller together with the active power compensation block provides the reference for the positive sequence active current \( (i^q_{v,p,ref}) \). The \( u_{C2} \) controller provides the reference value for the output direct voltage of the dual thyristor converter.

The active power compensation scheme and the control of the dc-side voltage of the VSC will be described in detail in the following sections.
5 Interface between the ES and the dc Link of the VSC

5.3.1.2 Active Power Compensation

The compensation scheme is depicted in Fig. 5.18. The active power that the VSC is supposed to deliver is $P_{ES,ref}$. It is taken as a feed-forward signal to command the required active current $i_{v,p,ref,ff}^q$ from the VSC. This current reference has to be limited according to the status of the ES energy, and the reference for the ES energy is modified based on the estimated energy change. The sum of the output from the ES energy controller and the feed-forward reference gives the reference for the positive sequence active current of the VSC. The reference for $u_{C_2}$ is obtained as the difference between the references for the dc-side voltage of the VSC and for the ES terminal voltage. A detailed description about the limitation of the feed-forward reference and the modification of the ES energy reference can be found in Section 4.1.1.1.
5.3 Design of the Interface Control System

5.3.1.3 Control of the ES Terminal Voltage

**Plant Model**  With the definition of the directions of the currents and voltages on the dc side of the VSC as shown in Fig. 5.1, the active power $P_d$ flowing from the dc side toward the VSC can be obtained as

$$
P_d = i_d u_d = (i_{thyd} - i_{C1} - i_{C2})(u_{C2} + u_{ES})

= i_{thyd} u_{C2} - i_{C1} u_d - i_{C2} u_{C2} - i_{ES} u_{ES}

= P_{thy} - \frac{dW_{C1}}{dt} - \frac{dW_{C2}}{dt} - \frac{dW_{ES}}{dt}

(5.39)
$$

where $P_{thy}$ is the power delivered from the thyristor converter; $W_{C1}$, $W_{C2}$, and $W_{ES}$ are the energies stored in the capacitors $C_1$, $C_2$, and the ES capacitor, respectively. If the power loss in the converter bridge and in the inductor are neglected, $P_d$ equals the power flowing from the ac side of the VSC to the network. This power is given by

$$
P_{ac} = \frac{3}{2} \omega (\psi_{B,p}^d i_{v,p}^d - \psi_{B,p}^q i_{v,p}^q)

(5.40)
$$

where $\psi_{B,p}^d$ and $\psi_{B,p}^q$ are the positive sequence dq components of the bus flux, $i_{v,p}^d$ and $i_{v,p}^q$ are the positive sequence components of the converter current, and $\omega$ is the angular frequency of the bus flux. In (5.40), the negative sequence power is disregarded.

Since the PLL locks on the positive sequence of the bus flux, $\psi_{B,p}^d$ is very
close to zero. The active power can, therefore, be approximated as

$$P_{ac} = \frac{3}{2} \omega \psi_{B,p}^d i_{v,p}^q$$  \hspace{1cm} (5.41)

Combining (5.39) and (5.41) results in

$$\frac{dW_{ES}}{dt} = P_{thy} - \frac{dW_{C2}}{dt} - \frac{dW_{C1}}{dt} - \frac{3}{2} \omega \psi_{B,p}^d i_{v,p}^q$$  \hspace{1cm} (5.42)

which can be rewritten as

$$\frac{dW_{ES}}{dt} = -\frac{3}{2} \omega \psi_{B,p}^d i_{v,p}^q + d$$  \hspace{1cm} (5.43)

where $d = P_{thy} - \frac{dW_{C2}}{dt} - \frac{dW_{C1}}{dt}$ can be seen as a disturbance to the plant.

The linearity between the derivative of $W_{ES}$ and $i_{v,p}^q$ shown in (5.43) suggests that it is advantageous to control the energy stored in the ES capacitor instead of the ES terminal voltage itself. Applying the Laplace transform to (5.43) gives the following plant model:

$$G_p(s) = \frac{W_{ES}(s)}{-I_{v,p}^q(s)} = \frac{a}{s}$$

$$G_d(s) = \frac{W_{ES}(s)}{d(s)} = \frac{1}{s}$$  \hspace{1cm} (5.44)

where $a = \frac{3}{2} \omega \psi_{B,p}^d$.

**Controller Design**  For the plant model given in (5.44), the controller design procedure described in Section 2.3.2 can be employed.

The controller is a PI controller of the form as given in (5.38) with

$$k_p = 1/(a \tau_c)$$

$$\tau_i = (a \tau_c R_{virt} C_{ES})/2$$  \hspace{1cm} (5.45)

where $1/\tau_c$ is the bandwidth of the closed loop system, and $R_{virt}$ is the virtual resistance introduced for active damping. The resulting closed-loop transfer functions for reference tracking and disturbance rejection are:

$$G_{cr} = \frac{1}{1 + \tau_c s}$$

$$G_{cd} = \frac{\tau_c s}{(1 + \tau_c s)(s + 2/R_{virt} C_{ES})}$$  \hspace{1cm} (5.46)
5.3 Design of the Interface Control System

5.3.1.4 Control of the Voltage across Capacitor C2

Overview of the Control and Triggering System With circulating-current-free control, the dc terminals of the two bridges are connected together directly, as shown in Fig. 5.1. Only one of the two thyristor bridges should be active at any time. To prevent any short-circuit between the two bridges, the up-coming thyristor bridge should not be triggered until the current in the off-going bridge goes down to zero. In practice, the triggering of the up-coming bridge is further delayed with a certain time (in the range of 2-5 ms) [67] known as ‘dead time’. Fig. 5.19 shows the control and triggering scheme for the dual thyristor converter. First the firing angle $\alpha_1$ for the positive bridge is calculated from the reference value of the converter output voltage $u_{thyd,ref}$, which is given by the $C_2$ voltage controller. The firing angle for the negative bridge is determined by:

$$\alpha_2 = 180^\circ - \alpha_1$$  \hspace{1cm} (5.47)

In order to avoid commutation failures, this angle should be limited to the maximum allowed firing angle for the thyristors, e.g., $165^\circ$.

After the triggering pulses for both of the two bridges are generated, only one set of pulses for either the positive or negative bridge is sent out. The selection of the bridge to be triggered depends on the information of the dc current $i_{thyd}$ of the dual thyristor converter and its reference $i_{thyd,ref}$ in a way as shown in Table 5.4. In the table, the ‘+’ and ‘−’ signs represent the positive and negative thyristor bridges, respectively. Take the right column as an example, where the reference for the thyristor current is negative. If the thyristor current is positive at a certain time, i.e., the positive bridge is...
5 Interface between the ES and the dc Link of the VSC

Table 5.4: Rules for triggering pulse selection

<table>
<thead>
<tr>
<th>$i_{thyd,ref} &gt; 0$</th>
<th>$i_{thyd,ref} = 0$</th>
<th>$i_{thyd,ref} &lt; 0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{thyd} &gt; 0$</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>$i_{thyd} = 0$</td>
<td>+</td>
<td>none</td>
</tr>
<tr>
<td>$i_{thyd} &lt; 0$</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

conducting, then it should continue conducting until the current goes down to zero. Therefore, the triggering pulses for the positive bridge are sent out at this time. When the thyristor current becomes zero, the negative bridge can be triggered and should continue conducting as long as the current is negative.

Design of the controller for the voltage across capacitor $C_2$ For the dc-side circuit in Fig. 5.1, the following equations hold:

$$L \frac{di_{thyd}}{dt} = u_{thyd} - u_{C_2}$$
$$C_2 \frac{du_{C_2}}{dt} = i_{ES} + i_{thyd}$$

(5.48)

Here, the resistance in the inductor is ignored. Since the dc current together with its reference must be accessible for the triggering system, it is straightforward to control the dc current in an inner loop of the control system for $u_{C_2}$.

The control structure is depicted in Fig. 5.20. The thyristor current is controlled by controller $G_{k1}(s)$ and its reference is given by the output of the controller $G_{k2}(s)$ for $u_{C_2}$.

When designing the controller, the thyristor converter can be modeled as a proportional gain 1 as long as the bandwidth of the $u_{C_2}$ control loop is smaller than $\omega_6/2$ [69], where $\omega_6 = 600\pi$ is the angular frequency of 6th harmonic in a 50Hz system.

As can be seen, the input, output, and control variables are interrelated in different loops. However, Fig. 5.20 can be re-drawn, after some manipula-
5.3 Design of the Interface Control System

Figure 5.20: Block diagram of the controller for the voltage across capacitor C2

Figure 5.21: Block diagram of the controller for the voltage across capacitor C2

The three shaded parts in the figure can be represented by three blocks with the following transfer functions:

\[
G_k(s) = G_{k2}(s) + \frac{1}{G_{k1}(s)} \quad (5.49)
\]
\[
G_{p1}(s) = \frac{G_{k1}(s)}{sL + G_{k1}(s)} \quad (5.50)
\]
\[
G_{p2}(s) = \frac{1}{sC_2} \quad (5.51)
\]

Fig. 5.21 may be further transformed into Fig. 5.22 with \( G_p(s) \) given by

\[
G_p(s) = G_{p1}(s)G_{p2}(s) \quad (5.52)
\]

The current \( i_{ES} \) to the energy storage can be seen as a disturbance entering at the plant output through the block \( G_{p2}(s) \).

Now, the control design has developed into a two-step design problem: design of \( G_{k1}(s) \) for the plant \( 1/(sL) \) and design of \( G_k(s) \) for the plant \( G_p(s) \)
with the disturbance $i_{ES}$.

Since the plant is an integrator, a proportional control $G_{k1}(s) = k_{p1}$ will result in a closed-loop system that behaves as a low-pass filter with a bandwidth of $\omega_{B1} = k_{p1}/L$:

$$G_{p1}(s) = \frac{k_{p1}}{sL + k_{p1}} \quad (5.53)$$

With $G_{p1}(s)$ given in (5.53), the plant $G_p(s)$ becomes:

$$G_p(s) = \frac{1}{LC_2} \frac{k_{p1}}{s + k_{p1}/L} \quad (5.54)$$

The plant has two poles, one of them at the origin. A proportional controller will result in a closed-loop bandwidth smaller than 212 rad/s if the damping ratio should be kept higher than 0.707. In order to speed up the response, a lead-lag compensator should be included. However, the steady state error caused by disturbances cannot be eliminated with only lead-lag compensation. This can be seen from the transfer function from the disturbance $i_{ES}$ to $u_{C2}$:

$$G_{cd}(s) = \frac{G_{p2}}{1 + G_p(s)G_k(s)} \quad (5.55)$$

The transfer function in (5.55) implies that the controller must have an integration function to achieve a good disturbance rejection at low frequencies. Therefore, a controller with the following form is proposed:

$$G_k(s) = K \frac{s + z_i}{s} \frac{1 + s/z}{1 + s/p} \quad (5.56)$$
5.3 Design of the Interface Control System

The zero-pole pair \((-z, -p)\) cancels the plant pole at \(-k_{p1}/L\) and places the pole at a desired location. The purpose of the zero at \(-z_i\) is to shape the closed-loop root locus and can be chosen close to the origin.

Finally, the controller \(G_{k2}(s)\) is obtained as

\[
G_{k2}(s) = G_k(s) - 1/G_{k1}(s)
\] (5.57)

**Control Action in the Idle-mode** The idle-mode here is defined as the operation mode when no active power support is required, i.e., all the three conditions below are met:

\[
|i_{v,p,ref}| < \varepsilon_1 \quad \& \\
|u_{C2,ref}| < \varepsilon_2 \quad \& \\
|u_{C2} - u_{C2,ref}| < \varepsilon_3
\] (5.58)

where \(\varepsilon_1\), \(\varepsilon_2\) and \(\varepsilon_3\) are the threshold values for the \(i_{v,p}\) reference, the \(C_2\) voltage reference, and the \(C_2\) voltage error, respectively.

Depending on the characteristics of the applications that the active power support is employed for, the \(C_2\) voltage controller can either be active continuously (for, e.g., cyclic active power support applications) or be active on demand (for, e.g., occasional active power support applications). In the latter case, if the system is detected as idling, the current reference for the dual thyristor converter is set to zero and the integral action in the \(C_2\) voltage controller is stopped. By doing this, unnecessary charging/discharging of capacitor \(C_2\) in the idle-mode can be avoided.

**5.3.1.5 Simulation Results**

Simulations have been performed with the system shown in Fig. 5.1 and the controllers described above. The system parameters are listed in Table 5.5. The StatCom delivered 20 MW active power from time 0.2 s to 0.7 s and was re-charged slowly afterwards.
Table 5.5: System parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer T1</td>
<td>100 MVA; 138 kV / 38.49 kV</td>
</tr>
<tr>
<td>Transmission line</td>
<td>165 km, short circuit power at the PCC: 275 MVA</td>
</tr>
<tr>
<td>Load</td>
<td>110 MW, 40 MVar</td>
</tr>
<tr>
<td>VSC rated power</td>
<td>100 MVA</td>
</tr>
<tr>
<td>VSC rated current</td>
<td>1.5 kA</td>
</tr>
<tr>
<td>VSC dc-side voltage</td>
<td>75 kV</td>
</tr>
<tr>
<td>Phase reactor</td>
<td>$L_v = 7.07$ mH (0.15 pu), $R_v = 0$</td>
</tr>
<tr>
<td>Transformer T2</td>
<td>20 MVA; 38.49 kV / 28 kV</td>
</tr>
<tr>
<td>Thyristor converter rated current</td>
<td>0.6 kA</td>
</tr>
<tr>
<td>Thyristor converter dc-side Inductor</td>
<td>$L = 0.1$ H</td>
</tr>
<tr>
<td>Capacitors</td>
<td>$C_1 = 450$ μF, $C_2 = 450$ μF, $C_{ES} = 5400$ μF</td>
</tr>
<tr>
<td>Time varying load</td>
<td>20 MW for 0.5 s</td>
</tr>
</tbody>
</table>

Table 5.6: VSC Outer Loop Controller Gains

<table>
<thead>
<tr>
<th>Controller</th>
<th>Proportional gain</th>
<th>Integration time constant</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCC voltage magnitude controller</td>
<td>5.9 pu / pu</td>
<td>7.4 ms</td>
</tr>
<tr>
<td>Negative sequence bus flux/voltage controller</td>
<td>5.9 pu / pu</td>
<td>7.4 ms</td>
</tr>
<tr>
<td>Energy controller</td>
<td>$\tau_c = 0.0075$ s, $R_{virt} = 1.85$ kΩ</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.6 and Table 5.7 give the controller parameters used in the simulations for the outer and inner loop controllers of the VSC respectively.

The controller parameters for $G_{k1}(s)$ and $G_k(s)$ are listed in Table 5.8, which
result in a closed-loop bandwidth of 934 rad/s. The parameters are chosen based on the following consideration.

When controlling the thyristor converter dc-current, a faster current response requires more control effort, which means a higher voltage rating of the thyristor converter. Hence, the bandwidth of the inner current control loop should not be chosen higher than necessary. As can be derived from \(5.48\), the voltage rating of the thyristor converter is related to the bandwidth by

\[
U_{thyd} = (u_{C_2,ref} + \omega B_1 L \Delta i_{thyd})_{\text{max}}
\]

where \(\Delta i_{thyd}\) is the error signal to the controller.

A reasonable bandwidth of \(\omega_{B_1} = 300\) rad/s is chosen for the simulations. The corresponding proportional gain is \(k_{p1} = 30\) kV/kA.

With the specified system parameters, the resulting plant \(G_p(s)\) has a pole at -300 and a pole at the origin. For the lead-lag compensator, the zero is set to \(-z = -300\) to cancel the plant pole. The pole is set to approximately two times the desired closed-loop bandwidth, i.e., \(-p = -1900\) such that the closed-loop system is well damped with the desired bandwidth. Another zero \(-z_i\) of \(G_k(s)\) is set to -30, far away from the crossover frequency such that the reduction in the phase margin is small.

In the root locus plot in Fig. 5.23, it can be found that a gain of
$K = 0.22 \text{ kA/kV}$ results in two equal real poles at -934 and a third pole at -32. The third pole is very close to the zero at -30. The effect of this pole is almost canceled. The closed-loop performance is dominated by the two equal real poles. The closed-loop bandwidth is smaller than $\omega_b/2$ and satisfies the assumption that the controller design is based on.

The results from the simulations in PSCAD are plotted in Fig. 5.24 through Fig. 5.27.

The dc-side voltage of the VSC, the voltage of the ES, and the voltage across capacitor $C_2$ are plotted in Fig. 5.24 for one discharging/charging cycle, and zoomed in Fig. 5.25. It can be seen that the dc-side voltage of the VSC was kept almost constant except during two small transients, which occurred immediately after the commencement of the discharging and charging processes. These transients were reflections of the transients in $u_{C_2}$, which were caused by the fast change in the charging and discharging current of the ES. The reason is that $i_{ES}$ acts as a disturbance to the $u_{C_2}$ control loop. It should be mentioned that no noticeable transient can be observed in the ac-side quantities (not shown) during this period.
5.3 Design of the Interface Control System

Figure 5.24: Dc-side voltages: VSC dc-side voltage (solid); ES terminal voltage (dashed); \( C_2 \) voltage (bold-solid).

Fig. 5.26 depicts the active power flow during the active power delivery period. The ES was controlled to deliver the required active power. The active power from the dual thyristor converter was the circulating power as explained in Section 5.1.2. The peak of the circulating power in this case was approximately 14 MW.

Fig. 5.27 shows the dc current from the dual thyristor converter. It can be seen that none of the two thyristor bridges was conducting when the system was idling.

In the design above, high bandwidths have been selected. It should be remarked that the design is robust even if the bandwidth is reduced.
5 Interface between the ES and the dc Link of the VSC

Figure 5.25: Dc-side voltages (zoomed): (a) VSC dc-side voltage; (b) ES terminal voltage; (c) voltage across capacitor $C_2$.

5.3.2 System Control Using Circulating-current Control Method for the Dual Thyristor Converter

5.3.2.1 Overview of the Control System

The system configuration is depicted in Fig. 5.16 and the block diagram of the control system in Fig. 5.28. The control structure is the same as that with the circulating-current-free control method, except the addition of the circulating-current control loop. The same design procedures as described in Section 5.3.1 can be adopted for the active power compensation, the control
5.3 Design of the Interface Control System

Figure 5.26: Active power flow during the energy delivery period: from the dual thyristor converter (solid); from the VSC (dashed); from the ES (bold-solid).

Figure 5.27: Dual thyristor direct current during the energy delivery period.

of ES terminal voltage, and the control of $u_{C2}$.

The triggering scheme for the thyristor converters is depicted in Fig. 5.29. Let the firing angles for these two converters be $\alpha_1$ and $\alpha_2$ respectively. The sum of these two angles is controlled around 180° such that the average output voltages from the two converters are very close. The difference in the instantaneous terminal voltages creates a circulating current with a derivative limited by the four inductors in between the two converters. The circulating current is controlled with variable $\beta$ and the two firing angles are related such that [68]:

$$165$$
5. Interface between the ES and the dc Link of the VSC

Figure 5.28: Overview of the control system.

Figure 5.29: Overview of the control and triggering scheme for the dual thyristor converter with circulating-current control
5.3 Design of the Interface Control System

\[ \alpha_1 + \alpha_2 = 180^\circ - \beta \]  
(5.60)

With \( u_{thyd,ref} \) and \( \beta \) determined by the \( uC_2 \) controller and the circulating-current controller respectively, an angle \( \alpha \), which can be seen as the pre-calculated firing angle for the plus bridge, can be obtained:

\[ \alpha = \cos^{-1}\left(\frac{u_{thyd,ref}}{1.35U_{LL} \cos(\beta/2)}\right) \]  
(5.61)

where \( U_{LL} \) is the RMS value of the line-to-line voltage of the thyristor converter.

The actual firing angles for these two thyristor converters are determined by

\[ \alpha_1 = \alpha - \beta/2 \]
\[ \alpha_2 = 180^\circ - \beta/2 - \alpha \]  
(5.62)

In order to avoid commutation failures, this angle should be limited to the maximum allowed firing angle for the thyristors, e.g., 165\(^\circ\).

5.3.2.2 Control of the Circulating Current

In order to design a controller for the circulating current, the plant model will be derived. The circuit equation can be written as

\[ L \frac{di_{crcl}}{dt} = \frac{u_{thyd1} + u_{thyd2}}{4} - \text{sign}(i_{thyd}) \left( \frac{L}{2} \frac{di_{thyd}}{dt} \right) \]  
(5.63)

Each quantity in (5.63) contains a dc (average) component and a ripple component. Since only the average component of the circulating current will be controlled, (5.63) can be re-written in terms of the average components of the quantities:

\[ L \frac{\bar{d}i_{crcl}}{dt} = \frac{\bar{u}_{thyd1} + \bar{u}_{thyd2}}{4} - \text{sign}(i_{thyd}) \left( \frac{L}{2} \frac{\bar{d}i_{thyd}}{dt} \right) \]  
(5.64)

The average output voltages of the two thyristor converters are determined by the firing angles according to

\[ \bar{u}_{thyd1} = \frac{3\sqrt{2}}{\pi} U_{LL} \cos(\alpha - \frac{\beta}{2}) \]
\[ \bar{u}_{thyd2} = \frac{3\sqrt{2}}{\pi} U_{LL} \cos(180^\circ - \frac{\beta}{2} - \alpha) \]  
(5.65)
The sum of these two is

\[ \bar{u}_{thyd1} + \bar{u}_{thyd2} = \frac{6\sqrt{2}}{\pi} U_{LL} \sin \alpha \sin \frac{\beta}{2} \]  

(5.66)

Since \( \beta \) is always small, \( \sin(\beta/2) \) can be approximated as \( \beta/2 \). Consequently, the linearized plant model is obtained as

\[ \bar{I}_{crcl}(s) = \frac{a}{4Ls} \beta(s) - \frac{1}{2} \text{sign}(i_{thyd}) I_{thyd}(s) \]  

(5.67)

where \( a = (3\sqrt{2}/\pi)U_{LL} \sin \alpha \) is the plant gain, and \( i_{thyd} \) can be seen as a disturbance to the plant.

For the purpose of active damping, an internal feedback of \( G_{ad} = 4Lp_{ad}/a \) is introduced as shown in Fig. 5.30. The plant model (the shaded part) becomes:

\[ G_p'(s) = \frac{\bar{I}_{crcl}(s)}{\beta'(s)} = \frac{a}{4L(s + p_{ad})} \]  

(5.68)

where \(-p_{ad}\) is the introduced pole.

The IMC design gives the following controller:

\[ G_k(s) = \frac{4L}{a\tau_c} + \frac{4Lp_{ad}}{a\tau_c} \frac{1}{s} = k_p + \frac{1}{\tau_i s} \]  

(5.69)

where \( 1/\tau_c \) is the bandwidth of the closed-loop transfer function. This is a PI controller with a proportional gain \( k_p = 4L/(a\tau_c) \) and an integration
### 5.3 Design of the Interface Control System

#### Table 5.9: Parameters for $C_2$ Voltage and Circulating Current Controllers

<table>
<thead>
<tr>
<th>Circulating current controller</th>
<th>$k_p$ (rad/kA)</th>
<th>$\tau_i$ (ms)</th>
<th>$\tau_c$ (s)</th>
<th>$p_{ad}$</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.58</td>
<td>63</td>
<td>0.01</td>
<td>10</td>
<td>0.075 kA</td>
</tr>
</tbody>
</table>

It should be pointed out that this is an adaptive controller since the gains are variable due to the presence of the controlled firing angle.

### 5.3.2.3 Simulation Results

Simulations have been performed with the system shown in Fig. 5.16 and the controllers described above. The system parameters are the same as those listed in Table 5.5 except the dc-side inductance of the dual thyristor converter. Instead of one 0.1 H inductor, there are four inductors with a inductance of 0.15 H for each. The StatCom delivered 20 MW active power from time 0.2 s to 0.7 s and was re-charged slowly afterwards.

The controller parameters used in the simulations for the outer and inner loop controllers of the VSC are the same as those listed in Table 5.6 and Table 5.7 except that the bandwidth of the energy controller is slightly smaller ($\tau_c = 0.009$ s compared to 0.0075 s) with circulating current. The reason is that the energy control loop is coupled with the $u_{C2}$ control loop due to the existence of the circulating-current control loop. In order to achieve system stability, the bandwidth of the energy controller has to be kept sufficiently lower than the bandwidth of the $u_{C2}$ controller, which is 934 rad/s.

The parameters for the $u_{C2}$ controller are the same as listed in Table 5.8. The parameters for the circulating-current controller are listed in Table 5.9.

The results from the simulations in PSCAD are plotted in Fig. 5.31 through Fig. 5.35. The dc-side voltage of the VSC, the voltage of the ES, and the voltage across capacitor $C_2$ are plotted in Fig. 5.31 for one discharging/charging
Figure 5.31: Dc-side voltages: VSC dc-side voltage (solid); ES terminal voltage (dashed); voltage across $C_2$ (bold-solid).

cycle, and zoomed in Fig. 5.32. Fig. 5.33 depicts the active power flow during the active power delivery period. Fig. 5.34 shows the direct current from the dual thyristor converter. It can be seen that there was no charging/discharging current out of the dual thyristor converter when the system was idling. However, there was always a circulating current flowing through the two bridges, as depicted in Fig. 5.35.

### 5.3.3 Comparison of the Two Control Methods

In general, the circulating-current-free control method has the advantage of simple and compact arrangement but with two drawbacks [21]. One is the dead time when the current changes its direction. The incoming rectifier must wait until the current in the outgoing rectifier dies out. The delay slows down the response to current control command. Another drawback is that the current becomes discontinuous at too large firing angles or too low load inductances. With circulating-current control, the converter current flows continuously. The main drawback is that large inductors must be installed to limit the circulating current.

When a dual thyristor converter is employed for motor drives, the drawbacks with circulating-current-free control might deteriorate the performance of the
5.3 Design of the Interface Control System

Figure 5.32: Dc-side voltages (zoomed): (a) VSC dc-side voltage; (b) ES terminal voltage; (c) voltage across capacitor $C_2$.

Figure 5.33: Active power flow during the energy delivery period: from the dual thyristor converter (solid); from the VSC (dashed); from the ES (bold-solid).
control system, which might be unacceptable for some applications. However, in the application investigated in this paper, the situation is different.

The same control structure has been employed in these two investigations. However, there is a small difference in the selection of the bandwidth of the energy controller. The controller bandwidth with circulating-current control method is chosen slightly lower (111 rad/s compared to 133 rad/s). A comparison in the performances with these two control methods did not show any significant difference. Even though there is a delay in the response of the thyristor current with circulating-current-free control when the current changes direction, the effect on the $u_{C2}$ response is very small. The reason is that the bandwidth of the controller for the thyristor dc current is relatively low due to the consideration of the voltage rating of the dual
5.4 Conclusion

In applications where a StatCom is required to deliver a certain amount of active power in addition to the reactive power support, energy storage devices should be installed on the dc side of the VSC. Due to the considerable voltage swing associated with the ES devices, a direct connection of the ES to the dc link of the VSC will result in an unnecessarily high voltage rating of the VSC. A dual thyristor converter topology is proposed as the interface between the ES and the dc link of the VSC. The high power handling capability and the low cost feature of thyristors make the topology an economical and attractive solution.

The study shows that the total cost can be reduced by introducing the proposed dual thyristor converter as the interface between the energy storage and the dc link of the VSC. The cost comparison between different types of ES, even considering the rough simplification and the uncertainty of cost figures, provides a guideline for choice of ES at intermediate energy levels.

Control strategies are presented for a StatCom with capacitive ES and with the proposed interface topology. The control strategies are validated by simulations in PSCAD. Large capacitor banks are considered as the ES. However, the control strategy is applicable to systems with other ES such as supercapacitors and batteries with some modification in the energy control of the ES. Two control methods for the dual thyristor converter, circulating-current control and circulating-current-free control have been compared. The comparison shows that the latter is preferable for the investigated application.
6 Conclusions

This thesis deals with the integration of ES into StatComs. The investigation involves the following aspects: possible benefits for power systems, main circuit design, and control strategies.

Flux modulation and converter control

A novel flux modulation scheme, combined with deadbeat current control, has been proposed for two-level VSCs. With this control system, all the three components (the positive sequence, the negative sequence, and the offset) of the converter current and the bus flux are controllable.

The difference between the flux modulation scheme and a conventional voltage modulation scheme is that the offset component of the bus flux is accessible and controllable whereas only the positive and negative sequence components of the bus voltage are controllable with the voltage modulation scheme. This difference of the two modulation schemes implies that they have different influence on the flux of the transformers connected at the same point as the StatCom (usually the PCC) in a transmission system. During fault recovery, transformers in the system might be driven into saturation due to the presence of the offset components in the transformer flux. With voltage modulation, there is no control over the bus-flux offset component. Hence, the elimination of the offset flux component depends on the system damping characteristics only. However, with flux modulation, the VSC also contributes to the offset suppression by controlling the bus-flux offset component. Consequently, the transformer saturation problem can be mitigated to a certain extent by utilization of flux modulation. Studies show that both the saturation degree and the saturation period are reduced. However, the bus voltage during the fault is slightly lower in the case with
flux modulation since the presence of the offset component in the converter current reduces the reactive power support during the fault. Meanwhile, the transient current peak of the VSC is higher with flux modulation.

Transformer saturation may not be a major problem in most applications. However, as saturation has to be taken into account during the design process and may be a cost-driving factor, any means to reduce the saturation effect without additional cost should be considered. It has been illustrated that the use of flux modulation may contribute in this respect and it further can be assumed that it can be implemented without additional cost. In a system in which transformer saturation is a concern, the flux modulation scheme is preferable.

**Power system benefits**

Effective active power compensation schemes for StatComs with capacitive energy storage have been proposed and verified by computer simulations and partly by experiments with a real-time simulator. It has been shown that phase jumps and magnitude fluctuations of the voltage at the PCC can be reduced significantly with the additional active power support from the StatCom. Active power compensation may be very beneficial to phase-sensitive loads connected in a weak network with large time-varying loads including cyclic loads.

The fault-recovery performance of a weak system with induction motor loads has been studied. The results show that a StatCom with a certain energy storage capacity can effectively help with the system recovery from faults. Although this incurs extra cost for the increasing direct voltage rating and size of the dc-side capacitor, the overall rating of the converter can be reduced by utilization of the proposed active power compensation scheme. In case no active power compensation is employed, a larger StatCom rating together with a sufficiently large dc-side capacitor is necessary for a successful system recovery.
Interface between the ES and the dc side of VSCs

ES devices such as capacitors, supercapacitors, and batteries exhibit considerable variation in the terminal voltage during a charging/discharging cycle. If ES devices are connected directly to the dc-link of the VSC, the dc-side voltage of the VSC will vary accordingly. As a result, the VSC rating has to be increased, and so does the cost. In order to reduce the voltage rating of the VSC, a dual thyristor converter topology has been proposed as the interface between the ES and the dc link of the VSC. The high power handling capability and the low cost feature of thyristors make the topology an economical and attractive solution.

The cost comparison shows that the total cost can be reduced by introducing the proposed dual thyristor converter as the interface between the ES and the dc link of the VSC. The cost comparison between different types of ES, even considering the rough simplification and the uncertainty of cost figures, provides a guideline for choice of ES at intermediate energy levels.

Control strategies have been suggested for a StatCom with capacitive ES and with the proposed interface topology. The control strategies are validated by simulations in PSCAD. Large capacitor banks are considered as the ES. However, the control strategy is applicable to systems with other ES devices such as supercapacitors and batteries with minor modifications in the energy control of the ES. Two control methods for the dual thyristor converter (circulating-current control and circulating-current-free control) have been compared. The comparison shows that the circulating-current-free control method is preferable for the investigated application.
7 Future Work

The work presented in this thesis covers several aspects of the integration of ES into StatComs. However, there are certain issues that might be interesting for future investigations. Below are some suggestions:

- The proposed interface topology between the ES and the dc link of VSCs is an attractive solution. It will be valuable to get it implemented in the real-time simulator.

- The protection issues of the proposed interface topology have not been covered in the thesis. Investigations are required when the topology is implemented.

- The detailed cost comparison presented is between the system with and without the proposed topology. However, a detailed cost comparison between the proposed topology and the ones commonly used in low voltage applications might also be interesting.

- In the investigation of the interface topology, the ES was assumed to be charged to a voltage level that is not higher than the dc-side voltage of the VSC. Since the dual thyristor converter can operate in all the four quadrants of the current-voltage plane, it is possible to charge the ES to a higher voltage level while keeping the dc-side voltage of the VSC constant. It might be valuable to investigate this possibility and the related issues such as protection issues.

- Research on other possible topologies, especially multilevel-converter-based solutions with a distributed ES, is suggested to be performed in the future.
References


[27] PSCAD/EMTDC manual.


[36] C. Banos, M. Aten, P. Cartwright, and T. Green, “Benefits and control of STATCOM with energy storage in wind power generation,” in *Proc. The 8th IEE International Conference on AC and DC Power Trans-
References


References


[55] “SAFT Ni-Cd SBH battery datasheet.”


## List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPC</td>
<td>direct power control</td>
</tr>
<tr>
<td>ES</td>
<td>energy storage</td>
</tr>
<tr>
<td>ESR</td>
<td>equivalent series resistance</td>
</tr>
<tr>
<td>FACTS</td>
<td>flexible ac transmission systems</td>
</tr>
<tr>
<td>GIC</td>
<td>geomagnetically induced current</td>
</tr>
<tr>
<td>HP</td>
<td>high pass (filter)</td>
</tr>
<tr>
<td>IGBT</td>
<td>insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IMC</td>
<td>internal model control</td>
</tr>
<tr>
<td>Li-Ion</td>
<td>lithium-ion (battery)</td>
</tr>
<tr>
<td>NaS</td>
<td>sodium-sulfur (battery)</td>
</tr>
<tr>
<td>Ni-Cd</td>
<td>nickel-cadmium (battery)</td>
</tr>
<tr>
<td>PCC</td>
<td>point of common coupling</td>
</tr>
<tr>
<td>PLL</td>
<td>phase-locked loop</td>
</tr>
<tr>
<td>PWM</td>
<td>pulse-width modulation</td>
</tr>
<tr>
<td>SPWM</td>
<td>sinusoidal pulse-width modulation</td>
</tr>
<tr>
<td>SSSC</td>
<td>static synchronous series compensation</td>
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**List of Acronyms**

<table>
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<th>Acronym</th>
<th>Description</th>
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<td>StatCom</td>
<td>static synchronous compensation</td>
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<tr>
<td>SVC</td>
<td>static var compensation</td>
</tr>
<tr>
<td>TCR</td>
<td>thyristor-controlled reactor</td>
</tr>
<tr>
<td>TCSC</td>
<td>thyristor-controlled series compensator</td>
</tr>
<tr>
<td>TSC</td>
<td>thyristor-switched capacitor</td>
</tr>
<tr>
<td>VSC</td>
<td>voltage source converter</td>
</tr>
<tr>
<td>ZEBRA</td>
<td>zero emission battery research activities (battery) or sodium/nickel chloride battery</td>
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# List of Symbols

## Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha$</td>
<td>firing angle of thyristors</td>
<td>$[^{\circ}]$</td>
</tr>
<tr>
<td>$\Delta \psi$</td>
<td>flux change</td>
<td>[Wb]</td>
</tr>
<tr>
<td>$\omega$</td>
<td>angular frequency</td>
<td>[rad/s]</td>
</tr>
<tr>
<td>$\varphi$</td>
<td>phase angle</td>
<td>[rad] or [deg]</td>
</tr>
<tr>
<td>$\psi$</td>
<td>flux</td>
<td>[Wb]</td>
</tr>
<tr>
<td>$\tau$</td>
<td>time constant</td>
<td>[s] or [ms]</td>
</tr>
<tr>
<td>$\tau_i$</td>
<td>integration time constant</td>
<td>[ms]</td>
</tr>
<tr>
<td>$\theta$</td>
<td>angle</td>
<td>[rad]</td>
</tr>
<tr>
<td>$C$</td>
<td>capacitance</td>
<td>[$\mu$F]</td>
</tr>
<tr>
<td>$CST$</td>
<td>relative cost</td>
<td>[pu]</td>
</tr>
<tr>
<td>$cst$</td>
<td>relative cost</td>
<td>[pu]</td>
</tr>
<tr>
<td>$c$</td>
<td>cost</td>
<td>[pu]</td>
</tr>
<tr>
<td>$f$</td>
<td>frequency</td>
<td>[Hz]</td>
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<tr>
<td>$G_p$</td>
<td>transfer function of a plant</td>
<td></td>
</tr>
<tr>
<td>$G_k$</td>
<td>transfer function of a controller</td>
<td></td>
</tr>
<tr>
<td>$G_d$</td>
<td>transfer function of a disturbance</td>
<td></td>
</tr>
<tr>
<td>$i$ or $I$</td>
<td>current</td>
<td>[A] or [kA]</td>
</tr>
</tbody>
</table>
### List of Symbols

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<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$K$</td>
<td>coupling function between converter ac-side and dc-side voltage</td>
<td></td>
</tr>
<tr>
<td>$k_p$</td>
<td>proportional gain</td>
<td></td>
</tr>
<tr>
<td>$L$</td>
<td>inductance</td>
<td>[mH]</td>
</tr>
<tr>
<td>$L_v$</td>
<td>phase reactor inductance</td>
<td>[mH]</td>
</tr>
<tr>
<td>$P$</td>
<td>active power</td>
<td>[W] or [MW]</td>
</tr>
<tr>
<td>$P_{dc}$</td>
<td>active power flowing into the dc-side of a VSC</td>
<td>[W] or [MW]</td>
</tr>
<tr>
<td>$P_{ac}$</td>
<td>active power flowing from the PCC into the ac-side of a VSC</td>
<td>[W] or [MW]</td>
</tr>
<tr>
<td>$Q$</td>
<td>reactive power</td>
<td>[Var] or [MVar]</td>
</tr>
<tr>
<td>$R$</td>
<td>resistance</td>
<td>[Ω]</td>
</tr>
<tr>
<td>$R_v$</td>
<td>phase reactor resistance</td>
<td>[Ω]</td>
</tr>
<tr>
<td>$S$</td>
<td>apparent power</td>
<td>[VA] or [MVA]</td>
</tr>
<tr>
<td>$T_s$</td>
<td>switching period</td>
<td>[s]</td>
</tr>
<tr>
<td>$u$ or $U$</td>
<td>voltage</td>
<td>[v] or [kV]</td>
</tr>
<tr>
<td>$u_d$</td>
<td>converter direct voltage</td>
<td>[V]</td>
</tr>
<tr>
<td>$u_v$</td>
<td>converter alternating voltage</td>
<td>[V]</td>
</tr>
<tr>
<td>$W$</td>
<td>Energy</td>
<td>[J] or [MJ]</td>
</tr>
<tr>
<td>$x_v$</td>
<td>phase reactor reactance</td>
<td>[Ω]</td>
</tr>
</tbody>
</table>

### Subscripts

- $a,b,c$: phase quantities
- $av$: average value
- $B$: bus
- $base$: base value
<table>
<thead>
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<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>btr</td>
<td>battery</td>
</tr>
<tr>
<td>C</td>
<td>capacitor</td>
</tr>
<tr>
<td>chg</td>
<td>charging (voltage)</td>
</tr>
<tr>
<td>crcl</td>
<td>circulating (current or power)</td>
</tr>
<tr>
<td>d</td>
<td>direct quantities (voltage, current)</td>
</tr>
<tr>
<td>ES</td>
<td>energy storage</td>
</tr>
<tr>
<td>f</td>
<td>quantities of the converter filter</td>
</tr>
<tr>
<td>ff</td>
<td>feed-forward signal</td>
</tr>
<tr>
<td>Ld</td>
<td>load</td>
</tr>
<tr>
<td>( k+1</td>
<td>k-1 )</td>
</tr>
<tr>
<td>( k-1 )</td>
<td>value at ( t_{k-1} )</td>
</tr>
<tr>
<td>max</td>
<td>maximum value</td>
</tr>
<tr>
<td>min</td>
<td>minimum value</td>
</tr>
<tr>
<td>N</td>
<td>nominal quantities</td>
</tr>
<tr>
<td>n</td>
<td>negative sequence component</td>
</tr>
<tr>
<td>ofs</td>
<td>offset component</td>
</tr>
<tr>
<td>PLL</td>
<td>quantities from the PLL (angle or frequency)</td>
</tr>
<tr>
<td>p</td>
<td>positive sequence component</td>
</tr>
<tr>
<td>ref</td>
<td>reference</td>
</tr>
<tr>
<td>S</td>
<td>sampled quantity</td>
</tr>
<tr>
<td>SC</td>
<td>supercapacitor</td>
</tr>
<tr>
<td>st</td>
<td>steady-state quantity</td>
</tr>
</tbody>
</table>
List of Symbols

\( T \)  
transformer quantity

\( thy \)  
quantities of the thyristor converter

\( tri \)  
triangular wave

\( V \)  
VSC

\( v \)  
VSC

\( virt \)  
quantities of the virtual resistor in the dc-voltage control (resistance, active power)

\( w \)  
quantity with interface

\( wo \)  
quantity without interface

\( x \)  
phase a, b, or c

Superscripts

\( d \)  
d component in the dq frame

\( q \)  
q component in the dq frame

\( \alpha \)  
\( \alpha \) component in the \( \alpha\beta \) frame

\( \beta \)  
\( \beta \) component in the \( \alpha\beta \) frame

\( r \)  
modified quantity

Accents

\( \bar{\cdot} \)  
vector in the \( \alpha\beta \) frame

\( \hat{\cdot} \)  
estimated value

\( \tilde{\cdot} \)  
vector in the dq frame

\( \tilde{\cdot} \)  
measured value
Appendices
A The Real-time Simulator

A.1 Real-time Simulator

In the laboratory of the Division of Electrical Machines and Power Electronics at Royal Institute of Technology (KTH), a real-time simulator has been built up for the purpose of research and education. The simulator contains a commercial general-purpose control system of type ABB Mach 2, which is adapted to control power electronic apparatus for high-power applications. Inductors, resistors, and capacitors are used to represent the transmission lines in the power system. The generators are modeled by electronic power amplifiers controlled by digital signal processors (DSPs).

A work program has been launched with the goal to have implementations of the power electronic apparatus, which have been established, in the power transmission field. These apparatus may be based on the classical thyristor technology such as SVC, TCSC, and high-voltage direct current transmission (HVDC), or on emerging VSC technology utilizing switching devices like IGBT or integrated gate commutated thyristor (IGCT).

The implementation involves several aspects:

- Hardware of the main circuit
- Software related to converter control
- Human-machine-interface (HMI) for the operators work station.

A two-level MOSFET-based voltage source converter has been built up in the real-time simulator. The converter utilizes $10\sqrt{3}$ V as the nominal line-
line voltage and 8VA as the nominal power. A special circuit is employed to compensate for the voltage drop across the anti-parallel diodes.

The method of using a real-time simulator for experiments with high-power converters is developed and used by all manufacturer of FACTS equipment and it is generally accepted. It has to be emphasized that analog real-time simulations should be considered as experimental verification. Since all essential parts of the high-power converter are modeled by hardware in the real-time simulator, an accurate representation of the high-power converter is achieved. Moreover, the whole control system is implemented with all interrupts, delays, measurements, conversions, sampling, and noise as in a commercial StatCom. Truly, this kind of real-time simulation is as close to reality as one can come without performing the test on a multi-megawatt power electronics apparatus installed in a power system.

A.2 Overview of the Mach2 System

This system consists of a number of general-purpose circuit boards. These can be divided into two parts:

1. I/O boards, normally equipped with one or a few micro-controllers. These boards are installed in standard 19\”-racks.

2. High-performance computing boards (PS801), equipped with 6 digital signal processors (DSP) and a field programmable gate array (FPGA). These are installed in an industrial computer (PC) in PCI-slots.

The inner loops of the firing control are implemented in the PS801 board using the graphical programming tool Hidraw. The timing accuracy is provided by the FPGA; in this application the resolution is 400 ns. Other controller algorithms can be implemented in the Pentium pro processors or in the Sharc DSPs.

The system also provides an internal measuring system with sampling frequencies up to 10 kHz. This can be used for studying the response of the
controller algorithms.

The block diagrams of the Mach2 system, the PCI board, and the analogue I/O board are shown in Fig. A.1 to A.3. Fig. A.4 through Fig. A.6 show photographs of the real-time simulator in the laboratory.
A The Real-time Simulator

Figure A.1: Overview of the Mach2 system
A.2 Overview of the Mach2 System

Figure A.2: PCI-Board overview

- **PCI-Bus**
- **Controller area network (CAN) Bus**
- **Internal Bus**
- **Time Divided Multiplexed Buses (TDM-Bus)**
- **Interrupt 1x2**

**DSPs and RAMs**
- DSP1
- DSP2
- DSP3
- DSP4
- DSP5
- DSP6
- RAM (shared)

**CPU**
- **CPU Pentium Pro**
- **CPU Pentium Pro**

**FPGA**
- Firing pulses to switching devices

**Controller**
- Host Processor or 486

**Dual Port Memory (DPM)**
- 108 Sd

**Time Divided Multiplexed Buses (TDM-Bus)**
- **Interrupt 1x2**

**Controller area network (CAN) Bus**
- PCI-Bus

**PCI-Bus**
- **Controller area network (CAN) Bus**
- **Internal Bus**
- **Time Divided Multiplexed Buses (TDM-Bus)**
- **Interrupt 1x2**

**CPU**
- **CPU Pentium Pro**
- **CPU Pentium Pro**

**FPGA**
- Firing pulses to switching devices

**Controller**
- Host Processor or 486

**Dual Port Memory (DPM)**
- 108 Sd
A The Real-time Simulator

One or several analogue interface boards

Analogue signal from main circuit, current or voltage signal

4 differential inputs/boards

One or several analogue interface boards

Galvanic isolation

4 differential inputs/boards

Backplane Bus

Figure A.3: Analogue I/O Board

Sampling Board:

CAN-Bus

TDM

PS 860

Share DSP

Sample xHold

MUX

DAC

4 channels
A.2 Overview of the Mach2 System

Figure A.4: The real-time simulator - Mach2 control system
Figure A.5: The real-time simulator - main circuit
Figure A.6: The real-time simulator - Mach2 inside
B Sequence Separation and Phase-locked Loop

B.1 Sequence Separation of Bus Flux

Flux modulation scheme as described in Chapter 2 was used in the investigations. With this modulation method, the control system is flux oriented. The bus flux is measured and the phase quantities are transformed into a space vector in the $\alpha\beta$ coordinate system using the following equation:

$$\begin{bmatrix} \psi_{\alpha B} \\ \psi_{\beta B} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} \psi_{B,a} \\ \psi_{B,b} \\ \psi_{B,c} \end{bmatrix}$$ (B.1)

The flux vector is resolved into a positive sequence, a negative sequence, and an offset component, with a PLL operating on the positive sequence component. A low-pass filter method as described in [2] is employed for sequence separation.

The flux vector is assumed to have a positive sequence component and a negative sequence component of the fundamental component, and an offset component. It has the form as shown in (2.4), which is rewritten below:

$$\begin{align*}
\bar{\psi}_{\alpha\beta} (t) &= \tilde{\psi}_{\alpha\beta,ofs} + \tilde{\psi}_{\alpha\beta,p} e^{j\theta(t)} + \tilde{\psi}_{\alpha\beta,n} e^{-j\theta(t)} \\
\dot{\theta} (t) &= \omega (t)
\end{align*}$$ (B.2)

where $\theta(t)$ and $\omega(t)$ are the angle and frequency from the PLL.

The phasors in the equation can be assumed to be constant since the fre-
quency of variation is usually much lower than the nominal frequency of the bus flux. After some manipulations, each of these phasors can be isolated on the left-hand side:

\[
\begin{align*}
\tilde{\psi}_{dqB,p} &= e^{-j\theta(t)} \left\{ \bar{\psi}_{\alpha\beta}^{\alpha\beta}(t) - \tilde{\psi}_{B,ofs}^{\alpha\beta} - \tilde{\psi}_{dqB,n}^{\alpha\beta} e^{-j\theta(t)} \right\} \\
\tilde{\psi}_{dqB,n} &= e^{j\theta(t)} \left\{ \bar{\psi}_{\alpha\beta}^{\alpha\beta}(t) - \tilde{\psi}_{B,ofs}^{\alpha\beta} - \tilde{\psi}_{dqB,p}^{\alpha\beta} e^{j\theta(t)} \right\} \\
\tilde{\psi}_{\alpha\beta}^{\alpha\beta}_{B,ofs} &= \bar{\psi}_{\alpha\beta}^{\alpha\beta}(t) - \tilde{\psi}_{dqB,p}^{\alpha\beta} e^{-j\theta(t)} - \tilde{\psi}_{dqB,n}^{\alpha\beta} e^{-j\theta(t)}
\end{align*}
\]  

(B.3)

Ideally, the signals obtained from (B.3) should be identical to the real signal. At the presence of noises and disturbances, the phasors can be obtained by low-pass filtering the signals on the right-hand side of (B.3). The block diagram of the sequence separation procedure is shown in Fig. B.1.

---

**Figure B.1: Block diagram: Sequence separation of bus flux**
B.2 Phase-locked Loop

Fig. B.2 shows the block diagram of the phase-locked loop. The PLL operates on the positive sequence component of the bus flux, which is obtained from the sequence separation block as shown in Fig. B.1. The phase angle of the positive sequence component should be regulated to zero by adjusting the angular frequency $\omega_{PLL}$. The PLL angle $\theta_{PLL}$ is obtained by integration of $\omega_{PLL}$.

![Block diagram: phase-locked loop](image)

Figure B.2: Block diagram: phase-locked loop

B.3 Sequence Separation and Phasor Estimation of the Converter Current

In general, the sequence separation procedure described in Section B.1 can be applied to the converter current to get the phasors of the positive sequence, the negative sequence, and the offset components. An inherent characteristic of this method of sequence separation is that these obtained components are filtered dc signals, implying a delay from the instantaneous values to the obtained ones. However, a faster acquisition of the positive sequence component is desired for a rapid control of the converter current. One approach is to take the instantaneous converter current and transform it into the rotating dq frame directly. The drawback is that the obtained positive sequence component will be oscillatory if the converter current con-
B Sequence Separation and Phase-locked Loop

tains a negative sequence or an offset component. The countermeasure is, obviously, to subtract the negative sequence and the offset components from the total current. Although the exact values of these two components (negative sequence component in the dq frame and the offset component in the αβ frame) cannot be obtained instantaneously, it can be assumed that they follow their references with a two-sample delay. The assumption is justifiable due to the utilization of the deadbeat current control. By subtracting the estimated negative sequence and offset components from the total converter current, the positive sequence component in the αβ frame is obtained instantaneously.

The modified block diagram is shown in Fig B.3. The block ‘Sequence separation’ has the same structure as shown in Fig. B.1. The negative sequence and the offset components are obtained from the low-pass filters.

---

**Figure B.3: Block diagram: Sequence separation of bus flux**
## C Motor Parameters

The table below lists the parameters of one of the induction motors (no. 6) used in the PSCAD simulations.

<table>
<thead>
<tr>
<th>Data generation/entry</th>
<th>EMTP Type 40</th>
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<tr>
<td>Multimass interface</td>
<td>disabled</td>
</tr>
<tr>
<td>Number of coherent machines</td>
<td>1</td>
</tr>
<tr>
<td>Number of sub-iteration steps</td>
<td>1</td>
</tr>
<tr>
<td>Rated rms phase voltage</td>
<td>2.4 kV</td>
</tr>
<tr>
<td>Rated rms phase current</td>
<td>1.17 kA</td>
</tr>
<tr>
<td>Base angular frequency</td>
<td>314.159 rad/s</td>
</tr>
<tr>
<td>Design ratio</td>
<td>0.47</td>
</tr>
<tr>
<td>Power factor at rated load</td>
<td>0.915</td>
</tr>
<tr>
<td>Efficiency at rated load</td>
<td>0.965</td>
</tr>
<tr>
<td>Slip at full load</td>
<td>0.00556</td>
</tr>
<tr>
<td>Starting current at full volts</td>
<td>6 pu</td>
</tr>
<tr>
<td>Starting torque at full volt / full load torque</td>
<td>0.6 pu</td>
</tr>
<tr>
<td>Maximum torque / full load torque</td>
<td>2 pu</td>
</tr>
<tr>
<td>Number of poles</td>
<td>2</td>
</tr>
<tr>
<td>Inertia constant</td>
<td>2 MJ/MVA</td>
</tr>
<tr>
<td>Mechanical damping</td>
<td>0.008</td>
</tr>
</tbody>
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<th>Description</th>
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<td>1.2</td>
<td>Possible power flow patterns between the VSC and the PCC</td>
<td>3</td>
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