Localized removal of the Au–Si eutectic bonding layer for the selective release of microstructures

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Abstract

This paper presents and investigates a novel technique for the footprint and thickness-independent selective release of Au–Si eutectically bonded microstructures through the localized removal of their eutectic bond interface. The technique is based on the electrochemical removal of the gold in the eutectic layer and the selectivity is provided by patterning the eutectic layer and by proper electrical connection or isolation of the areas to be etched or removed, respectively. The gold removal results in a porous silicon layer, acting similar to standard etch holes in a subsequent sacrificial release etching. The paper presents the principle and the design requirements of the technique. First test devices were fabricated and the method successfully demonstrated. Furthermore, the paper investigates the release mechanism and the effects of different gold layouts on both the eutectic bonding and the release procedure.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

For years, bonding substrates have been an important process in the fabrication of microelectromechanical systems (MEMS), since it allows the fabrication and packaging of complex devices as well as the heterogeneous integration of materials [1, 2]. The MEMS devices fabricated with wafer-bonding technologies often feature moving structures that must be released during the fabrication process.

In general, to allow a structure to move, its connection to the underlying layer must either be inhibited while the structure is fabricated or the underlying layer must be removed. This paper focuses on structures fabricated using wafer-to-wafer bonding technology, for which there are basically two methods to allow for a moving structure. The first method is the localized bonding of areas to be bonded while avoiding the bonding of the moving structures to the underlying substrate. The second method is a bond-and-release approach, in which a full wafer bond is followed by the removal of the bond interface material underneath the structures to be released.

Localized bonding between two substrates can be obtained using two different principles. The first principle is to modify the interface material prior to bonding, defining bonding and non-bonding areas. Examples of patterned bond interface layers include adhesive layers applied only on areas where bonding is desired [3] and bond blocking layers such as gold or platinum defining local non-bonding areas in anodic bonding [4]. The second localized bonding principle is to use heat triggered bonding methods and to localize the heat to the desired areas of the bond interface. Examples of this approach include integrated heaters for both localized eutectic and silicon fusion bonding [5], localized soldering using inductive heating [6] as well as local heating using lasers [7]. In localized bonding, the non-bonded parts are either fallout structures or they must remain mechanically connected to the bonded parts by mechanical supports to prevent them from falling out during the remaining process steps. The removal of mechanical support structures through dicing or through controlled fracture has been shown [8, 9]. However, such break-away structures limit the design freedom and potentially

Figure 1. Illustration of the different sacrificial etching methods. (a) Sacrificial underetching without etch holes, with footprint area determining selectivity; (b) sacrificial underetching with etch holes, allowing to selectively release structures independent from the footprint area; (c) localized removal of the bonding layer only underneath the structure to be released, allowing for the footprint and thickness independent selective release of structures.

increase the footprint area of the MEMS device. Furthermore, the moving structures could be damaged while removing the support structures.

In wafer-to-wafer bonding technology, moveable structures are in most cases fabricated using a bond-and-release scheme, i.e. all structures are bonded and the structures to move are released at a later stage of the fabrication process by removing their underlying bonding layer. This method is based on wafer-bonding methods with intermediate bonding layers that can be sacrificially etched with a high selectivity. Examples of such intermediate bonding materials are silicon dioxide [10] and polymers [2, 11]. It should be noted that processes using the buried oxide in silicon-on-insulator (SOI) wafers as sacrificial layer can be considered as bond-and-release technology. To the authors' knowledge there are no reports on bond-and-release technology other than for polymer and silicon dioxide bonding layers. Figure 1 overviews the sacrificial etching methods described below.

In general, there are two restrictions for the sacrificial underetching. First, for underetching large structures the whole substrate is exposed to the etchant for a long time, which may result in device destruction in harsh chemical environments such as hydrofluoric (HF) acid for the etching of oxide sacrificial layers. Second, the width of the structures to be released by fully underetching must be considerably smaller than the width of the structures to remain bonded, otherwise all structures will be underetched and released (figure 1(a)). Both issues are usually addressed by integrating etch holes in the structures to be underetched (figure 1(b)). These etch holes drastically minimize the distance to underetch, which results in two benefits. They allow both for a faster

underetching, minimizing the exposure to harsh chemical environments and for the underetching of structures with a larger footprint area than the structures to remain bonded. However, the etch holes potentially decrease the mechanical stability and the performance of the structures to be released. Furthermore, the fabrication of such etch holes is feasible only for structures consisting of thin layers, such as thin silicon layers for micromirror arrays [12]. If the moving structures are hundreds of micrometer thick, etch holes are difficult to fabricate with the required aspect ratio. Yet, without the etch holes the sacrificial underetch technique does not allow us to locally release selected structures with a larger footprint area than structures to remain bonded.

A technique for releasing structures without additional etch holes can be provided by localized removal of the bonding layer (figure 1(c)). An example for localized removal is the localized laser ablation of a polymer bonding layer [13]. However, this technology is limited to polymer bonding with a bond substrate that is transparent to the laser wavelength and a bond polymer that strongly absorbs the laser energy. For bonding technologies based on metal intermediate layers, an alternative and flexible approach is based on electrochemical etching of the intermediate metal layer in a neutral salt solution. This principle has been shown for surface micromachined structures [14], where an aluminum layer was electrochemically sacrificially etched. However, to the authors' knowledge there are no reports on sacrificial etching of metallic wafer bonding layers.

The current work introduces, successfully demonstrates and investigates for the first time the localized removal of the bonding layer between gold-silicon (Au-Si) eutectically bonded substrates.

2. Background

2.1. Localized electrochemical etching of gold layers

The release etch method described in this work is based on the electrochemical etching of gold in a chloride solution, as described in previous work [15]. This process has been used in microfabrication for electrochemical etching of gold seed layers [16] and of gold sealings of hollow microneedles for drug delivery [17], for the *in vivo* release of drugs [18] as well as for the localized removal of a gold layer during the fabrication of three-dimensional silicon-on-insulator based radio-frequency transmission lines [19]. Figure 2 illustrates the principle of the localized electrochemical gold etching. On a substrate, a gold layer is deposited using an adhesion layer such as titanium-tungsten (TiW). The latter is crucial for the gold etching, as described below. The metal films are deposited on a dielectric substrate to eliminate any unwanted electrical short circuits. To allow for a localized etching of the gold layer, selected areas of the gold layer should be connected to the etching potential while remaining areas must be electrically isolated. For the etching, the device is submerged in a sodium chloride (NaCl) electrolyte solution and the electrochemical cell is provided by coupling the selected gold areas as anode and a gold counterelectrode as cathode

Figure 2. Illustration of the principle of localized electrochemical gold etching: (a) pattern the gold and the underlying adhesion layer to define areas to be etched and areas to remain; (b) electrochemical etching of the gold layer areas connected to the etching potential; (c) the adhesion layer is not attacked and ensures electrical connection throughout the entire electrochemical etching; (d) the adhesion layer is removed in a standard wet chemical etch step.

(figure 2(b)). Applying a constant voltage versus a reference electrode drives the electrochemical etching of the connected gold areas. Because of non-uniformities in the gold layer thickness and local high field strengths caused by either surface roughness or by the geometry of the design [19], the gold layer can locally etch faster and form gold islands. However, the electrical contact is always ensured through the underlying adhesion layer, which is not attacked by the electrochemical etching. In the previous work [19], experiments showed that with titanium and $\text{Ti}_{30}\text{W}_{70}$ adhesion layers the gold was removed completely, while with chromium adhesion layers the gold etching stopped prematurely. Figure 2(c) illustrates the result of the electrochemical gold etching. The selected gold is removed and the underlying adhesion layer remains. In the last step (figure 2(d)), the exposed adhesion layer is etched using a standard wet chemical etch process, such as etching of the TiW in hydrogen peroxide (H_2O_2).

2.2. Eutectic Au–Si bonding

During eutectic bonding the involved materials form a eutectic mixture at temperatures much lower than their melting temperatures. The most common eutectic bonding material combination in MEMS is silicon and gold, which forms a eutectic mixture at a relatively low temperature of 363 °C. The bonding mechanism is well described in the literature [20, 21] and requires gold on one substrate surface and silicon on the other substrate surface. The silicon surface can be provided by several means. The first approach is to provide a silicon surface using a standard silicon wafer. A second option is to deposit a polysilicon layer [22] on a substrate made of any material compatible to the fabrication conditions. A variant of the second approach is provided by a silicon-on-insulator (SOI) wafer. This option provides the advantage that the buried oxide (BOX) layer acts as diffusion barrier for the gold. Hence, the structures fabricated in the silicon layer which is not bonded are not influenced by the eutectic formation.

Figure 3. Illustration of the eutectic bonding with a metal and silicon pattern, allowing for the subsequent electrochemical etching of only the electrically connected areas.

During the bonding the two substrates are pressed against each other and heated above 363 °C to start the eutectic formation. Investigations of the applied pressure and temperature can be found in the literature [20, 21, 23, 24].

3. Design of localized electrochemical etching of the eutectic bonding layer

The release etch technique presented in this paper is based on the localized electrochemical etching of the Au–Si eutectic bonding layer, however, the principle is applicable to any metallic bonding layer.

To ensure that only specific areas are etched while other remain unetched, the bonding layer must be properly patterned so that all areas to be etched can be electrically connected to an etching potential while all structures not to be etched are isolated. Figure 3 illustrates how a patterned eutectic layer is achieved.

The adhesion layer and gold layer on substrate 1 is patterned to define electrically isolated etch and non-etch areas. The areas are isolated to each other either by a underlying thin dielectric layer, such as thermal silicon dioxide (SiO_2), or by a dielectric substrate such as a glass wafer.

To ensure that there is no electrical short circuit through the silicon of substrate 2 after the eutectic bonding, an electrical isolation between the different areas can be provided by removing the silicon between the structures. Figure 3 illustrates how to pattern the device layer of a SOI wafer to provide an electrical isolation of the silicon surface.

Figure 4. Figure illustrating the fabrication process of the first test devices.

4. Fabrication of first test devices

For the first test devices fabricated in this work, the silicon surface was provided by a 300 μm thick bulk silicon wafer and the other substrate was a glass wafer for visual inspection. Figure 4 illustrates the fabrication flow for the test structures.

Figure 4(a) illustrates how the glass substrate was prepared. A 30 nm thick $Ti_{30}W_{70}$ adhesion layer followed by a 500 nm thick gold layer were sputter-deposited on a glass wafer. The TiW layer is necessary both for a good adhesion of the Au to the substrate and to ensure the electrical connection to the eutectic layer during the whole electrochemical etching time. Then, the metal layers were patterned to define the areas

Figure 5. Figure shows (a) the different metal patterns (layouts 1–4) on the tested chip. The eutectic layers underneath the structures to remain bonded (layout 1) are electrically isolated by removing all TiW and gold except for underneath the silicon structures. The eutectic layers underneath the structures to be released (layouts 2–4) are electrically interconnected via a common TiW layer. The different layouts are discussed in the evaluation section of this paper; (b) a photograph of a chip after the eutectic bonding and before the release procedure, showing that parts of the gold in layouts 2 and 3 disappeared. Investigations (section 5.2) indicate that the gold was consumed by the silicon structures during the eutectic bonding; (c) a photograph of the same chip after the release etching, showing that the structures in layout 1 are still bonded. The remaining structures in layout 2–4 are fully released, with silicon residues in layouts 2 and 3. Investigations (section 5.2) indicate that silicon was flowing out into the gold layer during the eutectic bonding. However, there are no residues in layout 4.

Figure 6. SEM pictures of the bond interface of the silicon (a) after the eutectic bonding and (b) after the electrochemical gold removal. During the cooling step of the eutectic bonding, the silicon and the gold separate with the silicon forming columns through the gold layer and locally bonding to the countersubstrate.

that will be electrochemically etched. The different patterns were isolated from each other by the dielectric glass substrate. Furthermore, different layer layouts for the TiW and the gold were tested to test their influence on the bonding and release etch process, however, this will be addressed in detail in the evaluation section of this paper.

Figure 4(b) illustrates how the other substrate with the silicon surface is prepared. The silicon was provided by a standard 300 μm thick (100) silicon wafer, which was etched in two steps using deep reactive ion etching (DRIE) to remove all conductive silicon between the structures. Figure 4(b) shows the silicon wafer after the first DRIE step. Next, the wafer was prepared for the eutectic bonding by sputter etch removal of the native oxide, followed by *in situ* sputter deposition of 500 nm gold directly on the silicon (figure 4(b)). The *in situ* deposition of gold onto the silicon surface inhibited the native oxide formation on the silicon surface, allowing for a successful eutectic bonding.

Then, the wafers were aligned with the gold sides facing each other and bonded for 10 min in vacuum at 400 $^{\circ}\text{C}$ and 1 bar load pressure (figure 4(c)). After the bonding, the remaining silicon between the fallout-structures and the structures to remain was removed during a second DRIE step (figure 4(d)). The TiW layer on the glass substrate was attacked by the DRIE gases, however, the devices were still functional for the evaluation.

After the second DRIE step, the wafers were diced into single chips (not illustrated in figure 4). Figure 5(b) shows a photograph of a chip before the release etching,

identifying which structures should remain bonded and which should be released. Furthermore, figure 5(b) shows that the gold surrounding some of the silicon structures disappeared. Investigations indicate that the gold was consumed by the silicon structures during the eutectic bonding, however, this will be addressed in detail in the evaluation section of this paper.

To test the electrochemical etching of the eutectic layer, the chips were submerged in 5 M NaCl electrolyte, which was degassed in a vacuum chamber to ensure the complete filling between all the structures on the chip. The electrochemical etching was performed as described in section 2.1. A probe needle was used to contact the common TiW layer connected to the eutectic layer underneath the silicon structures to be released, while the other structures remain electrically isolated. The eutectic layer was coupled as the anode of the electrochemical cell and a gold electrode was used as the counter electrode. A constant voltage of 1.1 V versus an Ag/AgCl KCl saturated reference electrode was applied to drive the electrochemical etching of the connected gold layers (figure 4(e)). While the gold was removed, the electrical contact was always ensured through the TiW adhesion layer, which is not attacked by the electrochemical etching.

After the electrochemical etching of the connected gold (figure 4(f)), a TiW wet etch was necessary to completely release the structures (figure 4(g)). The reasons for the TiW etch are investigated in detail in the evaluation section. For the TiW etching, the structures were submerged in H_2O_2 which was degassed in a vacuum chamber to ensure the complete

Figure 7. Diagrams showing (a) a typical current curve recorded during the electrochemical gold etching and (b) measurement points indicating the underetch length depending on the electrochemical etch time.

filling of all structures. Figure 5(c) shows a photograph of a chip after the release etching, showing that the structures were either still bonded or fully released.

5. Evaluation

5.1. Investigation of the release mechanism

The experiments in this study have shown that the electrochemical gold etch alone is not sufficient to fully release the silicon structures (figure 4(f)). To clarify this issue, the bond interface was studied in more detail. The glass was removed by underetching the TiW for more than 24 h in H_2O_2 and figure 6(a) shows a SEM picture of the bond interface of the silicon surface after the eutectic bonding step.

The bond interface consists of two phases with mainly gold and some silicon spots distributed across the surface. Figure 6(b) shows a SEM picture of the same surface after electrochemically etching the gold. The picture shows that after the gold has been removed, a porous silicon layer remains. During cooling after bonding, the silicon and the gold separate from each other [25]. The silicon phase grains grow, driven by surface energy minimization, and the size of the Si islands in the Au phase depends inversely on the temperature cooling ramp [26]. In our commercial bond equipment (Karl-Suss SB6 VAC), the maximum cooling ramp is limited. As a result, the silicon forms columns through the gold layer, thereby bonding the silicon of substrate 2 to the TiW on substrate 1. As a

Figure 8. Diagram showing the etch time necessary to etch TiW underneath silicon structures of different sizes, both for the TiW underneath non-etched eutectic layers (dotted line) and for the TiW underneath etched eutectic layers with porous silicon (solid line). The TiW underneath the silicon structures with electrochemically etched eutectic layer was fully removed after approximately 1 h of etching. After 1 h, the structures with non-etched eutectic layers were approximately 3 μm underetched.

consequence, two etch steps are necessary to release the silicon structures after the eutectic bonding.

First, the gold in the eutectic layer underneath the structures to be released must be electrochemically etched. Figure 7(a) shows a typical etch current curve when electrochemically etching the gold in the eutectic layer. In the beginning, the exposed gold at the surface is etched rapidly. Then, the etch current decreases since the gold etching is getting increasingly mass transport limited. Figure 7(b) shows measurement points indicating the underetch distance depending on the electrochemical etch time.

Then, after the gold is removed, the TiW underneath the remaining silicon columns must be sacrificially underetched to fully release the silicon structures. For the TiW etching, the chip is submerged in H_2O_2 . The porous silicon fulfills a similar function as standard sacrificial etch holes by drastically minimizing the underetch distance.

The diagram in figure 8 shows the time necessary to etch the TiW in degassed H_2O_2 , both for the TiW underneath electrochemically gold etched and non-gold etched eutectic layers, versus the underetch length under the attached silicon structures. The graph for the TiW etch underneath the porous silicon layer shows that all the attached silicon structures were released after approximately 1 h of TiW etching. The measurements for the TiW etch underneath the non-etched eutectic layer show, that after 1 h of etching the silicon structures are underetched approximately 3 μm , indicating a maximum width of the bonded silicon of 6 μm . Considering some overetching time, this value fits to the dimension of the silicon columns estimated to 3–4 μm from the SEM picture in figure 6(a).

In a summary, the electrochemical etching allows us to locally remove the gold in the eutectic layer, creating a porous silicon layer. The porous silicon layer, similar to standard etch holes, drastically minimizes the underetch distance and provides a large selectivity when sacrificially etching the TiW underneath structures to be released and to remain bonded.

Figure 9. SEM pictures showing (a) the porous silicon layer after the release etch procedure and (b) the silicon surface after removal of the porous silicon in a short KOH etch.

Figure 10. SEM pictures of (a) the silicon outflow during the eutectic bonding at the edges of the silicon structure, when the gold layer is wider than the silicon structures and (b) the resulting silicon residues after the release etch procedure.

However, in contrast to the etch holes, the porous silicon layer underneath the structures does not influence the mechanical performance of the structures, it allows for footprint and thickness independent release of silicon structures and it eliminates any complicated high-aspect ratio etching process to fabricate standard etch holes.

The released silicon structures are porous at the bond interface side, with the porous layer being approximately 2 μm thick. If needed, a short silicon wet etch removes the porous silicon layer [27]. Figure 9 shows the porous silicon layer (figure 9(a)) and the silicon surface after etching the porous silicon on a released structure (figure 9(b)) for 30 min in 50% KOH at approximately 45 °C. An alternative is to provide both the gold and the silicon as thin layers on top

of the TiW. Then, the eutectic layer is sandwiched between two TiW layers and the porous silicon formed is released from both surfaces during the TiW etch. Yet another method, avoid eutectic bonding altogether, would be to use a different metallic bonding method, such as thermocompression bonding [2].

5.2. Layout variations of TiW and gold and their effects

The eutectic layer must be patterned to allow for the selection of the structures to either remain bonded or to be released. One part of providing a patterned bonding layer is to pattern the metal layers on substrate 1 (figure 3).

It was found that the layout of the metal in relation to the layout of the bonded silicon structures has a considerable

influence on the eutectic bonding and as a consequence on the release etch results. Figure 5(a) illustrates the different combinations of TiW and gold layout on substrate 1.

For the structures to remain bonded (figure 5(a), layout 1), their underlying eutectic layer must be electrically isolated from the etching voltage. In this work, the isolation was provided by removing both the TiW and the gold layer except for underneath the silicon structures. Hence, in the cross-section the width of both the TiW and the gold layer was the same as the width of the silicon structures. Figure 5(c), layout 1 shows that the structures were still bonded after the release procedure.

For the structures to be released, the eutectic layers were electrically interconnected by a common TiW layer, however, several designs for the TiW and gold layer layout were tested. In the most straightforward design, both TiW and gold are not patterned and form a closed layer, only partially covered by the silicon (figure 5(a), layout 2). Hence, in the cross-section both the TiW and the gold layer were wider than the silicon structures. The experiments have shown that during the eutectic bonding the gold in between the silicon structures is partially consumed by the silicon, exposing the underlying TiW layer (figure 5(b), layout 2). After the release etching, silicon residues remain in the shape of the released silicon structure (figure 5(c), layout 2). Previous work [23] suggests that during eutectic bonding the silicon flows into the gold. Figure 10(a) shows a SEM picture showing the silicon flowing out into the surrounding gold and figure 10(b) shows a SEM picture of the silicon residuals which remain after the release etching.

To prevent the silicon outflow, both TiW and gold were removed around the edges of the silicon structures as illustrated in figure 5(a), layout 3. The electrical interconnection to the surrounding TiW and gold layer was provided by thin TiW/gold interconnections. However, figure 5(b), layout 3 indicates that the silicon is still flowing out via the thin interconnections and the gold is partially consumed by the silicon. Also here, silicon residues remain after the release procedure (figure 5(c), layout 3).

Finally, in the last design (figure 5(a), layout 4) the gold was fully removed except for underneath the silicon structures. The TiW layer is not patterned and ensures the electrical connection throughout the electrochemical etching. Since there was no gold except for underneath the silicon structures, the silicon could not flow out during the bonding (figure 5(b), layout 4). After the release etch procedure, all silicon structures were released without any residues (figure 5(c), layout 4), indicating that this design is the best-suited design for the release etching.

In a summary, the results indicate that the gold layer should be removed except underneath the silicon structures. The selection of which structures to release is provided by patterning the TiW layer, either electrically connecting the gold underneath the silicon structures to be released or electrically isolating the gold underneath the silicon structures to remain bonded.

6. Conclusion

This paper presents and investigates a novel technique for the localized removal of the bonding layer underneath Au–Si eutectically bonded silicon microstructures. The method is based on patterning the bonding layer and locally removing the selected areas by electrochemical etching. This method is general and allows for the footprint and thickness independent selective release of microstructures fabricated with eutectic bonding, not requiring mechanical support structures or etch holes. First test devices were fabricated and the presented method successfully demonstrated.

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References

- [1] Schmidt M 1998 Wafer-to-wafer bonding for microstructure formation *Proc. IEEE* **86** 1575–85
- [2] Niklaus F *et al* 2006 Adhesive wafer bonding *J. Appl. Phys.* **99** 031101
- [3] Oberhammer J *et al* 2003 Selective wafer-level adhesive bonding with benzocyclobutene for fabrication of cavities *Sensors Actuators A* **105** 297–304
- [4] Veenstra T *et al* 2001 Use of selective anodic bonding to create micropump chambers with virtually no dead volume *J. Electrochem. Soc.* **148** 68–72
- [5] Cheng Y *et al* 2000 Localized silicon fusion and eutectic bonding for MEMS fabrication and packaging *J. Microelectromech. Syst.* **9** 3–8
- [6] Yang H-A, Wu M and Fang W 2005 Localized induction heating solder bonding for wafer level MEMS packaging *J. Micromech. Microeng.* **15** 394–9
- [7] Kim J *et al* 2008 Thin layer laser bonding using spin-on-glass materials *Appl. Surf. Sci.* **254** 6842–8
- [8] van der Wijngaart W, Ridgeway A and Stemme G 2003 A micromachined knife gate valve for high-flow pressure regulation applications *Proc. 12th Int. Conf. on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS 2003)* (Boston, MA, USA, 8–12 June 2003) **2** 1931–4
- [9] Nasiri S S *et al* 2007 Method and system of releasing a MEMS structure *US Patent* 7250353
- [10] Gigan O *et al* 2002 Fabrication and characterization of resonant SOI micromechanical silicon sensors based on DRIE micromachining, freestanding release process and silicon direct bonding *Proc. SPIE* **4936** 194–204
- [11] Somjit N *et al* 2009 Novel concept of microwave MEMS reconfigurable $7 \times 45^\circ$ multi-stage dielectric-block phase shifters *Proc. 22nd IEEE Int. Conf. on Micro Electro Mechanical Systems (MEMS '09)* (Sorrento, Italy, 25–29 January 2009) pp 15–18
- [12] Lapisa M, Zimmer F, Niklaus F, Gehner A and Stemme G 2009 CMOS-integratable piston-type micro-mirror arrays for adaptive optics made of mono crystalline silicon using 3D integration *Proc. 22nd IEEE Int. Conf. on Micro Electro Mechanical Systems (MEMS '09)* (Sorrento, Italy, 25–29 January 2009) pp 1007–10

-
- [13] Guerre R *et al* 2008 Selective transfer technology for microdevice distribution *J. Microelectromech. Syst.* **17** 157–65
 - [14] Metz S *et al* 2005 Partial release and detachment of microfabricated metal and polymer structures by anodic metal dissolution *J. Microelectromech. Syst.* **14** 383–91
 - [15] Frankenthal R and Siconolfi D 1982 The anodic corrosion of gold in concentrated chloride solutions *J. Electrochem. Soc.* **129** 1192–6
 - [16] Hu Z and Ritzdorf T 2007 Cyanide- and thiourea-free electrochemical etching of gold for microelectronics applications *J. Electrochem. Soc.* **154** 543–9
 - [17] Roxhed N, Griss P and Stemme G 2008 Membrane-sealed hollow microneedles and related administration schemes for transdermal drug delivery *Biomed. Microdevices* **10** 271–9
 - [18] Santini J T Jr, Richards A C, Scheidt R, Cima M J and Langer R 2000 Microchips as controlled drug-delivered devices *Angew. Chem. Int. Ed. Engl.* **39** 2397–407
 - [19] Sterner M *et al* 2008 Maskless selective electrochemically assisted wet etching of metal layers for 3D micromachined SOI RF MEMS devices *Proc. 21st IEEE Int. Conf. on Micro Electro Mechanical Systems (MEMS '08) (Tucson, AZ, USA, 13–17 January 2008)* pp 383–6
 - [20] Wolffenbuttel R *et al* 1994 Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature *Sensors Actuators A* **43** 223–9
 - [21] Tiensuu A-L, Bexell M, Schweitz J-A, Smith L and Johansson S 1994 Assembling three-dimensional microstructures using gold–silicon eutectic bonding *Sensors Actuators A* **45** pp 227–36
 - [22] Chen P, Lin C and Liu C 2007 Amorphous Si/Au wafer bonding *Appl. Phys. Lett.* **90** 132 120–1
 - [23] Wolffenbuttel R 1997 Low-temperature intermediate Au–Si wafer bonding; eutectic or silicide bond *Sensors Actuators A* **62** 680–6
 - [24] Lani S, Bosseboeuf A, Belier B, Clerc C, Gousset C and Aubert J 2006 Gold metallizations for eutectic bonding of silicon wafers *Microsyst. Technol.* **12** 1021–5
 - [25] Jang J-W, Hayes S, Lin J-K and Frear D 2004 Interfacial reaction of eutectic AuSi solder with Si (100) and Si (111) surfaces *J. Appl. Phys.* **95** 6077
 - [26] Philofsky E, Ravi K, Brooks J and Hall E 1972 Phase transformations in gold–silicon alloys *J. Electrochem. Soc.* **119** 527–30
 - [27] Steiner P, Richter A and Lang W 1993 Using porous silicon as a sacrificial layer *J. Micromech. Microeng.* **3** 32–6