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Base Resistance Scaling for SiGeC HBTs with a Fully Nickel Silicided Extrinsic Base

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Abstract—A novel SiGeC HBT process with a quasi self-aligned emitter-base architecture and a fully nickel silicided extrinsic base region has been developed. A very low total base resistance R_B was achieved along with simultaneous NiSi formation on the poly-crystalline emitter and collector regions. Uniform silicide formation was obtained across the wafer and the resistivity of the Ni(SiGe:C) silicide layer was $24 \mu\Omega\text{-cm}$. About 50-100 nm of lateral growth of silicide underneath the emitter pedestal was observed. DC and HF results with balanced f_T/f_{MAX} values of 41/42 GHz were demonstrated for $0.5 \times 10 \mu\text{m}^2$ transistors.

Index terms: Heterojunction bipolar transistors (HBTs), silicon-germanium, carbon, SiGe, SiGeC, nickel, silicide, base resistance

I. INTRODUCTION

A low base resistance is needed to obtain high power gain and maximum frequency of oscillation (f_{MAX}) in SiGeC heterojunction bipolar transistors (HBT). Recently, novel structures using a raised polycrystalline base electrode have been developed to reduce the base resistance [1, 2]. A self-aligned silicide, typically CoSi_2 , is also used to obtain low contact and sheet resistance [3]. NiSi integration in bipolar processes has previously been demonstrated for Si-devices [4] and SiGe HBTs [5]. In this study we demonstrate the integration of nickel silicide in a quasi self-aligned (QSA) SiGeC HBT structure for the first time to our knowledge. Nickel monogermanosilicide, $\text{Ni}(\text{SiGe})$, is formed in a self-aligned manner on the polycrystalline SiGeC base electrode as well as on the in-situ doped polysilicon (IDP) emitter and collector regions. $\text{Ni}(\text{SiGe})$ has several important advantages over CoSi_2 including a lower formation temperature, and compatibility with sub 100 nm CMOS process flows [6]. However, the most important feature of nickel in this context is the increased phase stability in the presence of Ge and carbon [7]. While silicidation of the carbon doped SiGe base must be avoided in standard process flows the novel device in this study has a fully silicided base electrode, resulting in very low total base resistance. The silicide process was evaluated by base resistance measurements on devices with varying layout, emitter-poly overlap, emitter width, and length. The base resistance values were extracted from high frequency S-parameter measurements. Transfer line method (TLM) test structures were used to monitor the silicide sheet resistance across the wafer.

II. EXPERIMENTAL

SiGeC HBTs were fabricated in a QSA process, with a non-selectively grown epitaxial base. The base width was 150 Å, with a boron concentration of approximately $1 \times 10^{20} \text{ cm}^{-3}$, constant Ge concentration of 18 at. %, and 0.2 at. % C throughout the whole base. The base stack also included undoped SiGe spacers of 50 Å and a silicon cap of 150 Å. After the emitter-poly definition, an extrinsic base implantation and an RTA step at 925°C for 10 s was performed. The nickel silicide was self-aligned to the emitter-poly pedestal and no spacers were needed to avoid bridging since nickel is the dominant diffusing species during the silicidation reaction. The silicide process included a pre-cleaning step using a 10% HF solution for 10 seconds to remove any oxide on the surface. Thereafter 300 Å of nickel was deposited by electron beam evaporation. The silicidation was performed at 500°C for 30 seconds in nitrogen ambient. The remaining unreacted Ni was removed with a sulphuric/peroxide wet clean. The device fabrication was completed by low temperature oxide deposition, contact hole formation, and Al/TiW metallization. Fig. 1. shows a TEM cross section of the finished device. It is observed that the SiGeC base layer stack, on top of the isolation oxide, has been completely consumed during the silicidation step. The resulting total Ni(SiGe) thickness was 650 Å. Also, a small lateral diffusion (50-100 nm) of Ni(SiGe) underneath the emitter pedestal was observed, which contributes to a lower total base resistance. Since nickel is the main diffusing species during the silicide formation careful control of the deposited nickel thickness is needed to avoid excessive lateral growth, which might impact device performance as shown below. A slightly thinner silicide is formed on the emitter and collector IDP contact regions. This is attributed to a different grain size as well as a

chemical effect due to the presence of Ge in the base electrode. Comparison with blanket wafers confirmed the difference in growth rate on polycrystalline SiGeC and IDP but also indicated a possible pattern dependence [8]. Good silicide uniformity was obtained across a 100 mm wafer. It should be noted that the pre-cleaning step was necessary to form a continuous silicide layer on patterned device wafers. For the devices in this study Ni(SiGe) was only formed on the poly-crystalline part of the base electrode, *i.e.*, outside the active area window. Measurement of TLM structures shows a Ni(SiGe) sheet resistance of 3.7 Ω/sq . with standard deviation 0.29 Ω/sq across 13 dies. Using the silicide thickness determined from TEM analysis, close to the wafer center, a Ni(SiGe) resistivity of 24 $\mu\Omega\text{-cm}$ was obtained, in close agreement with previous reports [9]. The NiSi formed on the IDP regions had a resistivity of 16 - 17 $\mu\Omega\text{-cm}$. TLM measurements of Ni(SiGe) on epitaxial SiGeC layers, *i.e.*, inside the active area window, shows higher sheet resistance of 5.8 Ω/sq with significantly higher standard deviation of 1.9 Ω/sq . This is explained by the smaller thickness of the epitaxial SiGeC layers and indicates that the silicide process has started to consume part of the underlying silicon, leading to large variations in sheet resistance across the wafer. The sheet resistance of the highly-doped SiGeC base stack on a non-silicided reference wafer was determined from TLM measurements to be 520 Ω/sq .

III. ELECTRICAL RESULTS

The fabricated devices were evaluated by DC and HF S-parameter measurements up to 40 GHz, using an Agilent E8361A network analyzer. In Fig. 3. the DC gummel characteristics for devices with an emitter area (A_E) of $0.5 \times 10 \mu\text{m}^2$ and a varying

emitter-poly overlap (0.2 – 0.7 μm) are shown. Ideal collector currents are observed for all overlaps. For the investigated devices a relatively high base current was observed at low base-emitter voltage, which was probably caused by tunneling at the base-emitter junction due to the extremely high base doping in combination with the abrupt P emitter profile. The non-ideal base current component is almost independent of overlap and was also present on the non-silicided reference wafers. However, for the smallest overlap, a marked increase of the base current was observed for some devices. This corresponds to a situation where lateral silicide growth and misalignment of the emitter pedestal causes the distance from the silicide edge to the emitter window (emitter-base junction) to be too short.

The influence of the fully silicided base electrode on the total base resistance (R_B) was investigated on transistors with a single sided base contact geometry, emitter widths of 0.4 - 1.0 μm , and emitter lengths of 5 - 40 μm . The well-known relation $f_{MAX} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$ was used to calculate R_B , where f_T , f_{MAX} and the collector-base capacitance (C_{BC}) were extracted from the S-parameter measurements, after standard open-pad de-embedding. Figure 3 shows the variation of f_T and f_{MAX} with emitter-poly overlap. It is found that f_{MAX} shows a significant increase with smaller overlap while the f_T trend is weaker and in the opposite direction with decreasing values. Figure 4 shows the extracted R_B values as a function of collector current (I_C). A small overlap leads a to a significant reduction of R_B . Figure 5 shows the low-current R_B as a function of overlap, with a minimum value of 29 Ω . Note that this device, with 0.2 μm overlap, showed ideal DC-behavior. The low R_B values for small overlaps indicate that the intrinsic base resistance, including a short link region underneath the emitter-poly, totally dominates R_B in this novel device structure. Plotting R_B for different

emitter width shows that the intrinsic base resistance contributes about 70 % at low current with a medium poly overlap of 0.4 μm .

IV. CONCLUSION

A novel SiGeC HBT device structure featuring a fully nickel silicided extrinsic base region has been demonstrated. The fabricated transistors exhibited good DC and HF performance and a very low total base resistance of 29 Ω for a device with an emitter area of $0.5 \times 10 \mu\text{m}^2$. About 50-100 nm of lateral silicide growth contributed to the low total base resistance. The silicide sheet resistance showed good uniformity across the wafer and a resistivity of 24 $\mu\Omega\text{-cm}$ was obtained for the Ni(SiGe:C) silicide layer. NiSi silicide was also formed on the poly-crystalline emitter and collector regions.

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REFERENCES

- [1] B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. R. Greenberg, R. Groves, S. J. Jeng, J. Johnson, E. Mengistu, K. T. Schonenberg, C. M. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{MAX} and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Lett*, vol. 23, pp. 258-260, May 2002.
- [2] H. Rücker, B. Heinemann, R. Barth, D. Bolze, J. Drews, U. Haak, W. Höppner, D. Knoll, K. Köpke, S. Marschmeyer, H. H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, H.-E. Wulf, and Y. Yamamoto, "SiGe:C BiCMOS Technology with 3.6 ps Gate Delay," *IEDM Tech. Dig.*, pp. 121-124, 2003.
- [3] P. Chevalier, C. Fellous, B. Martinet, F. Leverd, F. Saguin, D. Dutartre, and A. Chantre, "180 GHz f_T and f_{max} self-aligned SiGeC HBT using selective epitaxial growth of the base," *Proceedings of 33rd ESSDRC*, pp. 299-302, 2003.
- [4] T. Iinuma, N. Itoh, K. Inou, H. Nakjima, S. Matsuda, I. Kunishima, K. Suguro, Y. Katsumata, and H. Iwai, "A Self-Aligned Emitter Base NiSi Electrode Technology for Advanced High-Speed Bipolar LSIs," *Proc. IEEE Bipolar Circuits and Technology Meeting*, pp. 92-95, 1992.
- [5] J. Eberhardt and E. Kasper, "Ni/Ag metallization for SiGe HBTs using a Ni silicide contact," *Semiconductor science and Technology*, vol. 16, pp. L47-9, Sept. 2001.
- [6] J. A. Kittl, A. Lauwers, O. Chamirian, M. van Dal, A. Akheyar, M. de Potter, R. Lindsay, and K. Maex, "Ni- and Co-based silicides for advanced CMOS applications," *Microelectronic Engineering*, vol. 70, pp. 158-165, Nov. 2003.
- [7] E. Haralson, T. Jarmar, J. Seger, H. H. Radamson, S.-L. Zhang, and M. Östling, "Ni silicide formation on polycrystalline SiGe and SiGeC layers," *Mater. Res. Soc. Symp. Proc.*, vol. 745, pp. 111-116, 2003.
- [8] E. Haralson, E. Suvar, B. G. Malm, H. Radamson, Y.-B. Wang, and M. Östling, "NiSi Integration in a Non-Selective Base SiGeC HBT Process," *Proc. Second International SiGe Technology and Device Meeting (ISTDM)*, pp. 17-18, 2004.
- [9] J. Seger, D. Mangelinck, H. H. Radamsson, and S.-L. Zhang, "Increased nucleation temperature of NiSi₂ in the reaction of Ni thin films with Si_{1-x}Ge_x," *Applied Physics Letters*, vol. 81, pp. 1978-1980, Sept. 2002.

Figure Captions

Fig. 1. TEM cross section of a SiGeC HBT with a fully silicided extrinsic base region and NiSi emitter and collector (not shown) contacts, drawn emitter width of $0.5\text{ }\mu\text{m}$ and an emitter-poly overlap of $0.6\text{ }\mu\text{m}$.

Fig. 2. Gummel DC characteristics of $A_E = 0.5 \times 10\text{ }\mu\text{m}^2$ transistors for different emitter-poly overlaps of $0.2 - 0.7\text{ }\mu\text{m}$, $V_{CB} = 0\text{ V}$.

Fig. 3. Comparison of f_T and f_{MAX} values for $A_E = 0.5 \times 10\text{ }\mu\text{m}^2$ transistors for different emitter-poly overlaps of $0.2 - 0.7\text{ }\mu\text{m}$. Arrow indicates direction of smaller overlap for f_{MAX} (f_T trend in the opposite direction), $V_{CB} = 1.0\text{ V}$.

Fig. 4. Total base resistance (vs. collector current) from high-frequency S-parameters for $A_E = 0.5 \times 10\text{ }\mu\text{m}^2$ transistors for different emitter-poly overlaps of $0.2 - 0.7\text{ }\mu\text{m}$.

Fig. 5. Low-current base resistance vs. emitter-poly overlap for $A_E = 0.5 \times 10\text{ }\mu\text{m}^2$ transistors.

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