Ink-jet printing of thin film transistors based on carbon nanotubes

Doctoral Thesis
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Ink-jet printing of thin film transistors based on carbon nanotubes

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Abstract

The outstanding electrical and mechanical properties of single-walled carbon nanotubes (SWCNTs) may offer solutions to realizing high-mobility and high-bendability thin-film transistors (TFTs) for the emerging flexible electronics. This thesis aims to develop low-cost ink-jet printing techniques for high-performance TFTs based on pristine SWCNTs. The main challenge of this work is to suppress the effects of “metallic SWCNT contamination” and improve the device electrical performance. To this end, this thesis entails a balance between experiments and simulations.

First, TFTs with low-density SWCNTs in the channel region are fabricated by utilizing standard silicon technology. Their electrical performance is investigated in terms of throughput, transfer characteristics, dimensional scaling and dependence on electrode metals. The demonstrated insensitivity of electrical performance to the electrode metals lifts constraints on choosing metal inks for ink-jet printing.

Second, Monte Carlo models on the basis of percolation theory have been established, and high-efficiency algorithms have been proposed for investigations of large-size stick systems in order to facilitate studies of TFTs with channel length up to 1000 times that of the SWCNTs. The Monte Carlo simulations have led to fundamental understanding on stick percolation, including high-precision percolation threshold, universal finite-size scaling function, and dependence of critical conductivity exponents on assignment of component resistance. They have further generated understanding of practical issues regarding heterogeneous percolation systems and the doping effects in SWCNT TFTs.

Third, Monte Carlo simulations are conducted to explore new device structures for performance improvement of SWCNT TFTs. In particular, a novel device structure featuring composite SWCNT networks in the channel is predicted by the simulation and subsequently confirmed experimentally by another research group. Through Monte Carlo simulations, the compatibility of previously-proposed long-strip-channel SWCNT TFTs with ink-jet printing has also been demonstrated.

Finally, relatively sophisticated ink-jet printing techniques have been developed for SWCNT TFTs with long-strip channels. This research spans from SWCNT ink formulation to device design and fabrication. SWCNT TFTs are finally ink-jet printed on both silicon wafers and flexible Kapton substrates with fairly high electrical performance.

Key words:
Single-walled carbon nanotube, thin film transistor, ink-jet printing, Monte Carlo simulation, stick percolation, composite network, flexible electronics.
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List of Appended Papers

I. Percolation in random networks of heterogeneous nanotubes

II. Contact-electrode insensitive rectifiers based on carbon nanotube network transistors

III. Distinguishing self-gated rectification action from ordinary diode rectification in back-gated carbon nanotube devices

IV. Improved electrical performance of carbon nanotube thin film transistors by utilizing composite networks

V. Understanding doping effects in biosensing using carbon nanotube network field-effect transistors

VI. Finite-size scaling in stick percolation
Jiantong Li and Shi-Li Zhang, Physical Review E 80, 040104(R) (2009).

VII. Conductivity exponents in stick percolation

VIII. Ink-jet printed thin-film transistors with carbon nanotube channels shaped in long strips
Summary of Appended Papers

**Paper I.** On the basis of Monte Carlo simulations, this paper establishes the fundamental relationship in SWCNT networks from the standpoint of heterogeneous stick percolation. It is found that the SWCNT density region featuring predominant semiconducting percolation paths is determined by the half-probability density and the fraction of m-SWCNTs. My contribution includes modeling and simulations, analysis and conclusion, and manuscript writing.

**Paper II.** This paper presents the electrical performance of low-density SWCNT TFTs fabricated by combining silicon technology with drop casting of SWCNT solution. The rectification behaviors based on diode connection of these TFTs are shown. It also demonstrates performance insensitivity of such devices to the electrode materials. My contribution includes device fabrication, electrical characterization, data analysis and manuscript writing.

**Paper III.** This paper investigates the effects of self-gating on the electrical performance of SWCNT TFTs fabricated with a back-gate device structure. My contribution includes device fabrication, electrical characterization, data analysis, modeling and simulations, and manuscript writing.

**Paper IV.** This paper introduces a novel device structure, *i.e.*, composite SWCNT network, based on extensive Monte Carlo simulations, for high-performance TFTs made from pristine SWCNTs. My contribution includes idea generation, preliminary structure design, modeling and simulations, and manuscript writing.

**Paper V.** This paper sets up the most comprehensive Monte Carlo simulation model based on heterogeneous stick percolation for SWCNT TFTs. It also presents applications of the model in unveiling the underlying physics of doping effects in SWCNT TFTs, especially for their application as sensors. The model provides insightful information on how the various components of an SWCNT TFT may contribute to the overall device performance. My contribution includes modeling and simulations, data analysis, mechanism study, and manuscript writing.

**Paper VI.** This paper proposes a high-efficiency algorithm for Monte Carlo simulation of large-size stick percolation systems. It also reports high-precision percolation threshold and universal finite-size scaling function for two-dimensional stick systems. My contribution includes algorithm and code development, percolation theory investigation, simulations and data analysis, and manuscript writing.

**Paper VII.** This paper clarifies the dependence of conductivity exponents on the stick-to-junction resistance ratio in two-dimensional stick systems. My contribution includes modeling and simulations, data analysis, and manuscript writing.

**Paper VIII.** This paper demonstrates the compatibility of long-strip-channel SWCNT TFTs with ink-jet printing based on Monte Carlo simulations, and presents the proof-of-the-concept electrical performance of the ink-jet printed SWCNT TFTs fabricated on silicon wafer and flexible Kapton substrates. My contribution includes modeling and simulations,
ink-jet printing technique development, device design and fabrication, electrical characterization, data analysis, and manuscript writing.
Related work not included in the thesis

1. Photo-activated interaction between P3HT and single-walled carbon nanotubes studied by means of field-effect response

2. Characterization of acid-treated carbon nanotube thin films by means of Raman spectroscopy and field-effect response

3. Inkjet printing of stripe-featured single-walled carbon nanotube thin film transistors

4. Thin-film field-effect transistors based on composites of semiconducting polymer and carbon nanotubes

5. Charge-injection-induced time decay in carbon nanotube network based FETs
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Jiantong Li
Stockholm 2010-08-24
Symbols and Acronyms

$C_{ox}$  Gate capacitance  
$D_c$  Linear stick density  
$f_M$  Fraction of m-SWCNT  
$G_{m}$  Conductance of m-SWCNT  
$G_s$  Conductance of s-SWCNT  
$G_q$  Two units of quantum conductance  
$I$  Current  
$I_D$  Drain current  
$I_{OFF}$  OFF state source/drain current  
$I_{ON}$  ON state source/drain current  
$I_S$  Source current  
$L$  Percolation system size  
$L_C$  Channel length  
$L_S$  Nanotube/Stick length  
$l$  Stick length or stick segment length  
$l_c$  Critical stick length  
$m$  Scaling exponent  
$m_{OFF}$  OFF-state scaling exponent  
$m_{ON}$  ON-state scaling exponent  
$N$  Stick number density  
$N_c$  Critical stick number density  
$p$  Nanotube/stick coverage (normalized number density)  
$R_j$  Stick-stick junction resistance  
$R_s$  Stick resistance  
$r$  Ratio of channel length to channel width  
$t$  Critical conductivity exponent  
$t_{ox}$  Gate dielectric thickness  
$V$  Voltage  
$V_D$  Drain voltage  
$V_{DS}$  Drain-to-Source drive voltage  
$V_G$  Gate voltage  
$V_{GS}$  Gate-to-Source drive voltage  
$V_S$  Source voltage  
$V_{th}$  Threshold voltage  
$v$  Critical correlation-length exponent  
$v_T$  Thermal velocity  
$W$  Channel Width
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
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<tbody>
<tr>
<td>$W_{\text{OSP}}$</td>
<td>Width of OSP density region</td>
</tr>
<tr>
<td>$W_{\text{strip}}$</td>
<td>Strip Width</td>
</tr>
<tr>
<td>$\mu$</td>
<td>Half-probability density</td>
</tr>
<tr>
<td>$\mu_{\text{eff}}$</td>
<td>Effective mobility</td>
</tr>
<tr>
<td>$\varepsilon_0$</td>
<td>Vacuum permittivity</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>Relative permittivity</td>
</tr>
<tr>
<td>$\theta_a$</td>
<td>Alignment angle</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Mean free path</td>
</tr>
<tr>
<td>$\rho$</td>
<td>Nanotube density</td>
</tr>
<tr>
<td>$\rho_c$</td>
<td>Critical nanotube density</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Conductivity</td>
</tr>
<tr>
<td>$\tilde{\sigma}$</td>
<td>Apparent conductivity exponent</td>
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<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
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<tbody>
<tr>
<td>AA-CNN</td>
<td>Composite CNN with primary aligned long-SWCNT arrays and secondary aligned short-SWCNT arrays</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic Layer Deposition</td>
</tr>
<tr>
<td>AR-CNN</td>
<td>Composite CNN with primary aligned long-SWCNT arrays and secondary random short-SWCNT networks</td>
</tr>
<tr>
<td>CNN</td>
<td>Carbon Nanotube Network</td>
</tr>
<tr>
<td>DI water</td>
<td>Deionized water</td>
</tr>
<tr>
<td>EM</td>
<td>Contact between electrode and m-SWCNT</td>
</tr>
<tr>
<td>ES</td>
<td>Contact between electrode and s-SWCNT</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchhoff’s current law</td>
</tr>
<tr>
<td>MM</td>
<td>Junction between two m-SWCNTs</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor field effect transistor</td>
</tr>
<tr>
<td>MS</td>
<td>Junction between an m-SWCNTs and an s-SWCNT</td>
</tr>
<tr>
<td>OSP</td>
<td>Only s-SWCNT percolation</td>
</tr>
<tr>
<td>PVP</td>
<td>Polyvinylpyrrolidone</td>
</tr>
<tr>
<td>SDBS</td>
<td>Sodium dodecylbenzene sulfonate</td>
</tr>
<tr>
<td>SDS</td>
<td>Sodium dodecylsulfate</td>
</tr>
<tr>
<td>SS</td>
<td>Junction between two s-SWCNTs</td>
</tr>
<tr>
<td>SWCNT</td>
<td>Single-Walled Carbon NanoTube</td>
</tr>
<tr>
<td>m-SWCNT</td>
<td>metallic Single-Walled Carbon NanoTube</td>
</tr>
<tr>
<td>s-SWCNT</td>
<td>semiconducting Single-Walled Carbon NanoTube</td>
</tr>
<tr>
<td>TFT</td>
<td>Thin Film Transistor</td>
</tr>
<tr>
<td>UFSSF</td>
<td>Universal finite-size scaling function</td>
</tr>
</tbody>
</table>
1. Introduction

In 1993, a Japanese research group led by Professor Iijima reported their discovery of a new kind of nanostructured materials: single-walled carbon nanotubes (SWCNTs) [1]. As shown in Fig. 1.1, an SWCNT represents a long and thin cylinder (with a diameter typically about 1 nm) of carbon atoms each sitting on one of the six corners of a honeycomb hexagon connected by the strong chemical bonds through the so-called \( sp^2 \) hybridization. An SWCNT can also be thought of as a ribbon of graphene rolled into a seamless, one-atom-thick cylinder. Such a unique quasi one-dimensional structure produces a range of intriguing properties. In particular, SWCNTs are mechanically strong, flexible, and electrically conductive or semiconducting [2]. Semiconducting SWCNTs possess fairly large band gaps which can produce high ON/OFF current ratios (generally \( 10^4 - 10^6 \)) for logic electronic devices such as field-effect transistors (FETs) [3]. In 1998, the first FETs based on individual SWCNTs were fabricated [4,5], which extended the promising application of SWCNTs into the field of electronics [6-9]. Thereafter, the demonstration of their ballistic transport or diffusive transport with long mean free paths (on the order of 1 \( \mu m \)) [7,10] and extraordinarily high mobility (~ 100,000 cm\(^2\)/V s) [11] at room temperature suggests their potential to outperform conventional inorganic materials and predominate in next-generation nanoelectronics [12].

![Figure 1.1. Schematic illustration of an SWCNT, a long and thin cylinder of carbon atoms.](image)

At present, however, at least two significant technological challenges need to be overcome in order to further develop FETs based on individual SWCNTs. One is the electrical
Ink-jet printing of thin film transistors based on carbon nanotubes

It is well known that SWCNTs are actually a mixture of two-thirds semiconducting SWCNTs (s-SWCNTs) and one-third metallic SWCNTs (m-SWCNTs). In addition, s-SWCNTs are inhomogeneous in the sense that their electrical properties vary with the tube chirality and diameter [6]. It is hence demanding to select SWCNTs of a specific electronic property from the pristine SWCNTs. The other challenge is the difficulty in precisely positioning such nanoscale materials for device assembly, as required for a deterministic integration into circuits [12]. To alleviate these challenges, thin film transistors (TFTs) based on random carbon nanotube networks (CNNs) were proposed to provide a viable route to the most immediate electronic applications of SWCNTs [13]. The involvement of large numbers of SWCNTs may minimize the device-level effects of the electrical heterogeneity in SWCNTs and relax the requirements of a precise spatial position or orientation of all individual tubes in the networks [12]. As a matter of fact, in combination with their excellent mechanical properties, CNN-based TFTs have already been demonstrated as promising building blocks for many emerging and rapidly growing advanced electronic systems, such as large-area electronics (macroelectronics) [14], stretchable electronics [15], and flexible or printed electronics [16-18].

In particular, their compatibility with flexible substrates and solution processability [19] make SWCNTs ideal materials for the ink-jet printing technique [18]. Ink-jet printing has now become a very popular technology for the emerging electronics because of its capacity of combining simple additive processing with novel materials [20], reducing fabrication processes and saving materials, generating fine and arbitrary patterns [21], and aligning well among multiple layers. Together with its high repeatability and scalability, ink-jet printing is of potential to effectively reduce the fabrication cost of integrated circuits for niche applications such as large-area displays, especially compared with the conventional silicon process technology [20].

Disappointedly, the electrical performance of today’s ink-jet printed SWCNT TFTs [18,22] is still inferior primarily because the TFTs mainly suffer from the common challenge in CNN-based electronic devices caused by the “m-SWCNT contamination” [23]. Nevertheless, there is still possibility to benefit from the fact that m-SWCNTs “only” make one third of the pristine SWCNT products. Starting from here, a likely approach to obtain
high ON/OFF current ratios is to construct long-channel SWCNT TFTs where individual SWCNTs are much shorter than the channel lengths and a transport path should rely on percolating CNNs. As long as the SWCNT density is low enough that m-SWCNTs themselves cannot form percolating networks and transport paths have to involve at least one s-SWCNT, high ON/OFF current ratios can be achieved. However, low-density CNNs also lead to a reduced ON current. As a result, the “m-SWCNT contamination” renders CNN-based electronic devices in a dilemma that large ON/OFF current ratios and high ON currents are difficult to achieve simultaneously. This dilemma may severely restrict the electronic applications of such devices.

To suppress the effects of “m-SWCNT contamination”, a variety of approaches have been proposed to remove or separate m-SWCNTs from s-SWCNTs, including dielectrophoresis [24], selective etching [25], electrical breakdown [26], density-gradient ultracentrifugation [27], chemical reaction [28], and DNA-assisted [29] or agarose gel-assisted [30] separation, etc. However, these methods to date only achieve low yields or throughputs, but possibly involve substantial cost [30] or performance degradation [12]. They are yet to meet the requirement of mass production in industrial applications and to become compatible with ink-jet printing. On the other hand, engineering as-synthesized SWCNTs into specially designed network structures [12] is also possible to provide an excellent solution to SWCNT TFTs with both high ON currents and large ON/OFF current ratios. It might offer an effective and feasible way for low-cost mass production of high-performance CNN-based electronic devices.

This thesis aims to develop reliable techniques for ink-jet printing of fairly high-performance TFTs based on as-synthesized SWCNTs with special network structures. Monte Carlo simulation models on the basis of stick percolation are constructed to generate fundamental knowledge, explore novel CNN structures for performance improvement, estimate their performance limits, evaluate their compatibility with the ink-jet printing technique, and guide the device design. Starting from ink formulation, experimental verifications are then carried out using both drop-casting and ink-jet printing in combination with standard silicon technology.

The thesis is organized as follows. Chapter 2 introduces in detail the device physics of
SWCNT TFTs in terms of network characteristics (homogeneous versus heterogeneous) and device dimension (short channel versus long channel). Chapter 3 presents our first experimental results concerning long-channel TFTs based on low-density random CNNs, including device fabrication (relying on conventional silicon technology), performance analysis and challenge discussion. This chapter necessitates the employment of well-designed CNN structures for performance improvement.

Chapter 4 constructs Monte Carlo simulation models on the basis of stick percolation for studies of CNN-based TFTs and develops efficient algorithms for the simulation. By conducting simulations, Chapter 5 presents crucial results for general stick percolation, such as percolation threshold, conductivity exponent and finite-size scaling. It further establishes fundamental relationships in heterogeneous stick percolation to estimate optimal SWCNT density regions for high-performance TFTs. The physics is also discussed for doping effects in SWCNT TFTs. Chapter 6 explores and demonstrates novel CNN structures, composite networks and strip-featured networks, to achieve both high ON currents and large ON/OFF current ratios for TFTs and evaluate their compatibility with ink-jet printing.

Chapter 7 demonstrates our attempts on ink-jet printing of SWCNT TFTs with long-strip channels on silicon wafers and flexible substrates (Kapton). Compatible and stable SWCNT inks are formulated with proper SWCNT concentration and suitable additives. Appropriate printing procedure and post-printing treatments guarantee excellent SWCNT strip patterns. Subsequently, SWCNT TFTs are ink-jet printed with high yield and improved electrical performance compared with similar efforts based on as-synthesized SWCNTs in the literature.

The thesis is concluded with an extensive summary as well as a future outlook in Chapter 8.
2. Device Physics

The first employment of SWCNT networks, or CNNs, as the channel materials for TFTs was demonstrated by Snow et al. in 2003 [13]. Since then, SWCNT-based TFTs have attracted extensive attentions [14] and been proposed as a promising building block for the emerging macroelectronics. Plenty of efforts, either experimental or theoretical, have been made to probe the performance limits [31-36] and unveil the underlying physics [37-41]. SWCNT TFTs are expected to follow a special set of device physics. On one hand, with respect to transistors based on conventional semiconductor materials, SWCNT TFTs have networked stick-like nanoparticles as the channel materials so that their electrical performance should significantly depend on the percolation behaviors of the networks. On the other hand, different from conventional percolation systems, CNNs involve both metallic and semiconducting materials. Classic percolation theory might not always be able to account for the electrical properties of CNNs either. As a result, special theoretical models need to be developed for SWCNT TFTs to fully understand the device physics and advance the art in this field. Through valuable endeavors of several groups [37-41], fairly sophisticated device physics has been established for SWCNT TFTs mainly on the basis of the theory for generalized heterogeneous stick percolation, i.e., a system consisting of different types of sticks.

In this chapter, the well-established device physics in the literature is introduced briefly. First, several typical device architectures are presented. Then, device physics is discussed in terms of the CNN characteristics for homogeneous s-SWCNT TFTs (short channel and long channel) and heterogeneous SWCNT TFTs.

2.1 SWCNT TFT device architectures

Similar to the structures of conventional field-effect transistors, an SWCNT TFT comprises three parts, a dielectric layer, a CNN layer as the channel and three electrodes. Two of the electrodes, the source and the drain, directly contact the CNN; the third, the gate, is separated from the CNN by the dielectric layer. The current flows between the source and
drain electrodes and is controlled by the voltage applied to the gate electrode. As discussed below, different architectures of SWCNT TFTs are often utilized dictated by the performance request and fabrication convenience.

According to the layout of the gate, there are two typical architectures for SWCNT TFTs, back-gate and top-gate, as illustrated in Fig. 2.1. The former contain SWCNT thin films deposited on top of predefined gate electrode and dielectric [Figs. 2.1(a) and 2.1(c)] while the latter deposit gate dielectric and electrode onto predefined SWCNT thin films [Fig. 2.1(b) and 2.1(d)]. Usually it is much more convenient to process gate electrode and dielectric prior to SWCNT deposition. Therefore, back-gate TFTs are easy to fabricate and extensively used for evaluating properties of SWCNT TFTs. An ideal example for gate

---

**Figure 2.1.** Schematic illustration of SWCNT TFTs: (a) back-gate with bottom-contact source/drain; (b) top-gate with top-contact source/drain, (c) back-gate with top-contact source/drain; (d) top-gate with bottom-contact source/drain.
electrode and dielectric in back-gate TFTs is a heavily-doped silicon wafer capped with a thin layer of SiO$_2$. However, due to the lack of a proper surface passivation coupled with weak resistance of CNNs to environmental impact, back-gate TFTs are usually difficult to produce reproducible and reliable performance. In addition, for circuit integration it is necessary that each device have its own gate, instead of using the entire silicon substrate as a common gate. In contrast, the natural passivation from the gate dielectrics in the top-gate configuration can yield reliable performance and thereby making the TFTs suitable for integrated circuits with complex device-to-device interconnects [12,16].

Similarly, in terms of the layout of the source/drain electrodes with respect to the SWCNT thin films, the architectures of SWCNT TFTs can be classified into bottom contact and top contact structures, as also illustrated in Fig. 2.1. Bottom-contact TFTs [Figs. 2.1(a) and 2.1(d)] have source/drain electrodes predefined before deposition of SWCNT thin films and are easy to fabricate. However, it has been demonstrated [42] that bottom-contact TFTs often have lower contact conductance than top-contact TFTs [Figs. 2.1(b) and 2.1(c)].

2.2 SWCNT TFT device physics

\begin{center}
\includegraphics[width=0.7\textwidth]{figure2.png}
\end{center}

\textbf{Figure 2.2.} Schematic illustration of a typical CNN. Red and green sticks represent m-SWCNTs and s-SWCNTs, respectively.

Figure 2.2 illustrates a typical CNN in a TFT. The device has channel length $L_C$ and channel width $W$. The SWCNTs are represented by sticks with length $L_S$ and number density $\rho$. So
far, no general formula has been proposed to describe the transport behaviors in such TFTs because of their complexity. Nevertheless, SWCNT TFTs with certain CNN structural characteristics have been well studied theoretically and in some particular cases analytical solutions have been acquired. Device physics of such special SWCNT TFTs are discussed below.

2.2.1 Homogeneous s-SWCNT TFTs

For simplicity, homogeneous CNNs comprising pure s-SWCNTs or s-SWCNT bundles are first considered. Previous studies [39-41] suggest that the current flowing between the source/drain electrodes in SWCNT TFTs mainly depends on the device geometry and carrier transport. Explicitly, it can be described as [40]

\[
I_D = \frac{A}{L_S} \xi \left( \frac{L_S}{L_C}, \rho L_S^2 \right) \times f(V_G, V_D),
\]

(2.1)

where \(A\) is a proportionality constant dependent on gate dielectric capacitance, SWCNT diameter, and SWCNT-SWCNT interaction. The function \(\xi(x)\) describes the effects of geometrical parameters (\(L_S, L_C\) and \(\rho\)) and the function \(f(x)\) describes the effects of bias conditions (drain bias \(V_D\) and gate bias \(V_G\)). The expressions of \(\xi(x)\) and \(f(x)\) are both expected to depend on the device characteristics and carrier transport properties and are discussed in detail as follows.

(1) Short-channel device (\(L_C < L_S\))

(i) Ballistic limit. When the channel length \(L_C\) is much shorter than the mean free path \(\lambda\), i.e., \(L_C < \lambda\), ballistic transport through the tubes can be assumed [39]. Therefore, \(f(V_G, V_D)\) is given by [6, 41]

\[
f(V_G, V_D) = (V_G - V_{th}) v_T,
\]

(2.2)

where \(V_{th}\) is the threshold voltage and \(v_T\) is the thermal velocity. Furthermore, if the tube
density is below the percolation threshold $\rho_c$, i.e., $\rho < \rho_c$, the tube-tube interaction can be neglected and the transport is independent of channel length but directly proportional to the number of tubes $N$, bridging source and drain [39]. Therefore, if the orientation of all tubes are randomly distributed [14,39,41],

$$\xi = N_S = \frac{2D_c L_S}{\pi} \left[ \sqrt{1 - \left( \frac{L_C}{L_S} \right)^2} - \frac{L_C}{L_S} \cos^{-1}\left( \frac{L_C}{L_S} \right) \right], \quad (2.3)$$

where $D_c$ is the linear tube density.

(ii) Diffusive limit. When $L_C >> \lambda$, the transport is assumed to be diffusive and $f(V_G, V_D)$ is given by [40]

$$f(V_G, V_D) = (V_G - V_{th}) V_D - \beta V_D^2, \quad (2.4)$$

where $\beta$ is a constant and usually takes the value of 1/2. In this case, the transport in each of the bridging tubes is inversely proportional to intercepted channel length. Therefore [41],

$$\xi = \frac{D_c}{\pi} \left[ \cos^{-1}\left( \frac{L_C}{L_S} \right) - \sqrt{1 - \left( \frac{L_C}{L_S} \right)^2} \right], \quad (2.5)$$

(2) Long-channel device ($L_C > L_S$)

In long-channel devices, no tube can bridge the source/drain electrodes and tube-tube interactions are significant. Therefore, usually only diffusive limit can be anticipated. Equation (2.4) is still valid at very high tube density ($\rho >> \rho_c$) [40]. However, in this case, $\xi$ cannot be analytically solved though is still found to be independent of bias conditions. It now follows [40]
Ink-jet printing of thin film transistors based on carbon nanotubes

\[
\xi \left( \frac{L_S}{L_C}, \rho L_S^2 \right) = \left( \frac{L_S}{L_C} \right)^m \rho L_S^2 ,
\]

(2.6)

where \( m \) is an exponent dependent on the tube density. Roughly, \( m \) scales inversely as \( \rho L_S^2 \) [37,40].

2.2.2 Heterogeneous SWCNT TFTs

In practice, TFTs made of as-synthesized SWCNTs actually feature heterogeneous CNNs in the sense that approximately only two thirds of the SWCNTs are semiconducting and the remaining one third metallic. The involvement of “m-SWCNT contamination” makes the CNN structure much more complicated and in principle no sophisticated physics has been established for such heterogeneous SWCNT TFTs. Nevertheless, some critical behaviors have been well understood based on the physics for homogeneous s-SWCNT TFTs.

It is well accepted in theoretical studies [37] that (1) the conductance of m-SWCNTs (\( G_m \)) is almost independent of the gate bias \( V_G \), (2) at ON state, the conductance of s-SWCNTs (\( G_s \)) is similar to \( G_m \), and (3) at OFF state, \( G_s \) is significantly lower than \( G_m \). Therefore, for short-channel (\( L_C < L_S \)) devices, almost inevitably there are m-SWCNTs directly bridging the source/drain electrodes and hence the ON/OFF current ratio usually cannot exceed \(~3\) [12]. As a result, short channel is not a viable device structure for heterogeneous SWCNT TFTs.

In contrast, for long-channel (\( L_C > L_S \)) devices, since no individual tube can span the source/drain directly, carriers must transport through percolating paths consisting of networks of SWCNTs. As long as the networks do not contain abundant percolation paths comprising only m-SWCNTs, high ON/OFF ratios can be achieved. Such characteristics of heterogeneous SWCNT TFTs determine their special scaling behaviors [37]. At ON state, since \( G_m \approx G_s \), the TFTs can be treated as homogeneous CNNs and Eq. (2.6) is valid, i.e., the ON-state current \( I_{ON} \sim \left( \frac{1}{L_C} \right)^{\rho L_S} \). At OFF state, the contribution of s-SWCNTs is negligible and the TFTs can also be treated as homogeneous CNNs only with m-SWCNT
2. Device Physics

and the OFF-state current $I_{\text{OFF}} \sim (1/L_C)^{m_{\text{OFF}}}$. Note that the effective SWCNT density at ON state (including both m-SWCNTs and s-SWCNTs) is about three times that at OFF state (only including m-SWCNTs). Since in Eq. (2.6) the exponent $m$ scales inversely with the density, $m_{\text{ON}} < m_{\text{OFF}}$ is expected. This suggests that in heterogeneous SWCNT TFTs, the ON-state current $I_{\text{ON}}$ follows different scaling rules from the OFF-state current $I_{\text{OFF}}$. Furthermore, the ON/OFF current ratio behaves as

$$\frac{I_{\text{ON}}}{I_{\text{OFF}}} \sim \left(\frac{1}{L_C}\right)^{m_{\text{ON}}} \left(\frac{1}{L_C}\right)^{m_{\text{OFF}}} = \left(L_C\right)^{m_{\text{OFF}}-m_{\text{ON}}}.$$  

(2.7)

This predicts that the ON/OFF current ratio increases with channel length.

In summary, the previously-established device physics indicates that in many cases, with respect to the bias conditions, the transport in SWCNT TFTs follows similar rules $[f(V_G, V_D)]$ to that of conventional MOSFETs. However, with respect to the device structure including geometry parameters and CNN density, SWCNT TFTs behave quite differently from conventional transistors, especially for long-channel heterogeneous SWCNT TFTs.

When ink-jet printed devices are considered, only long-channel heterogeneous SWCNT TFTs are usually available due to the resolution limit of current ink-jet printers. Therefore, particular attention should be paid to this specific device structure as well as to statistical effects during the development of ink-jet printing techniques for SWCNT TFTs. Chapter 3 will discuss our experimental results of SWCNT TFTs fabricated by lithography technique and further emphasize the importance of device structures.
3. SWCNT TFTs by Means of Silicon Technology

Compared with conventional silicon technology, ink-jet printing is an emerging and rather not fully explored technique. Besides the low resolution and relatively poor positioning and alignment, some critical limitations still exist for ink-jet printing of electronic devices and circuits. For example, nowadays not all available metals in microelectronics can be ink-jet printed, such as Al, Pd, Ti, etc. There are no sophisticated methods to formulate inks for these metals. Today, only Ag is widely used in ink-jet printing techniques. These restrictions severely affect many fundamental researches on electronics of SWCNT TFTs.

Solution casting or spin coating of interesting materials to predefined source/drain and gate electrodes by means of silicon technology is a convenient and effective method for evaluation of the printability of certain materials so as to facilitate study of device performance. As a matter of fact, by virtue of solution casting, scientists [19] have demonstrated some printable solutions for SWCNT-based electronic devices. In this thesis, prior to moving into a complete solution with ink-jet printing, SWCNT TFTs are also fabricated by combining solution casting and silicon technology in order to address important issues for ink-jet printing. This chapter first introduces the device fabrication for such SWCNT TFTs, then analyzes their electrical performance, and finally concludes with some suggestions for the development of ink-jet printing techniques. The discussion in this chapter refers to Papers II and III.

3.1 Device fabrication

Since the TFTs here are fabricated by casting SWCNT solutions or suspensions onto a silicon substrate with predefined electrodes, the device architecture here adopts the back-gate device structure with bottom-contact source/drain [Fig. 2.1(a)]. The procedure for device fabrication includes substrate preparation, solution formulation, and drop casting.
3.1.1 Substrate preparation

![Schematic device structure](image1)

**Figure 3.1.** Schematic device structure for a back-gate SWCNT TFT with bottom-contact source/drain on silicon substrate.

![SEM image](image2)

**Figure 3.2.** SEM of an electrode pattern fabricated by silicon technology. The picture actually contains two devices both with asymmetric (Pd-Al) electrodes. If symmetric (Pd-Pd) electrodes are required, the metal Al is not deposited.

As schematically shown in Fig. 3.1, the CNN-based transistors were fabricated on a heavily-antimony-doped silicon substrate capped with a ~150-nm-thick SiO₂. The SiO₂/Si structure served as the gate during electrical characterization for the devices. The source/drain electrodes were formed following the lift-off technique in the conventional silicon technology. First the wafer with the SiO₂ was coated by a layer of photoresist. Then the wafer was exposed and developed to obtain the designed patterns for source/drain electrodes. Afterwards, the metal film (~ 40 nm thick), such as Pd, Al, together with the thin
adhesive layer of Ti film (~2 nm thick), was deposited using electron-beam evaporation. Finally, the remaining photoresist was stripped together with the unwanted metals to complete the substrate preparation. The resultant electrode pattern is shown in Fig. 3.2. The width of the source/drain electrodes varies from 1 to 100 µm and the source-to-drain gap (channel length) from 1 to 200 µm. As shown in Fig. 3.2, the devices may include both symmetric (Pd-Pd) electrodes and asymmetric (Pd-Al) electrodes.

### 3.1.2 Solution formulation

![AFM images for (a) the channel region between the Al (lower) and Pd (upper) electrodes of a CNN device and (b) one corner of a CNN region, indicating that all SWCNTs lie inside the window defined by lithography.](image)

Figure 3.3. AFM images for (a) the channel region between the Al (lower) and Pd (upper) electrodes of a CNN device and (b) one corner of a CNN region, indicating that all SWCNTs lie inside the window defined by lithography.

The SWCNTs used in the present work were commercially available from Carbon Nanotechnologies Inc., Houston and fabricated by means of high-pressure conversion of CO (HiPco). To formulate the SWCNT suspensions for drop casting, SWCNTs were dispersed into deionized water (DI water) with the surfactant (~1 wt.%) of sodium dodecylbenzene sulfonate (SDBS) or sodium dodecylsulfate (SDS). Then ultra-sonication for ~30 min was applied, followed by centrifugation at 16,000 g for over 10 hours in order to precipitate big bundles of SWCNTs. In the end, only the upper part of clear suspension was retrieved as the final SWCNT solution for device fabrication. Since the device physics has been well studied both experimentally and theoretically in the literature [37,40] for high-density (\(\rho \gg \rho_c\)) long-channel SWCNT TFTs, this chapter only deals with low-density (\(\rho \sim \rho_c\)) long-channel SWCNT TFTs [Fig. 3.3(a)]. In order to obtain low-density SWCNTs, more DI water might be further added to dilute the starting SWCNT solution.
3.1.3 Drop casting

To ensure a good adhesion of SWCNTs, the wafer surface was first functionalized with an \( \text{NH}_2 \)-terminated self-assembled monolayer by immersion in a 1-mM chloroform solution of 3-aminopropyl-triethoxysilane for 30 min, and then baked at 110 °C for 10 min [43]. The wafer was subsequently coated with a 1.2-µm-thick photoresist (a standard positive novolac resist, SPR 700-1.2). Rectangular windows extending to the electrode pairs were opened by means of photolithography in order to define the channel regions. Afterwards, the SWCNT solution was cast onto the wafer surface. Shortly after the solution became dried through natural evaporation, the photoresist was removed to obtain the final SWCNT TFTs. The SWCNT density is around 2 \( \mu \text{m}^{-2} \) and the average SWCNT length is about 1.5 \( \mu \text{m} \) (Fig. 3.3). It is worth noting that the combination of solution casting and lift-off technique allows for precisely positioning of SWCNTs. Figure 3.3(b) shows the AFM image of one corner of a CNN region. It is clear that all the SWCNTs stay within the predefined area.

3.2 Electrical performance

All the device electrical performance in this chapter was characterized using an HP4516A precision semiconductor parameter analyzer in ambient environment at room temperature.

3.2.1 Transfer characteristics

![Figure 3.4. Transfer \( I_D-V_G \) characteristics of a typical SWCNT TFT \( L_C = 30 \mu \text{m and } W = 100 \mu \text{m} \) with symmetric Pd-Pd electrodes, displayed in linear (left vertical axis) and logarithmic (right vertical axis) scales.](image-url)
As shown in Fig. 3.4, the device exhibits unipolar \( p \)-type transistor behavior with the threshold voltage \( V_{th} = -14.5 \) V and ON/OFF ratio over \( 10^3 \). The effective mobility can be estimated according to the following equation,

\[
\mu_{eff} = \frac{\left( \partial I_D / \partial V_G \right) L_C}{W C_{ox} V_D}.
\]  \( (3.1) \)

For this device, the peak transconductance is \( \partial I_D / \partial V_G \approx 8.2 \times 10^{-9} \) A/V at \( V_D = -5 \) V. And the capacitance is calculated from the simple parallel-plate capacitor model as \( C_{ox} = \varepsilon_0 \varepsilon_r t_{ox} = 2.30 \times 10^{-8} \) F/cm\(^2\). As a result, \( \mu_{eff} \approx 0.02 \) cm\(^2\)/V s is obtained. This value is rather low and only comparable to some organic semiconductors (usually < 0.1 cm\(^2\)/V s) [44].

### 3.2.2 Performance scaling

\[ \text{Figure 3.5. Plots of (a) ON current and (b) ON/OFF current ratio against W/L for large SWCNT TFTs (with Pd-Pd symmetric electrodes) of various channel dimensions (L ranging from 20 \( \mu \)m to 200 \( \mu \)m and W from 50 \( \mu \)m to 100 \( \mu \)m).} \]

The device preparation procedure described above leads to a relatively high yield of the TFTs. Out of the randomly-selected 50 long-channel devices, 37 TFTs are obtained and 26 of them display effective gate modulation with an ON/OFF current ratio over \( 10^3 \) without any further elaborated control of the SWCNT density or any post-treatment aiming at elimination of the m-SWCNTs. The devices include various length (from 3 \( \mu \)m to 200 \( \mu \)m) and width (from 1 \( \mu \)m to 100 \( \mu \)m). Such a high yield permits the studies on scaling.
behaviors for the low-density SWCNT TFTs. Figure 3.5 shows how $I_{ON}$ and $I_{ON}/I_{OFF}$ vary with the device width-to-length ratio $W/L_C$. Neither $I_{ON}$ nor $I_{ON}/I_{OFF}$ indicates any clear dependence on $W/L_C$. Therefore, the scaling rules expected by Eqs. (2.6) and (2.7) might not apply to these low-density SWCNT TFTs. The reason might be that near percolation threshold, the CNN is very sensitive to the SWCNT density. Therefore, a little fluctuation in the SWCNT density may generate a huge change in the electrical performance resulting in unexpected scaling behavior.

**3.2.3 Effects of electrode metals**

![Figure 3.6](image_url)

*Figure 3.6. $I_D-V_G$ curves for SWCNT TFTs with (a) asymmetric Pd-Al electrodes and (b) symmetric Pd-Pd electrodes.*

The effects of electrode metals on the electrical performance are also studied by comparing devices with asymmetric and symmetric source/drain electrode metals. For this purpose, each device was measured twice by exchanging the source and drain terminals. Figures 3.6(a) and 3.6(b) show the transfer characteristics for SWCNT TFTs of Pd-Al and Pd-Pd electrodes, respectively. Literature data indicate that Pd is suitable for Ohmic contact with s-SWCNT while Al is for Schottky contact [9,45,46]. Therefore, it is reasonable to expect that the electrical behaviors would be significantly different between SWCNT TFTs with Pd and Al as the source electrodes. However, it is of interest and importance to note that no matter whether the source/drain electrodes are symmetric or asymmetric, an exchange of the source and drain terminals during the $I_D-V_G$ measurement gives no substantial difference in device performance, in terms of the ON-state current, OFF-state current as well as the
threshold voltage. It is therefore inferred that the electrode/SWCNT contacts play a negligible role in the electrical performance of SWCNT TFTs.

![Figure 3.7](image)

*Figure 3.7. $I_D$-$V_D$ curves for the corresponding diode-connected transistors in Fig. 3.6 with (a) asymmetric Pd-Al electrodes and (b) symmetric Pd-Pd electrodes.*

The reason that the electrical performance of SWCNT TFTs is insensitive to the electrode materials might still be ascribed to the “m-SWCNT contamination” in the sense that m-SWCNTs may cause short-circuit between the CNNs and the electrodes. As a result, the contact property seems not to be controllable by selecting desired metal electrodes. For this reason, it is inconvenient to fabricate Schottky diodes or rectifiers by using different types (Ohmic or Schottky) of metals to form asymmetric contacts with CNNs, though this method has been verified for fabrication of Schottky diodes based on individual s-SWCNTs [45,46]. Rectifiers represent another important family of active devices in microelectronics and are also indispensable for developing circuits and systems in macroelectronics. It is thus highly likely that the “m-SWCNT contamination” in CNNs has inhibited an effective way to fabricate rectifiers straightforwardly based on undoped CNNs, except for the $p$-$n$ diodes which involving complicated partial doping of a CNN [32]. In this study, it is demonstrated that the diode connection mode of an SWCNT TFT may be an ideal solution for such rectifiers. As shown in Fig. 3.7, by connecting the source and the gate of a CNN-based transistor, we immediately observed excellent rectifying characteristics when performing two-terminal current-voltage measurements between the cathode (source) and anode (drain) of the resulting rectifier. The forward/reverse current ratio can exceed $10^5$. 

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Based on the similar mechanism of diode-connected transistors, our research suggests that for back-gate transistors constructed on SiO$_2$/Si substrates, rectifier behavior can be observed even when the source and gate are not connected, i.e., when the substrate is floating. This issue is not unique to CNN-based rectifiers. It also applies to rectifiers based on individual s-SWCNT or even silicon.

![Image of potential distribution in various substrates](image)

**Figure 3.8.** Two-dimensional numerical simulation results for the potential distribution in various substrates (before depositing SWCNTs) where the left electrode above is set to ground: heavily-doped Si substrate with the right electrode being biased at (a) +10 V and (b) -10 V, insulator substrate with the right electrode being biased at +10 V (c), and (d) lightly-doped Si substrate with the right electrode being biased at +10 V. The gate oxide SiO$_2$ is 150 nm thick.

As revealed by the simulation results in Fig. 3.8, if the substrate is a heavily-doped silicon, the substrate potential is independent of the source/drain biases even when it is intentionally kept floating. Therefore, there can be potential difference between the source and substrate (gate), which can act as the gate-to-source drive voltage $V_{GS}$. Under positive bias, the grounded electrode (source) actually acts as the drain and the biased electrode (drain) actually as the source. Hence, the floating substrate, which is nearly uniformly set to zero potential by the source through the capacitive coupling [Fig. 3.8(a)], provides a negative $V_{GS}$ and helps to turn on the transistor. Under negative bias, the grounded electrode acts as the source and the biased electrode as the drain. Then, the substrate can only provide zero $V_{GS}$ [Fig. 3.8(b)] and cannot turn on the transistor. Therefore, the device attains a high forward current at positive bias and a low reverse current at negative bias even when the substrate (back gate) is intentionally unbiased. This phenomenon is called *self-gating*. 

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induced rectification. On the other hand, when the substrate is a lightly-doped silicon or an insulator, its potential varies laterally between the two locations beneath the source/drain electrodes [Figs. 3.8(c) and 3.8(d)] and hence self-gating becomes insignificant.

However, though the self-gating induced rectification is able to serve as two-terminal rectifiers, it is evidently different from the rectifier behaviors of a normal $p$-$n$ diode or Schottky diode. According to the mechanism, the self-gating induced rectification always attains a high forward current at positive bias and a low reverse current at negative bias no matter which electrode is biased or grounded, that is to say, self-gating induced rectification only depends on bias and there is no polarity of the electrodes. As shown in Fig. 3.9(a), after switching the probes during the measurement, the $I$-$V$ characteristics almost remain identical. In contrast, for a conventional diode, the two $I$-$V$ curves should be symmetric about the origin of the coordinates after exchanging the probes [Fig. 3.9(b)]. Therefore, self-gating induced rectification presents an anomalous rectification but it is easy to be confused with the conventional rectifier behaviors. Particular care must be taken of the effects of self-gating induced rectification in practice.

Figure 3.9. Two-terminal $I$-$V$ curves for SWCNT TFTs with Pd-Pd symmetric electrodes on (a) heavily-doped Si wafer and (b) glass substrates before (squares) and after (circles) switching the probes. Note that most of the devices fabricated on heavily-doped silicon wafer exhibited rectification behavior like that in (a) while only a few devices fabricated on glass substrate exhibited rectification like that in (b).
In conclusion, high-yield TFTs with large ON/OFF ratio can be achieved by using low-density SWCNT networks. In addition, its diode connection mode is an ideal solution for CNN-based rectifiers with excellent performance of forward/reverse current ratio over $10^5$. However, low-density SWCNT TFTs suffer from low mobility and unclear scaling behaviors, which may restrict their practical applications in electronics. As a result, low-density SWCNT TFTs might not be a good solution to ink-jet printed electronic devices. On the other hand, this chapter demonstrates that the electrical performance of SWCNT TFTs is insensitive to the electrode materials most likely due to the effects of “m-SWCNT contamination”. This is an important and useful conclusion for ink-jet printing of SWCNT TFTs since it opens the door for more mature metal inks such as silver to be printed for fabrication of SWCNT TFTs.
4. Monte Carlo Simulation Models

In the preceding chapters, it was demonstrated that low-density SWCNT TFTs might not be suitable for applications in electronic circuits. Therefore, high-performance SWCNT TFTs are likely to rely on high-density CNNs. However, in high-density SWCNT TFTs, the device performance can be defeated by the “m-SWCNT contamination”; the m-SWCNTs may form all-metallic conduction pathways from source to drain and electrically short the devices, resulting in small ON/OFF current ratios. Encouragingly, our researches indicated that for high-density SWCNT TFTs with some novel device structures, all-metallic percolation paths can be effectively suppressed. Consequently, high-performance TFTs with both high ON state current and large ON/OFF current ratio can be attained. The characteristics of such device structures include special CNN morphology and/or device geometry. An effective and convenient way to explore or demonstrate such novel device structures is to conduct Monte Carlo simulations on the basis of stick percolations [14,16]. This chapter introduces the percolation models as well as some high-efficiency algorithms for Monte Carlo simulations. The discussion in this chapter refers to Papers I, V, VI, and VII.

4.1 Generalized stick percolation models

The models in our work consider two-dimensional percolation systems consisting of widthless sticks. In principle, the models use sticks to represent SWCNTs and the formed percolation systems to model the CNNs. The electrical properties of the CNNs are calculated from solutions of simultaneous equations based on Kirchoff’s current law (KCL). In order to be able to consider as many complicated factors as possible for approaching true SWCNT TFTs, generalized stick percolation models are described in detail as follows.

As illustrated in Fig. 4.1, an SWCNT TFT is of channel length $L_C$ and width $W$. The source (drain) electrode is attached to the left (right) boundary of the CNN. Each SWCNT is treated as a “stick” with a fixed length $L_S$. Since typical CNNs contain both m-SWCNTs and s-SWCNTs, a fixed fraction, $1/n$, of the SWCNTs are randomly chosen as m-SWCNTs.
and the rest as s-SWCNTs, as respectively represented by the red and green sticks in Fig. 4.1. The boundary conditions can be free boundary conditions (fbc), limited boundary conditions (lbc) or periodic boundary conditions (pdc). For fbc, a part of a stick is permitted to exceed the boundaries. For lbc, the part of a stick beyond the boundaries is trimmed. For pdc, the part of a stick beyond one of the boundaries reappears on the opposite side [39]. The stick systems are percolating if there exists at least one continuous path comprising intersecting sticks to connect the source and drain boundaries. Every two intersecting sticks (SWCNTs) produce one junction. The junction between two m-SWCNTs (MM), two s-SWCNTs (SS) or one m-SWCNT and one s-SWCNT (MS) has different electrical conductance [47].

**Figure 4.1.** Schematic illustration of an SWCNT TFT for the percolation model. All SWCNTs are represented by sticks, red ones for m-SWCNT and green ones for s-SWCNT. The nanotube network consists basically of three kinds of components: SWCNTs (m or s), electrode-SWCNT contacts (ES or EM) and intertube junctions (SS, MM or MS). The hatched areas mark two examples of percolation paths.

During simulation, when two sticks intersect at a position within the channel region, an internal junction is created at the intersection. When a stick intersects with the source or drain boundary, an external junction is created at the intersection. If the system is percolating, all the junctions along the percolation path(s) are marked as “active” junctions. Afterwards, KCL is applied at every active internal junction in order to establish
simultaneous equations and calculate the system conductance. In terms of SWCNT properties (m-SWCNT or s-SWCNT), each stick is assigned an appropriate stick resistivity or resistance. In terms of junction properties (MM, SS or MS), each active internal junction is assigned a proper junction resistance. In terms of the electrode/SWCNT contact properties, each active external junction is attached to a proper contact resistance. Each active internal junction is associated with two electric potentials, \( V_i \) and \( V_i' \), corresponding to the electric potentials of the two sticks at the junction position. Since the internal (stick-stick) junctions are of a finite conductance, \( V_i \) is usually not equal to \( V_i' \). Then, the equations in terms of KCL are written for both \( V_i \) and \( V_i' \) at every active internal junction. All active external junctions connecting the source and drain are applied with the source bias \( V_S \) and drain bias \( V_D \), respectively, which serve as the boundary conditions of the KCL simultaneous equations. By solving these equations, the transported current in the TFT can be readily represented by the sum of currents flowing into (out of) all external junctions connecting the source (drain) boundary. And in the end, the SWCNT TFT conductance can be obtained from dividing the transported current by the applied drain-to-source bias difference \( V_{DS} = V_D - V_S \).

### 4.2 Component conductance

![Figure 4.2. Equivalent circuit scheme of a typical high-density nanotube network consisting of m-SWCNT and s-SWCNT sub-networks connecting each other by MS junctions.](image)

The roles of each of the components in Fig. 4.1, i.e., m-SWCNTs, s-SWCNTs, ES, EM,
MM, SS, and MS, in an SWCNT TFT are illustrated by an equivalent circuit in Fig. 4.2. Before setting up the KCL simultaneous equations to calculate the SWCNT TFT conductance, all the components should each be assigned with a reasonable conductance. Usually they can be obtained from two ways: numerical calculations based on established models and experiential values from previous experiments.

**4.2.1 Model calculated component conductance**

Figure 4.3 shows the geometry of all the classic physical models for the components in SWCNT TFTs. The component conductance can be calculated based on Poisson equation, Landauer formula and WKB approximation. The details are described in Paper V.

![Figure 4.3. Geometries of the components in the simulated SWCNT TFTs for (a) an SWCNT, (b) an ES/EM contact, and (c) an MS junction.](image)

**4.2.2 Experiential component conductance**

In order to avoid complicated model calculations, it is convenient to adopt previous experiment results for the component conductance. However, in experiments usually the conductance of a whole transistor is measured. It is not easy to distinguish the contribution of the electrode/SWCNT contact from that of the SWCNT itself. Therefore, in our work the electrode/SWCNT conductance is not explicitly considered. Instead, the SWCNT takes the average or apparent conductance of the whole device (including electrode/SWCNT contact and SWCNT). At ON state, the conductance along an SWCNT, either m-SWCNT or s-SWCNT, is assumed to be uniform and can therefore be calculated using $G = G_0 \lambda / (\lambda + l)$,
where $G_q = 1.54 \times 10^{-3}$ S is two units of the quantum conductance [10], $l$ is the length of the SWCNT segment, and $\lambda$ is the electron mean free path that is taken as 1.0 µm for m-SWCNTs and 300 nm for s-SWCNTs [48]. Also according to Ref. [47], the intertube junctions have the following conductance: $0.03G_q$ for the MM junctions, $0.015G_q$ for the SS junctions and $0.0003G_q$ for the MS junctions. As for the gate modulation, the OFF conductance of s-SWCNTs is assumed to be $10^6$ lower than the ON conductance described above, since the ON/OFF current ratio is usually about $10^6$ for well-performing transistors based on individual SWCNTs [10]. The conductance of m-SWCNTs and that of intertube junctions are assumed identical in both ON and OFF states.

4.3 High-efficiency algorithms for large-size systems

At present, the minimum device dimension fabricated by ink-jet printing is usually more than 50 µm while the SWCNT length is typically only a few µm. Therefore, the ink-jet printed SWCNT TFTs often correspond to large-size percolation systems with system size $L > 50$. In order to effectively study the percolation behaviors and electrical properties for such large-size systems, high-efficiency algorithms need to be developed in order to evaluate the system percolation status (whether percolating or not) and calculate the system conductance. For simplicity, the algorithms here only consider square systems, but their applications in the more general rectangle systems are straightforward.

4.3.1 Percolation status

In contrast to the classical lattice percolation where all the lattices are regularly deposited [49], stick percolation is a kind of irregular percolation, or continuum percolation. In stick percolation systems, two sticks lie in the same cluster if they intersect. The system percolates if there is at least one cluster connects the two opposite boundaries, for example, the source and drain boundaries in SWCNT TFTs. Usually, the simulation for continuum percolation requires much more calculation efforts than those for lattice percolation, especially in the case of large-size system ($L$ is large). Because of this reason, previous simulations of stick percolation are only performed for small amounts of sticks ($\leq 10^3$) or at small numbers ($< 10^3$) of realizations.
In our work, a high-efficiency algorithm has been developed on the basis of the tree-based algorithm of Newman and Ziff [50,51] and the subcell algorithm [52]. Suppose that the square system is of size (square length) \( L \), the stick is of unity length \( l \) and there are in total \( n \) sticks. As shown in Fig. 4.4, the system is virtually divided into \( L \times L \) subcells (or sub-squares), each with unity length \( l \). Each stick is registered into the subcell in which the center point lies. In terms of such a registration, a stick in a subcell (e.g., the one with solid boundaries in Fig. 4.4) is only possible to intersect sticks in the same or the neighboring subcells (the shaded ones in Fig. 4.4) since the distance between its center and any stick center in other subcells is greater than \( l \), the maximum center distance of two intersecting sticks. Then, it is only needed to check the connectivity property between the newly-generated stick and those sticks belonging to the same or neighboring subcells.

![Figure 4.4. Schematic illustration of stick percolation in a square system (L=5). Each stick is of unity length l=1 and described by its center site and orientation. For clarity, most sticks are presented here only by their centers (black dots). The two interesting system boundaries (the left and right ones) are described also by L connecting sticks. The system is divided into \( L \times L \) subcells (dashed lattices) with unity length l. Each stick is registered in the subcell where its center lies. It is explicitly shown that a stick in a subcell (with solid boundaries) is impossible to intersect any sticks at other subcells than the same one or its neighbors (the shaded ones).](image-url)

As in Ref. [50], a tree structure is used to store the stick clusters. Benefiting from the
“union-find” algorithm and “path compression” technique for the tree structures [50], it is very efficient to obtain the spanning probability $R_{n,L}$ for $n$ sticks on the system of size $L$. Convolving all the measured observables $R_{n,L}$ with the Poisson distribution can generate a common “canonical ensemble” of $R(N,L)$ for any density $N$ as

$$R(N,L) = \sum_{n=0}^{\infty} \frac{\lambda^n}{n!} e^{-\lambda} R_{n,L},$$

where $\lambda = NL^2$ for any $N$ with arbitrary precision. Therefore, this algorithm, in combination with the subcell algorithm, only takes time $O(N^2L^2)$, $i.e.$, $\sim O(n)$, to produce $R(N,L)$ for all available $N$, which is a significant improvement over previous algorithms for stick percolation and comparable to those efficient algorithms for lattice percolation [50].

### 4.3.2 Conductance calculation

The most time-consuming part in the simulation is the conductance calculation. It depends on the solution of the KCL simultaneous linear equations, which in matrix form are

$$Ax = b$$

(4.2)

where $A$ is determined by the stick deposition and component conductance, $b$ is determined by the boundary conditions (external active nodes and their biases) and the unknown $x$ represents the potentials on all the internal active nodes. When the percolation system is of large size, $A$ can become too large to handle by direct methods such as the Cholesky decomposition. For the systems of interest in our studies, $A$ is always sparse, symmetric and positive definite. It is hence effective to implement the iterative method, preconditioned conjugate gradient method (with Jacobi preconditioner) to solve Eq. (4.2).

The algorithm of the preconditioned conjugate gradient method used in our work is adopted from Wikipedia (http://en.wikipedia.org/wiki/Conjugate_gradient_method) and listed in Table 4.1. For our work, $x_0$ is initially set to 0 and the preconditioner $M$ is the diagonal of $A$. In addition, for further optimization, all dangling sticks along with the corresponding
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junctions that do not carry any current [49] are erased prior to establishing KCL simultaneous linear equations. For large-size systems near the percolation threshold, this treatment can also save considerable calculation time.

Table 4.1. The algorithm of the preconditioned conjugate gradient method to solve equation $Ax = b$ [Eq. (4.2)]. $x_0$ is the initial guess of the solution, $M$ is the preconditioner and the subscript “$T$” represents the transpose.

In summary, this chapter establishes the percolation models for Monte Carlo simulations and introduces high-efficiency algorithms for large-size systems compatible with ink-jet printed SWCNT TFTs. Their applications in addressing fundamental issues for stick percolation and exploring novel device structures for high-performance SWCNT TFTs will be introduced in the following chapters.
5. Fundamental Results in Stick Percolation

The Monte Carlo simulation models and the proposed high-efficiency algorithms have enabled us to address several fundamental issues in stick percolation theory. These issues are of crucial importance to electronics based on SWCNT TFTs and hence essential to ink-jet printing of SWCNT TFTs. The issues include percolation threshold, finite-size scaling and critical conductivity exponent for stick systems, the percolation behaviors in heterogeneous percolation, and the physics of doping effects in SWCNT TFTs. The discussion in this chapter refers to Papers I, V, VI, and VII.

5.1 Percolation threshold

Percolation threshold is the critical value of the occupation probability at which an infinite system percolates for the first time. With respect to stick percolation systems, the percolation threshold should refer to the critical stick density $N_c$. The stick density $N$ is measured by the number of sticks per unit area. Previously the percolation threshold has been reported for 2D stick systems in terms of critical stick length $l_c$, as $l_c \sqrt{N}/2 = 2.118 \pm 0.045$ [53], which is equivalent to $N_c l_c^2 = 4.236/\pi$ or $N_c l_c^2 = 5.71 \pm 0.24$ according to the excluded volume (area) theory [54, 55] that $N l_c^2 = N_c l_c^2$. However, this value is rather rough and could be unsuitable for studying many critical behaviors at the percolation threshold for stick systems. Unfortunately, no further work has provided a more precise value.

By virtue of our Monte Carlo models and the high-efficiency algorithms, the spanning functions $R(N,L)$ are well established, as shown in Fig. 5.1(a), for 2D homogeneous square stick systems with free boundary conditions at large system size ($L$ is up to 256) on the basis of a large number ($> 10^7$) of realizations. It is expected that the “finite-size percolation threshold”, $N_{0.5}(L)$, given by the solution of $R[N_{0.5}(L),L]=0.5$, converges to the true $N_c$ as

$$N_{0.5}(L) - N_c = -c L^{-1/v} + \ldots,$$

(5.1)
where $c$ is a constant and $v$ is the correlation-length exponent ($v=4/3$ for two-dimensional systems), as shown in Fig. 5.1(b). The best fit of $N_{0.5}(L)$ to Eq. (5.1) gives an estimate of $N_c=5.63726\pm0.00002$. For a general stick length $l$, the percolation threshold should therefore be

$$N_c l^2 = 5.63726\pm0.00002.$$  
(5.2)

It is consistent with, but significantly more precise than, the previous result [53].

![Figure 5.1. Monte Carlo simulation results for stick percolation on square systems with free boundary conditions. (a) Spanning probability $R$ as a function of stick density $N$ for different system sizes $L$. The horizontal dashed line represents $R=0.5$. (b) Estimated critical density $N_{0.5}(L)$, for $L=32$, 36, 40, 48, 64, 128, and 256, as a function of $L^{-1/v}$. (c) $L(R-0.5)$ vs. $\log_2(L)$ for $N$ near $N_c$, with $L=4$, 8, 16, 32, 64, 128, and 256. (d) Finite-size scaling plot of $R$ after finite-size corrections with $N_c=5.63726$.](image)

### 5.2 Finite-size scaling

Percolation theory [56] predicts that in general, for square systems with free boundary conditions, the spanning function in a percolation system follows
\[ R(N,L) = F(x) + b_0/L, \]  

(5.3)

where the first term \( F(x) \) is the scaling function with \( x = (N - N_c) L^{1/v} \) and the second term is the finite-size correction with \( b_0 \) being a constant. \( F(x) \) has the following polynomial form for small \( x \)

\[ F(x) = a_0 + a_1 x + a_3 x^3 + \ldots, \]  

(5.4)

with \( a_i \) (\( i = 0,1,2,\ldots \)) as constants. The system symmetry and self-duality require that \( a_0 = 1/2 \) and \( a_i = 0 \) for other even \( i \) [56,57].

Figure 5.1(c) plots \( L(R-0.5) \) against \( L \) at different \( N \) near \( N_c \) for stick systems and demonstrates that all the curves converge to the same value when \( L \to 0 \), which validates Eq. (5.3) for stick systems and implies that \( a_0 = 1/2 \). The plots of the scaling function \( F(x) \) for different \( L \) in Fig. 5.1(d) show excellent scaling behaviors for stick systems. Replacing \( x \) with \( \hat{x} = Ax \) in Eq. (5.4), one can obtain a universal finite-size scaling function (UFSSF) form [56] of Eq. (5.4) as

\[ \hat{F}(\hat{x}) = \frac{1}{2} + \hat{x} + K_3 \hat{x}^3 + K_5 \hat{x}^5 + \ldots. \]

The data in Fig. 5.1(d) can give a perfect fit by this UFSSF with \( K_3 = -1.055 \pm 0.002 \), \( K_5 = 0.783 \pm 0.004 \), and \( A = \partial F(0)/\partial x = a_1 = 0.106910 \pm 0.000009 \). It agrees excellently with the UFSSF for regular lattice percolation, where \( K_3 = -1.02 \pm 0.02 \) [58] and \( K_5 = 1 \) [59]. This agreement confirms that stick percolation shares the same UFSSF as lattice percolation.

### 5.3 Critical conductivity exponent

It is well known that for a percolation system, its conductivity \( \sigma \) near the percolation threshold \( p_c \) behaves \([49]\) as \( \sigma \sim (N-N_c)^t \), where \( t \) is the critical conductivity exponent. It has been demonstrated that continuum percolation systems share the same value of \( t \approx 1.30 \) as for lattice percolation systems \([49,52,54]\). However, recent studies \([60]\) propose that in CNNs or stick systems, \( t \) should vary with the ratio of stick-stick junction resistance \( (R_s) \) to stick resistance \( (R_s) \), \( i.e. \), \( R_s/R_s \).
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![Graph](image)

**Figure 5.2.** $R_j/R_s$ dependence of (a) $t/v$ for systems exactly at the percolation threshold and (b) $\tilde{t}$ for stick system of $L=20$ and with $(N-N_c)/N$, between 0.3 and 1, extracted from the three kinds of mean (arithmetic, geometric and harmonic) conductivities.

In order to make clear the dependence of $t$ on $R_j/R_s$, systematic Monte Carlo simulations have been conducted in our work. It is found that exactly at the percolation threshold, $t$ is independent of $R_j/R_s$. By varying $R_j/R_s$ in a wide range from $10^{-5}$ to $10^5$, the critical exponents are all found at $t/v = 0.960\pm0.010$ or $t = 1.280\pm0.014$, as shown in Fig. 5.2(a). However, for systems well above the percolation threshold, the conductivity exponents are no longer the critical $t$, but the apparent conductivity exponents $\tilde{t}$. As shown in Fig. 5.2(b), $\tilde{t}$ is significantly dependent on $R_j/R_s$. This dependency can be well described with an error function of the logarithm of $R_j/R_s$, as $\tilde{t}(x) = \tilde{t}_0 + A \text{erf}(x)$, where $x = \log_{10}(R_j/R_s)$, $\tilde{t}_0$ and $A$ are constants, and erf$(x)$ is the error function.

### 5.4 Heterogeneous percolation theory

Heterogeneous percolation systems, such as the practical CNNs consisting of m-SWCNTs and s-SWCNTs, if conducting, are categorized in four groups according to their percolation characteristics: (i) only m-SWCNT paths exist (OMP); (ii) only s-SWCNT paths exist (OSP); (iii) both m-SWCNT and s-SWCNT paths exist (BOTH); and (iv) neither m-SWCNT nor s-SWCNT path exists but the whole network is percolated by a mixed path comprising m-SWCNTs and s-SWCNTs (MIX). It is readily expected that when the CNN attains OSP, the corresponding TFT can simultaneously achieve large $I_{ON}/I_{OFF}$ and high $I_{ON}$
throughout the studied coverage range.

![Graph showing percolation probability for different percolation characteristics.](image)

**Figure 5.3.** Simulation (discrete symbols) and modeling (continuous curves) results of the percolation probability for different percolation characteristics: overall SWCNT percolation $R(p)$ (overall), s-SWNT percolation $R(2p/3)$, m-SWNT percolation $R(p/3)$, OSP percolation $R_{OSP}(p)$, and MIX percolation $R_{MIX}(p)$. $p = \rho L_S^2$ is the normalized density (coverage).

Figure 5.3 shows the Monte Carlo simulation results as discrete symbols for the overall spanning probability $R(p)$ as well as the probability of m-SWCNT percolation (comprising OMP and BOTH), MIX, and OSP at different $p$ for a CNN with $L_C = 5 \mu m$, $L_S = 3 \mu m$, and m-SWCNT fraction $f_M = 1/3$. It is clear in Fig. 5.3 that there is a density range over which OSP predominates. Such a density range can be called OSP density window. Theoretical deductions (see Paper I for details) reveal that if the half-probability coverage is defined as $\mu$, i.e., $\mu = N_{0.5}(L)$ or $R(\mu)=0.5$, the OSP-dominant region, or the OSP density window is roughly given by

$$n\mu/(n-1) < p < n\mu$$  \hspace{1cm} (5.5)

### 5.5 Physics of doping effects

Systematic studies [Paper V] based on the comprehensive heterogeneous stick percolation, with classic model calculated component conductance, have also unveiled the underlying physics of doping effects in high-density SWCNT TFTs, especially for the applications of sensors. It is found that upon low-level doping, the electrode-SWCNT contacts are the
responsible regions for the conductance change of ON-state SWCNT TFTs, due to their high sensitivity to doping and significant contribution to the overall TFT conductance (owing to their appropriate conductance). SWCNTs themselves are of too high conductance but low doping sensitivity, symmetric intertube junctions (MM and SS) are insensitive to doping, and asymmetric intertube junctions (MS) have extremely low conductance and therefore give rise to negligible influence to the overall TFT conductance. As a result, neither SWCNTs nor intertube junctions can make significant contribution to the overall TFT conductance response. This conclusion is in contrast to previous studies which assumed that upon doping, the responsible region of the SWCNT TFTs is the channel. On the other hand, simulations demonstrate that the presence of symmetric intertube junctions may reduce the sensitivity of the overall TFTs and lead to the channel-length dependent sensitivity, i.e., the sensitivity decreases with increasing channel length upon low-level doping.

In this chapter, some important fundamental results have been introduced for stick percolation, including the high-precision percolation threshold, finite-size scaling function, critical conductivity exponents, heterogeneous percolation theory, and the physics of doping effects in SWCNT TFT-based sensors. These results are generally important and also crucial for developing ink-jet printing techniques for SWCNT TFTs as well as their applications in sensors.
6. Novel Device Structures

The main goal of the Monte Carlo simulations in this thesis is to explore novel device structures for SWCNT TFTs aiming to improve the electrical performance with both high ON-state current and large ON/OFF current ratio. Certainly, these device structures should be compatible with ink-jet printing techniques. Using simulations, so far we have managed to explore one novel device structure of composite CNNs and validate the compatibility with ink-jet printing of the strip-featured SWCNT TFTs, which was proposed and demonstrated previously based on silicon technology [16]. The discussion in this chapter refers to Papers IV and VIII.

6.1 SWCNT TFTs with composite CNNs

It has been well demonstrated both theoretically [38] and experimentally [36] that aligned SWCNTs can significantly enhance the drive current (ON-state current $I_{ON}$) in short-channel devices ($L_C < L_S$). With aligned SWCNTs, the length of percolation paths bridging the source and the drain is reduced, resulting in an increased $I_D$. However, for long-channel SWCNT TFTs with $L_C > L_S$, the alignment causes reduction of the probability for each nanotube to form junctions with its neighbors [37] and hence reduces the number of available percolation paths. As a result, a decreased $I_{ON}$ is found. Apparently, a perfect alignment is not optimal since the CNN would carry less current than partially aligned or even randomly oriented CNNs [37,38]. Our simulation work has reproduced this tendency [Fig. 6.1(a)]. However, it is also indicated that a partially aligned CNN may not be an optimal solution for SWCNT TFTs either. As shown in Fig. 6.1(b), when a partially aligned CNN reaches the peak ON-state current at a certain alignment (marked with the dashed lines in the figure), the ON/OFF current ratio decreases severely. In Fig. 6.1, the CNN alignment is measured by an angle $\theta_a$.

Our simulations demonstrate that utilizing composite CNNs presents an effective means to improve the electrical performance of CNN TFTs. Such composite CNNs comprise two sets of SWCNTs. A primary set consists of dense arrays of almost perfectly-aligned long
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SWCNTs along the transistor channel direction [Fig. 6.2(a)]. A secondary set is composed of short SWCNTs with a density far below the percolation threshold. These short SWCNTs can be randomly distributed [AR-CNN, Fig. 6.2(b)] or perpendicularly aligned to the primary set [AA-CNN, Fig. 6.2(c)]. At least, three advantages can be found with the concept of composite CNNs in terms of performance improvement. First, the use of aligned long SWCNTs reduces the length of the percolation paths. Second, the addition of short SWCNTs increases the percolation probability and hence the number of available percolation paths. Last, the combination of long and short SWCNTs effectively reduces the probability of metallic percolation paths, as justified by the OSP probability in Fig. 6.1(c). As a result, the composite CNN TFTs can simultaneously achieve the desired high $I_{ON}$ and large $I_{ON}/I_{OFF}$ (see Fig. 6.1).

**Figure 6.1.** Simulation results showing how (a) $I_{ON}$, (b) $I_{ON}/I_{OFF}$ and (c) OSP probability $R_{OSP}$ vary with the degree of alignment $\theta_a$ for three different cases. $L_C = 5 \mu m$. Squares: Primary, with single CNNs comprising SWCNTs of $L_S = 3 \mu m$ and $\rho = 10 \mu m^{-2}$. Circles: AR-CNN, the primary CNN plus a secondary CNN with randomly oriented short SWCNTs of $L = 0.1 \mu m$ and $\rho = 60 \mu m^{-2}$. Triangles: AA-CNN, the primary CNN plus a secondary CNN with vertically aligned short SWCNTs of $L = 0.1 \mu m$ and $\rho = 60 \mu m^{-2}$; identical $\theta_a$ for both primary and secondary CNNs.

The superiority of the concept of composite CNNs for SWCNT TFTs has been confirmed experimentally by other researchers [61]. The structure of such composite CNNs is likely to be suitable for ink-jet printing as well. Short SWCNTs are currently available, and a
number of methods to trim SWCNTs to a range of short lengths can be found in the literature, such as fluorination [62], oxidation by acids [63], sonication and homogenization [64]. The challenge is how to fabricate aligned SWCNTs through ink-jet printing. A possible solution might rely on the method [65] of large area-aligned arrays from direct deposition of SWCNT inks. This method thermally treats the deposited polymer-composited SWCNT inks and obtains unique arrays of well-aligned SWCNTs self-assemble across large fissures of the depositions. If the conductance of the deposition is dominated by the fissures, it is possible to realize our composite CNN structure by first printing long-SWCNT/polymer inks followed by thermal treatments, and then printing short SWCNT inks. In practice, however, a process for fissure-leading alignment of SWCNTs is currently absent at our lab and verification of this idea for ink-jet printing SWCNT TFTs with composite CNN structures has to be put aside due to time constraints.

![Figure 6.2](image.png)

**Figure 6.2.** Percolation paths in CNNs of 5 µm×1 µm dimension for (a) Primary, with single CNNs comprising SWCNTs of \( L = 3 \ \mu m, \ \rho = 10 \ \mu m^{-2}, \ \text{and} \ \theta_a = 0.5^\circ \); (b) AR-CNN, with a secondary CNN of randomly oriented short SWCNTs of \( L = 0.1 \ \mu m \) and \( \rho = 60 \ \mu m^{-2} \); and (c) AA-CNN, with a secondary CNN of vertically aligned short SWCNTs of \( L = 0.1 \ \mu m \), \( \rho = 60 \ \mu m^{-2} \), and \( \theta_a = 90^\circ \). Open circles mark the intertube junctions in the percolation paths.

### 6.2 SWCNT TFTs with long-strip channels

It has been proposed previously [16] that, through the combination of soft lithography and reactive-ion etching, cutting fine lines in large-area high-density CNNs to produce parallel
SWCNT strips is an effective way to eliminate pure m-SWCNT transport pathways, without significant reduction of the effective carrier mobility. Compared with the original SWCNT TFTs, the resulting “strip-featured” SWCNT TFTs can have considerable increase in ON/OFF current ratio by up to four orders of magnitude only at the expense of ON-current degradation by less than a factor of 2.

Furthermore, a follow-up systematic work [23] outlines a set of design rules to guarantee high performance; the strip width $W_{\text{strip}}$ should be smaller than the SWCNT (stick) length $L_S$, i.e., $W_{\text{strip}}/L_S < 1$. However, this requirement is demanding for ink-jet printing techniques available nowadays. As mentioned earlier, usually a commercial ink-jet printer can reliably produce lines no narrower than ~50 µm, whereas the SWCNT length is typically around a few µm. Therefore, ink-jet printed strips should often have $W_{\text{strip}}/L_S > 10$, which seriously violates the proposed design rules.

In this chapter, more stick percolation systems are studied and the applicability of strip-featured SWCNT TFTs in ink-jet printing techniques is evaluated on the basis of the heterogeneous percolation theory and Monte Carlo simulations for large-size stick systems to account for strips of $W_{\text{strip}}/L_S > 10$.

The essential physics of the strips is still to achieve OSP-dominated SWCNT TFTs. As discussed earlier in Chapter 5, the OSP density window width $W_{\text{OSP}}$ is determined by the half-possibility density $\mu$. According to Eq. (5.5), $W_{\text{OSP}} = 1.5\mu$ if the m-SWCNT fraction remains $f_M = 1/3$ for TFTs based on pristine SWCNTs. To understand the superiority of the strips for SWCNT TFTs from the viewpoint of percolation theory, the percolation behaviors, especially the half-possibility density $\mu$, must be well studied first for systems with strip (rectangle) structures.

A rectangular system is characterized by its length-to-width ratio, $r$, see Fig. 6.3(a). Figures 6.3(b) and 6.3(c) show the spanning probability as a function of density for rectangular stick systems with different $r$ and $W_{\text{strip}}$. It is clear that for any fixed $W_{\text{strip}}$, with the increase of $r$, the spanning probability curves, surely including the half-possibility density $\mu$, shift in the high-density direction. This means that a large $r$ corresponds to a large $\mu$ or a large $W_{\text{OSP}}$. As a result, long and narrow strips (rectangles with large $r$) are superior to square systems.
of similar (channel) length with respect to the electrical performance of SWCNT TFTs. It should be pointed out that even with large $W_{\text{strip}}$ [Fig. 6.3(c)], the superiority of large-$r$ systems still holds though the increase of $\mu$ is not so significant as that in systems of small $W_{\text{strip}}$ [Fig. 6.3(d)]. This implies that by choosing suitable SWCNT density, strips with large $r$ are also, in principle, compatible with the ink-jet printing techniques to fabricate relatively high-performance SWCNT TFTs with large $W_{\text{strip}}/L_S$, though the performance is not expected to be as excellent as those with very small $W_{\text{strip}}/L_S$.

![Figure 6.3](image)

**Figure 6.3.** (a) Schematic SWCNT (stick) strips for Monte Carlo simulation, red and green sticks represent m-SWCNTs and s-SWCNTs, respectively. (b) and (c) Spanning probability $R$ as a function of stick density $p$ for strip width, $W_{\text{strip}}/L_S = 10$ (b) and $W_{\text{strip}}/L_S = 40$ (c), with different length-to-width ratio $r$. From left to right, the curves are for $r = 1, 2, 4, 8, \text{ and } 16$. Each of the curves is obtained from $10^6$ realizations in the Monte Carlo simulations. The intersection between a curve and the horizontal dashed line ($R=0.5$) indicates the half-probability density $\mu$. (d) Dependence of the half-probability density $\mu$ on the length-to-width ratio $r$ for $W_{\text{strip}}/L_S = 10$ and $W_{\text{strip}}/L_S = 40$.

In summary, in order to improve the electrical performance of SWCNT TFTs, this chapter explores, by using Monte Carlo simulation, a novel device structure of composite CNNs.
Such a composite CNN comprises a primary set of perfectly-aligned long-SWCNTs arrays and a secondary set of short-SWCNT networks. It further demonstrates that the strip structures proposed previously by other studies are also compatible with ink-jet printing techniques. The following chapter will discuss our experiments of ink-jet printed SWCNT TFTs with long-strip channels.
7. Ink-jet Printing of SWCNT TFTs With Long-Strip Channels

The studies in Chapter 6 based on Monte Carlo simulations and heterogeneous stick percolation predict that CNNs consisting of wide strips (with respect to SWCNT length, \( W_{\text{strip}}/L_S \gg 1 \)) with large length-to-width ratio \( r \) are still of potential to retain fairly high electrical performance and suitable for ink-jet printed SWCNT TFTs, though the performance is expected to be inferior to those devices comprising narrow strips (\( W_{\text{strip}}/L_S < 1 \)). This chapter presents the practical ink-jet printing techniques for strip-featured SWCNT TFTs and their electrical properties. The discussion in this chapter refers to Paper VIII.

7.1 Ink-jet printing techniques

In practice, the ink-jet printing procedures for SWCNT TFTs include substrate selection and architecture design, SWCNT ink formulation, and device fabrication by means of ink-jet printing. The ink-jet printer used in this thesis is Fujifilm Dimatix DMP-2800.

7.1.1 Substrate selection and device architecture design

In our studies, two types of substrates are considered for the ink-jet printed SWCNT TFTs. One is, as previously, heavily-doped silicon wafer capped with a thin layer (~ 150 nm thick) of SiO\(_2\), and the other is a kind of flexible plastic foil, Kapton.

It is very convenient to print SWCNT TFTs on top of SiO\(_2\)/Si substrates by taking the back-gate device architecture [Fig. 2.1(c)] with heavily-doped silicon as the gate electrode and SiO\(_2\) as the gate insulator. Due to the excellent capacitance performance of SiO\(_2\)/Si substrates, the electrical properties of the printed SWCNT TFTs can be reliably studied. However, in order to meet the interest in the emerging flexible electronics, SWCNT TFTs are also printed on flexible substrates (Kapton, Fig. 7.1) with the top-gate device architecture [Fig. 2.1(b)].

Besides SWCNTs, all the electrodes, including source/drain and gate, are also printed by
the ink-jet printing. The electrodes are printed using commercial silver inks while the SWCNT inks are formulated in-house.

7.1.2 SWCNT ink formulation

There are sophisticated skills in the literature for preparation of SWCNT solutions or suspensions especially in the aqueous solvents. However, in order to achieve optimal performance of the printer and produce reliable printed patterns, the inks should possess proper fluidic characteristics, including viscosity and surface tension [66,67]. It is found in our studies that in combination with an appropriate kind of polymer, polyvinyl-pyrrolidone (PVP), water-based SWCNT solutions have proper fluidic characteristics and hence are compatible for ink-jet printing. Although the preparation of similar SWCNT solutions has already been introduced previously [65], their compatibility with ink-jet printing was not studied. It is now demonstrated in this study. The ink formulation is very simple and only includes dispersion of SWCNTs into water in the presence of surfactant SDBS (~ 0.1% by weight), with the assistance of bath ultrasonication for half an hour. This was followed by addition of PVP and then a second sonication for a few minutes. Usually, such kind of SWCNT inks can be stable for several months. However, the performance of the printing and the electrical property of the printed devices are strongly influenced by the concentration of PVP in the inks. There should be sufficient PVP in the inks since PVP is an excellent additive for the SWCNT ink. It can increase the ink viscosity, debundle SWCNTs,
stabilize the inks for a long time, and improve the printed device patterns. On the other hand, there should not be too much PVP in the inks. The ink with too much PVP may have too high viscosity and cannot drip out of the nozzles. In addition, PVP itself is insulating and too much PVP can severely degrade the conductance of the printed SWCNT TFTs. Our studies suggest that the optimal SWCNT ink for high printability and good electrical performance includes 2 mg/ml PVP and 0.2 mg/ml SWCNTs. For this ink, the printed SWCNT strips are uniform (20-40 nm thick) and most nanotubes are fairly individual SWCNTs or small bundles with the length around 1 µm, and distribute randomly and uniformly in PVP.

### 7.1.3 Device printing

For SWCNT TFTs fabricated on silicon wafers, the printing procedure is fairly simple. First the SWCNT strips are printed using the SWCNT/PVP ink. Then the source/drain electrodes are printed using the commercial silver inks followed by baking in an oven at 150 °C for around 30 min. Note that the source/drain electrodes are printed at the two ends of each SWCNT/PVP strip in order to realize the top-contact configuration in Fig. 2.1(c), instead of the bottom-contact in Fig. 2.1(a). Finally, a layer of 10-nm-thick Al₂O₃ thin film as the passivation layer is deposited by means of Atomic Layer Deposition (ALD) at 150 °C.

![Figure 7.2](image)

*Figure 7.2. Optical images of ink-jet printed strip-featured SWCNTs on (a) SiO₂/Si and (b) Kapton. All the electrodes, Source (S), Drain (D) and Gate (G) are printed using a commercial silver ink. In (b), beneath the gate electrode, there is a 50-nm-thick layer of Al₂O₃ thin film as the gate insulator.*

For SWCNT TFTs on Kapton, the fabrication procedure is also rather straightforward. First
the SWCNT strips are printed on Kapton, followed by printing of silver source/drain electrodes at the two ends of each strip. Then a layer of 50-nm-thick Al$_2$O$_3$ thin film as the gate dielectrics is deposited by ALD at 150 °C. At the end, the silver gate electrode is printed on top of the Al$_2$O$_3$ gate dielectric and located above the channel (SWCNT/PVP) region. Figure 7.2 shows optical images of the final printed devices on silicon and Kapton. In both cases, each device can comprise one single strip or multiple (5 or 10) strips.

### 7.2 Electrical properties

#### 7.2.1 SWCNT TFTs on silicon

On silicon wafer, over 1000 TFTs have been printed with either single strip or multiple strips. Each strip has a width around 100 µm and a length varying from 200 µm to 1000 µm. For these devices, the ON current decreases with the increasing channel length $L_C$ whereas the ON/OFF current ratio increases with the increasing $L_C$. In addition, they follow the scaling rules [Eqs. (2.6) and (2.7)] as $I_{ON} \sim L_C^{1.55}$ and $I_{ON}/I_{OFF} \sim L_C^{1.14}$. SWCNT TFTs with $L_C \sim 1000$ µm have the best electrical performance; about 50% of which have $I_{ON} > 250$ nA at $V_D = 5$ V and $V_G = 40$ V, and meanwhile $I_{ON}/I_{OFF} > 150$. Typically, the effective mobility of these devices is $\mu_{eff} \approx 0.6 \text{ cm}^2/\text{V s}$. As a result, it is clear that wide strips ($W_{strip}/L_S \sim 100$) may still offer SWCNT TFTs with good performance provided that the length-to-width ratio $r$ is sufficiently large. This experimental observation has thus verified the previous simulation results.

Furthermore, for SWCNT TFTs with multiple strips, the performance can be further improved. Now, $I_{ON}$ can exceed $10^{-6}$ A at $V_D = 5$ V, ~10 times higher than that of the single-strip TFTs, while their $I_{ON}/I_{OFF}$ is still around 100. Therefore, multiple-strip SWCNT TFTs yield better device performance than single-strip ones.

Note that the passivation layer is crucial for our ink-jet printed SWCNT TFTs. Figures 7.3(a) and 7.3(b) exhibit, respectively, the transfer characteristics of a printed one-strip (1000 µm long) SWCNT TFT before and after deposition of an Al$_2$O$_3$ passivation layer. Without passivation, the ON/OFF ratio can exceed 700 with the ON current approaching $7 \times 10^{-8}$ A at $V_D = 5$ V. The transfer characteristics display obvious ambipolar behavior with the
transition voltage at $V_G = -20 \text{ V}$. However, at the OFF state, the absolute value of the drain current does not agree well with the source current, which could be caused by surface leakage since the gate leakage current is much smaller than the source/drain currents. With the passivation, the source and drain currents coincide with each other. Furthermore, the ON current of the $n$-type branch increases by about three times. On the contrary, the ON/OFF current ratio decreases by about three times. In addition, the transition gate voltage between the $p$-type and $n$-type branches shifts to a more negative value and the device looks more like an $n$-type transistor. Therefore, it can be concluded that the deposition of the $\text{Al}_2\text{O}_3$ layer has significant influences on the device property. The cause for this influence needs to be explored. Usually TFTs comprising pure SWCNTs exhibit $p$-type transistor behavior; see Figs. 3.4 and 3.6. The ambipolar behavior of the present devices might result from the addition of PVP, which covers the SWCNTs without making them exposed to the air.

![Figure 7.3](image-url)

**Figure 7.3.** Transfer characteristics of an ink-jet printed SWCNT TFT with one single strip (a) before and (b) after deposition of $\text{Al}_2\text{O}_3$ passivation layer. The strip is 100 µm wide and 1000 µm long.

### 7.2.2 SWCNT TFTs on Kapton

The transfer and output characteristics are also studied for SWCNT TFTs fabricated on Kapton. The electrical performance of one of the best devices is shown in Fig. 7.4. $I_{\text{ON}}$ is around 25 nA at $V_D = 5 \text{ V}$ with $I_{\text{ON}}/I_{\text{OFF}}$ about 25. The effective mobility is $\mu_{\text{eff}} \approx 0.07 \text{ cm}^2/\text{V s}$. However, the applied gate bias has to be limited within the range between -5 V and 5 V
since when $V_G$ was over 10 V, a large gate current was observed likely caused by breakdown of the Al$_2$O$_3$ thin film. Compared with those results of the devices on silicon wafer, SWCNT TFTs on Kapton have a somewhat degraded electrical performance. The reason might be that Al$_2$O$_3$ on Kapton is inferior in capacitance performance as compared to SiO$_2$ on silicon substrates.

**Figure 7.4.** (a) Transfer and (b) output characteristics for a top-gate single-strip SWCNT TFT fabricated on Kapton. The strip is about 1000 µm long and 100 µm wide. In (b), $V_G$ decreases from 5 V to 0 V in steps of 1 V from the top curve to the bottom one.

In summary, this chapter develops the ink-jet printing technique for SWCNTs and presents the inkjet printed SWCNT TFTs featuring long-strip channels. This effort is guided by our Monte Carlo simulations presented earlier in the preceding chapters. As a result, high-yield SWCNT TFTs can be printed on silicon wafer with ON current $> 250$ nA at $V_D = 5$ V and ON/OFF ratio $> 150$. SWCNT TFTs with multiple strips can achieve ON current $> 1$ µA and ON/OFF ratio $\sim 100$. With the assistance of ALD-deposited Al$_2$O$_3$ as the gate dielectric, SWCNT TFTs can be printed on Kapton. The best performance so far is ON current $\sim 25$ nA at $V_D = 5$ V and ON/OFF ratio $\sim 25$. The effective mobility is $\sim 0.6$ cm$^2$/V s for the TFTs on silicon and $\sim 0.07$ cm$^2$/V s on Kapton. These results are encouraging with better performance than ink-jet printed SWCNT TFTs reported in the literature [18,22]. Compared with those devices under similar circumstances, the present SWCNT TFTs have an increase by about 10 times in effective mobility and meantime an increase by at least 25 times in ON/OFF current ratio. They further justify our proposal, based on Monte Carlo simulations, of ink-jet printed SWCNT TFTs with channels shaped in long strips.
8. Summary and Future Outlook

This thesis presents my endeavor in developing ink-jet printing techniques for relatively high-performance TFTs based on pristine SWCNTs. The main challenge of this work is to suppress the undesired effects of “metallic SWCNT contamination”.

At first sight, low-density CNNs could be a good solution. Prior to the real ink-jet printing, SWCNT TFTs have been fabricated through drop casting in combination with silicon technology. It is found that high-yield TFTs with high ON/OFF current ratio can be achieved by using low-density SWCNT networks. In addition, its diode connection mode presents an attractive solution for CNN-based rectifiers with excellent performance of forward/reverse current ratio over $10^5$. However, low-density SWCNT TFTs suffer from low mobility, poor reproducibility, and unclear scaling behaviors. These drawbacks put severe challenges to the applications of low-density SWCNT TFTs in electronic circuits. As a result, low-density SWCNT TFTs are unlikely to be a good solution to ink-jet printed electronic devices. Nevertheless, it has also been demonstrated that the electrical performance of such SWCNT TFTs is insensitive to the electrode materials probably also due to the effects of “metallic SWCNT contamination”. This observation is not only interesting but more importantly also of advantages for ink-jet printing of SWCNT TFTs since it allows plenty of metal inks, e.g., the mature silver ink, to be considered for fabrication of SWCNT TFTs.

A more effective and feasible way to improve the electrical performance of SWCNT TFTs is to employ high-density CNNs with novel device structures. In order to explore such device structures, Monte Carlo models on the basis of generalized stick percolation have been established. The conductance of the stick percolation systems representing CNNs is calculated by employing Kirchoff’s current law. The conductance of the SWCNTs, SWCNT-SWCNT junctions and SWCNT-electrode contacts are obtained from either model calculations or experiential data. In particular, since a normal ink-jet printer can only produce large-dimension devices due to its low spatial resolution, high-efficiency algorithms based on subcells and tree-based algorithms have been proposed to investigate
Ink-jet printing of thin film transistors based on carbon nanotubes.

percolation behaviors for large-size stick systems. Furthermore, preconditioned conjugate gradient method has been employed to calculate the conductance for these systems.

By conducting Monte Carlo simulations, important conclusions have been reached for fundamental issues in stick percolation. First, the percolation threshold for 2D square stick systems has been estimated with high precision as \( N_c \approx 5.63726 \pm 0.00002 \). Second, it has been demonstrated that stick systems, as a representative of continuum percolation systems, shares the same universal finite-size scaling function as lattice percolation systems. Third, it has been made clear that the critical conductivity exponent for stick systems exactly at the percolation threshold is independent of the stick-to-junction resistance ratio, whereas the apparent conductivity exponents for stick systems well above the percolation threshold significantly vary with this ratio. These results are essential to stick percolation theory and hence to its application in electronics concerning SWCNT TFTs. The extensive simulation work has also led to fundamental knowledge for heterogeneous stick systems or CNNs in that the SWCNT density window, within which only semiconducting SWCNT percolation dominates, depends on the half-probability density (the density where the spanning probability is 0.5) and the fraction of m-SWCNTs. Finally, simulations demonstrate that the responsible region for the doping effects on SWCNT TFTs is the electrode/SWCNT contacts, in contrast to the previous assumption of the channel. This confirmation can be of important implications in applications of SWCNT TFTs as gas or bio-chemical sensors.

The Monte Carlo simulations have led to prediction of a novel device structure for high-performance SWCNT TFTs, i.e., composite CNNs. This concept has subsequently been confirmed experimentally by other researchers. This structure comprises a primary set of perfectly-aligned long-SWCNTs arrays and a secondary set of short-SWCNT networks. The aligned long SWCNTs reduce the length of the percolation paths and the short SWCNTs increase the percolation probability and hence the number of available percolation paths. Moreover, the combination of long and short SWCNTs effectively reduces the probability of metallic percolation paths. Therefore, most TFTs with such composite CNNs are expected to achieve high ON current and large ON/OFF current ratio simultaneously. In addition, Monte Carlo simulations have also demonstrated the compatibility of previously-proposed “strip-featured” SWCNT TFTs with ink-jet printing. With the increase of the length-to-width ratio of SWCNT strips (rectangular CNNs), the
half-probability density shifts to higher value (thus allowing for higher $I_{\text{ON}}$) and hence results in wider density window at which only semiconducting SWCNT percolation dominates (thus permitting higher throughput). This conclusion implies that long and narrow strips are good device structures for performance improvement of SWCNT TFTs.

In practical ink-jet printing, the composite CNN approach awaits experimental realization due to the challenge in fabrication of aligned SWCNT. Instead, we have fabricated strip-featured SWCNT TFTs by means of ink-jet printing on both silicon wafer and flexible Kapton substrates. The SWCNT ink is formulated with the assistance of an insulating polymer PVP. The electrodes are all also ink-jet printed using commercial silver ink. As a result, high-yield SWCNT TFTs can be printed on silicon wafer with an ON/OFF ratio $> 150$ and ON current $> 250$ nA at $V_D = 5$ V. With ALD-deposited $\text{Al}_2\text{O}_3$ as the gate insulator, SWCNT TFTs have also been printed on Kapton with the best performance so far of ON current $\sim 25$ nA at $V_D = 5$ V and ON/OFF ratio $\sim 25$. These results are much better than previously reported ink-jet printed SWCNT TFTs in the literature. Compared with those literature devices under similar circumstances, our SWCNT TFTs have an increase by about 10 times in effective mobility and meantime an increase by at least 25 times in ON/OFF current ratio.

However, the printed TFTs are still far from satisfactory and there is need for further development of the ink-jet printing techniques in order to improve the performance of SWCNT TFTs. Some potential efforts are suggested as follows.

(1) It is valuable to evaluate the electrical performance of SWCNT TFTs with composite CNNs fabricated by ink-jet printing. For this purpose, more sophisticated ink-jet printing techniques need to be developed in order to produce aligned SWCNT arrays.

(2) The Monte Carlo simulations suggest that narrower strips can yield better performance than wide ones. Therefore, advanced ink-jet printer with high resolution (~ a few µm) [68,69] need to be developed and employed aiming to improve the performance of strip-featured SWCNT TFTs.

(3) More advanced SWCNT inks need to be formulated without involvement of insulating polymers in order to increase the device conductance.

(4) For SWCNT TFTs on flexible substrates, superior gate dielectrics, such as ion gels [70], are needed to achieve high performance.
References


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References


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(2010).
