LOW-COST THROUGH SILICON VIAS (TSVs) WITH WIRE-BONDED METAL CORES AND LOW CAPACITIVE SUBSTRATE-COUPPLING

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ABSTRACT

The three-dimensional (3D) integration of electronics and/or MEMS-based transducers is an emerging technology that vertically interconnects stacked dies using through silicon vias (TSVs). They enable the realization of devices with shorter signal lengths, smaller packages and lower parasitic capacitances, which can result in higher performance and lower costs. This paper presents a novel low-cost fabrication technique for metal-filled TSVs using bonded gold-wires as conductive path. In this concept the wires are surrounded by polymer, which acts both as an electrical insulator causing low capacitive coupling towards the substrate and as a buffer for thermo-mechanical stress.

INTRODUCTION

During the past decades the hybrid integration of IC and MEMS technology has been dominated by (2D) side-by-side approaches for Multi Chip Modules (MCM) and System on Chips (SoC). CMOS and MEMS processing are both well-established and cost-effective base technologies where each technology itself is typically characterized by short development times, low fabrication costs and high yields. The separate manufacturing of CMOS and MEMS and the integration of both devices as a final step in packaging offers highest versatility and low process costs and thus is an attractive alternative to System on Chips, where these two technologies are laboriously merged onto a common die. 3D-integrated System in Packages (SiP) are therefore a general trend in many integration concepts. This vertical integration by chip stacking does not only decrease the costs by reducing the package size, its volume and weight but also improves the systems performance in terms of enhanced transmission speed, lower power consumption and lower parasitic capacitances due to shorter signal lengths, which is of importance for various demanding applications [1]. 3D-SiP concepts require vertical interconnects through certain chips of the stack in order to connect their functional layers. Large development efforts for the realization of reliable and cost-effective TSVs are currently ongoing and first commercial products already successfully incorporate this technology.

Via etching, insulation layer deposition and the metallization step to form the conducting path of

the TSV are the most costly parts of the TSV fabrication, which has currently a cost-target of about 200 USD per 200 mm wafer [2]. Especially electroplating of copper, which is a very well established semiconductor manufacturing process, is widely used by most research groups [3, 4, 5, 6, 7]. The process benefits from its good availability and processability of high aspect ratio features at close to room temperature conditions but is not yet economically attractive due to its complexity [8]. Especially the void-free formation of high-aspect ratio features is a big challenge [5].

Wire bonding is an extremely mature and cost-effective backend process for electrical interconnects due to the broad availability and its very high performance in terms of reliability and throughput. The estimated cost per 100,000 wire bonds has been reported to be on the order of 10 USD [9] in high-volumes and thus can be considered as a serious alternative to plating processes in TSV fabrication scenarios with that number of vias per wafer. In this paper we present an entirely novel and cost effective process for the fabrication of TSVs with wire bonded metal cores.

DESIGN

The main feature of the presented TSV design is the through-wafer wire bonded metal core. The wire bonding technique easily enables the fabrication of high-quality and void-free metal cores with extremely high aspect ratios.

Figure 1: CAD image with cross sectional view of the basic wire bonded TSV design. The metal core in the center of the via is a ball-bonded wire on a metal membrane and is surrounded by a polymer.

As depicted in Fig. 1, the wire is ball-bonded on a metal membrane on the bottom of the via cavity. In order to be able to wire-bond at the bottom of the via cavity and to achieve a low capacitive coupling of the metal core towards the substrate, a relatively large diameter of the cavity (200 μm) was chosen. The remaining hollow space of the cavity is subsequently filled with a dielectric, which acts both as an insulator and mechanical support for the via core.

The resistivity of the metal core should be sufficiently low but on the other hand ensure a small metal core diameter for small TSV pitches. Typical diameters of commercially available gold, aluminum or copper bond wires are 12.5 to 50 μm .

The electrical characteristics of the presented concept was evaluated by basic calculations of the resistance of the TSV and the coupling capacitance of the via core to the substrate. As depicted in Fig. 2, the resistance for a 300 μm long gold wire decreases from 56 to 3.5 $\text{m}\Omega$ for the commercial available range of wire diameters.

Figure 2: Computed graph of the dependency of the the diameter d on the resistance R of a wire bonded gold core for a via length l of 300 μm .

The capacitive coupling of a TSV with a height of 300 μm and a metal core diameter of 25 μm decreases significantly for polymer-diameters (Benzocyclobutene, BCB) larger than 75 μm , as depicted in Fig. 3. This calculation is based on an ideal co-axial cable model and neglects the influence of the ball-bond and the top- and bottom-metallization layers on the coupling capacitance. Material properties such as the dopant concentration of the silicon substrate (i.e. conductivity) will also have a significant influence, which is not captured by this abstraction of a single permittivity value.

Figure 3: Computed graph of the dependency of the the diameter D of the dielectric filling on the coupling capacitance C of a TSV with a height h of 300 μm and a metal core diameter d of 25 μm .

FABRICATION

The fabrication process for the TSVs is depicted in Fig. 4 and is based on 300 μm thick double-side polished 100 mm-substrates with a 2.5 μm thick silicon oxide layer on both sides, which was created by thermal wet oxidization. The oxide acts both as a hard mask for the DRIE step and as an electrical insulator for the metal lines, which will finally connect the via on the front- and backside of the substrate. The oxide of the backside is thinned down to 400 nm by a wet blank BHF etch with frontside protection by a photoresist. A standard lithography and RIE process on the front-side of the substrate removes the oxide and defines the circular openings for the vias in the hardmask. An aluminum layer is sputtered on the unpatterned backside of the wafer (Fig. 4 b). As a precaution a layer thickness of 5 μm was chosen to withstand the stress during the wire bonding process, which will be performed on a membrane of this layer. A Bosch DRIE process creates the via holes with straight side walls; the etch stops on the silicon oxide on the bottom of the cavity. A second blank BHF etch removes the thin layer of oxide on the the aluminum membrane but not the thicker oxide layer on the frontside of the substrate (Fig. 4 c).

As depicted in Fig. 4 d, a bond capillary with a small tip-diameter for ultra-fine pitch applications is used in order to be able to place the wire bond on the bottom of the cavity. The bond head moves down after the free-air-ball (FAB) formation by an electrical discharge. The ball-bond is performed at room-temperature with the help of force and ultrasonics. The bond head moves subsequently straight upwards, generating a tail length of about 400 μm (Fig. 4 e). A second electrical flame off (EFO) cuts the wire on a spot above the upper substrate surface (Fig. 4 f). The bonding process was performed with

Figure 4: The fabrication scheme can be divided into three major tasks. First is the formation of the via hole by DRIE etching, second is the wire bonding of the conductive TSV core and last is the filling with the dielectric.

a semiautomatic wire bonder (Delvotec 5410) with a minor hardware modification in order to trigger the second electrical flame off.

The filling of the cavities with the thermosetting polymer BCB (Fig. 4 g) and subsequent soft- and hard-curing is performed in vacuum environment in order to prevent any void formation. A grinding and polishing step of the frontside removes the remaining gold of the bond wire and the BCB from the surface of the substrate (Fig. 4 h). A final aluminum deposition on the frontside contacts the gold core of the via. The structuring of both aluminum layers forms the signal lines leading to the TSV (Fig. 4 i).

EXPERIMENTAL RESULTS

The wire bonding and the filling process are the most crucial steps in the presented fabrication scheme and have therefore been extensively investigated. A process for wire bonding on a metal membrane has been developed with a set of bond parameters optimized for room temperature conditions, low bond force and moderate ultrasonic power. The formation of truncated bond wires with the help of a second flame-off showed the best results in terms of straightness of the wire and overall process reliability. Experiments using other wire cutting methods such as tearing the wire or cutting the wire with a micro-scissor were not successful. The manual alignment of the bonding position in our experiments resulted in a wire position, which is slightly displaced from the via center (Fig. 5, 6). Fully automated state-of-the-art wire bonders offer a typical bond placement accuracy of 2.5 μm with the help

of pattern recognition systems.

Figure 5: Tilted SEM image of a 200 μm wide via cavity and a bonded Au-wire with a diameter of 25 μm prior to the filling with BCB (Fig. 4 f).

The void-free dielectric filling with BCB and its characteristics have been investigated with the help of focused ion beam (FIB) milling and the subsequent inspection with a scanning electron microscope (SEM) (Fig. 6). There were no damages such as cracks or holes in the Aluminum membrane visible, which could have been caused by the wire bonding process. The filling with BCB could be successfully conducted without any visible air-voids or defects after the complete hard curing procedure. However, a for the polymer typical shrinkage during cross-linking led to a delamination at parts of the Au/BCB interface with a gap width of less than 1 μm (Fig. 6 c). There are however no in-

Figure 6: Tilted SEM images with a cross-section of a ball-bonded TSV after the complete fabrication. The cross-sectional opening was realized by focused ion beam (FIB) milling. a) shows the backside of the substrate prior to the FIB milling. The Al-membrane is slightly deformed by the wire bond, which was performed from the other side. b) cross section of the ball bond and the wire. c) close-up of the ball bond facing the Al-membrane. The shrinkage of the BCB filling leads to delamination from at the Au/BCB interface.

dications that the delamination causes mechanical or electrical failures of the via. However, the general reliability of this TSV concept remains to be experimentally verified.

The electrical characterization of six TSVs was performed with a 4-point probe station and a digital multimeter. The measurements showed an average resistance value of 86 m Ω . This is higher than the theoretical value of 14 m Ω , which most likely is due to interface resistances to the metallization layers on the front- and backside.

DISCUSSION AND CONCLUSIONS

We have demonstrated a proof of concept for the fabrication of TSVs with an overall aspect ratio of 1.5 and an aspect ratio of 12 of the metal core. Smaller TSV diameters and higher aspect ratios are feasible but ultimately limited by the wire bonding process. The use of bond capillaries with smaller tip-diameters and/or thinner substrates would enable via diameters down to 100 μm and therefore allows the use of this concept for scenarios with a TSV-pitch in that scale. Superior electrical characteristics in terms of low resistivity and low capacitive substrate coupling of the presented concept enable the cost-effective utilization of TSVs for sensitive applications, such as the heterogeneous integration of capacitive MEMS sensors and IC technology. This method is compatible with typical via hole formation processes, such as DRIE and laser-ablation. The presented concept exclusively utilizes well-established standard processes and is therefore suitable for mass-production. The presented metal filling technology by wire bonding should be cost competitive for high volumes for applications with up to 100,000 vias per wafer.

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