Design and Implementation of Common Drain Class-B RF Power Amplifier in 90 nm CMOS Technology

Master of Science Thesis in System-on-Chip Design

by

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Abstract

Power Amplifier (PA), is a key component in a wireless communication system. It is challenging to design a PA having sufficient gain, linearity and efficiency all at the same time. Linearity is important to avoid interference among the channels while high efficiency corresponds to longer battery life. Gain is important to reduce multiple stages. All the RF power amplifiers are made in common source configuration which offers high power gain but significant nonlinearity. To improve linearity, the amplifier is operated in backoff or advanced techniques like digital predistortion are used. On the other hand, common drain amplifier has inherent potential to provide both linearity and efficiency. Operating the common drain in class B mode can provide high efficiency as well as additional linearity due to suppression of nonlinear gate-source capacitance.

The scope of this thesis is to design a stable single-ended as well as differential common drain class-B RF power amplifier, while maintaining adequate transducer gain so that the power added efficiency (PAE) is not compromised by low gain and thus resulting in better overall performance. The technology to be employed for the implementation of the amplifier is the 90 nm CMOS process and the operating frequency is 2.55 GHz, the 3GPP Long Term Evolution (LTE) standard. For additional performance evaluation, the results are to be compared with that of a single-ended common source amplifier.
Dedication

To my beloved parents and other members of my family for their infinite support and constant prayers.

“A man travels the world over in search of what he needs, and returns home to find it.” (George Moore)
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<tr>
<td>PA</td>
<td>Power Amplifier</td>
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<tr>
<td>LTN</td>
<td>Load Transformation Network</td>
</tr>
<tr>
<td>UMC</td>
<td>United Microelectronics Corporation</td>
</tr>
<tr>
<td>IMD</td>
<td>Intermodulation Distortion</td>
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<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
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<tr>
<td>LTE</td>
<td>Long Term Evolution</td>
</tr>
<tr>
<td>ACLR</td>
<td>Adjacent Channel Leakage Ratio</td>
</tr>
<tr>
<td>ACPR</td>
<td>Adjacent Channel Power Ratio</td>
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<tr>
<td>EVM</td>
<td>Error Vector Magnitude</td>
</tr>
<tr>
<td>RFC</td>
<td>Radio Frequency Choke</td>
</tr>
<tr>
<td>LINC</td>
<td>Linear Amplification using Nonlinear Components</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metaloxidesemiconductor</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>SMPA</td>
<td>Switched-mode Power Amplifier</td>
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<tr>
<td>3GPP</td>
<td>3rd Generation Partnership Project</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency Shift Keying</td>
</tr>
<tr>
<td>GMSK</td>
<td>Gaussian Minimum Shift Keying</td>
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<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
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1 Introduction

1.1 Motivation

3GPP Long Term Evolution (LTE), is the latest mobile network standard. The LTE specification provides the peak downlink rate of 100 MBps while the uplink is 50 MBps with Radio Access Network (RAN) round trip time of 10 ms. LTE supports both frequency division duplexing (FDD) and time division duplexing (TDD). The subcarrier bandwidths are scalable ranging from 1.4 MHz to 20 MHz. In uplink channels, single carrier frequency division multiple access (SC-FDMA) is used whereas for downlink orthogonal frequency division multiple access (OFDM) is employed. The advantage of using SC-FDMA is that it reduces peak-to-average power ratio (PAPR). High value of PAPR demands high linearity and thus, emerging wireless technologies require highly linear power amplifiers [1].

In a wireless communication system, the power amplifier (PA) is the last building block in a transmitter chain as given in Fig. 1.1. In the transmitter chain, the IQ-signals are generated by a digital signal processor (DSP) or by field programmable gate array (FPGA). The IQ-signals are converted to analog form by digital to analog (D/A) converter. After low pass filtering, the IQ-signals are converted from baseband frequency to RF frequency by an upconversion mixer. This upconverted signal is the input to the differential power amplifier (PA). The job of the PA is to amplify the incoming signal using DC power which is finally transmitted to the antenna; after converted to single-ended using a balun. If the modulated signal has constant envelope, then switched-mode power amplifiers (SMPAs) can be used to get high efficiency without the fear of signal being corrupted by amplifier’s nonlinearity. In first-generation (1G) and second-generation (2G) systems of mobile communication, e.g. GSM, SMPAs are employed. But in new technologies like Long Term Evolution (LTE), the signals have nonconstant envelope. So, SMPAs cannot be used without having advanced transmit-
1 Introduction

Power amplifiers are used in common source configuration as it offers large power gain, but it comes at a price i.e. the nonlinearity due to transconductance \( g_m \) and especially \( C_{gs} \), which results in high intermodulation distortion [3]. As in modern communication systems with crowded spectrum, intermodulation distortion can severely degrade the performance of a PA. Common drain amplifier has a full 100\% negative feedback between its output and input and thus maximum linearity can be obtained. Class-B mode of operation minimises \( C_{gs} \) and gives highest efficiency which when combined with the linear nature of common drain amplifier may result in amplifier which is both efficient and linear. As per knowledge of the author, only one stable common drain RF PA has been reported in literature (but in GaN technology [3]). Analysis and design of common drain power amplifier has not been reported in CMOS. The main task of this thesis is to design a stable single-ended as well as differential common drain class-B RF

Figure 1.1: RF transmitter front-end

1.2 Scope of work

Power amplifiers are used in common source configuration as it offers large power gain, but it comes at a price i.e. the nonlinearity due to transconductance \( g_m \) and especially \( C_{gs} \), which results in high intermodulation distortion [3]. As in modern communication systems with crowded spectrum, intermodulation distortion can severely degrade the performance of a PA. Common drain amplifier has a full 100\% negative feedback between its output and input and thus maximum linearity can be obtained. Class-B mode of operation minimises \( C_{gs} \) and gives highest efficiency which when combined with the linear nature of common drain amplifier may result in amplifier which is both efficient and linear. As per knowledge of the author, only one stable common drain RF PA has been reported in literature (but in GaN technology [3]). Analysis and design of common drain power amplifier has not been reported in CMOS. The main task of this thesis is to design a stable single-ended as well as differential common drain class-B RF
PA with a 2.5 V supply voltage in LTE frequency band (2.5-2.7 GHz). The operating frequency of the PA is 2.55 GHz. The amplifier must be designed for maximum gain and efficiency. All the steps involved in designing common drain amplifier along with its thorough performance evaluation has to be done. Additionally, common source class-B RF PA should be designed for comparison with the common drain class-B PA.

1.3 Thesis Overview

- Chapter 1 is introductory and describes the motivation and scope of this work.

- Chapter 2 is about the general theory of RF PA and its performance parameters. After that, linear power amplifier classes are discussed.

- Chapter 3 explains the design of a single-ended common drain and common source amplifiers in UMC 90 nm CMOS process. All the steps involved are shown in a systematic design flow. The two designs are analysed using transient, S-parameters and harmonic balance simulations. Special attention is given to linearity and stability issues of the two amplifiers and are explained in detail along with results.

- In Chapter 4, the single-ended common drain amplifier as discussed in previous chapter is converted to differential form. Five different Load Transformation Networks (LTNs) for differential common drain amplifier are presented and their performances are finally compared.

- Chapter 5 presents a single ended and differential common drain class-B PA in Landshut Foundry (LF) 150 nm CMOS process. It is expected to have the amplifier tape-out in LF rather than UMC 90 nm due to technology availability.

- Chapter 6 summarises the overall work done in this thesis and suggests recommendations for future work.
1 Introduction
2 RF Power Amplifiers

2.1 Introduction

One of the key components in a transmitter is a radio frequency power amplifier (RF PA). The main purpose of a RF PA is to amplify the input signal to a sufficient power level so that it can propagate across the channel (e.g. air, space) and is received at the receiver end. Apart from that, the transmitter has to be linear in order to avoid interference and spectral regrowth among the closely spaced channels.

![RF power amplifier block diagram](image)

Figure 2.1: RF power amplifier block diagram.

The input to the PA can be from the filter stage in a transmitter or the output from the previous stage in case of multistage PA design ([4]-[5]). The active device
consists of a transistor (e.g. MOSFET, BJT, or MESFET) working single-ended or in a differential configuration. The input and output matching networks are used to transform input and output impedances to get maximum output power. The device is biased through an RF choke which feeds DC power to the drain and is assumed to be large enough so that the current through it remains constant. The load network provides the necessary impedance conditions to the transistor according to the PA class of operation. The class of the amplifier is determined by its gate bias as well as the load network impedance conditions and input drive level. The block diagram of a PA is illustrated in Fig 2.1

2.2 Performance Parameters

Some of the important performance parameters of PAs are described below

2.3 Output Power

The total output power delivered to load in dBm is given by [4]

\[ P_{dBm} = 10 \log \left( \frac{P_{out}}{0.001} \right) = 10 \log(P_{out}) + 30, \]  

(2.1)

where \( P_{out} \) is given in Watts.

2.4 Power Gain

It is the ratio between the power delivered to the load \((P_o)\) to the power delivered by the source \(P_{in}\) in dB as [4]:

\[ G_{dB} = 10 \log \left( \frac{P_{out}}{P_{in}} \right), \]  

(2.2)

where \( P_{out} \) and \( P_{in} \) are given in Watts.
2.5 Drain Efficiency

Drain efficiency ($\eta$) is the ratio between the available output power and the consumed DC power. It is the metric for DC-RF conversion, which is given by [4]

$$\eta = \frac{P_{\text{out}}}{P_{\text{dc}}}. \quad (2.3)$$

2.6 Power Added Efficiency

The widely used metric of efficiency for PA is Power Added Efficiency (PAE). It differs from the drain efficiency in the sense that it takes the gain of the amplifier into account. Mathematically it is given by [4]

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{dc}}}, \quad (2.4)$$

where $P_{\text{in}}$ is the input RF power. Another form of PAE in terms of gain ($G$) and drain efficiency ($\eta$) is

$$\text{PAE} = \eta \left(1 - \frac{1}{G}\right). \quad (2.5)$$

If $G \gg 1$, then $\text{PAE} \approx \eta$.

2.7 Output Power Capability

It is the ratio between the output power and the product of maximum instantaneous drain source voltage $V_{DS,max}$ and maximum instantaneous drain current $I_{DM}$. It is given by [4]

$$c_p = \frac{P_o}{NI_{DM}V_{DS,max}}, \quad (2.6)$$

where $N$ is the number of transistors which are not connected in series or parallel. For example, for a single stage amplifier $N = 1$ whereas for differential configuration $N = 2$. 
2.8 Rollet Stability Factor

The Rollet stability factor also known as K-factor is used for deciding whether the amplifier is stable or not. If $K > 1$ the amplifier is unconditionally stable. If $K < 1$ the amplifier might be unstable certain combination of load or source impedances. The K-factor is given by [6]:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{21}s_{21}|} \quad (2.7)$$

$$\Delta = s_{11}s_{22} + s_{12}s_{21} \quad (2.8)$$

For complete stability analysis, stability circles are plotted for every possible bias point from DC to RF frequencies, beyond the operating frequency.

2.9 Linearity

Modulation schemes can be divided into two categories

1. Constant envelope modulation

2. Nonconstant envelope modulation

Constant envelope modulation schemes like FSK, GFSK, MSK, GMSK allows the power amplifier to operate near or at the saturation without fear of information being corrupted as all information is stored in phase [4]. Whereas, nonconstant envelope modulation schemes such as QAM contains information in amplitude as well as phase. A 3 to 6 dB output power backoff is used to eliminate spectral leakage which causes Adjacent Channel Interference (ACI). Therefore, in nonconstant envelope modulation schemes a linear PA is necessary [7]. The PA can be described mathematically by a Taylor series expansion as

$$y(t) \approx a_1x(t) + a_2x^2(t) + a_3x^3(t) + \ldots \quad (2.9)$$

If a sinusoid is applied to a nonlinear system, the output contains frequency components that are integer multiple of input frequency. These components are undesired
and are filtered. This type of nonlinear distortion is called harmonic distortion. Substituting $x(t) = A\cos(\omega t)$ for input sinusoid in Eq. 2.9 gives

$$y(t) = a_1 A\cos(\omega t) + a_2 A^2 \cos^2(\omega t) + a_3 A^3 \cos^3(\omega t) + ....$$ (2.10)

by expansion $y(t)$ becomes

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right) \cos(\omega t) + \frac{a_2 A^2}{2} \cos(2\omega t) + \frac{a_3 A^3}{4} \cos(3\omega t) + ....$$ (2.11)

The term with fundamental frequency is called the ‘fundamental’ and the higher-order terms the ‘harmonics’. For small signal operation, $a_1 A$ is greater than all factors containing $A$, then the gain is just $a_1$. An important measure of linearity is 1 dB compression point $P_{1dB}$. When the input power is increased the amplifier enters the saturation region in which it no longer acts as a linear device. The input (or output) referred 1 dB compression point is defined as the point at which the small-signal gain of the amplifier drops by 1 dB as given in Fig. 2.2. For significantly large input levels with amplitude $A$ and if $a_3 < 0$, the gain becomes zero as given by Eq. 2.9. The $A_{1dB}$ is given by:

$$20 \log |a_1 + \frac{3}{4}a_3 A_{1dB}^2| = 20 \log |a_1| - 1dB$$ (2.12)

which becomes

$$A_{1dB} = \sqrt{\frac{0.145 a_1}{a_3}}$$ (2.13)

Another type of distortion is intermodulation distortion and is more serious than harmonic distortion. It is characterized by metrics like $IP_3$, $IMD_3$ and $IMD_5$ as described in the next section.

### 2.9.1 Intermodulation Distortion and Third Order Intercept Point ($IP_3$)

When two closely spaced signals are applied to a nonlinear system, it results in frequency components that are not multiples of the fundamental frequency [7]. Third order intermodulation ($IM_3$) falls in the desired band and corrupt the required information as shown in Fig. 2.3. If $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$ then,
Figure 2.2: P1dB compression point.

\[
y(t) = a_1 (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)) + a_2 (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^2
\]
\[
= +a_3 (A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^3
\]

(2.14)

By expanding Eq. 2.14 and collecting the fundamental terms and in-band IM3 products at 2\omega_1 - \omega_2 \text{ and } 2\omega_2 - \omega_1

\[
\omega = \omega_1, \omega_2 : \left( a_1 A_1 + \frac{3}{4} a_3 A_1^3 + \frac{3}{2} a_3 A_1 A_2 \right) \cos(\omega_1 t) + \left( a_1 A_2 + \frac{3}{4} a_3 A_2^3 + \frac{3}{2} a_3 A_2 A_1 \right) \cos(\omega_2 t)
\]

(2.15)

\[
\omega = 2\omega_1 \pm \omega_2 : \frac{3 a_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2) t + \frac{3 a_3 A_2^2 A_1}{4} \cos(2\omega_1 - \omega_2) t
\]

(2.16)

\[
\omega = 2\omega_2 \pm \omega_1 : \frac{3 a_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1) t + \frac{3 a_3 A_1^2 A_2}{4} \cos(2\omega_2 - \omega_1) t
\]

(2.17)
2.9 Linearity

![Diagram of a two-tone test with third order intermodulation products generated in a PA network.](image)

Figure 2.3: Third order intermodulation products generated in a two tone test.

If \( a_1 \gg \frac{9a_3A^2}{4} \), then the input level at which the magnitude of components at \( \omega_1 \) and \( \omega_1 \) becomes equal to those at \( 2\omega_1-\omega_2 \) and \( 2\omega_2-\omega_1 \) is given by [7],

\[
|a_1|A_{IP3} = \frac{3}{4}|a_3|A_{IP3}^3
\]  

(2.18)

or

\[
A_{IP3} = \sqrt{\frac{4}{3} \frac{a_1}{a_3}}
\]  

(2.19)

The \( IP_3 \) point is the intersection of the fundamental component which increases in proportion to \( A \) and \( IM_3 \) products which increases in proportion to \( A^3 \) as shown in Fig. 2.4. The \( IP_3 \) is used for mixers, LNAs and power amplifiers. The intermodulation power specified at particular power level with respect to the carrier frequency is also used and given in dBc as

\[
IMD_3 = 10\log\frac{P_{3rd}}{P_{fund}}
\]  

(2.20)

\[
IMD_5 = 10\log\frac{P_{5th}}{P_{fund}}
\]  

(2.21)

\( IMD_3 \) and \( IMD_5 \) are measured at 3 dB and 5 dB output power backed-off from \( P_{1dB} \) respectively.

2.9.2 Error Vector Magnitude (EVM)

In an ideal scenario, a signal sent by the transmitter or received by the receiver would have all the constellation points at the exact locations but in a real scenario they deviate from their locations [2]. EVM is the scalar distance of the deviated constellation points
from the ideal points. Mathematically,

\[ EVM = \sqrt{(I_{\text{meas}} - I_{\text{ideal}}) + (Q_{\text{meas}} - Q_{\text{ideal}})} \]  

(2.22)

where \( I_{\text{ideal}} \) and \( Q_{\text{ideal}} \) are the in-phase and quadrature components of the signal in the ideal scenario whereas \( I_{\text{meas}} \) and \( Q_{\text{meas}} \) are the components for measured signal as shown in Fig. 2.5.

### 2.9.3 Adjacent Channel Power Ratio (ACPR)

The intermodulation products (IMD\(_3\), IMD\(_5\), etc.) generated by the nonlinear behaviour of power amplifier fall in-band or close to desired band and cannot be filtered. The IM products have an associated bandwidth which extends into the useful signal (channel) bandwidth. The ratio between the power of the adjacent chan-
2.9 Linearity

Figure 2.5: Error vector magnitude.

nel (having IM products) to the main channel (having useful signal) is called adjacent channel power ratio (ACPR). It is expressed in dBc. The concept is illustrated in Fig. 2.6.

2.9.4 AM-PM Distortion

If the amplifier operates beyond \( P_{1dB} \), the signal suffers from phase distortion besides amplitude distortion [2]. This is called AM-PM distortion. For modulation schemes that employs phase modulation; like 16QAM, QPSK, FM; the AM-PM distortion is very detrimental. AM-PM distortion (or AM-PM conversion) is defined as the change in phase of the output signal due to increase in the input signal power. Its units are degrees-per-dB (°/dB).
2.10 Classes of Power Amplifiers

The transistor (MOSFET, BJT, MESFET) in a power amplifier can be operated as

1. a dependent current source
2. a switch
3. combination of 1 and 2 (i.e. overdriven mode)

The power amplifiers in which the transistor is operated as a dependent current source are known as linear power amplifiers. In these amplifiers the output signal is amplified replica of input signal. They are used for nonconstant envelope signals which contain information in their amplitude. These amplifiers are categorised into class A, AB, B and C. The other category of power amplifiers are called nonlinear power amplifiers or switched-mode power amplifiers. In nonlinear PAs, the transistor is operated as a switch. They are classified as class D, E, F, F−1, J, S. Sometimes, combination of linear and switched-mode operation is used like in class-AE ([4]-[5]).
2.10 Classes of Power Amplifiers

2.10.1 Linear Power Amplifiers

When a MOS transistor is operated as a dependent current source, the drain current waveform is a function of the input voltage waveform and the transistor gate bias voltage. The drain voltage waveform is a function of the current source and the load network impedance. To get maximum power out of the transistor, the load impedance of 50 Ω must be transformed into a lower value $R_{opt}$. The $R_{opt}$ is determined through the DC-loadline which is a line drawn between the maximum voltage and maximum current in the IV plot of the transistor. This is also called loadline match as shown in Fig. 2.7 [5]. The point of intersection of the DC-loadline on the current axis (y-axis) is called saturation point, given by $I_{max}$ while the point on the voltage axis (x-axis) is called cutoff point and its value is $2V_{dd}$ (only ideally). These points set a limit on both the current and voltage handling capability of the device. Thus, power which is the product of current and voltage is maximized. The $R_{opt}$ is given by

$$R_{opt} = \frac{V_{dd}}{I_{max}/2} = \frac{2V_{dd}}{I_{max}}$$

(2.23)

Secondly, conjugate matching is used on the input side of the amplifier [5]. In conjugate matching; 50 Ω source is matched to the conjugate of the impedance seen at the gate of the transistor. In this way, maximum power is transferred from the source to the gate of the transistor. The impedance transformation on the input and output sides of the transistor are done through passive matching networks. In the next section, the classes of linear PAs waveforms are briefly discussed.

2.10.2 Class-A Amplifier

Class-A is the most linear PA as the transistor conducts during the entire cycle of the input. The transistor is biased in the middle of the loadline as shown in Fig. 2.7. Hence, maximum voltage and current swings are obtained as the output goes from cutoff to saturation. The problem with class-A amplifier is its poor efficiency as it always carry current even when the signal is not present. The total output signal power is given by

$$P_{out} = \frac{i_{out}^2R_L}{2};$$

(2.24)
Assuming that $I_{dc} = i_{out}$, then the power dissipation across the transistor is

$$P_{dc} = V_{dd}I_{dc} \tag{2.25}$$

The drain efficiency becomes

$$\eta = \frac{P_o}{P_{dc}} = \frac{i_{out}R_L}{2V_{dd}} \tag{2.26}$$

For maximum power transfer to the load, $V_{dd} = i_{out} R_L$, which gives maximum drain efficiency of 50%. The output power capability is given as

$$c_p = \frac{V_{dd}^2/2R_L}{(2V_{dd})(2V_{dd}/R_L)} = \frac{1}{8} \tag{2.27}$$

Class-A amplifiers are used when efficiency is not required and linearity is the major goal e.g. in amplitude modulation scenarios (actually in fixed installations).

Class-A operation is shown in Figure 2.8a.
2.10 Classes of Power Amplifiers

2.10.3 Class-B Amplifier

In class-B amplifiers, the transistor conducts only when an input signal is present at the gate. In class-B, the device is biased at the threshold voltage $V_t$. Thus, at the output, the current waveform is a half rectified sine wave and therefore, class-B offers higher efficiency than class-A. The drain current during the positive cycle is given by

$$i_d = i_{out} \sin(\omega_o t)$$  \hspace{1cm} (2.28)

Integrating over half the period gives the fundamental component of drain current

$$i_{fund} = \frac{1}{\pi} \int_0^{\pi/2} (i_{out} \sin(\omega_o t)) \sin(\omega_o t) dt = \frac{i_{out}}{2}$$  \hspace{1cm} (2.29)

The voltage across the load is

$$v_{out} = i_{fund} R_L \sin(\omega_o t) = \frac{i_{out}}{2} R_L \sin(\omega_o t)$$  \hspace{1cm} (2.30)

Maximum value of $\sin(\omega_o t)$ is 1 so that maximum value of $v_{out}$ and $i_{out}$ are

$$v_{out, max} = V_{dd}$$  \hspace{1cm} (2.31)
RF Power Amplifiers

\[ i_{\text{out, max}} = \frac{2V_{dd}}{R_L} \] (2.32)

The maximum power delivered to the load is

\[ P_{\text{out, max}} = \frac{V_{dd}^2}{2R_L} \] (2.33)

Since the transistor conducts only during one half cycle, the average drain current is

\[ i_{d, av} = \frac{1}{T} \int_{0}^{T} \frac{2V_{dd}}{R_L} \sin\omega t \ dt = \frac{2V_{dd}}{\pi R_L} \] (2.34)

The DC power consumed from the supply is the product of average drain current and supply voltage as given below

\[ P_{\text{DC}} = V_{dd} \times i_{d, av} = \frac{2V_{dd}^2}{\pi R_L} \] (2.35)

Dividing Equation 2.33 by 2.35 gives the maximum efficiency as given below:

\[ \eta = \frac{P_{\text{out, max}}}{P_{\text{DC}}} = \frac{\pi}{4} = 78.5\% \] (2.36)

class-B operation is shown in Fig. 2.8c.

2.10.4 Class-AB Amplifier

Class-A offers more linearity while class-B is more efficient than class-A. A trade-off between the two leads to class AB amplifier. Here, the gate bias is between is between class-A and class-B. Hence, the corresponding conduction angle is between \( \pi \) radians to \( 2\pi \) radians as shown in Fig. 2.8b. The ideal efficiency is therefore between 50% to 78.5%.

2.10.5 Class-C Amplifier

In class-C operation, the transistor is biased below threshold which results in the current conduction angle in the range of 0° to \( \pi \) radians as given in Figure 2.8c. Since the conduction angle is less than that of class-B, correspondingly efficiency is much greater. In theory, class-C amplifiers can attain maximum efficiency of 100% (but only
at 0 Watt output power). Class-C amplifiers are widely used where frequency and phase modulation schemes are employed.

### 2.10.6 Fourier Analysis of Conduction Angle

In linear power amplifiers a pattern can be noted, that there is a trade-off between the amplifier’s linearity and efficiency both of which are connected to the value of conduction angle \([4]-[5]\). For example, in class-A, the conduction angle is \(2\pi\) radians and it has maximum linearity and minimum efficiency, whereas class-C has maximum efficiency and minimum linearity for a conduction angle less than \(\pi\) radians. Applying Fourier analysis technique to the drain current waveform and plotting it as a function of conduction angle \(\theta\) reveals that class-C has maximum harmonic content while class-A has the least. This is illustrated in the Table 2.1 & Table 2.2 and Fig 2.9 & Fig. 2.10.

#### Table 2.1: Fourier components as a function of drain current.

<table>
<thead>
<tr>
<th>Class</th>
<th>DC Current</th>
<th>Fundamental Component</th>
<th>Harmonic Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Maximum</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>AB</td>
<td>Moderate</td>
<td>Highest</td>
<td>Yes</td>
</tr>
<tr>
<td>B</td>
<td>Less</td>
<td>Same as A</td>
<td>No odd harmonics</td>
</tr>
<tr>
<td>C</td>
<td>Lowest</td>
<td>Lowest</td>
<td>Yes</td>
</tr>
</tbody>
</table>

#### Table 2.2: Efficiency and output power as a function of conduction angle.

<table>
<thead>
<tr>
<th>Class</th>
<th>Conduction Angle</th>
<th>Output Power</th>
<th>Max Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>100 %</td>
<td>Moderate</td>
<td>50 %</td>
</tr>
<tr>
<td>AB</td>
<td>50-100 %</td>
<td>Highest</td>
<td>50-78.5 %</td>
</tr>
<tr>
<td>B</td>
<td>50 %</td>
<td>Moderate</td>
<td>78.5 %</td>
</tr>
<tr>
<td>C</td>
<td>&lt;50 %</td>
<td>Small</td>
<td>100 %</td>
</tr>
</tbody>
</table>
Figure 2.9: Fourier analysis of drain current for linear power amplifier classes.

Figure 2.10: Efficiency and output power as a function of conduction angle.
3 Single-Ended Class-B RF Power Amplifier

3.1 Introduction

In this chapter, two single-ended designs of class-B RF power amplifiers are presented. The first design is in common drain configuration while the other is in common source topology [9]. A systematic design flow of single-ended PA is explained. The differences and similarities between the two amplifiers in terms of their performances are elaborated. The simulations are done using ideal components. The technology employed is UMC 90 nm and the simulator is SpectreRF from Cadence Design Systems. The simulation includes transient, DC, S-parameter and harmonic balance simulations. The harmonic balance simulations are used for calculating gain, efficiency, single-tone harmonic distortion and two-tone intermodulation distortion [10].

3.2 Power Amplifier Design Flow

The design flow of a linear RF power amplifier is illustrated in Fig. 3.1. It is worth mentioning that the design flow for switched-mode PA is the same except that it does not have stability network as the device does not have any gain due to the fact that it is operating as a switch rather than a controlled current source. Given the specifications of amplifier (like output power, gain, class, efficiency, linearity, etc) and technology (hybrid or integrated), the first step is to determine the optimum load resistance $R_{opt}$ of the amplifier for a given output power and current. The $R_{opt}$ is calculated via load-line or load-pull simulation. In case of integrated amplifiers the transistor is sized for the required output power and the load transformation network (LTN) is designed for a particular PA class. After that, stability and input matching networks are imple-
mented. Since the PA has significant nonlinear behavior due to large signal operation, its performance might not be the same as done through calculation. So, the amplifier needs to be tuned either by changing the size of device, the $R_{opt}$, corresponding input and stability network, tuning out parasitics, using high $Q$ components in load network or making the load network off-chip for maximum gain and efficiency etc. Thus, proper PA design requires lots of iterations as well as experience.

### 3.3 The Load Transformation Network (LTN)

For linear PAs in CMOS, a large transformation ratio is necessary in the load network to deliver reasonable power from the device to 50 Ω load (e.g. antenna).

$$P_{out} = \frac{(V_{dd} - V_{knee})^2}{2R_{opt}}$$  \hspace{1cm} (3.1)

As can be seen from the above equation that lower supply voltage ($V_{dd}$) and high knee voltage ($V_{knee}$) are the limiting factors in CMOS for delivering substantial amount of power to the load. This design is based on 2.5 V drain supply with a knee voltage of 0.75 V [5]. There are two approaches to determine $R_{opt}$ of the device

1. Loadline
2. Load-pull simulation

In this design, load-line is used to determine the $R_{opt}$ of the amplifier.

For 28 dBm peak output power, $R_{opt}$ is

$$R_{opt} = \frac{V_{dd}^2}{2P} = \frac{6.25}{2 \cdot (0.6)} = 5.2 \ \Omega.$$  \hspace{1cm} (3.2)

The maximum output current is given by

$$I_{max} = \frac{2V_{dd}}{R_{opt}} = \frac{5}{5.2} = 960 \ mA.$$  \hspace{1cm} (3.3)

The device is scaled to deliver the required amount of current. The dimensions of the device are: (gate width) x (no of fingers) x (no of transistors connected in parallel). In this case it is: (9.6 u x 28 x 8) m = 2.15 mm. Sweeping the gate voltage in linear
3.3 The Load Transformation Network (LTN)

Figure 3.1: Power amplifier design flow.
steps of 0.1 V to 2.2 V, the IV-characteristics are obtained which are used to calculate the loadline and, hence, the $R_{\text{opt}}$ as given by Eq. 3.4 and Fig. 3.2.

$$R_{\text{opt}} = \frac{2(V_{\text{dd}} - V_{\text{knee}})}{I_{\text{max}}} = \frac{2(2.5 - 0.75)}{0.82} = 4.27 \ \Omega. \quad (3.4)$$

Since the number of transistors must be in even numbers for symmetry. The $R_{\text{opt}}$ calculated from load line (Eq. 3.4) is very close to that given in Eq. 3.3. The $R_{\text{opt}}$ remains the same for linear amplifiers whether they are used in common drain or common source configuration [11]. The current remains the same at the fundamental frequency for class-A ($\Theta = 2\pi$), class-AB ($\pi < \Theta < 2\pi$) and class-B ($\Theta = 2\pi$) as given in Fig. 2.9. This is also true for the voltage waveform. Hence, the $R_{\text{opt}}$ is the same for these classes of the amplifier. The same reasoning holds for amplifiers in common drain or common source configuration as voltage and current waveforms are same. The major difference between common source and common drain configuration is that in the former current and voltage are out of phase while in later the current and voltage are in phase. The common drain has 100% negative feedback between its input (gate) and output (source). The device parameters are given in Table 3.1.

A deep n-well device is chosen to eliminate body effect as source and bulk terminals are isolated but more importantly it has lower $C_{gs}$ which is a major source of $3^{rd}$ order intermodulation distortion (IMD$_3$) [8]. The body effect is troublesome in common drain amplifiers as it lowers the gain and varies the threshold voltage, $V_{th}$ of the

Figure 3.2: IV characteristics and DC loadline for device BPW-N25-RF from UMC 90 nm
3.3 The Load Transformation Network (LTN)

<table>
<thead>
<tr>
<th>Technology</th>
<th>Device</th>
<th>Width</th>
<th>Length</th>
<th>Multiplier</th>
<th>Fingers</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMC 90 nm</td>
<td>BPW-N25-RF</td>
<td>9.6</td>
<td>240</td>
<td>8</td>
<td>28</td>
<td>2.15</td>
</tr>
</tbody>
</table>

Table 3.1: Device Features

device [9]. For class-B mode of operation, the impedance conditions for LTN are

\[
Z_{\text{opt}} = \begin{cases} R_{\text{opt}} @ f_0 \\ 0 @ n f_0 \end{cases}, \text{ where } n = 2, 3, 4, \ldots
\]

where \( Z_{\text{opt}} \) denotes optimum impedance of the load transformation network at fundamental and harmonic frequencies. The LTN consists of two parts ([2], [5])

1. Harmonic tank
2. Impedance transformation network

If \( R_s < R_p \); i.e., low-to-high impedance transformation; then, the values of \( L \) and \( C \) are given below [12]

\[
q = \sqrt{\frac{R_p}{R_s}} - 1 \quad \text{(3.5)}
\]

\[
X_s = \pm q R_s = \mp \frac{R_p}{q}, \quad X_p = \mp \frac{1 + q^2}{q^2} X_s \quad \text{(3.6)}
\]

\[
L = \frac{X_{s/p}}{2\pi f_o}, \quad C = \frac{1}{\frac{2\pi f_o X_{p/s}}{}} \quad \text{(3.7)}
\]

It should be noted that all matching networks are bilateral, i.e., if the port on left with impedance \( X \) sees impedance \( Y \) looking at port-2, then looking from port-2 the impedance seen is \( X \). If one element in L-matching network is capacitive, then the other must be inductive and vice versa (as given by signs in the design equations) and this forms either lowpass or highpass networks. The values of \( L \) and \( C \) are found to be 0.95 nH and 3.67 pF respectively. The quality factor \( Q \) of the matching network is fixed in case of L-matching network and the designer has no control over it. However, by using T or \( \pi \) or a combination of them, the quality factor of the transformation network can be controlled which results in broadband impedance matching network at the cost of additional components. For example, a T-matching network is a combination of two
L-matching networks placed side by side with parallel elements adding up, whereas in \( \pi \)-matching network the series elements add up as shown in Fig. 3.3.

![Diagram of L-matching, \( \pi \)-matching, and T-matching networks](image)

**Figure 3.3:** Different impedance transformation networks.

In this design, lowpass L-matching network is employed on the input and output sides. The harmonic tank is a parallel LC resonator resonating at fundamental frequency. The energy oscillates back and forth between the capacitor and the inductor until internal resistance makes the oscillations die out. Its action, known mathematically as a harmonic oscillator, is similar to a pendulum swinging back and forth, or water sloshing back and forth in a tank. For this reason the circuit is also called a tank circuit. The tank circuit can be narrowband or broadband depending on the loaded quality factor \( Q_L \)

\[
Q_L = \frac{f_o}{BW}.
\]  

(3.8)

The narrower the bandwidth the better the harmonic suppression and vice versa. Narrower bandwidth corresponds to a small inductor and a large capacitor. This is elaborated by the following design equations for harmonic tank as given below

\[
X_L Q = X_c Q = R_p,
\]  

(3.9)
3.4 Stability Analysis

\[ L = \frac{R_p}{2\pi f_o Q}, \quad (3.10) \]

\[ C = \frac{Q}{2\pi f_o R_p}, \quad (3.11) \]

where \( R_p \) is the equivalent parallel resistance, usually equal to the 50 Ω. Two different harmonic tanks are designed depending on the availability of inductor values in the UMC 90 nm technology.

<table>
<thead>
<tr>
<th>Tank</th>
<th>L [nH]</th>
<th>C [pF]</th>
<th>Q</th>
<th>BW [MHz]</th>
<th>( Z_{f_0} ) [Ω]</th>
<th>( Z_{2f_0} ) [Ω]</th>
<th>( Z_{3f_0} ) [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tank-1</td>
<td>0.165</td>
<td>23.6</td>
<td>18.9</td>
<td>134</td>
<td>5.085-j0.0029</td>
<td>0.002242-j0.03725</td>
<td>-j0.02</td>
</tr>
<tr>
<td>Tank-2</td>
<td>1</td>
<td>3.82</td>
<td>3.12</td>
<td>817</td>
<td>5.085-j0.0029</td>
<td>0.07756-j0.216</td>
<td>0.022-j0.132</td>
</tr>
</tbody>
</table>

Table 3.2: Design parameters and the impedances provided the LTN utilising two different tanks

The harmonic tank is series connected to L-matching network. The lowpass L-network consists of a series \( L \) and shunt \( C \). The impedance charts of load network with Tank-1 and Tank-2 are given in Fig. 3.4 and Fig 3.5 respectively. It can be inferred from the impedance charts and Table 3.2 that the tank with narrower bandwidth greatly suppresses the harmonics. The minimum inductor in UMC 90 nm technology is 165 pH. Therefore, Tank-1 is chosen in this design. The AC path to ground is provided by connecting a capacitor at the drain of the amplifier. This big capacitor is troublesome for integrated PA as it consumes lots of area. An RF choke is also used for providing DC current from the power supply which also enables to have the voltage swing in the negative cycle. The schematic of the common drain class-B PA with load network and a bypass capacitor is shown in Fig. 3.6

3.4 Stability Analysis

Stability is an important aspect in a PA design [6]. At RF, the assumption of a device being unilateral \( (S_{12} = 0) \) does not hold. The feedback term \( S_{12} \) makes the amplifier unstable. The common drain amplifier has serious stability issues over a large frequency range as compared to common source configuration. The stability is best explained by a small signal model of FET as given in Fig. 3.7 [13]
Figure 3.4: Impedances for load network with Tank-1 (narrowband) in the Smith chart.

Figure 3.5: Impedances for load network with Tank-2 (broadband) in the Smith chart.
3.4 Stability Analysis

$$V_{dd}$$

RFC
$$C_{bypass}$$

$$v_{in} + V_{gs}$$

$$R_{opt} @ f_0$$

$$Z_{opt}$$

0 @ n f_0 ,

n=2,3,4..

Harmonic Tank

Impedance Transformation

Network @ f_0

$$L_m$$

$$C_m$$

$$50 \Omega$$

Figure 3.6: Common drain class-B PA with LTN.

1. The intrinsic elements $$g_m$$, $$g_d$$, $$C_{gs}$$, $$C_{gd}$$, $$C_{ds}$$, $$R_i$$ and $$\tau$$ are bias dependent.

2. The extrinsic elements $$L_g$$, $$R_g$$, $$C_{pg}$$, $$L_s$$, $$R_s$$, $$R_d$$, $$C_{pd}$$ and $$L_d$$ are bias independent.

The intrinsic device exhibits a π-topology and it is convenient to use the admittance ($$Y$$) parameters to characterise its electrical properties. The Y-matrix of a common source amplifier is

$$\begin{bmatrix}
Y_{11} & Y_{12} \\
Y_{21} & Y_{22}
\end{bmatrix} = \begin{bmatrix}
\frac{R_i C_{gs} \omega^2}{D} + j \omega (\frac{C_{gs}}{D} + C_{pd}) & -j \omega C_{gd} \\
g_m \exp(-j \omega \tau) \frac{1}{1 + j R_i C_{gs} \omega} - j \omega C_{gd} & g_d + j \omega (C_{ds} + C_{gd})
\end{bmatrix}, \quad (3.12)
$$

where $$D=1+\omega^2 C_{gs}^2 R_i^2$$
The Y-matrix can be mapped onto common drain configuration from common source with the following transformation [14]

\[
[Y_{\text{drain}}] = \begin{bmatrix}
Y_{11,s} & -(Y_{11,s} + Y_{12,s}) \\
-(Y_{11,s} + Y_{21,s}) & Y_{11,s} + Y_{12,s} + Y_{21,s} + Y_{22,s}
\end{bmatrix},
\] (3.13)

Where the \(Y_{ij,s}\) in Eq. 3.13 denotes Y parameters for common source amplifier for \(i, j = 1\) or \(2\). Substituting Y-parameters of common source configuration gives the following Y-matrix for common drain

\[
[Y_{\text{drain}}] = \begin{bmatrix}
\frac{R_i C_{gs}^2 \omega^2}{D} + j\omega \left(\frac{C_{gs}}{D} + C_{gd}\right) & \frac{g_m \exp(-j\omega T)}{1 + j R_c C_{gs} \omega} + j\omega C_{gs} + Y_{12} \\
R_i C_{gs}^2 \omega^2 + j\omega \left(\frac{C_{gs}}{D} + C_{gd}\right) + g_m \exp(-j\omega T) & Y_{22}
\end{bmatrix}
\] (3.14)

with

\[
Y_{22} = \left(\frac{g_m \exp(-j\omega T)}{1 + j R_c C_{gs} \omega} + \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega \left(\frac{C_{gs}}{D}\right)\right) + g_d + j\omega C_{ds}
\] (3.15)
3.4 Stability Analysis

\[ Y_{12} = - \left( \frac{R_i C_{gs}^2 \omega^2}{D} + j \left( \omega C_{gs} \right) \right) \]  

(3.16)

The instability of a common drain amplifier is attributed to \( Y_{12} \) which is a function of \( R_i \) and nonlinear \( C_{gs} \). To stabilise the common drain amplifier, a positive admittance must be presented at the gate to cancel out the effects of \( Y_{12} \). The stability network consists of a series \( RC \) circuit in parallel at the gate of the device. The \( RC \) network has low impedance at high frequencies as indicated by its response in Fig. 3.8. Therefore, it shortens considerable amount of input RF power to ground, thereby further degrading the overall gain (i.e. current gain) of a common drain amplifier. Without stability network, the K-factor is below 1 for a wide range of frequencies as shown in Fig. 3.9 and given by Eq. 3.16. The amplifier is made unconditionally stable for all bias points as indicated by Fig. 3.10 and stability circles in Fig. 3.11. An alternative approach for stability analysis of common drain amplifiers is presented in [15].

![Figure 3.8: Impedance plot for RC stability network in the Smith chart.](image-url)
3 Single-Ended Class-B RF Power Amplifier

Figure 3.9: K-factor for an unstable common drain amplifier at class-B bias of 0.56 V.

Figure 3.10: K-factor for a stable common drain amplifier at class-B bias of 0.56 V

3.5 Input Matching

As compared to loadline matching for LTNs, conjugate matching is used on the input side [5]. The input matching is necessary to avoid reflections to the input and to get maximum power from the input source to the gate of the device. On the input side different matching networks like L-, T-, π- matching networks or their derivatives can be used to provide narrowband or broadband impedance matching. Usually, the network with series inductor is preferred due to the following two reasons:

1. To provide a DC path if a bias-Tee is used.
3.5 Input Matching

Figure 3.11: Source stability circles using parametric sweep of $V_{gs}$ from -2 to 3 V and frequency sweep from 0 to 10 GHz for common drain amplifier. The amplifier is made unconditional stable [6].

2. Series resistance due to finite quality factor of the inductor prevents low frequency oscillations.

The S-parameters plots are shown in Fig. 3.12 and Fig. 3.13.

The complete schematic of the designed single-ended common drain class-B amplifier is shown in Figure 3.17. The various performance parameters for the whole system level simulation of common drain amplifier are given in Table 3.3 and 3.4. The common drain amplifier provides 6 dB gain in the linear region.
3 Single-Ended Class-B RF Power Amplifier

Figure 3.12: Impedance plot looking from 50 Ω input of the amplifier.

Figure 3.13: S-parameters plot for common drain amplifier.

<table>
<thead>
<tr>
<th>$f_o$ [GHz]</th>
<th>$P_{in}$ [dBm]</th>
<th>$P_{1dB}$ [dBm]</th>
<th>$I_{out}$ [mA]</th>
<th>$V_{out}$ [V]</th>
<th>$IP_3$ [dBm]</th>
<th>PAE [%]</th>
<th>$\eta$ [%]</th>
<th>$G$ [dB]</th>
<th>$P_{f0}$ [dBm]</th>
<th>$P_{2f0}$ [dBm]</th>
<th>$P_{3f0}$ [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.55</td>
<td>17</td>
<td>27.23</td>
<td>552</td>
<td>1.5</td>
<td>20.5</td>
<td>43</td>
<td>59</td>
<td>6.1</td>
<td>23.1</td>
<td>-12.6</td>
<td>-40.3</td>
</tr>
</tbody>
</table>

Table 3.3: Performance parameters for the single-ended common drain class-B RF PA.
3.5 Input Matching

Figure 3.14: Time-domain source voltage and source current waveforms for common
drain amplifier class-B PA with $Q_L = 18.9$.

Figure 3.15: Time-domain source voltage and source current waveforms for common
drain amplifier class-B PA with $Q_L = 3.12$. The flattening of the current
waveform is a clear indication of dominant even order harmonics.

Table 3.4: S-parameters at fundamental frequency of 2.55 GHz while $K_{min}$ is at
2.6 GHz for single-ended common drain class-B RF power amplifier.
3 Single-Ended Class-B RF Power Amplifier

Figure 3.16: Harmonic power spectrum at $P_{in} = 17$ dBm for common drain class-B PA.

Figure 3.17: Schematic of a complete common drain class-B RF PA.

3.6 Single-Ended Common Source Class-B RF Power Amplifier

The amplifier in common drain configuration is converted to common source configuration by connecting the load network to the drain of the device in order to compare the performance of two PAs in terms of linearity, efficiency and gain. The load net-
Figure 3.18: Power gain, drain efficiency and power added efficiency plots for common drain class-B PA.

work remains the same as discussed earlier. The only changes which need to be done are on the input side. The stability network has to be redesigned to meet the requirements of common source amplifier. After that, conjugate matching accordingly at the input. The Y-matrix of a common source amplifier is given in Sec. 3.4. The cause of instability in common source is the Miller Capacitance \( C_{gd} \). In fact, in common source amplifiers, the instability occurs at low frequencies as the device has enormous amount of power gain (both voltage and current) as shown in Fig. 3.22. This is in sharp contrast to common drain amplifier which only has current gain and the voltage gain is even less then unity as shown in Fig. 3.14 for \( P_{in} = 17 \) dBm. The common drain amplifier has stability problems over a wide range of frequencies. The complete common source amplifier with stability network is shown in Fig. 3.19. As can be seen from Fig. 3.20 the minimum K-factor is at lower frequencies and tends to increase with increasing frequency.

The parallel RC network at the gate of the amplifier increases the real part of \( Z_{11} \) whereas the parallel resistor increases the low frequency stability by reducing the input impedance of the amplifier [16].

The common source PA has 4.3 dB higher gain and 10 % higher peak PAE than the common drain amplifier with the same load transformation network. The lower performance of common drain is attributed to its stability network and the fact that it only provides current gain. The reverse isolation of common source is much better due to little feedback whereas common drain has a 100 % negative feedback structure.
Figure 3.19: Schematic of a complete common source class-B RF PA.

Figure 3.20: K-factor of unstable common source amplifier.

<table>
<thead>
<tr>
<th>$f_o$ [GHz]</th>
<th>$P_{in}$ [dBm]</th>
<th>$P_{1dB}$ [dBm]</th>
<th>$I_{out}$ [mA]</th>
<th>$V_{out}$ [V]</th>
<th>$IP_3$ [dBm]</th>
<th>PAE [%]</th>
<th>$\eta$ [%]</th>
<th>$G$ [dB]</th>
<th>$P_{fo}$ [dBm]</th>
<th>$P_{2fo}$ [dBm]</th>
<th>$P_{3fo}$ [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.55</td>
<td>14</td>
<td>26.84</td>
<td>605</td>
<td>4.22</td>
<td>20.7</td>
<td>54</td>
<td>60</td>
<td>10.36</td>
<td>24.4</td>
<td>-12.13</td>
<td>-39.9</td>
</tr>
</tbody>
</table>

Table 3.5: Performance parameters for single ended common source class-B RF PA.

which accounts for its unity voltage gain. The reverse isolation ($S_{12}$) for common drain is at -13.5 dB whereas for common source it is at -22 dB as given in Tables 3.4 and 3.6.
3.6 Single-Ended Common Source Class-B RF Power Amplifier

![Graph showing K-factor of stable common source amplifier.](image)

**Figure 3.21:** K-factor of stable common source amplifier.

![Graph showing time-domain drain voltage and source current waveforms.](image)

**Figure 3.22:** Time-domain drain voltage and source current waveforms for common source amplifier class-B PA.

<table>
<thead>
<tr>
<th>$S_{11}$ [dB]</th>
<th>$S_{12}$ [dB]</th>
<th>$S_{21}$ [dB]</th>
<th>$S_{22}$ [dB]</th>
<th>$K_{min}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-52</td>
<td>-22</td>
<td>9.39</td>
<td>-2.4</td>
<td>1</td>
</tr>
</tbody>
</table>

**Table 3.6:** S-parameters at fundamental frequency of 2.55 GHz while $K_{min}$ is at 2.6 GHz for single ended common source class-B RF power amplifier.

respectively. Common drain configuration also do not have cascode form which is used in common source amplifiers to eliminate Miller capacitance for providing input and output decoupling.
3 Single-Ended Class-B RF Power Amplifier

Figure 3.23: Harmonic power spectrum at $P_{in} = 14$ dBm for common source class-B PA.

Figure 3.24: Power gain, drain efficiency and power added efficiency plots for common source class-B PA.

3.7 Linearity Analysis

Linearity in power amplifiers is very important so that the SNR requirement in a wireless communication system can be met. The linearity can be categorised into two major categories

1. Harmonic distortion

2. Intermodulation distortion
Harmonic distortion is generated at integer multiples of fundamental frequency. It is usually not problematic as it can be filtered out. The other type of distortion is intermodulation distortion which falls in-band and cannot be filtered. The increasingly crowded spectrum in modern communication systems puts severe constraints on system linearity to avoid interference and spectral regrowth due to intermodulation distortion. The usual approach to tackle distortion apart from linearization is power backoff which leads to reduced efficiency and overall degradation of system performance. The linearization can be done at [17]-[18].

1. Device level
2. Circuit and system level

The device level linearization includes

1. Capacitive compensation using PMOS device to tackle nonlinear gate source capacitance
2. Deep n-well NMOS also reduces distortion caused by $C_{gs}$
3. Back-gate effect

The circuit and system level linearization includes:

1. Feed-forward
2. Predistortion
3. Use of parallel amplifiers with different bias conditions to cancel gain/phase variations

### 3.8 Large- and Small- Signal IMD Behaviour in RF Power Amplifiers

The transfer function of a nonlinear device such as MOSFET is represented by its $I_d-V_{gs}$ plot as shown in Fig. 3.27. If the system is excited by two-tones as $V_{in} = A[\cos(\omega_1 t + \phi_1) + \cos(\omega_2 t + \phi_2)]$, then the response of the system in small signal
regime from Y to Z and large signal regime from Z onwards as given in Fig. 3.27 is ([19], [20], [21], [22]):

\[ I_{\text{out}}(2\omega_2-\omega_1) = \frac{3A^3}{8}H_3(\omega_2-\omega_2-\omega_1)e^{j2\phi_2-\phi_1} + \frac{50A^5}{32}H_5(\omega_2-\omega_2-\omega_1)e^{j2\phi_2-\phi_1} + LS(A, 2\omega_2-\omega_1) \]

(3.17)

where H₃ and H₅ are the 3rd and 5th order Volterra series coefficients. These terms are used to describe the small-signal behaviour, whereas LS is the large-signal behaviour described by TSIDF (two tone input describing function). The interaction between the large and small signal terms create intermodulation nulls or sweet spots in RF power amplifiers. By changing the bias conditions of the amplifiers these nulls can be moved to different locations. For example as shown in Fig. 3.41 and Fig. 3.34 for class-C; 3rd order derivative has an increasing (positive) slope as shown in Fig. 3.25 at bias voltage of 0.2 V. This combined with the nonlinearity due to turn-on voltage which can be described by higher order derivative (for example 5th order) raises the slope of IMD3 curve to almost 5 dB/dec. When the transistor saturates the IM3 becomes negative and a null occurs near compression point. For class-A, class-B voltages of 1.2 V and 0.56 V, respectively. The nulls are created by the interaction between small and large signal regimes. In class-A, the null appears at lower input power levels than for class-B as the input signal will reach the power saturation region before the turn-on region as indicated in Fig. 3.32 and Fig. 3.37 for common drain and common source class-A, respectively, and Fig. 3.31 and Fig. 3.39 for common drain and common source class-B, respectively. In fact in common source amplifier, it is noted that, for its class-B bias of 0.56 V it has a possible second minima at low power levels as shown in Fig. 3.39 which is not observed is common drain bias of 0.56 V. If it is biased at a slightly low voltage, e.g. 0.5 V, the minima disappears as shown in Fig. 3.38. More precisely, for a null to be created the small-signal regime must have precise 180° phase difference with the larger signal in class-A and class-B. Class-AB shows two distinct intermodulation patterns. Biasing the device just above threshold Vₜₚ (= 0.56 V), V₂1 (= 0.7 V) (i.e. V₂1 > Vₜₚ) creates two intermodulation nulls. The first one is created by the cancellation due to 3rd order derivative cancelled by turn-on nonlinearity. As the output power saturates another null is created by the large-signal nonlinearity similar to that in class-B and class-A. Another form of class-AB behaviour is a flat region having low IMD3 level. This is created by further biasing the device away from threshold at
3.9 Nonlinearities in CMOS

V_{g2} (where V_{g2} > V_{g1} > V_{th}). In this case as soon as the nulls appear due to 3rd order and 5th order nonlinearity the signal reaches large-signal nonlinearity and the curve rises up giving a flat region. This flat region is observed in both common drain and common source amplifiers as given in Fig. 3.40 and Fig. 3.33. The nonlinearity due to sharp turn-on occurs as the device moves from exponential sub-threshold region to quadratic ones. The large-signal nonlinearities are loadline entering the triode region, device break down and operation in deep saturation region.

3.9 Nonlinearities in CMOS

The crucial nonlinearity in CMOS is nonlinear gate source capacitance \( (C_{gs}) \) and the other one being transconductance \( (g_m) \) variation. The third-order intermodulation current due to \( C_{gs} \) and \( g_m \) using the model in Fig. 3.26 is given by [8].

\[
i_{C_{gs}, 2\omega_2\omega_1} = j(2\omega_2 - \omega_1) \frac{3}{4} C_{gs} v_{gs,\omega_2}^2 v_{gs,\omega_1}^* + j(2\omega_2 - \omega_1) C_{gs2} [v_{gs, 2\omega_2} v_{gs,\omega_1}^* + v_{gs, 2\omega_2} v_{gs,\omega_1}^*],
\]

(3.18)

\[
i_{g_m, 2\omega_2\omega_1} = \frac{3}{4} g_m v_{gs,\omega_2}^2 v_{gs,\omega_1}^*,
\]

(3.19)

Figure 3.25: 3rd and 5th order normalized derivatives of the transfer function \( (I_d vs V_{gs}) \)

where subscript indicate the term in the Taylor series expansion. Results have shown
that $C_{gs}$ effects significantly the linearity of a PA as compared to $g_m$ by more than 10 dB for a standard device [8]. But with deep n-well device the $C_{gs}$ contribution to IMD$_3$ is significantly reduced. The measure of IMD$_3$ distortion is carrier to intermodulation ratio ($C/I$) and is also denoted by IMD$_3$, is given by

$$\frac{C}{I} = IMD_3 = 10 \log \frac{P_{3rd}}{P_{fund}} [dBc], \quad (3.20)$$

where $P_{3rd}$ is the third-order intermodulation power and $P_{fund}$ is the fundamental power.

![Nonlinear Volterra series model described by Eq. 3.18 and Eq. 3.19](image)

Biasing the device at threshold produces minimum or theoretically zero $C_{gs}$. Consider any transfer function which can be written in terms of even and odd parts as [3]

$$I_o = f(V_{in}) = \frac{1}{2}(f(V_{in}) + f(V_{-in})) + \frac{1}{2}(f(V_{in}) - f(V_{-in})) \quad (3.21)$$
Figure 3.27: Transfer function (\(I_d \text{ vs } V_{gs}\)) plot. The small-signal behaviour is the region between X and Y whereas the large-signal behaviour is beyond Z

where

\[
\frac{1}{2} (f(V_{in}) + f(V_{-in})) = I_{dc} + I_2 V^2_{in} + I_4 V^4_{in} + \ldots \\
\frac{1}{2} (f(V_{in}) - f(V_{-in})) = I_1 V_{in} + I_3 V^3_{in} + \ldots.
\]

The even part of transfer function generates even order IMDs and harmonic frequency contents which can be filtered by a tank whereas odd part creates in-band IMDs which cannot be filtered. The effect of \(C_{gs}\) nonlinearity is prominent in frequencies greater than current gain cutoff frequency of \(f_t\). The nonlinearity in gate (i.e. input capacitance) produces distortion in the gate voltage waveform. The charge stored by this nonlinear input capacitance \(C_{gs}\) is

\[
Q = q_o + q_1 V + q_2 V^2 + q_3 V^3 + \ldots.
\]

Then the gate current is

\[
i = \frac{\partial Q}{\partial t} = q_1 \frac{\partial V}{\partial t} + 2q_2 V \frac{\partial Q}{\partial t} + 3q_3 V^2 \frac{\partial Q}{\partial t}
\]

Since capacitance is given as

\[
C(V) = \frac{\partial Q}{\partial V} = q_1 + 2q_2 V + 3q_3 V^2 + \ldots = c_o + c_1 V + c_2 V^2 + \ldots.
\]
Then the gate current is
\[ i = c_0 \frac{\partial V}{\partial t} + c_1 V \frac{\partial V}{\partial t} + c_2 V^2 \frac{\partial V}{\partial t} \ldots = C(V) \frac{\partial V}{\partial t} \] (3.27)

Equating the above equations suggests that even order terms contribute to IMDs. Thus for zero IMD the \( C_{gs,even} \) must be zero.

\[ C_{gs,even} = c_2 V^2 + c_4 V^4 + \ldots \] (3.28)
\[ = \left( \frac{1}{2} \right) \left( C_{gs}(V_{in}) + C_{gs}(-V_{in}) \right) - C_0 \] (3.29)

For MOSFETS \( C_{gs}(V_{gs}) \) has almost even symmetry about threshold voltage \( (V_{th}) \) as shown in Fig. 3.28 [9]. So, in theory class-B operation must produce zero IMD as shown in Fig. 3.29. Common drain amplifier offers better linearity due to inherent negative feedback nature. The transfer function for common source at class-B or above bias is
\[ \frac{\partial V_{out}}{\partial V_{in}} = -R_L g_m(V_{gs}) \] (3.30)

variation in \( g_m \) directly effects the overall transfer function. The transfer function of common drain amplifier is
\[ \frac{\partial V_{out}}{\partial V_{in}} = \frac{R_L g_m(V_{gs})}{1 + R_L g_m(V_{gs})} \] (3.31)

As \( g_m \) is increased as compared to the conductance of the load (i.e \( g_m R_L \gg 1 \)), the effect of transconductance variation \( g_m(V_{gs}) \) on the amplifier gain is mitigated. The 100% negative feedback from the gate to the source linearises the amplifier. The class-B mode of operation offers better IMD\(_3\) suppression for both common drain and common source configuration. This is shown in Fig. 3.35, Fig. 3.36, Fig 3.43 and Fig. 3.44. The common drain configuration offers 30 dBc of IMD\(_3\) rejection while common source has 21 dBc of IMD\(_3\) rejection at 3 dB power backoff as shown in Fig. 3.45 from the \( P_{1-dB} \). Thus, for common drain amplifier, 11 dBc of additional IMD\(_3\) suppression is obtained. This is due to strong negative feedback which linearises the amplifier and compensates the variations in nonlinear \( C_{gs} \) which is the major cause of IMD\(_3\).
3.10 Conclusions

In this chapter, two single-ended designs of common drain and common source RF power amplifiers are presented in UMC 90 nm CMOS technology. The common drain configuration achieves a maximum linear gain of 6 dB and peak PAE of 43 % while the common source configuration has maximum linear gain of 10.3 dB and peak PAE of 54 %. The serious stability issue of common drain amplifier is compensated by a lossy RC network which ensures unconditional stability at the cost of gain. The common source amplifier on the other hand has stability problems at low frequencies and the parallel RC network provides the required stability without effecting the power gain at higher frequencies considerably. The class-B mode of operation offers better IMD\textsubscript{3} suppression for both common drain and common source configuration. The common drain configuration offers 30 dBc of IMD\textsubscript{3} rejection while common source has 21 dBc rejection.

Figure 3.28: MOSFET $C_{gs}$ variation as a function of gate voltage [9].

Figure 3.29: Bias design for class-B amplifier (a) $I_d$ vs $V_{gs}$ nonlinearity (b) The even part (without $C_0$) of $C_{gs}$ characteristic [3].

3.10 Conclusions
Figure 3.30: IMD$_3$ power spectrum at $P_{in} = 17$ dBm for common drain class-B PA. The two tones are placed at 2.5501 GHz and 2.5502 GHz. The intermodulation products at $2f_1 - f_2$ and $2f_2 - f_1$ are at 2.55 GHz and 2.5503 GHz respectively.

Figure 3.31: Fundamental output power at 2.55 GHz vs IMD$_3$ power at 2.5503 GHz using two tone test for common drain class-B with bias voltage of $V_g = 0.56$ V. The sweet spot is near to the compression of IMD$_3$ rejection at 3-dB power backoff. Thus, for common drain amplifier, 11 dBc of additional IMD$_3$ suppression is obtained. This is due to strong negative feedback which linearizes the amplifier and rejects the variations in nonlinear $C_{gs}$ which is the major cause of IMD$_3$. 
3.10 Conclusions

Figure 3.32: Fundamental output power at 2.55 GHz vs IMD$_3$ power at 2.5503 GHz using two tone test for common drain class-A with bias voltage of $V_g = 1.2$ V. The sweet spot is away from the compression.

Figure 3.33: Fundamental output power at 2.55 GHz vs IMD$_3$ power at 2.5503 GHz using two tone test for common drain class-AB with bias voltage of $V_g = 0.7$ V with a flat region of low IMD$_3$ power level.
Figure 3.34: Fundamental output power at 2.55GHz vs IMD3 power at 2.5503 GHz using two tone test for common drain class-C with bias voltage of $V_g = 0.2$ V. Note the increase in IMD3 slope for lower input power levels and a sweet spot near compression.

Figure 3.35: IMD3 suppression vs input power of class-A, class-B, class-AB and class C mode of operation for common drain amplifier. Class-B offers better IMD3 suppression over a wide input power range.
3.10 Conclusions

Figure 3.36: IMD\textsubscript{3} suppression vs output power of class-A, class-B, class-AB and class-C mode of operation for common drain amplifier. Class-B offers better IMD\textsubscript{3} suppression over a wide output power range.

Figure 3.37: Fundamental output power at 2.55 GHz vs IMD\textsubscript{3} power at 2.5503 GHz using two tone test for common source class-A with bias voltage of $V_g = 1.2$ V. The sweet spot is away from the compression.
3 Single-Ended Class-B RF Power Amplifier

Figure 3.38: Fundamental output power at 2.55 GHz vs IMD3 power at 2.5503 GHz using two tone test for common source class-B with bias voltage of $V_g = 0.5$ V. The sweet spot is near to the compression as compared to that shown in Fig. 3.37. Note the disappearance of possible sweet spot at lower input power levels as one shown in Fig. 3.39.

Figure 3.39: Fundamental output power at 2.55 GHz vs IMD3 power at 2.5503 GHz using two tone test for common source class-AB with bias voltage of $V_g = 0.56$ V. Another possible sweet spot at lower input power levels.
3.10 Conclusions

Figure 3.40: Fundamental output power at 2.55 GHz vs IMD\textsubscript{3} power at 2.5503 GHz using two tone test for common source class-AB with bias voltage of $V_g = 0.7$ V with a flat region of low IMD\textsubscript{3} power level.

Figure 3.41: Fundamental output power at 2.55 GHz vs IMD\textsubscript{3} power at 2.5503 GHz using two tone test for common source class-C with bias voltage of $V_g = 0.2$ V. Note the 5 dB/dec slope and the sweet spot near compression.
Figure 3.42: IMD$_3$ power spectrum at $P_{in} = 14$ dBm for common source class-B PA. The two tones are placed at 2.5501 GHz and 2.5502 GHz. The intermodulation products at $2f_1 - f_2$ and $2f_2 - f_1$ are at 2.55 GHz and 2.5503 GHz respectively.

Figure 3.43: IMD$_3$ suppression vs input power of class-A, class-B, class-AB and class C mode of operation for common source amplifier.
3.10 Conclusions

Figure 3.44: IMD3 suppression vs output power of class-A, class-B, class-AB and class-C mode of operation for common source amplifier. Class-A IMD3 suppression is better at lower output power range.

Figure 3.45: IMD3 suppression vs output power for common drain and common source in class-B operation.
3 Single-Ended Class-B RF Power Amplifier
4 Differential Common Drain Class-B RF Power Amplifier

4.1 Introduction

In this chapter, the differential version of common drain class-B RF power amplifiers is presented. The transition from single-ended to differential and the issues related to load network design for common drain configuration are discussed. The chapter concludes with a final version of an off-chip load transformation network.

4.2 Differential Design of Common Drain Class-B RF PA

Most of the integrated circuits operate in differential configuration as it rejects common-mode noise and it offers additional 3 dB of output power. Differential configuration can be obtained in the following ways:

1. Using transformer
2. Using LC-balun

Different load networks using the above topologies are presented in the next section.

4.2.1 Differential Design Using Transformer

In a differential design of a PA, two identical single-ended designs are connected through one-to-one transformer on the input side. This transformer acts as a 3 dB combiner at its output which is connected to 50 Ω load, while it converts differential signal to single-ended output. This topology can be utilised more efficiently if the inductor in
the L-matching network is realised through bond-wire and the rest (i.e. capacitor and transformer) forms an off-chip load network as shown in Fig. 4.1. The disadvantage of this network is additional components required for the load network. The time domain source voltage and source current waveforms are shown in Fig. 4.2 and Fig. 4.3 respectively. The performance results of Type-1 network are shown in Fig. 4.4.

Figure 4.1: Differential common drain class-B amplifier using two single ended amplifiers connected through one-to-one transformers (Type-1).

An efficient way to design a differential amplifier is to use transformer for both impedance transformation and differential to single-ended conversion as shown in Fig. 4.5. This topology is suitable for full on-chip integration of load network and does not require tank circuit for harmonic suppression. However, integrated transformers have a complex model and are quite lossy. The time-domain source voltage and source current waveforms are shown in Fig. 4.6 and Fig. 4.7 respectively. The performance results of Type-2 network are shown in Fig. 4.9. For single-stage common drain amplifiers, this design is not recommended but this design offers best even harmonic rejection as shown in Fig. 4.8.
4.2 Differential Design of Common Drain Class-B RF PA

Figure 4.2: Time-domain source voltage waveform for amplifier at $P_{in} = 17$ dBm (Type-1).

Figure 4.3: Time-domain source current waveform for amplifier at $P_{in} = 17$ dBm (Type-1).

4.2.2 Differential Design Using LC-balun

Another way to achieve impedance transformation as well as differential to single-ended conversion is to use lattice type LC-balun [23]. The LC-balun is a cross-coupled network of inductors and capacitors which produce precisely $\pm 90^\circ$ phase shift.

At the frequency of operation $f_0$,

$$\omega = 2\pi f_0 \quad \text{and} \quad Z_c = \sqrt{R_i R_L}$$  \hfill (4.1)
4 Differential Common Drain Class-B RF Power Amplifier

Figure 4.4: Power gain, drain efficiency and power added efficiency plots for differential common drain class-B PA (Type-1).

\[ L_m = \frac{Z_c}{\omega} ; \quad C_m = \frac{1}{\omega Z_c} \] (4.2)

Figure 4.5: Differential common drain amplifier with transformer (Type-2).
4.2 Differential Design of Common Drain Class-B RF PA

Figure 4.6: Time-domain source voltage waveform for amplifier at $P_{\text{in}} = 20$ dBm (Type-2).

Figure 4.7: Time-domain source voltage waveform for amplifier at $P_{\text{in}} = 20$ dBm (Type-2).

The schematic of lattice LC-balun is shown in Fig. 4.10. The tank circuit is also used to suppress the harmonics as the lattice LC-balun has low network quality factor as shown in Fig. 4.11. The time-domain voltage and current waveforms are shown in Fig. 4.12 and Fig. 4.13, respectively. The performance results of Type-3 network are shown in Fig. 4.14. The tank circuit is inconvenient due to large value of capacitor. So, to provide the necessary harmonic conditions of the load; the tank is replaced by a 2nd harmonic trap as illustrated in the Fig. 4.15. As the 2nd harmonic is most important to determine PA performance and for practical purposes,
4 Differential Common Drain Class-B RF Power Amplifier

Figure 4.8: Harmonic spectrum for amplifier in Fig. 4.5 (Type-2).

Figure 4.9: Power gain, drain efficiency and power added efficiency plots for differential common drain class-B PA (Type-2).

only a second harmonic short is provided.

The advantage of using a harmonic trap is that the component values are small as compared to parallel tank. The inductor $L_m$, is realised off-chip as bond wires can replace inductors while the capacitor is an off-chip component. For practical purposes, it is only possible to provide 2\textsuperscript{nd} harmonic termination since the capacitances for harmonics higher than 2\textsuperscript{nd} harmonic are comparable with the pad capacitances (usually of the order of 400 fF) which makes harmonic termination challenging. To provide a DC path, an extra RFC is also used in the upper branch. From the time-domain voltage and current waveforms, the higher order even harmonics like 4\textsuperscript{th}, 6\textsuperscript{th}, ..
and odd like $3^{rd}$, $5^{th}$, .. imparts significant nonlinearity to the waveforms as shown in Fig. 4.16 and Fig. 4.17. The performance results of Type-4 network are shown in Fig. 4.18.

The final design consists of an off-chip harmonic termination as well as an off-chip balun. The finite quality factor ($Q_b$) of bond inductances is taken into account. The quality factor of inductor is given by:

$$Q_b = \frac{\omega L}{R}$$  \hspace{1cm} (4.3)

with bond inductance of 1 nH and quality factor ($Q_b$) equal to 20. (The quality factor of bond inductances is usually 30 or greater but here worst case scenario is assumed).

$$R = \frac{\omega L}{Q_b} = \frac{(2\pi)(2.55 \cdot 10^9)(1 \cdot 10^{-9})}{20} = 0.8 \ \Omega$$ \hspace{1cm} (4.4)

The harmonic suppression network is realised using section of transmission line in series with bond inductors. The schematic of the load network is shown in Fig. 4.20.

The harmonics are shorted by connecting three bond-wires to transmission line whose electrical length is slightly less than $\lambda/4$ at 2.55 GHz and this series network in total
acts as a $\lambda/4$ transformer. The capacitor $C_s$ is used to cancel the effect of the two bond wires connecting to balun. The transmission line section (as one shown in Fig. 4.19) is
4.2 Differential Design of Common Drain Class-B RF PA

Figure 4.13: Time domain source current waveform for amplifier at $P_{in} = 20$ dBm (Type-3).

Figure 4.14: Power gain, drain efficiency and power added efficiency plots for differential common drain class-B PA (Type-3).

designed in Agilent ADS LineCalc on a Rogers RF 5870 substrate, whose parameters are listed in Table 4.1. The calculated parameters are then used in analoglib Mtline component in Cadence SpectreRF. The response of the load network with corresponding impedances is shown in the Smith chart in Fig. 4.21. It can be seen that the even harmonics are fully shorted while odd harmonics are not. Finally, Fig. 4.22 shows the differential common drain class-B amplifier with an off-chip load transformation network (Type-5). For class-B operation, the even harmonics are of most interest as half-rectified current waveform is obtained due to shorting of even harmonics as shown
Figure 4.15: Differential common drain amplifier with balun and 2nd harmonic trap (Type-4).

Figure 4.16: Time domain source voltage waveform for amplifier at $P_{in} = 17$ dBm (Type-4).
4.2 Differential Design of Common Drain Class-B RF PA

Figure 4.17: Time domain source current waveform for amplifier at $P_{in} = 17$ dBm (Type-4).

Figure 4.18: Power gain, drain efficiency and power added efficiency plots for differential common drain class-B PA (Type-4).
in Fig. 4.24. The odd harmonics evident in voltage waveform half cycle in the form of a small step as shown in Fig. 4.23. The performance results of Type-5 network are shown in Fig. 4.25. This design offers a peak PAE of 29.6% with a gain of 4.6 dB. The $2^{nd}$ and $3^{rd}$ harmonic power are at -20.17 dBm and -23.13 dBm at an output power of 24.6 dBm. The IMD$_3$ suppression is at 31.07 dBc and 20.8 dBc at 3 dB and 6 dB output power backoff (BO). This design is chosen because it is a fully off-chip solution with reasonable gain and efficiency as well as ease of implementation.

![Microstrip transmission line](image)

Figure 4.19: Microstrip transmission line of dimensions $W \times L \times t_c$ on substrate with thickness $t_s$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Permittivity</td>
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</tr>
<tr>
<td>Substrate Thickness</td>
<td>.508 mm</td>
</tr>
<tr>
<td>Copper Thickness</td>
<td>35 $\mu$m</td>
</tr>
<tr>
<td>Conductivity</td>
<td>$5.8e7$ S.m$^{-1}$</td>
</tr>
<tr>
<td>Loss Tangent</td>
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</tr>
<tr>
<td>Signal Line Width</td>
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</tr>
<tr>
<td>Signal Line Length</td>
<td>19.393 mm</td>
</tr>
<tr>
<td>Signal Electrical Length</td>
<td>83 deg</td>
</tr>
<tr>
<td>Characteristic Impedance</td>
<td>50$\Omega$</td>
</tr>
</tbody>
</table>

Table 4.1: Transmission line parameters used in the final design (LTN Type-5).
4.3 Evaluation

In this chapter, different load networks for differential common drain class-B PA has been presented as summarised in Table 4.2 and Table 4.3. Broadly the load networks can be characterised into two sub-categories. The first category is a transformer based and the other is LC-balun based. The full transformer based load network, Type-2 (Fig. 4.5), offers perfect even order rejection with 2nd order harmonic power at -98 dBm at an input power of 20 dBm and a gain of 4.6 dB. The only disadvantage of this topology is that real integrated transformers are quite lossy which severely degrades PAE, gain and output power. Alternatively, we can use an off-chip transformer for differential to single-ended conversion while the tank circuit has to be realised on-chip whereas the inductor of the matching network can be realised through bond-wire. The load network utilising this topology shows a gain of around 6.4 dB and peak PAE of 35 % as given in Type-1 (Fig. 4.1) but this design is not selected as transformers are not used for impedance transformation and the number of components thus increases.

Figure 4.20: Off-chip load network setup (Type-5) for S-parameter simulation $Q_{bond} = 20$. 
Transformerless designs utilize the LC-balun network for impedance transformation and differential to single-ended conversion. In this case, the harmonic network can be a single 2\textsuperscript{nd} harmonic trap via a bond wire and an off-chip capacitor or an on-chip harmonic tank circuit operating at \( f_0 \) can also be used. The balun-tank network, Type-3 (Fig. 4.11) gives a gain of 5.4 dB with a peak PAE of 38 \%. This is a fully on-chip solution. The off-chip harmonic network and on-chip impedance transformation network is given by Type-4 (Fig. 4.15). This network gives a peak PAE of 42 \% and a gain of 4.16 dB. In this network the balun is on-chip and harmonic suppression network is highly susceptible to component variations. Also, significant nonlinearity is evident in the voltage waveform of this network as shown in Fig. 4.16. So, this network is not selected. A better approach is to make the harmonic network independent of component variations as well as to get maximum gain and efficiency. Thus, a load network of Type-5 (Fig. 4.22) is selected, which is a full off-chip solution. This network is made by utilizing transmission lines in series with bond-wires. This fully off-chip solution offers a reasonable peak PAE of 29 \%. The 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonics stands at -20 dBm and -23 dBm at the output power of 24.6 dBm with a gain of 4 dB. The IMD\textsubscript{3} suppression is 31 dBC at 3 dB backoff from \( P_{1dB} \) with the peak PAE of
27%. The IMD$_3$ null occurs around input power levels of 22.5 dBm and a flat region of low IMD$_3$ is evident around 0 dBm as shown in Fig. 4.27. The component values...
of this network are given in Table. 4.4 and Table. 4.5. The other reason for using an off-chip LTN is the fact that there is no single stable CMOS common drain RF power amplifier in literature. As per author knowledge, only one stable common drain RF power amplifier (but in GaN technology) has been reported (simulation results only) \[3\]. Another author \[11\] had stability issues and the technology used was InGaP. Keeping these factors in mind, it was decided to make the load network off-chip.

\[1\] simulation results taking into account bond-wire resistance of 0.8 Ω.
4.3 Evaluation

Figure 4.26: Harmonic spectrum for amplifier in Fig. 4.22 (Type-5).

Figure 4.27: Fundamental output power vs IMD₃ power with two tones at 100 KHz spacing for amplifier in Fig. 4.22 (Type-5).
4 Differential Common Drain Class-B RF Power Amplifier

<table>
<thead>
<tr>
<th></th>
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<tr>
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<td>35.25</td>
<td>6.4</td>
<td>19.2</td>
<td>30.46</td>
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<td>-36.4</td>
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<td>2</td>
<td>40.6</td>
<td>4.6</td>
<td>37.7</td>
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<td>24.6</td>
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<td>-16.4</td>
<td>36</td>
<td>37</td>
</tr>
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<td>3</td>
<td>38</td>
<td>5.46</td>
<td>19.5</td>
<td>31.5</td>
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<td>-1.91</td>
<td>-19.56</td>
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<td>34.5</td>
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<td>4</td>
<td>42</td>
<td>4.16</td>
<td>23.7</td>
<td>31.4</td>
<td>24.09</td>
<td>-58</td>
<td>-12</td>
<td>25.4</td>
<td>35.9</td>
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<td>5</td>
<td>29.6</td>
<td>4.6</td>
<td>18.45</td>
<td>30.07</td>
<td>24.6</td>
<td>-20.17</td>
<td>-23.13</td>
<td>31.07</td>
<td>20.8</td>
</tr>
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</table>

Table 4.2: Differential common drain class-B power amplifier performance using different load networks (P_in = 20 dBm).

<table>
<thead>
<tr>
<th>LTN Type</th>
<th>Remarks</th>
<th>Figure</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>Tank + L-Match + Transformer</td>
<td>4.1</td>
</tr>
<tr>
<td>2</td>
<td>Transformer</td>
<td>4.5</td>
</tr>
<tr>
<td>3</td>
<td>Tank + Balun</td>
<td>4.11</td>
</tr>
<tr>
<td>4</td>
<td>Trap + Balun</td>
<td>4.15</td>
</tr>
<tr>
<td>5</td>
<td>Transmission Line + Balun</td>
<td>4.22</td>
</tr>
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</table>

Table 4.3: Different load networks for differential common drain class-B PA.

<table>
<thead>
<tr>
<th>LTN Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lm</td>
<td>1 nH</td>
</tr>
<tr>
<td>Cm</td>
<td>3.88 pF</td>
</tr>
<tr>
<td>L_bonds</td>
<td>1 nH x 5</td>
</tr>
<tr>
<td>Cs</td>
<td>8 pF</td>
</tr>
</tbody>
</table>

Table 4.4: Load transformation network’s component values for PA (Type-5).
4.3 Evaluation

Table 4.5: Input and stability network’s component values for PA (Type-5).

<table>
<thead>
<tr>
<th>Input &amp; Stability Components</th>
<th>Value</th>
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<tbody>
<tr>
<td>$L_{in}$</td>
<td>3.3 nH</td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>1.58 pF</td>
</tr>
<tr>
<td>$C_s$</td>
<td>3.7 pF</td>
</tr>
<tr>
<td>$R_s$</td>
<td>2.7 $\Omega$</td>
</tr>
<tr>
<td>$L_g$</td>
<td>1 nH</td>
</tr>
<tr>
<td>RFC</td>
<td>3 nH</td>
</tr>
<tr>
<td>$C_{byp}$</td>
<td>47 pF</td>
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</table>
5 Design in 150 nm CMOS

5.1 Introduction

The major goal of the thesis was to design the common drain class-B amplifier using UMC 90 nm technology, but due to an abrupt increase in the tape-out cost and budget issues, the design has to be converted to Landshut Foundry (LF) 150 nm. The simulation results and the corresponding waveforms for single-ended and differential (as the ones shown in Fig. 3.17 and Fig. 4.22, respectively) are mapped onto LF 150 nm, the and results are presented in this chapter.

5.2 Simulation Results

The amplifier presented here is designed for 26 dBm output power. Components from the process library are used for input matching and stability. The supply voltage is 3.3 V and the bias voltage is 0.7 V. The $R_{opt}$ is determined through DC loadline and its value is 12.3 Ω. The device size and the performance parameters for single-ended as well as differential version is given in Table. 5.1 to Table. 5.4. The issues with this technology is the low transconductance ($g_m$) of the transistors and limited number of inductors availability. The single-ended and differential designs have maximum gain of 1 dB. The peak PAE is around 10%. The time-domain source voltage and current waveforms as well as performance plots for single-ended and differential versions are shown from Fig. 5.1 to Fig. 5.5.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Device</th>
<th>Width [μm]</th>
<th>Length [nm]</th>
<th>Multiplier</th>
<th>Fingers</th>
<th>Size [mm]</th>
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<td>L-Foundry</td>
<td>NMOS-RF-3i-3</td>
<td>97</td>
<td>350</td>
<td>8</td>
<td>16</td>
<td>1.94</td>
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Table 5.1: Device Features.
Table 5.2: Performance parameters for single-ended common drain class-B RF power amplifier ($P_{in} = 17$ dBm).

<table>
<thead>
<tr>
<th>Pin [dBm]</th>
<th>$P_{1dB}$ [dBm]</th>
<th>$I_{out}$ [mA]</th>
<th>$V_{out}$ [V]</th>
<th>PAE [%]</th>
<th>$\eta$ [%]</th>
<th>G [dB]</th>
<th>$IP_3$ [dBm]</th>
<th>$P_{1dB}$ [dBm]</th>
<th>$P_{f0}$ [dBm]</th>
<th>$P_{2f0}$ [dBm]</th>
<th>$P_{3f0}$ [dBm]</th>
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<tr>
<td>17</td>
<td>25.5</td>
<td>213</td>
<td>1.2</td>
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<td>56</td>
<td>1</td>
<td>1.218</td>
<td>25</td>
<td>18.2</td>
<td>-19.5</td>
<td>-57.3</td>
</tr>
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</table>

Table 5.3: S-parameters at fundamental frequency of 2.55 GHz while $K_{min}$ is at 2.6 GHz for single-ended common drain class-B RF power amplifier.

<table>
<thead>
<tr>
<th>$S_{11}$ [dB]</th>
<th>$S_{12}$ [dB]</th>
<th>$S_{21}$ [dB]</th>
<th>$S_{22}$ [dB]</th>
<th>$K_{min}$ [dB]</th>
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<td>-23</td>
<td>-130</td>
<td>1.2</td>
<td>-9.1</td>
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Table 5.4: Differential common drain class-B power amplifier performance parameters.

<table>
<thead>
<tr>
<th>LTN Type</th>
<th>PAE [%]</th>
<th>$\eta$ [%]</th>
<th>Gain [dB]</th>
<th>$IP_3$ [dBm]</th>
<th>$P_{1dB}$ [dBm]</th>
<th>$P_{f0}$ [dBm]</th>
<th>$P_{2f0}$ [dBm]</th>
<th>$P_{3f0}$ [dBm]</th>
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<td>1</td>
<td>19.5</td>
<td>29.5</td>
<td>21</td>
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<td>-29</td>
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</table>

Figure 5.1: Time-domain source voltage and source current waveforms for single ended common drain amplifier class-B PA.
5.2 Simulation Results

Figure 5.2: Time-domain source voltage waveforms for differential design.

Figure 5.3: Time-domain source current waveforms for differential design.
Figure 5.4: Output power, gain, PAE and drain efficiency for the single-ended design.

Figure 5.5: Output power, gain, PAE and drain efficiency for the differential design.
6 Conclusion

6.1 Summary

In this thesis, single-ended as well as differential common drain class-B power amplifiers have been presented. The technology employed is UMC 90 nm and L-Foundry 150 nm CMOS technology. The frequency of operation is 2.55 GHz which is in the LTE frequency band (2.5-2.7 GHz). The single-ended design employ harmonic terminations through tank network and impedance transformation via L-matching network provides a gain of 6 dB and peak PAE of 43 %. The same load network connected to common source configuration gives peak PAE of 54 % and gain of 10.3 dB. The lower gain in common drain is due to the fact that this configuration offers only current gain whereas the common source offers both current and voltage gain. The common drain amplifier is unstable across a wide frequency range due to nonlinear gate-source capacitance $C_{gs}$. Another contributing factor for further lowering of gain in common drain configuration is the RC stability network which presents a low impedance at high frequencies resulting in shorting of significant input RF power to ground. The common source amplifier, on the other hand, has serious stability problems at lower frequency due to its large power gain (both current and voltage). Thus, by providing a positive resistance at low frequencies solve this low frequency stability problem. The effect of Miller capacitance ($C_{gd}$, which can cause high frequency instability) is reduced by putting a series capacitor at the gate of the device. The stability network for common source amplifier consists of parallel RC network placed in series at the gate of the device. Thus, the loss of RF power due to stability network in common source amplifier is lower. It has been shown that class-B mode of operation offers good linearity in terms of third order intermodulation distortion rejection and by operating the amplifier in common drain configuration further enhances the linearity due to inherent series-series negative feedback as compared to common source. The common drain
amplifier offers 11 dBc extra IMD3 rejection as compared to the common source at 3 dB output power backoff from \( P_{1dB} \). Different patterns of intermodulation distortion have been mathematically analyzed for class-A, class-B, class-AB and class-C mode of operation. Finally, different load networks for differential common drain configuration have been presented. The final selected load network consists of bond wires, transmission line and lattice LC-balun. The maximum gain for the differential version with full off-chip load network is 4.6 dB and peak PAE of around 29% in the UMC 90 nm CMOS technology. The bond wire quality factor has been chosen to be 20. The results for single-ended as well as differential in L-Foundry 150 nm have also been presented. This technology does not seem to be suitable for RF PAs as gain of just 1 dB and peak PAE of 12 % is achieved.

### 6.2 Future Work

This thesis work has lot of scope for further research. A few of them are given below:

1. All the power amplifiers (whether linear or nonlinear) are used in common source configuration which results in significant nonlinearity. To overcome this, complicated techniques are used. If one is willing to sacrifice some gain, then common drain amplifier offers high linearity and also it does not suffers from oxide break down (reliability issue).

2. To enhance the gain, a two stage amplifier is the candidate of choice. One solution can be a cascode stage driving a common drain amplifier with proper inter-stage matching.
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