KTH Information and Communication Technology

Application of SiGe(C) in high performance MOSFETs and infrared detectors

Doctoral Thesis
By
Mohammadreza Kolahdouz Esfahani
Stockholm, Sweden
2011

Department of Integrated Device and Circuits
School of Information and Communication Technology (ICT)
KTH (Royal Institute of Technology)

Cover illustration:
Top: Cross section of SiGe epitaxial layers inside 100nm source/drain.
Bottom: The final view of the IR detectors (without measurement pads).

Application of SiGe(C) in high performance MOSFETs and Infrared detectors

A dissertation submitted to Kungliga Tekniska Högskolan (KTH, Royal Institute of Technology), Stockholm, Sweden, in partial fulfillment of the requirements for the degree of Teknologie Doktor (Doctor of Philosophy).

TRITA-ICT/MAP AVH Report 2011:02
ISSN 1653-7610
ISRN KTH/ICT-MAP/AVH-2011:02-SE
ISBN 978-91-7415-865-6

This thesis is available in electronic version at: http://media.lib.kth.se
Printed by Kista Snabbtryck AB

Mohammadreza Kolahdouz Esfahani, Application of SiGe(C) in high performance MOSFETs and Infrared detectors
Integrated Devices and Circuits (IDAC), School of Information and Communication Technology (ICT), KTH (Royal Institute of Technology), Stockholm, Sweden
TRITA-ICT/MAP AVH Report 2011:02, ISSN 1653-7610, ISRN KTH/ICT-MAP/AVH-2011:02-SE

ABSTRACT

Epitaxially grown SiGe(C) materials have a great importance for many device applications. In these applications, (strained or relaxed) SiGe(C) layers are grown either selectively on the active areas, or on the entire wafer. Epitaxy is a sensitive step in the device processing and choosing an appropriate thermal budget is crucial to avoid the dopant out–diffusion and strain relaxation. Strain is important for bandgap engineering in (SiGe/Si) heterostructures, and to increase the mobility of the carriers. An example for the latter application is implementing SiGe as the biaxially strained channel layer or in recessed source/drain (S/D) of pMOSFETs. For this case, SiGe is grown selectively in recessed S/D regions where the Si channel region experiences uniaxial strain.

The main focus of this Ph.D. thesis is on developing the first empirical model for selective epitaxial growth of SiGe using SiH_2Cl_2, GeH_4 and HCl precursors in a reduced pressure chemical vapor deposition (RPCVD) reactor. The model describes the growth kinetics and considers the contribution of each gas precursor in the gas–phase and surface reactions. In this way, the growth rate and Ge content of the SiGe layers grown on the patterned substrates can be calculated. The gas flow and temperature distribution were simulated in the CVD reactor and the results were exerted as input parameters for the diffusion of gas molecules through gas boundaries. Fick's law and the Langmuir isotherm theory (in non–equilibrium case) have been applied to estimate the real flow of impinging molecules. For a patterned substrate, the interactions between the chips were calculated using an established interaction theory. Overall, a good agreement between this model and the experimental data has been presented. This work provides, for the first time, a guideline for chip manufacturers who are implementing SiGe layers in the devices.

The other focus of this thesis is to implement SiGe layers or dots as a thermistor material to detect infrared radiation. The result provides a fundamental understanding of noise sources and thermal response of SiGe/Si multilayer structures. Temperature coefficient of resistance (TCR) and noise voltage have been measured for different detector prototypes in terms of pixel size and multilayer designs. The performance of such structures was studied and optimized as a function of quantum well and Si barrier thickness (or dot size), number of periods in the SiGe/Si stack, Ge content and contact resistance. Both electrical and thermal responses of such detectors were sensitive to the quality of the epitaxial layers which was evaluated by the interfacial roughness and strain amount. The strain in SiGe material was carefully controlled in the meta–stable region by implementing

carbon in multi quantum wells (MQWs) of SiGe(C)/Si(C). A state of the art thermistor material with TCR of 4.5 %/K for 100×100 μm^2 pixel area and low noise constant ($K_{1/f}$) value of 4.4×10^{-15} is presented. The outstanding performance of these devices is due to Ni silicide contacts, smooth interfaces, and high quality of multi quantum wells (MQWs) containing high Ge content.

The novel idea of generating local strain using Ge multi quantum dots structures has also been studied. Ge dots were deposited at different growth temperatures in order to tune the intermixing of Si into Ge. The structures demonstrated a noise constant of 2×10^{-9} and TCR of 3.44%/K for pixel area of 70×70 μm^2. These structures displayed an improvement in the TCR value compared to quantum well structures; however, strain relaxation and unevenness of the multi layer structures caused low signal–to–noise ratio. In this thesis, the physical importance of different design parameters of IR detectors has been quantified by using a statistical analysis. The factorial method has been applied to evaluate design parameters for IR detection improvements. Among design parameters, increasing the Ge content of SiGe quantum wells has the most significant effect on the measured TCR value.

Keywords: Silicon Germanium Carbon (SiGeC), Reduced Pressure Chemical Vapor Deposition (RPCVD), Epitaxy, Pattern Dependency, MOSFET, Mobility, bolometer, Quantum Well, Infrared (IR) Detection, Ni Silicide, High Resolution X-ray Diffraction (HRXRD), High Resolution Scanning Electron Microscopy (HRSEM)

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PREFACE

This doctoral thesis describes research work carried out in the department of Integrated Devices and Circuits at the Microelectronics and Applied Physics (MAP) in the School of Information and Communication Technology (ICT) at KTH (Royal Institute of Technology). The thesis contains an introduction and the following appended papers.

List of appended papers:

1. *Selective Epitaxial Growth with Full Control of Pattern Dependency Behavior for pMOSFET Structures*
   M. Kolahdouz, J. Hållstedt, M. Östling, R. Wise, and H. H. Radamson, Journal of the Electrochemical Society, Volume 156, Issue 3, Pages H169-H171, January (2009).

2. *Comprehensive Evaluation and Study of Pattern Dependency Behavior in Selective Epitaxial Growth of B-Doped SiGe Layers*
   M. Kolahdouz, J. Hållstedt, A. Khatibi, R. Wise and H. H. Radamson, IEEE Transactions on Nanotechnology, Volume 8, Issue 3, Pages 291-297, May (2009).

3. *New method to calibrate the pattern dependency of selective epitaxy of SiGe layers*
   M. Kolahdouz, J. Hållstedt, M. Östling, D. Riley, R. Wise and H. H. Radamson, Solid-State Electronics, Volume 53, Issue 8, Pages 858-861 August (2009).

4. *Selective Growth of B- and C-Doped SiGe Layers in Unprocessed and Recessed Si Openings for p-type Metal-Oxide-Semiconductor Field-Effect Transistors Application*
   M. Kolahdouz, P. Tabib Zadeh Adibi, A. Afshar Farniya, S. Shayestehaminzadeh, E. Trybom, L. Di Benedetto, and H. H. Radamson; Journal of The Electrochemical Society, Volume 157, Issue 6, Pages H633-H637 January (2010).

5. *Kinetic model of SiGe selective epitaxial growth using RPCVD technique*
   M. Kolahdouz, L. Maresca, R. Ghandi, A. Khatibi and H. H. Radamson, Journal of The Electrochemical Society, 158 (4) H457-H464 (2011).

6. *Improvement of infrared detection using Ge quantum dots multilayer structure*
   M. Kolahdouz, A. Afshar Farniya, L. Di Benedetto, M. Östling and H. H. Radamson, Applied Physics Letter, Volume 96, Issue 21, Page 213516 May (2010).

7. *Carbon-doped single-crystalline SiGe/Si thermistor with high temperature coefficient of resistance and low noise level*
   H. H. Radamson, **M. Kolahdouz**, S. Shayestehaminzadeh, A. Afshar Farniya, and S. Wissmar, Applied Physics Letter, Volume 97, Issue 23, Page 223507 December (2010).

8. *The performance improvement evaluation for SiGe-based IR detectors*
M. Kolahdouz, A. Afshar Farniya, M. Östling, H. H. Radamson, *Solid-State Electronics*, In Press, Corrected Proof, Available online 12 February 2011.

Related contributions not included in the thesis:

Journal papers:

9. J. Hållstedt, R. Ghandi, **M. Kolahdouz**, M. Östling and H. H. Radamson, "Integration of HCl chemical vapour etching and SiGe:B selective epitaxy for source/drain application in MOSFETs" Semicond. Sci. Technol. Volume 22, Pages S123–S126 (2007).

10. R. Ghandi, **M. Kolahdouz**, J. Hållstedt, Jun Lu, R. Wise, H. Wejtmans, M. Östling and H. H. Radamson, "High boron incorporation in selective epitaxial growth of SiGe layers" Journal of Materials Science: Materials in Electronics, Volume 18, Issue 7, Pages 747-751(5), July (2007).

11. **M. Kolahdouz**, R. Ghandi, J. Hållstedt, R. Wise, H. Wejtmans, and H. H. Radamson, "The influence of Si coverage in a chip on layer profile of selectively grown $Si_{1-x}Ge_x$ layers using RPCVD technique" Thin Solid Films, Volume 517, Issue 1, 3, Pages 257-258, November (2008).

12. R. Ghandi, **M. Kolahdouz**, J. Hållstedt, R. Wise, H. Wejtmans, and H. H. Radamson, "Effect of strain, substrate surface and growth rate on B-doping in selectively grown SiGe layers" Thin Solid Films, Volume 517, Issue 1, 3, Pages 334-336, November (2008).

13. H. H. Radamson, **M. Kolahdouz**, R. Ghandi, and J. Hållstedt, "Selective epitaxial growth of B-doped SiGe and HCl etch of Si for the formation of SiGe:B recessed sources and drains (pMOS transistors)" Thin Solid Films, Volume 517, Issue 1, 3, Pages 84-86, November (2008).

14. J. Hållstedt, **M. Kolahdouz**, R. Ghandi, R. Wise, J. W. Wejtmans and H. H. Radamson, "Pattern dependency in selective epitaxy of B-doped SiGe layers for advanced metal oxide semiconductor field effect transistors" Journal of Applied Physics, Volume 103, Issue 5, Pages 0549071-7 (2008).

15. H. H. Radamson, **M. Kolahdouz**, R. Ghandi, and M. Östling, "High strain amount in recessed junctions induced by selectively deposited boron-doped SiGe layers" Materials Science and Engineering: B, Volumes 154-155, Pages 106-109, 5 December (2008).

16. J. Y. Andersson, P. Ericsson, H. H. Radamson, S. G. E. Wissmar, **M. Kolahdouz,** "SiGe/Si quantum structures as a thermistor material for low cost IR microbolometer focal plane" Solid-State Electronics, In Press, Corrected Proof, Available online 10 March 2011.

Conference papers:

17. **M. Kolahdouz**, J. Hållstedt, M. Östling, D. Riley, R. Wise and H. H. Radamson," New method to calibrate the pattern dependency of selective epitaxy of SiGe layers", ISTDM conference (2008)

18. **M. Kolahdouz**, R. Ghandi, J. Hållstedt, R Wise, H. Wejtmans, and H. H. Radamson, "The influence of Si coverage in a chip on layer profile of selectively grown $Si_{1-x}Ge_x$ layers using RPCVD technique", ICSI conference (2007)

19. R. Ghandi, **M. Kolahdouz**, J. Hållstedt, R. Wise, H. Wejtmans, and H. H. Radamson, "Effect of

strain, substrate surface and growth rate on B-doping in selectively grown SiGe layers", ICSI conference (2007)

20. H. H. Radamson, **M. Kolahdouz**, R. Ghandi, and J. Hållstedt, "Selective epitaxial growth of B-doped SiGe and HCl etch of Si for the formation of SiGe:B recessed sources and drains (pMOS transistors)", ICSI conference (2007)

21. **M. Kolahdouz**, J. Hållstedt, M. Östling, D. Riley, R. Wise and H. H. Radamson," HCl in-situ etching of Si prior to and during the epitaxial growth of SiGe using RPCVD", ISTDM conference (2008)

22. S. G. E. Wissmar, **M. Kolahdouz**, Y. Yamamoto, B. Tillack, C. Vieider, J. Y. Andersson and H. H. Radamson, "Monocrystalline SiGe for high-performance uncooled thermistor", ISDRS conference (2007)

23. **M. Kolahdouz**, J. Hållstedt, M. Östling, R. Wise and H. H. Radamson, "Selective Epitaxial Growth with Full Control of Pattern Dependency Behavior for pMOSFET Structures", ECS conference (2008)

24. H. H. Radamson, **M. Kolahdouz**, R. Ghandi, and M. Östling, "High strain amount in recessed junctions induced by selectively deposited B-doped SiGe layers", EMRS conference (2008)

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27. **M. Kolahdouz**, P. Tabib Zadeh Adibi, A. Afshar Farniya, E. Trybom, L. Di Benedetto, M. Shayestehaminzadeh and H. H. Radamson; "Selective growth of B- and C-doped SiGe layers in unprocessed and recessed Si openings for pMOSFET application" 216th Electrochemical society meeting Vienna (2009)

28. L. Di Benedetto, **M. Kolahdouz**, B. G. Malm, M. Östling and H. H. Radamson; "Strain balance approach for optimized signal-to-noise ratio in SiGe quantum well bolometers" oral presentation for ESSDERC 2009 and ESSDERC proceeding (2009).

29. B. G. Malm, **M. Kolahdouz**, H. H. Radamson, M. Östling; "Comprehensive Temperature Modeling of Strained Epitaxial Silicon-Germanium Alloy Thermistors" ISDRS 2009.

30. Z. Kolahdouz Esfahani, S. Mohajerzadeh, **M. Kolahdouz**, J. Koohsorkhi, H. H. Radamson, "Substrate Engineering for Ni-assisted Growth of Carbon Nano-Tubes" ISTDM 2010

31. J. Y. Andersson, S. G. E. Wissmar, **M. Kolahdouz**, H. H. Radamson, "SiGe quantum structures development for low cost IR" invited talk in ISTDM 2010, Stockholm, Sweden.

32. S. Shayestehaminzadeh, **M. Kolahdouz**, R. Wise and H. H. Radamson, "Critical Oxygen and Moisture Levels for Defect-free Si and SiGe Epitaxial layers grown at Low Temperature for BiCMOS Applications" ISTDM 2010, Stockholm, Sweden. (awarded the poster prize)

33. S. G. E. Wissmar, A. Afshar Farniya, **M. Kolahdouz**, H. H. Radamson, "Strain Engineering Using Ge-based Quantum Structure Design" ISTDM 2010, Stockholm, Sweden.

34. **M. Kolahdouz**, L. Maresca, R. Ghandi, A. Khatibi, H. H. Radamson, "Kinetic model of SiGe selective epitaxial growth using RPCVD technique" oral presentation in 218th Electrochemical society meeting Las Vegas (2010).

35. **M. Kolahdouz**, A. Afshar Farniya, M. Östling, and H. H. Radamson, "Improving the performance of SiGe-based IR detectors" in 218th meeting of the Electrochemical society, Las Vegas (2010).

Chapter book:

36. **M. Kolahdouz**, H. Radamson, R. Ghandi, "B-doped SiGe(C) materials for high performance devices" in the book "Boron: Compounds, Production and Applications." with Nova Science Publishers, Inc (in proof, to be published in 2011).

SUMMARY OF APPENDED PAPERS

Paper 1: Selective Epitaxial Growth with Full Control of Pattern Dependency Behavior for pMOSFET Structures

This article presents the pattern dependency of selective epitaxy and ways to control it in order to obtain uniform deposition of SiGe layers. It is shown that the exposed Si coverage of the chip is the main parameter in the mask layout which determines the layer profile. The SiGe layer profile uniformity was achieved over a wide range of device sizes by optimized process parameters in combination with chips design consisting of dummy features causing uniform gas depletion over the chips of the wafer.

The author of this thesis performed wafer processing, epitaxy growth, and material characterization. He also analyzed the results and wrote the manuscript.

Paper 2: Comprehensive Evaluation and Study of Pattern Dependency Behavior in Selective Epitaxial Growth of B-Doped SiGe Layers

This work focuses on the influence of chip layout and architecture on the pattern dependency of selective epitaxy of B-doped SiGe layers. The variations of Ge–, B–content, and growth rate have been investigated. The results are described by the gas depletion theory. The interaction among chips on a patterned substrate during the epitaxy has been studied. The influence of any individual chip on neighboring chips is additive within the radius of depletion volume. It is shown that using thicker oxide in the pattern lowers Ge content but had no significant influence on the growth rate. The impact of oxide thickness originates from less heat conduction for thicker oxides that impacts the kinetics of gases over the chip.

The author performed the wafer processing, CVD growth and a major part of the material characterization and the manuscript writing.

Paper 3: New method to calibrate the pattern dependency of selective epitaxy of SiGe layers

A comprehensive study on the interaction between chips on a wafer was presented. The results are explained by kinetic gas theory for CVD techniques. A test pattern was designed with a series of chips to study the pattern dependency. The layer profile of the test pattern was later linked to the profile on fully–patterned wafers. An empirical model was developed to estimate the Ge content on substrates with a fully–patterned design.

The author of this thesis performed the major part of the wafer processing, modeling and material characterization. The author also wrote the manuscript.

Paper 4: Selective Growth of B– and C–Doped SiGe Layers in Unprocessed and Recessed Si Openings for p–type Metal–Oxide–Semiconductor Field–Effect Transistors Application

This work presents the pattern dependency of the selective epitaxial growth of boron– and carbon–doped SiGe layers in recessed and unprocessed openings. It is shown that the layer profile is dependent on deposition time, chip layout, and growth parameters. Carbon and boron doping compensates the strain in SiGe layers, and when both dopants are introduced, the strain reduction is additive. In this article, the incorporation of boron and carbon in the SiGe matrix is found to be a competitive action. The concentration of carbon decreases, whereas the boron amount increases in SiGe layers with increasing the Ge content. In recessed openings, the Ge content is independent of the recess depth. The strain amount in the grown layers is graded vertically, which is due to the fact that the thickness of the epilayers exceeding the critical thickness.

The author of this thesis performed almost wafer processing and material characterization and wrote the manuscript.

Paper 5: Kinetic model of SiGe selective epitaxial growth using RPCVD technique

In this study, a detailed empirical model for dichlorosilane (DCS)–based selective epitaxy growth of SiGe has been developed to predict the layer profile using a reduced pressure CVD reactor. The model considers each gas precursor contributions from the gas–phase and the surface. The gas flow and temperature distribution were simulated in the CVD reactor and the results were exerted as input parameters for Maxwell energy distribution. The diffusion of molecules from the gas boundaries was calculated by Fick's law and the Langmuir isotherm theory (in non–equilibrium case) was applied to analyze the surface. The pattern dependency of the selective growth was also modeled through an interaction theory between different subdivisions of the chips. Overall, a good agreement between the kinetic model and the experimental data were obtained.

The author contributed in a major part of the modeling, processing and material characterization and wrote the manuscript.

Paper 6: Improvement of infrared detection using Ge quantum dots multilayer structure

In this study, mono–crystalline SiGe/Si multi–quantum dot and well structures have been presented as thermistor materials for infrared detection. The main goal of making such prototypes was to create high strain using Ge dots. However, due to the intermixing of Si into the Ge at the growth temperature, Ge dots are not pure Ge and are in fact SiGe (the growth temperature of 600–650 C). As a result, the strain relaxation occurred which degrades signal–to–noise ratio and TCR values. The performance of the devices (both thermal and electrical) has been very sensitive to the quality of the epitaxial layers which is evaluated by the interfacial roughness and strain amount. This study demonstrates that the devices containing quantum dots have higher thermal coefficient of resistance (TCR) 3.4%/K with a noise constant ($K_{1/f}$) value of 2×10^{-9}.

The author of this thesis took a major part in all stages of the investigation from idea, experiments, electrical and processing characterization and wrote the manuscript.

Paper 7: Carbon-doped single-crystalline SiGe/Si thermistor with high temperature coefficient of resistance and low noise level

This article investigates SiGe(C)/Si(C) multi–quantum wells as a thermistor material for future bolometers. The structures demonstrated temperature coefficient of resistance (TCR) value of 4.5%/K for 100×100 μm^2 pixel sizes and low noise constant ($K_{1/f}$) value of 4.4×10^{-15}. The outstanding performance of the devices is due to Ni silicide contacts, smooth interfaces, and high quality multi–quantum wells containing high Ge content.

The author performed the wafer processing, CVD growth and the material characterization. The author took part in the manuscript writing.

Paper 8: The performance improvement evaluation for SiGe-based IR detectors

In this study, the effect of Ge content, pixel size and the Ni silicide on the performance of SiGe/Si thermistor material have been presented. The noise level was decreased by more than one order of magnitude when the Ni silicide layer was integrated below the metal contacts. The presence of Ni silicide slightly improved TCR values for the detectors (+0.22%/K). However, the Ge content had the most significant effect on the TCR. A statistical analysis (factorial method) was applied to evaluate the effect of each parameter. Using this method, it was realized that decreasing the pixel size would enhance the TCR value.

The author of the thesis suggested this study and performed the device processing. The author also performed most of the electrical characterization and wrote the manuscript.

ACKNOWLEDGEMENTS

I received my Master of Applied Science degree in Electrical Engineering from the Royal Institute of Technology in March 2007 and was eager to continue as a Ph.D. student in the attracting field of the device technology. This thesis summarizes my four years work as a Ph.D. student at Integrated Devices and Circuits department. I am very thankful to everyone who supported me, and made it possible to complete my project effectively and moreover on time.

I would like to thank Doc. Henry Radamson not only as my supervisor but also as an older brother who helped me find my way through the world of science and patiently taught me many valuable things one needs to know in order to be a part of his research group. Besides his experience and knowledge in semiconductor laboratory, he supported me morally and guided me in different situations. He has been very kind and patient while suggesting the outlines of this project and correcting my doubts.

I would like to thank Prof. Mikael Östling who accepted me as a Ph.D. student in the MAP department and also for his ideas, guidance, support and encouragement throughout this thesis work.

Dr. Julius Hållstedt and Stanley Wissmar are particularly thanked for all valuable cooperation, fruitful discussions and assistance in the lab. Special thanks to Reza Ghandi for being a generous and kind friend, companion and colleague through the journey we have taken together since 1989. I have always found him by my side whenever I needed any kind of support.

Also many thanks to all the people in the MAP group for providing a nice working atmosphere. Furthermore, I must acknowledge all who have provided answers to my questions and have helped me in the clean room. To mention some; Prof. Carl-Mikael Zetterling, Prof. Anders Hallen, Prof. Mattias Hammar, Dr. Gunnar Malm, Dr. Per-Erik Hellström, Dr. Margareta Linarsson, Dr. Yong-Bin Wang, Dr. Max Lemme, Dr. JianTong Li, Christian Ridder, Benedetto Buono (specially for the Italian coffee), Luca Maresca, Valur Gudmundsson, Luigia Lanni, Oscar Gustafsson, Muhammad Usman, Timo Söderqvist, Cecilia Aronson, Reza Nikpars, Gunnar Andersson and Sven Valerio for clean room assistance and Gunilla Gabrielson for administrative matters.

My co-workers in our epitaxy group during these years; Ali Khatibi, Luca Maresca, Luigi Di Benedetto, Erik Trybom, Pooya Tabib Zadeh Adibi, Ali Afshar

Farniya, Mohammad Shayestehaminzadeh, Arash Salemi and Mahdi Moeen are specially thanked for valuable cooperation and discussions.

I owe a special thanks to Dr. Rick Wise and Dr. Deborah Rilley in Texas Instruments for the discussions and financial support through the SRC program.

Last but not least, I would like to thank my parents and my beloved wife who in spite of their busy schedules have helped me consistently in every ways they could. I know that I can't retrieve a piece of their irrecoverable helps and pains; therefore, I dedicate this thesis to them.

Thank you all

Mohammadreza Kolahdouz Esfahani
Stockholm, March 2011

ACRONYMS AND SYMBOLS

AFM	Atomic Force Microscopy
B	Boron
B_2H_6	Diborane
BJT	Bipolar Junction Transistor
C	Carbon
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
D	Drain
FET	Field Effect Transistor
Ge	Germanium
GeH_4	Germane
HCl	Hydrogen Chloride
HBT	Heterojunction Bipolar Transistor
HH	Heavy Hole
HRXRD	High-Resolution X-Ray Diffraction
HRRLM	High-Resolution Reciprocal Lattice Mapping
HRSEM	High-Resolution Scanning Electron Microscopy
LH	Light Hole
MB	Matthew and Blakeslee theory
MBE	Molecular Beam Epitaxy
MFC	Mass Flow Controller
MOS	Metal Oxide Semiconductor
MOSFET Transistor	Metal Oxide Semiconductor Field Effect
NSEG	Non-Selective Epitaxial Growth
PH_3	Phosphine
RPCVD	Reduced Pressure CVD
RTA	Rapid Thermal Annealing

SEG	Selective Epitaxial Growth
S	Source
Si	Silicon
$SiC/Si_{1-y}C_y$	Silicon Carbon alloy (subscript ~ fraction of constituent)
$SiGe/Si_{1-x}Ge_x$	Silicon Germanium alloy (subscript ~ fraction of constituent)
$SiGeC/Si_{1-x-y}Ge_xC_y$	Silicon Germanium Carbon alloy (subscript ~ fraction of constituent)
SiH_3CH_3	Methylsilane
SiH_4	Silane
SIMS	Secondary Ion Mass Spectrometry
SOI	Silicon On Insulator
sSi	Strained Silicon
TED	Transient enhanced diffusion
TEM	Transmission Electron Microscopy
XRD	X-Ray Diffraction
XTEM	Cross-section Transmission Electron Microscopy
c	Exposed Si coverage
E_C	Minimum of conduction band energy
E_g	Bandgap
E_V	Maximum of valence band energy
f	Lattice mismatch
$f_{x,y}$	Lattice mismatch parallel to surface
f_z	Lattice mismatch perpendicular to surface
k_B	Boltzmann's constant
m^*	Effective mass
N_{Sub}	Doping concentration in substrate
n_i	Intrinsic carrier concentration
R	Relaxation
R_s	Sheet resistance
t_{ox}	Oxide thickness

$\varepsilon_{x,y}$	Strain perpendicular to surface
ε_{z}	Strain parallel to surface
μ	Carrier mobility
σ	Stress
P_{B2H6}	Partial pressure of diborane
P_{DCS}	Partial pressure of dichlorosilane
P_{GeH4}	Partial pressure of germane
P_{SiCH6}	Partial pressure of methylsilane
q	Elementary charge
R	Growth rate
T	Temperature
x	Ge content
ß	Tooling factor
λ	Interaction fraction
τ	Consumption length

CHAPTER 1

INTRODUCTION

Implementation of selective epitaxial growth (SEG) in recessed source and drain (S/D) junctions of the complementary metal–oxide–semiconductor (CMOS) structures has generated considerable interest in the device technology during the recent years. The practice of embedding SiGe:B films in p–channel MOS field–effect transistors (pMOSFETs) S/D regions increases carrier mobility by inducing uniaxial strain to the channel [1-5].

Although the uniaxial strain in S/D has demonstrated outstanding results in terms of mobility and threshold voltage, pattern dependency is still an issue for chips with nonuniform pattern densities. This means that in selective epitaxy growth, the profile of the deposited layer in different mask opening may differ from each other. A nonuniform deposition can also be observed from wafer to wafer when the mask type (oxide or nitride) or its thickness has been changed [6-16]. Many papers have presented a detailed study of pattern dependency and also proposed methods to improve the nonuniform growth, but eliminating this effect still remains a challenge [14,15,17,18]. Some of these reports show that the pattern dependency can be decreased (<5%) [14], but so far there is no remedy to totally eliminate this problem.

Some important goals in the p–channel transistor profile which can be affected by the pattern dependency issue are as follows: low sheet resistance in S/D junctions, high thermal stability of the contact silicide layers, considerable strain in the channel (25%–40%) and low dopant out–diffusion from S/D to the channel region [19]. The first two requirements can be achieved by high boron doping in SiGe epilayers. Because the presence of boron compensates the compressive strain in SiGe layers [20], a high level of both boron and germanium is necessary for such transistors. A remedy for the out–diffusion of boron in MOSFETs is to implement carbon in the S/D SiGe layers. Since the pattern dependency of the growth results in different doping profiles in the SiGe layers, having both carbon and boron in S/D regions complicates the device process.

A considerable number of experimental results have been published on the growth and integration of SiGe layers for different applications; meanwhile, remarkably fewer reports are available about the modeling of the growth [21-23]. This thesis introduces the first empirical model for the selective epitaxial growth of SiGe layers in a reduced pressure chemical vapor deposition (RPCVD) reactor. The model takes into account gas and surface kinetics and reactions for the growth rate and Ge composition calculation. Pattern dependency has also been evaluated through the modeling of gas consumption in a chip and the interaction between chips on the wafer. The presented model in its current form can be utilized in the manufacturing line to predict the pattern dependency and layer profile of CVD deposited layers. It is also capable of providing a 2D layer growth simulation for any provided pattern (deposition mask).

SiGe has been also utilized for different sensor applications. For example, SiGe/Si multilayer structure has been proposed as an outstanding thermistor material for infrared (IR) detection. Since the EU commission is investigating to legislate an anti–collision warning system for cars in the near future, research for a cheap thermistor material has been boosted. The evaluation parameters for a high

performance IR detector consist of high temperature coefficient of resistance (TCR) and high signal–to–noise ratio. Chapter 5 of this thesis reviews the existing group IV-based thermistor materials and the integration challenges. In this chapter, SiGe is presented as a new generation of low cost thermistor materials [24-28]. Today's materials include VOx, amorphous and polycrystalline semiconductors with TCR values in the range of 2%–4% and low/moderate signal–to–noise ratio [29-34]. Although the first generation of SiGe thermistor materials, based on multilayer quantum wells (MQWs), was presented a few years ago [25], so far none of these reports have been able to demonstrate TCR values above 4% as claimed earlier [35]. For these structures, high quality SiGe QWs with high Ge content are required to obtain high signal–to–noise ratio and high temperature response. However, the limited QW thickness due to the critical thickness is an obstacle for having more energy quantization levels in the QWs.

Our solution to this problem was to use Ge multilayer quantum dot (MQD) structures for the first time for IR detection. The other proposed solution for the growth limitations in this thesis is a MQW based on the strain–controlled SiGeC/SiC layers. The main idea is based on the formation of SiGe layers embedded in Si through the intermixing of Si into the Ge thin layers (grown by exposing the Si surface to GeH_4). The intermixing of Si and Ge can be controlled by the growth temperature and carbon doping in the Si layer [36]. In this way, high quality SiGe layers with high Ge content can be created. The formation of defects in this method is not favored since the diffusion of Si into Ge minimizes the lattice strain. Thus, growing Ge–delta layers at low temperature embedded in $Si_{1-y}C_y$ will be an ideal solution which has been applied for the first time to create state of the art SiGe(C) QWs for high performance IR detectors.

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CHAPTER 2

STRAIN

1. Introduction

Rapid scaling of complementary metal–oxide–semiconductor (CMOS) technology during the past 45 years has been enhancing the microprocessor performance, density and rapid nanotechnology revolution [1,2]. Previously, shrinking the transistor dimensions by classic Dennard scaling (i.e. scaling the dimensions by a factor (1/k)) was a successful approach to maintain the power density constant. However, recently due to material and process limitations, this technology has become less influential. Problems such as mobility degradation, threshold voltage roll-off, short channel effect (SCE) and high leakage current can be listed as the consequence of the classic scaling. During the recent years, classic scaling has been supplanted by application of performance boosters (such as strain and high-k metal gate) to overcome these issues. In this chapter, the incorporation of strained–silicon materials in MOSFETs to improve the mobility of electron and hole carriers will be discussed.

2. Strain engineering in MOSFETs

2.1. Mobility in an inversion layer

Mobility in silicon is proportional to the inverse scattering rate of the carriers with lattice phonons and ionized impurities. Generally, the mobility can simply be defined as:

$$\mu = \frac{q\tau}{m^*}$$

where τ is the average time between collisions, q is the electron charge and m* is the effective mass of the carriers. However, the mobility concept in the inversion layer of MOSFETs is different from the bulk mobility. As it is shown in Figure 2.1, the electrons are flowing with the electric field-dependent mobility in the channel of the transistor (y direction). As it is illustrated in the figure, the inversion layer thickness is not uniform in the x direction along the channel.

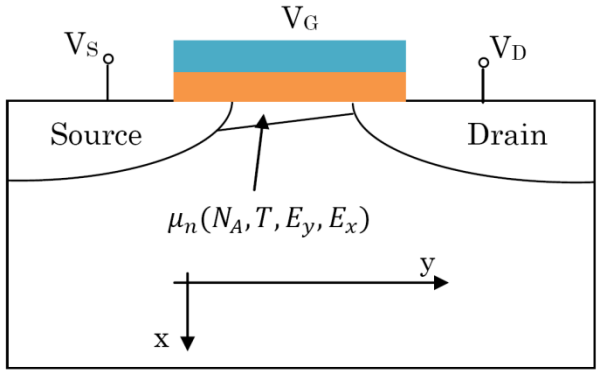

Figure 2.1 Schematic view of a nMOSFET

In MOSFETs, there are different scattering mechanisms which limit the mobility. Due to scattering with phonons (lattice vibrations), the mobility of carriers through channel depends on the temperature (T). Because of scattering with ionized impurities, it also depends on the doping density. The two-dimensional electric field (E_x and E_y) in the inversion layer also affects the carriers' mobility. Therefore, the mobility in the channel is a complicated subject which is not very easy to deal with.

2.2. Transport in the inversion layer

The physical explanation behind the transport for holes in bulk Si (or the inversion layer) is much more complicated than electrons due to the complexity of the valence band. Figure 2.2 illustrates the conduction band minima along six directions in the k-space. There are six equivalent ellipsoid p-orbitals in bulk silicon under low field which have similar transverse and longitudinal effective masses. Thus, 1/6 of the density of electrons in the conduction band is located in each ellipsoid. If the electrons move for instance in the x direction, two of the ellipsoids respond with a heavy longitudinal effective mass and four others respond with a light transverse effective mass. The conductivity effective mass can thus be given by:

$$m_c^* = \left(\frac{2}{6m_l^*} + \frac{4}{6m_t^*}\right)^{-1} = 0.26\, m_0$$

The dominant scattering processes in bulk silicon are acoustic phonons, ionized impurities and intervalley phonons. Due to low energy of acoustic phonons, scattering with these phonons in a valley will only move the electrons around within that valley. However, intervalley phonons have enough energy and momentum to move electrons from one valley to another.

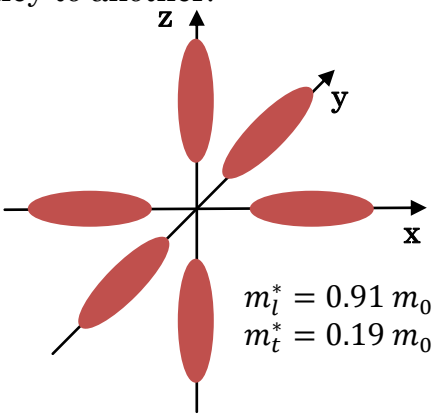

Figure 2.2 The six degenerate p-orbitals in bulk silicon under low field.

Nevertheless, the transport in MOSFETs is different from bulk silicon for several reasons. Due to the formation of an inversion layer, a potential well is formed near the oxide-silicon interface. As a result, the electrons are confined in the quantized energy states of the quantum well (see Figure 2.3b). If the confinement applies in the x direction, the electrons in the ellipsoids will respond to the quantum confinement with the effective mass in the same direction. As it can be seen in Figure 2.3a, the two blue ellipsoids are responding with heavy longitudinal effective

mass ($0.91m_0$) and they have a set of energy levels in the quantum well (blue dash lines in Figure 2.3b). The other four ellipsoids respond to the confinement with their transverse effective mass ($0.19m_0$) which means that they are much lighter than the electrons in the blue ellipsoids. Therefore, they have much higher energy levels in the quantum well than those of the two blue orbitals (primed energy levels in Figure 2.3b).

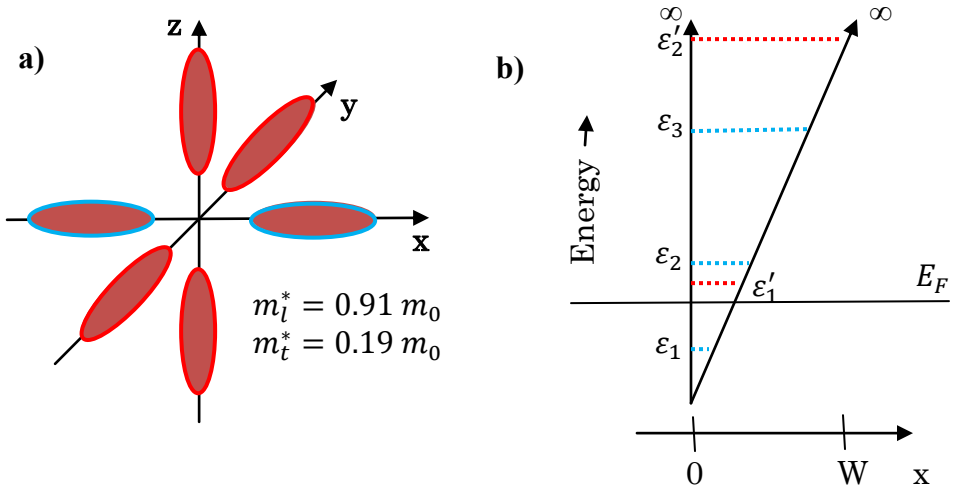

Figure 2.3 An illustration of a) six non-degenerate p-orbitals in nMOSFETs and b) the quantized energy states formed near the oxide and silicon interface.

Consequently, the six valleys are no longer equivalent. The lowest energy level belongs to blue orbitals. In typical working conditions of nMOSFETs, most of the electrons fill the blue valleys because they have the lowest energies. If in a MOSFET, x is the confinement direction then the y and z directions are the plane of the transistor. Therefore, most of the electrons have their light transverse effective mass in that plane. As a result, the electron mobility is higher than bulk silicon in this case and can be estimated by using the transverse effective mass ($0.19m_0$).

Since the six valleys are no longer degenerate, the intersubband scattering is suppressed. However, due to high concentration of electrons in the blue valleys, the electrons experience enhanced intra subband phonon scattering rate in these valleys.

The other important parameter which complicates the transport in MOSFETs, compared to bulk silicon, is the interface roughness between the oxide and the channel. This interface is atomically rough, and this leads to an increased scattering rate. Under low normal field condition (E_x in Figure 2.1), the mobility is dominated by the ionized impurity scattering. By increasing the normal field and attracting more inversion electrons, the number of carriers in the channel will suffice to screen out the ionized impurity charges. Thus, the dopant scattering becomes less important. As normal field increases, lattice scattering which is the interaction between electrons and phonons dominates, and drops the mobility modestly. Under high normal field, all the carriers are pulled towards the interface and the scattering rate dominates by the surface roughness scattering which drops the mobility significantly.

By considering the 45nm technology node and calculating the effective field from its typical profile at V_G=1V, E_{eff} ≈2MV/cm which is a pretty strong field. It is realized that the effective mobility is much lower than bulk silicon. This result had also been pointed out by Takagi et al. (see Figure 2.4) [3]. This can be explained by a very high surface roughness scattering rate.

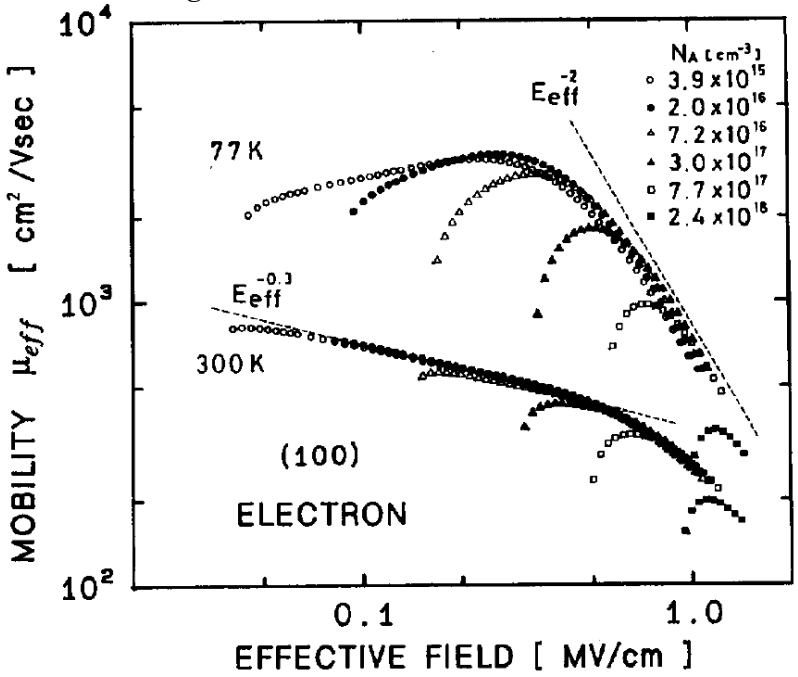

Figure 2.4 Electron mobility in the inversion layer at 300 K and 77 K versus effective field as a parameter of substrate acceptor concentration [3]

In each technology generation, according to the classic scaling, the oxide thickness must be decreased. In order to prevent SCE, the channel doping concentration must be increased. Together, these two processes increase the effective field which in turn lowers the mobility. This fact motivated researchers to look for other solutions to increase the mobility in MOSFETs. As a result of the efforts put into this field, today's technology is benefiting from strain engineering. It actually engineers the band structure of Si to obtain lighter effective mass or reduced scattering rate between valleys and, as a result higher mobility. Another approach to maintain scaling roadmap continual mobility enhancement is to fabricate the device channel in different orientations. But in this chapter, we only investigate the stress mobility enhancement in MOSFETs.

2.3. Mobility enhancement

As it is shown in Figure 2.5, strain contribution in mobility enhancement for the coming generations is increasing remarkably. There are four different techniques to apply strain to the Si channel of MOSFETs which are briefly summarized in this chapter.

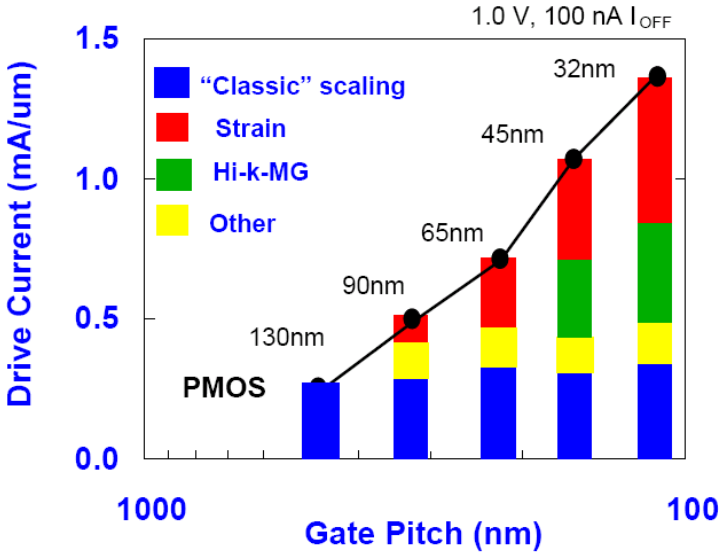

Figure 2.5 Importance of each performance booster in different technology nodes [2]

2.3.1. Biaxial strain through relaxed SiGe

The traditional approach for mobility enhancement was to introduce biaxial strain to both p- and nMOSFETs by growing strained Si on a relaxed SiGe layer (see Figure 2.6 [4]). But similar to any new process, it had integration challenges. Although it showed fairly good results for nMOSFETs, it could not maintain the improvement for hole mobility specially at large electric fields [5]. The latter drawback significantly dropped the manufacturers' interest in this approach for further transistor scaling.

In pMOSFETs, as the stress applied to the channel increases (i.e. increasing the Ge content in $Si_{1-x}Ge_x$), the mobility improves linearly. As shown in Figure 2.7, Strain induced band/subband energy shift, band warping and repopulation are the main reasons of this linear improvement [6]. The deteriorated mobility of hole carriers under high electric fields relates to the reduced separation between the light and heavy hole-like bands which increases the scattering rate.

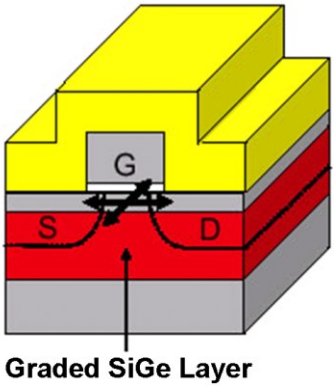

Figure 2.6 Traditional approach to introduce biaxial tensile strain.

However, the mechanism of electron mobility enhancement using biaxial strain is through splitting the six degenerate valleys. Under biaxial stress, the six degenerate

valleys split into two-fold and four-fold degenerate valleys. The two-fold low energy degenerate valleys respond with light transverse effective mass in the channel direction. The four-fold valleys have high energy which makes them less populated. As strain increases, the electrons experience additional repopulation of two-fold valleys and additional reduction in the intervalley scattering.

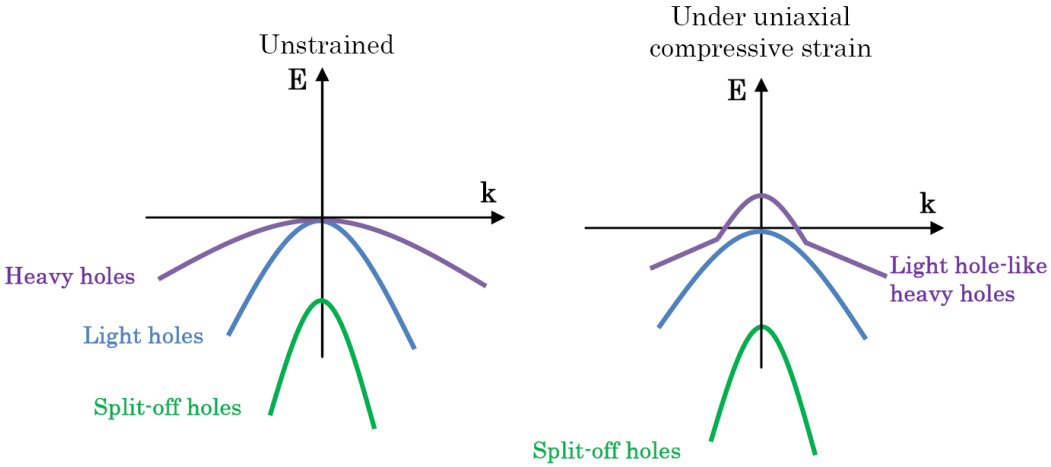

Figure 2.7 Valence band changes under uniaxial compressive strain in pMOSFETs

2.3.2. Uniaxial strain using embedded $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$

Facing near zero hole mobility enhancement for pMOSFETs using biaxial stress on one hand, and the strong improvement of uniaxial strain for pMOSFETs on the other, attracted attention towards integrating uniaxial strain for these devices.

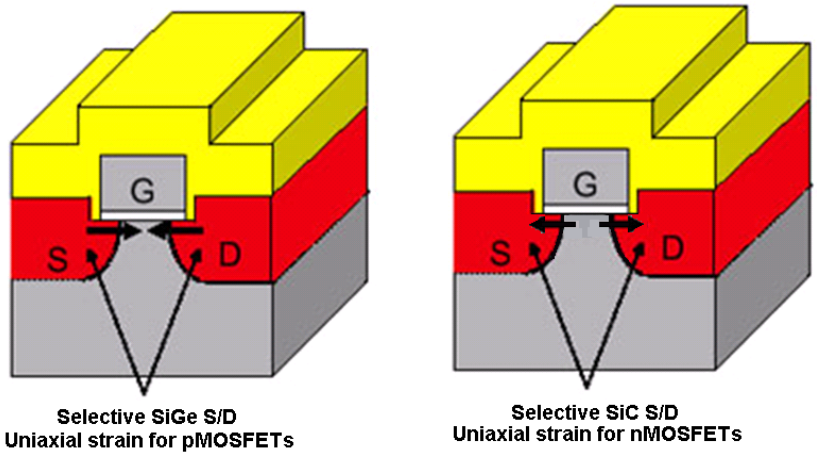

Figure 2.8 Application of uniaxial stressors for p- and nMOSFETs

Selective epitaxial growth of $S_{1-x}Ge_x$ or $Si_{1-y}C_y$ (Si:C) are two well-known processes to introduce uniaxial strain to the channel region. The grown layer in recessed source and drain of MOSFET has different lattice constant compared to the Si substrate. This mismatch of the lattice constants stresses the grown material biaxially and the channel uniaxially. This leads to mobility enhancement in the channel of the device.

Epitaxially grown SiGe or Si:C alloys are the typical stressor materials which have been integrated for this process (see Figure 2.8 [4]).
The longitudinal uniaxial compressive strain generates a remarkable lower in-plane conductivity effective mass compared to biaxial stress. By increasing the strain level, large energy band shift plays the important role in decreasing the intervalley scattering rate. In nMOSFET, the mobility enhancement mechanism of uniaxial strain is similar to that of biaxial strain.

2.3.3. Compressive and tensile stress liners

In this technique, the stress is introduced to the channel by deposition of nitride layers (stress liners) over the transistors' gate (as shown in Figure 2.9 [4]). The advantage of this technique is that this process is applicable for both n- and pMOSFETs. Therefore, these layers are also referred to as dual stress liners (DSL) and can be implemented after formation of the transistor structure. A brief description of the process flow is as follows: first, a compressive liner is deposited on the wafer which is removed selectively from the NMOS region. Then, the same process repeats for NMOS region but with a tensile stressor. The stress liners and embedded SiGe in the S/D can be integrated in the fabrication line to benefit from both techniques.

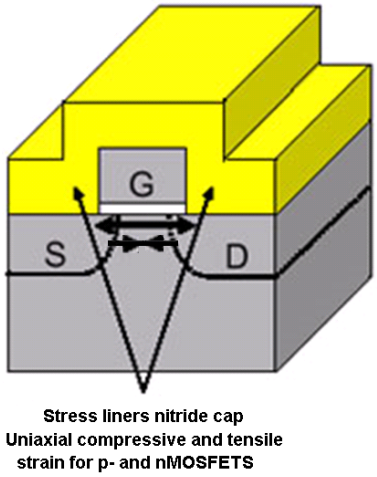

Figure 2.9 Application of stress liners for mobility enhancement in MOSFETs.

2.3.4. Stress memorization technique

This technique can generate additional tensile stress to the channel of nMOSFETs. This can simply be done by deposition of a stressed dielectric and subsequent thermal annealing. In the stress memorization technique, a highly tensile-stressed nitride layer is deposited selectively on the gate and will be removed after some annealing treatment steps. Basically, this nitride layer acts in a way that even after removal, the strain becomes locked in the polycrystalline gate. Thus, it continues to hold the channel under stress. That is why the silicon is said to have "memorized" the stress state.

3. Summary

In this chapter, strain effects on Si band structure, carrier mobility, effective mass and scattering mechanism were discussed. Strain can be introduced to the channel either uniaxially or biaxially. Uniaxial stress can be introduced by using embedded SiGe/SiC, dual stress liners or stress memorization technique. The results show that uniaxial tension/compression is the most promising configuration of n/pMOSFETs for operating under a high stress level. Biaxial stress is exerted by using a relaxed SiGe as the substrate for the strained Si channel layer.

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CHAPTER 3

PROCESSING

1. Introduction

A brief scope of different processing steps for manufacturing advanced CMOS and IR detectors are presented in this chapter. A focus has been made on epitaxy and lithography techniques.

2. Epitaxy

The epitaxial growth means that the bonding symmetry and periodicity of the substrate are replicated in the grown layer. Since any interruption of symmetry increases the potential energy of a crystal, epitaxial growth is energetically favorable and occurs spontaneously under certain conditions. CVD epitaxial growth consists of a number of process steps as are shown in Figure 3.1.

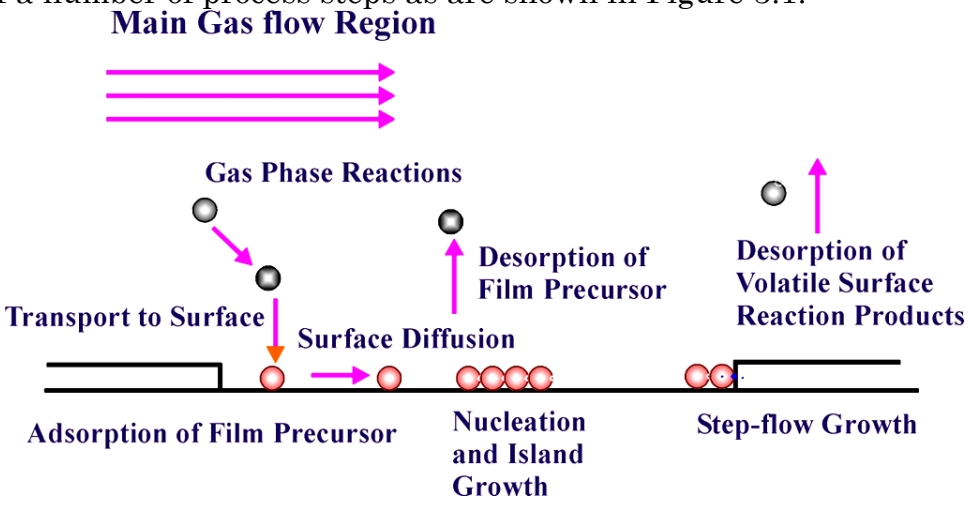

Figure 3.1 Schematic view of CVD process.

The gas precursors of the elements to be deposited are carried by an inert carrier gas (usually H_2). The gas molecules diffuse from the gas phase to the surface and adsorb on the surface. After being adsorbed, the species may diffuse to the surface, dissociate, incorporate, form nuclei on the surface or desorb to the gas phase. Additional phenomena can also occur; such as inter–diffusion (diffusion from surface to bulk) and segregation (diffusion from bulk to surface).

There are some major advantages of epitaxial growth compared to other techniques e.g. implantation or dopant diffusion. Not only, an abrupt doping profile with low defect density can be obtained, but also, epitaxy growth can be performed at low temperatures, which solves the out–diffusion problems.

There are epitaxy techniques such as molecular beam epitaxy (MBE) and pulsed laser deposition (PLD) which can only be used in research applications due to its low production rate. For industrial applications, however, chemical vapor deposition (CVD) has become the preferred technology. In this field reduced pressure CVD (RPCVD) provides a good trade–off between quality of the grown layer and deposition rate. By appropriate adjustment of the growth parameters, deposition

will only occur on selected Si areas of the patterned substrates. This operation is referred to as selective epitaxial growth (SEG). Otherwise, the normal operation is deposition on both oxide and Si areas which is so–called non–selective epitaxial growth (NSEG).

2.1. Non-selective & Selective Epitaxial Growth

As mentioned above, non–selective epitaxial growth (NSEG) is a deposition process where a film is deposited all over the whole substrate (see Figure 3.2b), independent of the fact that the exposed areas are single–crystalline, polycrystalline, or amorphous (e.g. oxide). However, the deposited film will only be single–crystalline if the exposed area has a single–crystalline structure, the deposition temperature is sufficiently high and the dopant concentration is not extremely high.
The polycrystalline film can be deposited on the oxide surface by using hydrogen–based Si sources. Furthermore, the thickness of the deposited single and polycrystalline films are not generally equal. For films deposited at higher pressure (usually higher than 30 torr), the polycrystalline film is normally significantly thicker than the single–crystalline film. However, by lowering the growth pressure the polycrystalline layer thickness becomes thinner and the difference vanishes totally at 20 torr.
Selective epitaxial growth (SEG) of Si or SiGe is a deposition process where the layer will only be deposited on exposed crystalline areas and not on oxide (or nitride) (see Figure 3.2c). This type of growth can be obtained by introducing HCl to the process gases in order to suppress the formation of nucleation sites on the oxide. However, the presence of HCl will also cause a low deposition rate for the single–crystalline silicon, thus it is preferable to apply high growth temperatures. Nevertheless, high temperature SEG results in defect–rich layers.

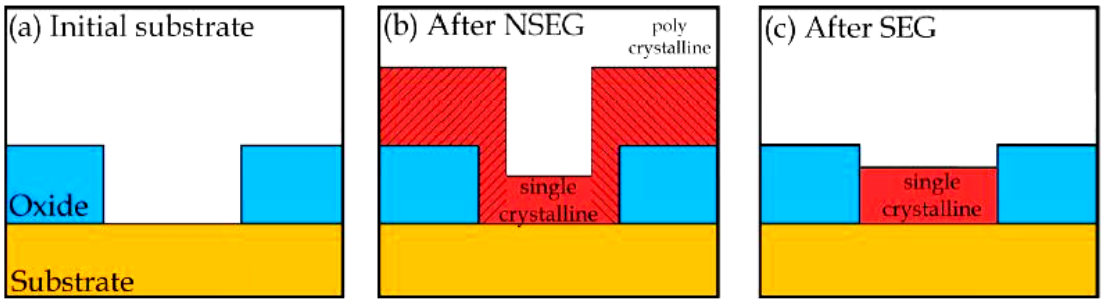

Figure 3.2 Schematic illustration of different deposition modes in a RPCVD reactor where (a) represents initial substrate before deposition, (b) represents substrate after a non-selective deposition, and (c) after a selective epitaxy growth.

Another problem regarding selective epitaxy is facet formation in the circumference of the oxide openings. These facets for Si substrate are (311) oriented and appear at early stage after deposition of few monolayer. During the epitaxy, the silicon atoms on the (311) planes have a longer diffusion length compared to atoms on (100) planes in the middle of the oxide openings. Consequently, the flow of atoms from the edges

towards the central part is established. Applying low temperature epitaxy causes a larger pile-up at the edges (especially in case of SiGe). Thus, a compromise growth temperature has to be taken to reduce the pile–up and achieve high quality material.

3. Lithography

3.1. Mask aligner, i-line and g-line stepper

The XLS 7500/2145 i-line stepper, DSW 8500/2035 g-line stepper and Mask aligner MA6/BA6 Karl Suss have been used to define different patterns employed in this work on the photoresist. This was achieved by exposing a thin polymer (i.e., photoresist) through a mask which has been designed for each individual project. The line width is defined by the exposure tool. A line width of 1 µm is routinely obtained by mask aligners, and i-line and g-line steppers offer line widths of down to 0.5 µm and an alignment accuracy of 90 nm.

3.2. Hole colloidal lithography (HCL)

Hole colloidal lithography (HCL) was used to fabricate the submicron pattern while the available projection lithography instruments were not able to achieve this goal. Uniformity all over the wafer and cheap process can be listed as the advantages of this lithography technique for creating nano–structures. The schematic view of HCL lithography is shown in Figure 3.3. In this figure, layers in yellow, orange and green are 12nm Ni, 50 nm SiO_2 and 15nm gold, respectively. Blue dots are polystyrene spheres which are removed by tape (see Figure 3.3c).

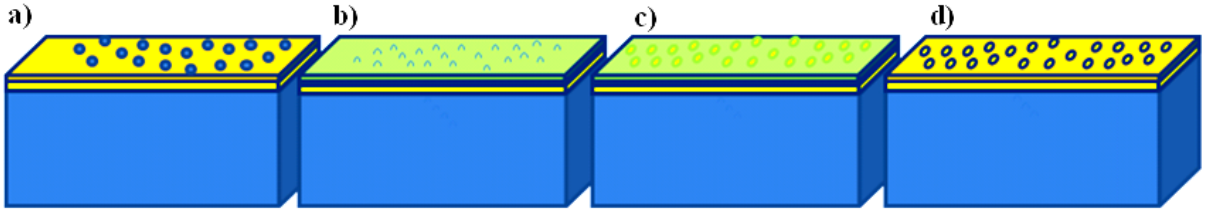

Figure 3.3 Schematic view of HCL process; a) spinning PMMA and spreading molecules on the oxide mask surface, b) Gold deposition on the surface, c) removing the molecules and the gold cover upon by tape and d) dry etch of the oxide mask through the openings.

4. Processing steps

In this section, a brief description of the process flow for manufacturing infrared (IR) detectors is presented. A reliable cleaning procedure is used in order to gain a high quality epitaxial layer because this process is very sensitive to contaminations. For *ex–situ* chemical cleaning, an oxidizing step in a mixture of H_2SO_4 and H_2O_2 (2.5L:1L) at 120°C for 5 min followed by 5% HF-dip for 10 sec is applied. Here in

between each step of cleaning, the wafers were rinsed for five minutes in N_2 bubbled DI H_2O. Finally the wafers are rinse–dried and inserted into the load locks. The *in–situ* cleaning consists of a 2 min bake at 1050°C in H_2 for blanket wafers and 5-20 min bake at 900–950°C for patterned substrates.

The thermistor materials, SiGe(C)/SiC stack, for IR detection were grown by RPCVD at 20 torr. The SiGe layer profiles are calibrated by using high-resolution x-ray diffraction (HRXRD). The growth parameters were optimized carefully to obtain high epitaxial quality with smooth/abrupt interface SiGe(C)/Si(C) multilayer structures. In these structures, two spacer layers are grown to avoid any auto–doping or thermal diffusion from the highly boron–doped contact layers to the active region of the detectors. The pixels were fabricated by optical lithography (see Figure 3.4b) and dry etching (see Figure 3.4c & 3.4d) with different shapes (squares and circles) and areas (200×200, 140×140, 100×100, 70×70, 50×50 and 25×25 μm^2). To form the pixels, CF_4, HBr, and Cl_2 gases were used to etch photoresist resolved areas (see Figure 3.4c).

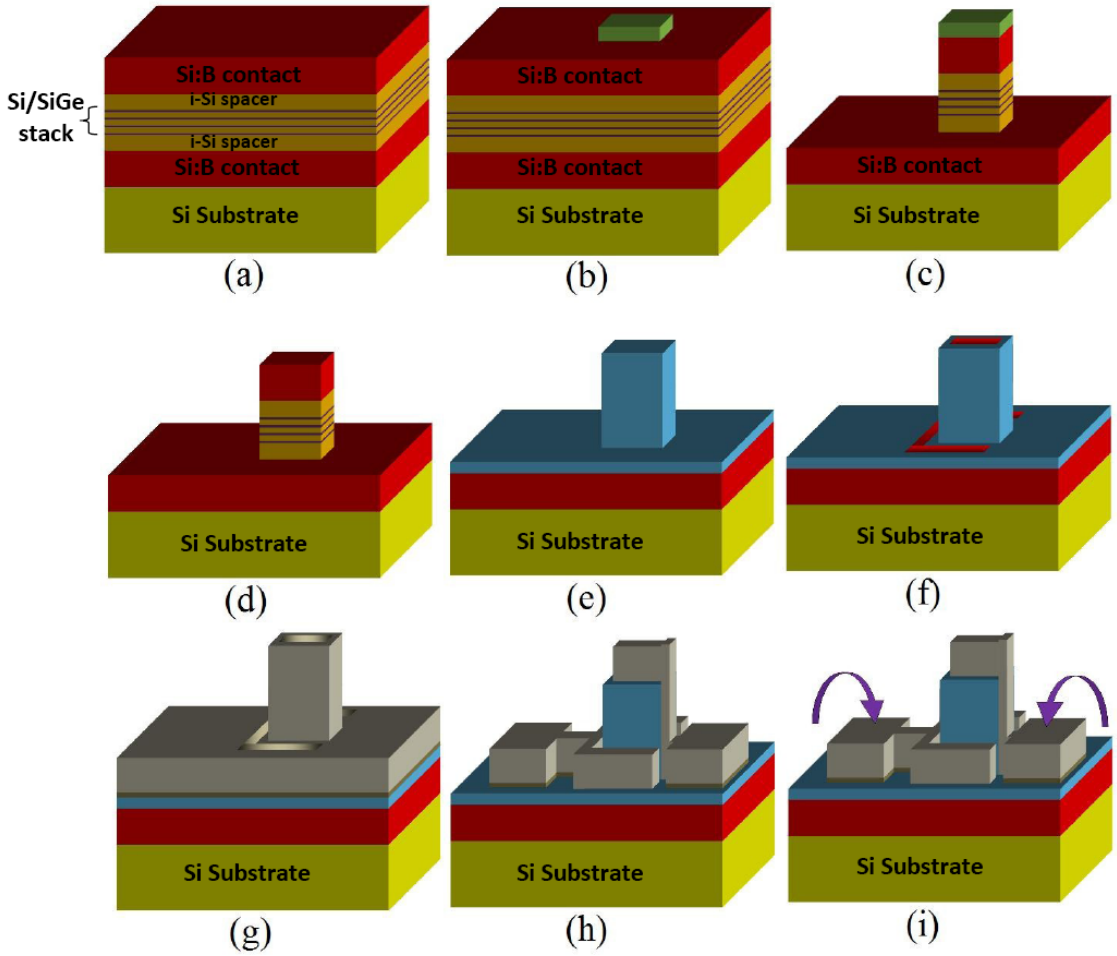

Figure 3.4 Device fabrication process flow: a) Deposition of epitaxial layers on cleaned Si wafers by RPCVD; b) Lithography; c) Dry etching of the mesa; d) Photoresist removal; e) Deposition of SiO_2 insulation layer; f) Lithography and dry etching of the contact; g) Ni silicidation and metal deposition; h) Lithography and dry etching of the contact pads; i) schematic illustration of where probes connect to the pads.

The standard oxide surface passivation (100nm SiO_2) is used as the thermal/electrical insulation layer of the device (see Figure 3.4e). This oxide layer isolates the contacts electrically and decreases the heat loss of the devices. The contact openings are fabricated using the second optical lithography and a dry etching step using CHF_3, CF_4 and Ar gases by reactive ion etching (RIE) (see Figure 3.4f). The Ni salicidation step was performed at 450 °C followed by TiW/Al metallization (see Figure 3.4g, 3.4h & 3.5). The metallization or Ni silicidation for the pixels have been performed on the highly B–doped top and bottom layers. Formal gas annealing is the final step of the process flow (H_2 anneal at 450°C for 30min).

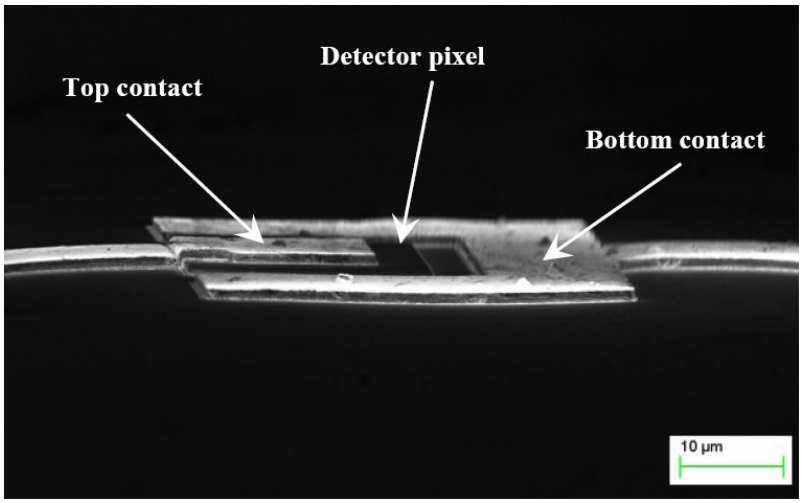

Figure 3.5 Final view of the device

For the modeling of the selective epitaxy growth of Si and SiGe, chips with different patterns were fabricated on the oxide mask. The exposed silicon coverage of these chips ranged from 0.01 to 37 % made from openings with different shapes and densities. The oxide openings in the pattern were formed by dry etching of the oxide mask of the wafers (100 to 400nm) using CHF_3, CF_4 and Ar gases. To form recessed openings CF_4, HBr, and Cl_2 gases were used to etch Si through the oxide mask. The epi–layers were grown at 625-725°C in the ASM 2000 RPCVD reactor with total pressure of 10–40 torr. Dichlorosilane (SiH_2Cl_2), 10% germane (GeH_4), 1% methylsilane (CH_3SiH_3) and 1% diborane (B_2H_6) in H_2 were used as Si, Ge, C and B precursors, respectively.

CHAPTER 4

KINETIC MODEL OF SIGE SELECTIVE EPITAXIAL GROWTH USING RPCVD

1. Introduction

SiGe epitaxy growth has attracted attention in both micro– [1-3] and opto–electronics due to its low cost and feasibility. Achieving a very high quality epitaxial SiGe is crucial for CMOS application. Tremendous experimental results have been presented on the growth and integration of SiGe layers for different applications, meanwhile, remarkably fewer reports are available about the modeling of the growth [4-6]. This point is highlighted when selective epitaxial growth (SEG) faces pattern dependency in which the SiGe layer profile is affected by the pattern layout [7-14]. During recent years, various methods have been proposed to decrease the pattern dependency in SEG of SiGe layers but an effective method which completely eliminates this problem has not yet been presented [14].
Bodnar et al. [7] suggested that increasing the HCl partial pressure can improve the uniformity of the growth. According to his group, the growth rate is dependent on the size of the opening. Figure 4.1 demonstrates that the Si deposition rate is independent of the window size. However, the SiGe growth rate without HCl increases strongly with decreasing the exposed window areas. This non–uniformity can be minimized by adding HCl to the gas mixture.

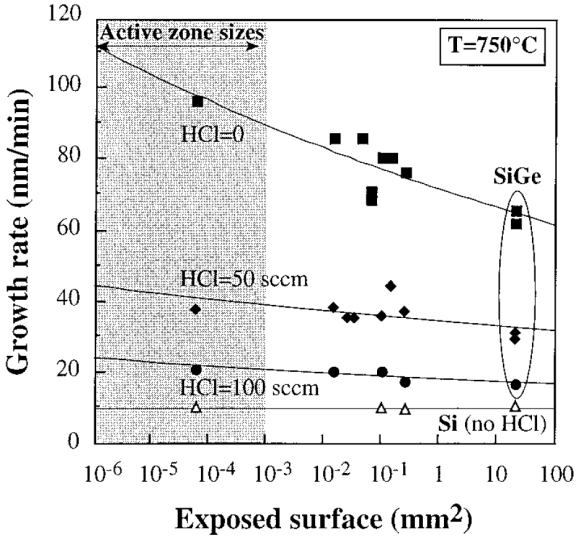

Figure 4.1 Variation in SiGe growth rate at 750 °C on 80% oxide covered wafers, as a function of exposed area. Gas conditions: (Ge/Si)g=0.0125, HCl=0, 50, and 100sccm for SiGe growth and DCS=200 sccm for Si [7].

Another report [8] stated that the "pattern sensitivity" decreases as the pressure reduces. They have attributed this behavior to the longer diffusion lengths of the incoming molecules at lower pressures (see Figure 4.2). For this experiment, a chip composed of 216×250 openings of 3×18 μm² had been used. Position 1 was measured on the opening at the chip edge (close to unpatterned oxide), whereas, position 5 was located at the chip center.

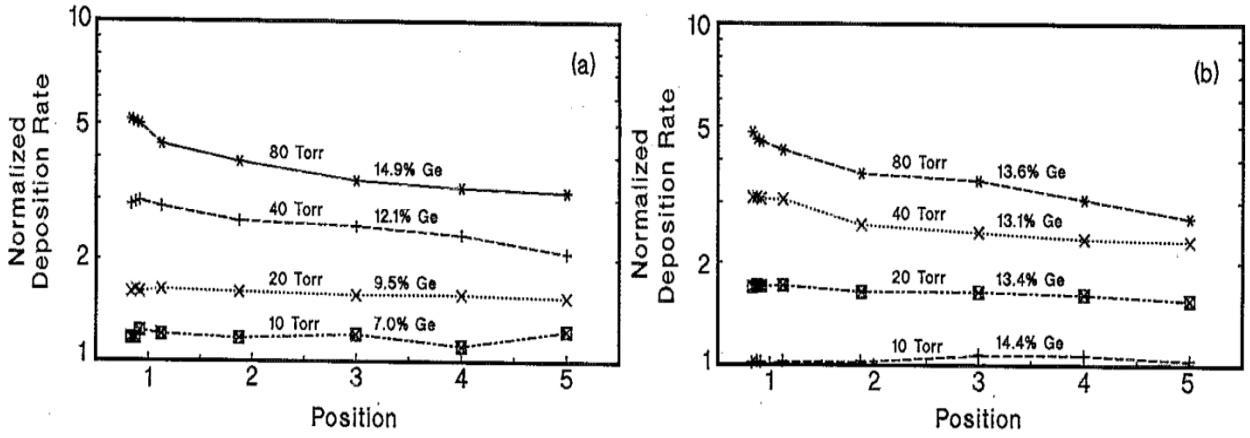

Figure 4.2 Normalized deposition rate at different pressures. SiH_2Cl_2 mole fraction=10^{-3}; HCl mole fraction=10^{-3}. (a) Constant GeH_4 mole fraction=1.3×10^{-5}. (b) GeH_4 mole fractions were varied to obtain approximately constant Ge content in large area; GeH_4 mole fractions: 9×10^{-6} (80 Torr); 1.5×10^{-5} (40 Torr); 2.6×10^{-5} (20 Torr); 4.9×10^{-5} (10 Torr) [8].

Loo et al. [11] suggested the combination of low growth pressure (10 torr) and high H_2 carrier gas (40 slm) to tackle the pattern dependency problem. However, high H_2 flux makes it difficult to grow SiGe layers with either high Ge content or high doping level. Subsequent publications from various groups manifested these conclusions [15-21].

This chapter introduces an empirical model for the selective epitaxial growth of SiGe layers in a reduced pressure chemical vapor deposition (RPCVD) reactor. The model takes into account gas and surface kinetics and reactions for the growth rate and Ge composition calculation. Pattern dependency has also been evaluated through the modeling of gas consumption in a certain chip and the interaction between chips on the wafer. Since SEG of SiGe suffers from point defects [22] and relaxation [23] at respectively low (<625˚C) and high (>725˚C) temperatures, the model is developed for the temperature range between 625 and 725˚C.

2. Experimental Details

The epitaxial layers were grown on blanket or patterned Si(100) substrates in an ASM Epsilon 2000 RPCVD reactor at different temperatures and pressures. Dichlorosilane (SiH_2Cl_2) and 10% germane (GeH_4) in H_2 were used as Si and Ge sources, respectively. HCl was utilized as the etchant to obtain selectivity during the epitaxy. In order to verify the model, different partial pressures of SiH_2Cl_2 (P_{DCS}), GeH_4 (P_{GeH4}) and HCl (P_{HCl}) were applied while 150nm oxide layer was used as the mask against Si. The hydrogen partial pressure has been considered as an important point for the gas kinetics in the reactor. This parameter has been altered to achieve different partial pressures of the precursors.

The substitutional Ge content and the thickness of SiGe layers were measured directly by high resolution x–ray diffraction (HRXRD) for the blanket wafers. For

the measurements on the pattern substrates, the x–ray beam was focused on arrays of openings with the same size. In order to obtain adequate beam intensity, a mirror was applied in the primary optics and long acquisitions were performed to generate high quality rocking curves. Nevertheless, no thickness fringes were observed in the rocking curves to estimate the layer thickness in the small openings. The Ge content was obtained from simulation of the rocking curves using the Takagi–Taupin equations. Atomic force microscopy (AFM) and cross–sectional high resolution scanning electron microscopy (HRSEM) were employed to measure the layer thickness of the grown SiGe layers inside the oxide openings.
In this study, the PHOENICS-CVD simulation program has been used to determine the gas kinetics in the CVD chambers for different total pressures (10, 20 and 40 torr) and temperature distribution during epitaxy. The simulation provided essential information about the gas boundaries, which is a very important parameter for the modeling of the epitaxy process.

3. Results

3.1. Theory of selective epitaxy growth of SiGe layers

The kinetics of CVD growth can physically be described by classical boundary layer theory assuming a laminar gas flow over the wafer. Figure 4.3 illustrates a schematic view of the gas kinetics.

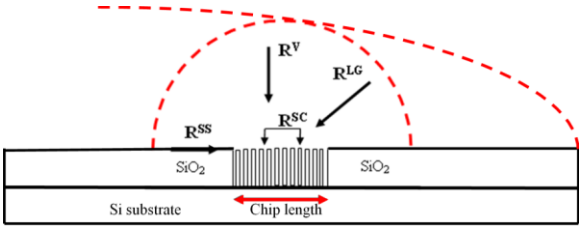

Figure 4.3 Schematic illustration of how a classical boundary layer is produced from laminar gas stream flowing over the wafer in SEG during the CVD process. In this figure, black arrows demonstrate different ways through which diffused molecules from the boundary reach the dangling bonds.

Due to the frictional force between the gas stream and the stationary susceptor/substrate, a stagnant boundary layer is established during the gas flow (see Figure 4.3). Beyond this boundary layer, the gas is assumed to be well–mixed and moving at a constant speed. Gas molecules which have diffused through the gas boundary layer, eventually reach the substrate surface. They are attracted towards the dangling bonds and are then consumed. The vertical diffusion path of the gas molecules was 10–15 mm for the total pressure of 20–40 torr in the ASM Epsilon 2000 reactor [24]. In the case of a chip with opening arrays, a virtual volume (depletion volume) is established as shown in Figure 4.3. The radius of this volume above a chip is related to the boundary layer thickness. The migration length of the species on the oxide (or nitride) controls this radius on the surface.

The gas–phase depletion for the patterned substrate occurs both vertically and laterally around a single chip. Inside the chip depletion volume, there are four different sources of species which contribute to selective epitaxy growth:

a) Vertical gas–phase diffusion
b) Lateral gas–phase diffusion
c) Surface diffusion from the oxide (or nitride) surrounding the chip
d) Surface diffusion from the oxide (or nitride) within the chip

For each of the inlet sources, the identified components contribute to the total growth rate (R_{tot}) in the following expression:

$$R_{Tot} = R_{Si}^{V}+R_{Si}^{LG}+R_{Si}^{SS} + R_{Si}^{SC} + R_{Ge}^{V} + R_{Ge}^{LG} + R_{Ge}^{SS} + R_{Ge}^{SC} - R_{E}^{V} - R_{E}^{LG} - R_{E}^{SS} - R_{E}^{SC} \quad (1)$$

R^V and R^{LG} refer to the incoming SiH_2Cl_2, GeH_4 and HCl molecules in vertical and lateral direction (see Figure 4.3). These molecules are drawn toward the dangling bonds due to the lower gas pressure at the bottom. The chip openings are actually acting like a sinkhole for the coming molecules in the gas–phase. R^{SS} and R^{SC} represent the atoms from the dissociated reactant molecules diffusing on the insulator surface either surrounding a chip or within a chip. R_E is the etch rate of the etchant species.

3.1.1. Temperature distribution

The kinetics of the gas molecules is dependent on both temperature and growth pressure. Therefore, the temperature distribution for an ASM Epsilon 2000 RPCVD reactor was simulated using PHOENICS–CVD software at three different growth pressures: 10, 20 and 40 torr.

The main gas transport mechanism through the boundary layer (as shown in Figure 4.3) is diffusion. During a fast deposition process, the boundary layer will become depleted (from gas molecules). The velocity of a well–mixed stream of gas molecules (V) is an important factor to predict the boundary layer thickness which has been obtained by simulation at those conditions. The boundary layer thickness (δ) as a function of the position over the susceptor/substrate (x) is derived from $\delta(x)=A(\mu x/\rho V)^{1/2}$ [25] where μ is the gas kinematical viscosity, ρ is the gas density and A is a constant. In this equation, several unknown parameters are involved; for example, kinematical viscosity and gas velocity are highly dependent on the actual gas temperature, which can be significantly different from the susceptor temperature.

In order to simplify the process, hydrogen was considered as the main gas stream passing above the susceptor (and wafer). According to the deposition recipe, a 20 slm (standard litter per minute) H_2 inlet flow was applied. In Epsilon 2000 reactor, growth temperature is controlled through the assembly of lamps which heat up the susceptor; this heat is then transferred to the flowing gas (650°C). Figure 4.4 demonstrates the temperature distribution in the flow direction at the center of the reactor for 10, 20 and 40 torr total pressures.

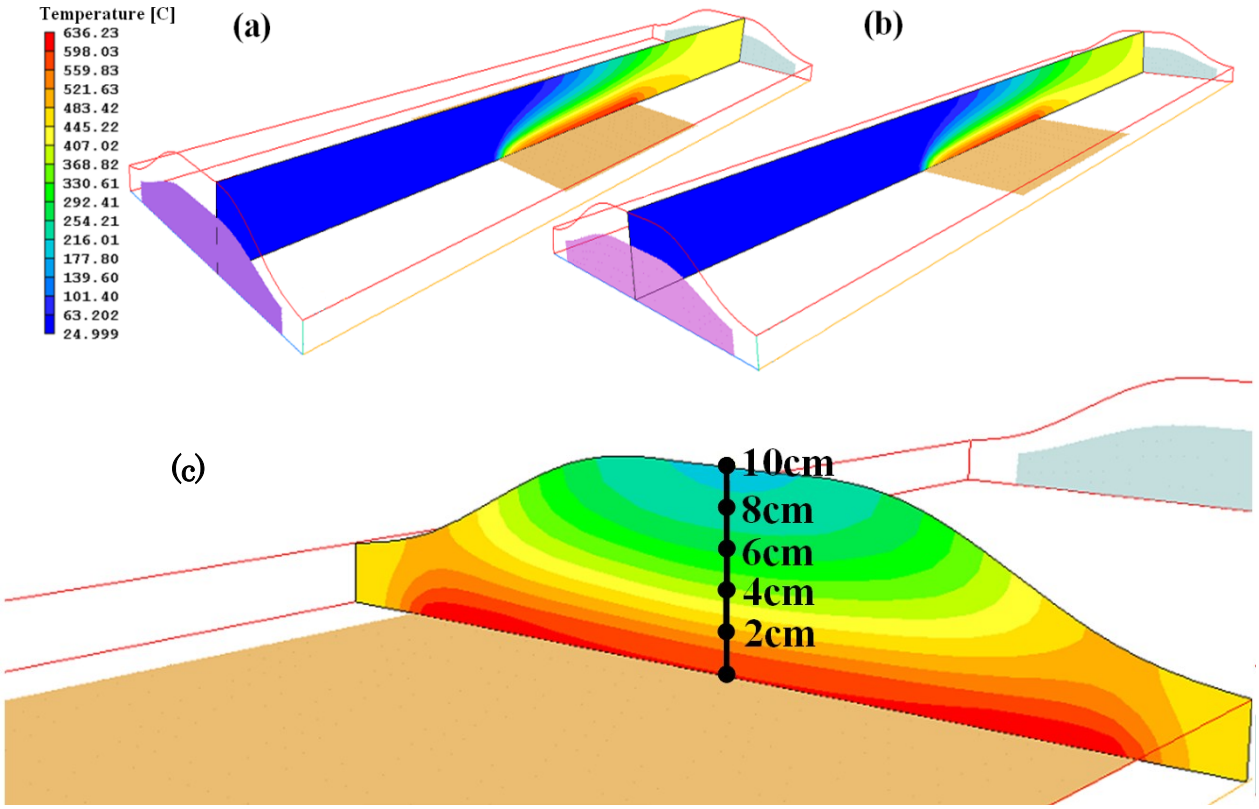

Figure 4.4 Side view illustration of the temperature profile simulated at a) 40 torr, b) 10 torr and c) cross-sectional view of the chamber at 20torr. The purple, grey and orange colors represent the inlet, outlet and the susceptor areas, respectively.

It can be observed from the figures that by decreasing the growth pressure, the velocity of the gas increases and this affects the temperature distribution inside the chamber. Moreover, by decreasing the growth pressure the formed gas boundary moves closer to the substrate and subsequently the number of diffusing molecules decreases [14]. As it is shown in Figure 4.4c, the temperature deviation is less than 2% at 1.5 cm above the susceptor which means that using susceptor temperature (recipe temperature) as the depletion volume temperature can be a good estimation.

3.1.2. Gas distribution

In CVD process, the partial pressure of the reactant gas is adjusted by varying the gas flow rates. Since most of the introduced gases flow over the substrate, the gas flow which reaches the substrate is not the same as the input value. Therefore, only a fraction of the total gas flow diffuses downwards to the dangling bonds (F_F in unit volume/min)). In this case, for a Si opening in a chip, the following fluxes are defined:

$$F_S = -D\nabla C_P \qquad \text{Fick's law} \tag{2}$$

$$F_{to} = 2F_F\pi r^2 \tag{3}$$

where Fs is the gas flow per unit area per min (flux) (see Figure 4.5) on the depletion volume of each opening and C_P is the concentration of gas species in the flux. F_F is the real (final) flow reaches to the dangling bonds in the opening. Since

the radius of the depletion volume in the gas phase and on the oxide surface are found to be in mm range [13], spherical estimation is not far from the reality. The species concentration as a function of distance from the opening can be obtained by combining Eq.2 and Eq.3 which leads to:

$$C_p(r) = C_\infty - \frac{K}{r} \qquad \text{where: } K = \frac{F_{to}}{2\pi D} \tag{4}$$

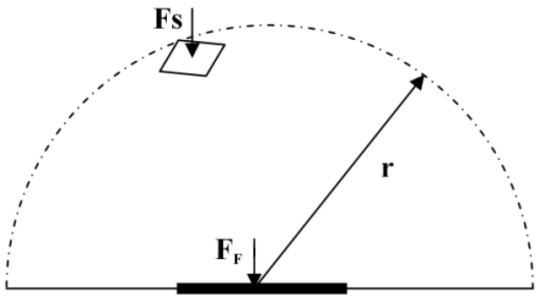

Figure 4.5 A schematic sketch of the flux of molecules over an opening in a spherical symmetric

where C_∞ is the specie concentration in the inlet gas. This can be applied to define a function for the depletion power of an opening on the coming molecules. It can be concluded from Eq. 4 that by moving closer to the openings, the species concentration decreases. This reduction, which originates from the opening depletion power, is the main reason for the movement of species inside the stationary region.

3.2. Modeling of the SEG of SiGe on non–patterned substrate

3.2.1. Vertical growth components

The vertical parameters in eq. 1 are identified with the growth on the blanket wafer where no lateral diffusion exists. There are a series of publications about the epitaxial growth of SiGe layers using the CVD technique. The Meng Tao approach [26] is presented here as a basis for the upcoming model regarding the growth rate in SEG of SiGe. In Tao's model, the impinging reactant molecules on the Si surface are incorporated to the dangling bonds. By applying the Maxwell distribution function in unit time, the number of the reactant molecules ($d\Gamma$) which interact with a unit area of the substrate with kinetic energy between E_K and E_K + dE_K can be thus estimated:

$$d\Gamma = 8\pi N_R \left(\frac{1}{2\pi m_R k_b T}\right)^{\frac{3}{2}} m_R E_K \exp\left(-\frac{E_K}{k_b T}\right) dE_K \tag{5}$$

where N_R is the number of reactant molecules in a unit volume of the gas phase and m_R is the mass of a reactant molecule. Integrating the formula from E_A (deposition activation energy) to + ∞, the number of the activated reactant molecules which strike a unit area of the substrate in a unit time is given by:

$$\Gamma = \frac{N_R}{(2\pi m_R k_b T)^{\frac{1}{2}}} (E_A + k_b T) \exp\left(-\frac{E_A}{k_b T}\right) \tag{6}$$

The deposition of Si layers on a Si surface is notably the simplest case of epitaxial growth. The main contributing specie in this case is dichlorosilelyne ($SiCl_2$) which has a unity sticking coefficient on the dangling bonds according to the previous reports [5]. The growth rate for Si deposition can be calculated as follows:

$$R = \frac{\Gamma}{N_0} = \beta \frac{(1 - \theta_{H(Si)} - \theta_{Cl(Si)})}{N_0} \frac{P_{SiH_2Cl_2}}{(2\pi m_{SiH_2Cl_2} k_b T)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2}}{k_b T} + 1\right) \exp\left(-\frac{E_{SiH_2Cl_2}}{k_b T}\right) \quad (7)$$

where ß, θ, P, m, N_0 and E are respectively: unit–less tooling factor, surface coverage of hydrogen or chlorine, partial pressure of DCS, molecular mass of DCS, number of atoms in a unit volume of the substrate layer, and the activation energy which is required for deposition. The constant ß is considered as a tooling factor which is reactor– and gas–dependant. This constant must be calibrated for each CVD reactor.

At temperatures lower than 900 °C, a high percentage of surface sites are blocked by Cl(s) and H(s); whereas at temperatures above 900 °C almost all sites become available [27]. Hydrogen desorbs at a much lower temperature than does chlorine; this explains the smaller growth rates achieved in chlorine–based Si epitaxy compared to that of hydrogen.

The surface coverage temperature dependency of an adsorbed gas can be obtained through the Langmuir isotherm. For Si deposition, the dominant reactions occur through a series of Cl dissociation but ultimately the following chemical reactions and adsorption can be written:

$$SiH_2Cl_2(g) + \_ \rightarrow \underline{Si}Cl_2 + H_2(g) \quad (R1)$$

$$\underline{Si}Cl_2 + \_ \rightarrow \underline{Si}Cl + \underline{Cl} \quad (R2)$$

The Langmuir isotherm for an equilibrium case can be written as:

$$B(T) = \frac{\theta_{Cl}^2}{P(1 - \theta_{Cl})^2} \quad (8)$$

where B is the reaction constant and P is DCS partial pressure. However, epitaxy is a non–equilibrium process on account of which the above expression must be thus modified:

$$\theta_{Cl} = \frac{1}{1 + \sqrt{B(T) \times P^{-4.5}}} \quad (9)$$

This expression provides the chlorine coverage on the Si surface for different temperatures during the growth of Si from the DCS source. According to previous reports in the temperature range used for SEG of SiGe layers (600–725˚C), hydrogen occupies less than 5% of the surface sites. This value (θ_H = 5%) has been applied to the whole deposition range in the model [27].

3.2.2. HCl–etching of silicon

HCl has been used as the Si etchant in two applications; in SEG to obtain selectivity against oxide (or nitride) and in the direct etch of exposed Si materials [28]. The latter application is called chemical vapor etch (CVE), and has been used in combination with SEG of B–doped $Si_{1-x}Ge_x$ (or As–doped $Si_{1-y}C_y$) to form recessed

junctions [29]. The primary benefit of HCl CVE is avoidance of complex defects which are normally introduced during RF–plasma etching techniques [30].
The presence of HCl molecules during SEG is necessary to remove formed nuclei on the oxide (or nitride) surface. At the same time, HCl etches away part of the deposited Si material in the exposed Si areas. Presence of this gas has also a strong effect on the layer profile and defect density of the epitaxial layers.
Previous studies have demonstrated that HCl CVE is anisotropic and results in formation of (311) and (111) facets [31]. For process temperatures less than 800°C, rough surfaces with etch–pits are obtained. When the temperature exceeds 1000°C, the SiO_2 mask is damaged. A temperature range of 850–950°C is found to result in the most reliable etch process.
Figure 4.6 illustrates the Arrhenius plots of the Si etch process on blanket samples at HCl partial pressures of 50, 100 and 200 mtorr. The thickness of etched Si in these samples was determined from the weight difference of the wafer pre– to post–etch. The etching is characterized by a mass–controlled regime from 900 to 1000°C with a small dependence on temperature.

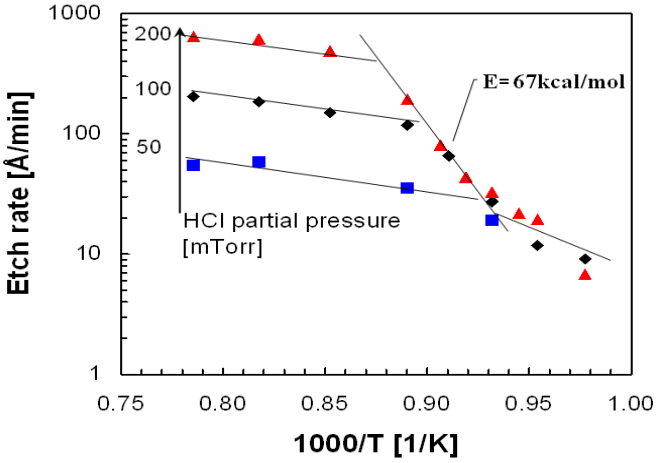

Figure 4.6 Etch rate of silicon as a function of the reciprocal temperature for three different HCl partial pressures.

For lower temperatures, the etching is reaction–controlled showing the activation energy of 67 Kcal/mol. This value corresponds to the Si–Cl bond energy [32]. The minor variations in the slope for 1000/T > 0.92 K^{-1} (<~800 C) are due to uncertainties in the thickness estimation technique.

3.2.3. HCl–etching during selective epitaxy growth

The etch rate during selective epitaxy of Si is defined from the following general equation:

Etch rate (HCl) = Growth rate (DCS) – Growth rate (DCS+HCl) (10)

Figure 4.7 shows the growth rate of silicon, and demonstrates two well–known regimes in CVD. At low temperatures, epitaxy is limited by kinetic reactions, while at high temperatures, deposition is controlled by mass transfer of the reactant species to the surface. Since the growth of SiGe layers for recessed S/D application is

limited to low temperatures to avoid strain relaxation, only the kinetic–controlled regime is highlighted in this work.

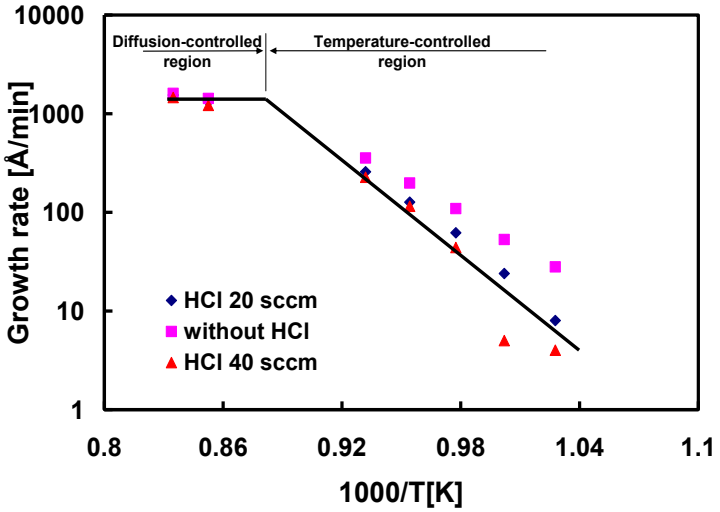

Figure 4.7 Silicon growth rate in the absence and presence of different HCl inlet flows at different temperatures. DCS partial pressure is 60 mtorr.

Figure 4.8 illustrates the etch rate of silicon during silicon epitaxy for HCl partial pressures between 20–60 mtorr. This data is extracted using eq. 10. In this figure, the curves are parallel to each other, and their slope indicates the activation energy of 37.5 Kcal/mol. This value is between the 22 and 44 Kcal/mol needed to break one and two Si–Si bonds [33]. The value is notably lower than the energy required for breaking three bonds of Si atoms at a crystalline site. This proves that compared to bulk Si atoms, Cl is able to remove adsorbed Si atoms (before they become incorporated in the Si lattice) more easily.

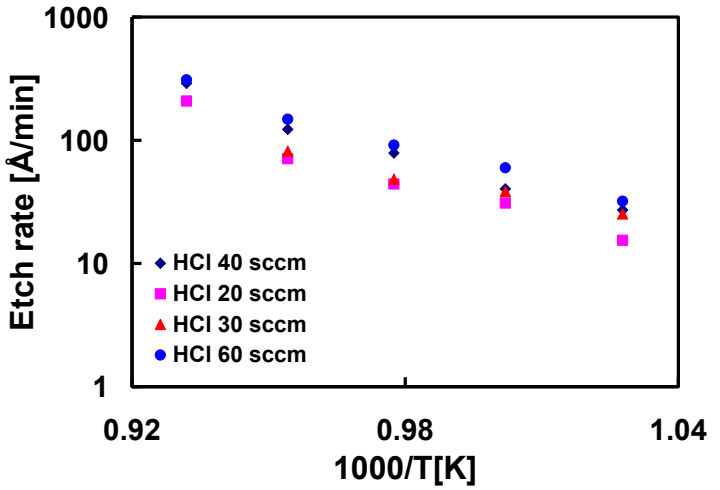

Figure 4.8 HCl etch rate vs. temperature during Si epitaxy for different HCl partial pressures. DCS partial pressure is 120 mtorr.

The growth rate equation for Si deposition in presence of HCl is given by:

$$R_T = R_{Si}^V - R_E^V \qquad (11)$$

$$R_T = \beta \frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{SiH_2Cl_2}}{\left(2\pi m_{SiH_2Cl_2} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2}}{k_b T}+1\right) \exp\left(-\frac{E_{SiH_2Cl_2}}{k_b T}\right) - \frac{\gamma(1-\theta_{H(Si)})}{N_0} \frac{P_{HCl}^{0.596}}{(2\pi m_{HCl} k_b T)^{\frac{1}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right) \quad (12)$$

where γ is another unit–less constant which includes the gas properties and gas distribution in a CVD chamber. The HCl etching of Cl atoms can happen through adsorption to Si or SiCl which removes the θ_{Cl} parameter from the pre–exponential of the etch part of eq.11. Experimental results show that the dependency of etch rate on P_{HCl} is actually not linear. Instead, a sublinear relationship ($P_{HCl}^{0.596}$) is observed. This discrepancy is caused by the migration of Cl atoms on the Si surface.

For the SEG of SiGe layers, GeH_4 precursor has been added to the reactant gases. In this case, eq.1 changes as follows:

$$R_T = R_{Si}^V + R_{Ge}^V - R_E^V \quad (13)$$

The presence of Ge atoms on the surface enhances the growth rate for two reasons; first, they require lower activation energy for deposition than do Si (0.61 eV for Ge compared to 2.08 eV for Si); and second, the desorption energy of other species (e.g. H and Cl) from these atoms is also lower than Si which makes them favorable desorption sites for undesired atoms on the surface. Thus, Si atom binding becomes easier in the presence of Ge atoms. This can emerge through the coefficient "m" in the total growth rate equation.

Therefore, eq.13 can be modified for SiGe growth in presence of HCl as:

$$R_T = R_{Si/Si}^V + R_{Ge/Si}^V + R_{Si/Ge}^V - R_E^V = R_{Si/Si}^V + R_{Ge/Si}^V + mR_{Ge/Si}^V - R_E^V \quad (14)$$

where m is called the substitution coefficient. Theory must now be added in the form of effective reaction rate constants. In this way growth rates are related to chemical reaction kinetics:

$$R_T = \beta \frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{GeH_4}}{\left(2\pi m_{SiH_2Cl_2} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{SiH_2Cl_2\ on\ Si}}{k_b T}\right) + \chi \frac{(1+m)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{GeH_4}}{\left(2\pi m_{GeH_4} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{GeH_4 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{GeH_4 on\ Si}}{k_b T}\right) - \frac{\gamma(1-\theta_{H(Si)})}{N_0} \frac{P_{HCl}^{0.596}}{(2\pi m_{HCl} k_b T)^{\frac{1}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right) \quad (15)$$

where χ is a unit–less constant which is dependent on the gas properties. The m coefficient is suggested to be the number of silyl groups which have been substituted for hydrogen atoms in germane molecules by a chemical gas reaction ($0 \le m \le 4$). In the range 600°C≤ T ≤725°C, it is reported [34] that the deposition degree of germane–hydrogen substitution is fixed by m = 2.

Using eq. 10, it is also possible to determine etch rates during SiGe epitaxy. In Figure 4.9, the activation energy has been calculated from Arrhenius curves of experimental data for various Ge partial pressures. The curve reveals that the

activation energy decreases with increasing Ge partial pressure. This behavior can be explained by the effect of strain which weakens the atomic bonds.

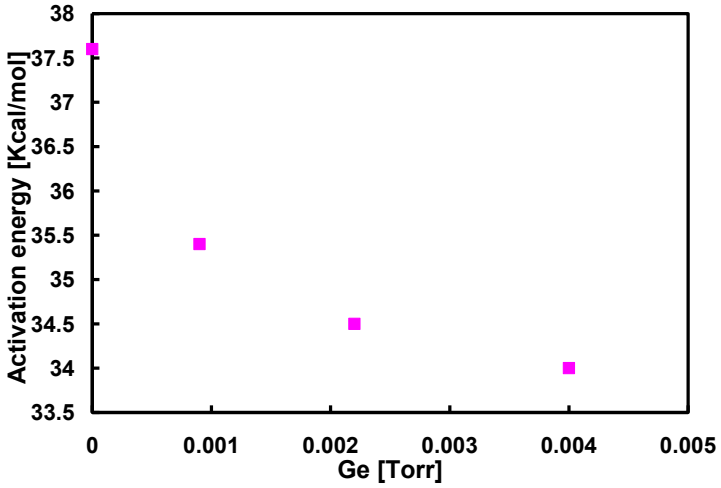

Figure 4.9 Variation of the activation energy for different Ge partial pressures.

Since the SiGe layers contain a compressive strain, the bonding energy becomes weaker. As a result, the activation energy of the etching will decrease by increasing the Ge content (or strain). The experimental data demonstrate the following expression for etching activation energy:

$$E_{Etching} = E_{a,Etching(Si)} e^{-12.535 P_{GeH_4}} \quad (16)$$

where $E_{a,Etching(Si)}$ is the etching activation energy. The practical minimum value for this activation energy in this temperature regime (>600˚C) is 7 Kcal/mol [35] which is the required energy to etch the bulk Ge. The dependency of activation energy on Ge content has been confirmed by the previous reports [35]. Meanwhile there is a discrepancy between the extracted value in this study with the reported value in reference [35]. This difference in activation energies is explained by the fact that the required energy to etch the bulk SiGe (after epitaxy) and a SiGe bond on the surface during the epitaxy are very different. Although an increase in the etch rate is observed in SiGe epitaxy, its growth rate is still higher compared to that of Si.

The Ge content in SiGe layers is also an important factor which is obtained from the flux/partial pressure ratio between Ge and Si [36] as shown in the following equation:

$$\frac{x^2}{1-x} = \alpha \left(\frac{P_{GeH_4} - (1-\lambda) P_{HCl}}{P_{SiH_2Cl_2} - \lambda P_{HCl}} \right) \quad (17)$$

where x is the Ge content. λ is a reaction fraction of Cl which indicates the interaction amount of Cl with Si ((1–λ) with Ge). In the presence of HCl during selective epitaxy, Cl atoms preferably remove Si atoms rather than Ge ones. This parameter (λ) is in a range between 0.9 and 1 depending on the HCl amount during epitaxy. The results of this study show that λ is close to 1 when the partial pressure of HCl is low (less than the Si source) and close to 0.9 for high HCl amount. α is the result of adsorption and desorption of the main species involved in the deposition:

$$\alpha = \frac{k_{a,GeH_2} \times k_{d,H}}{k_{a,SiCl_2} \times k_{d,Cl}} = Aexp(\frac{E}{kT}) \quad (18)$$

The adsorption energy difference in eq.18 ($E_{a,SiCl2}$–$E_{a,GeH2}$) is about 0.1eV [37] and the desorption energy difference is 0.48 eV [38]. Thus, the overall activation energy is estimated to 0.58 eV which is close to the extracted energy (0.697 eV) in this study.

3.3. Modeling of the SEG on the fully–patterned substrate

3.3.1. Pattern dependency of selective SiGe epitaxial growth

The selective epitaxy growth (SEG) of Si and Si–based group IV materials is very attractive especially for MOSFET application. The main issue for SEG arises when a non–uniform patterned wafer is used as the substrate. It is so–called the "pattern dependency" of the growth which causes a variation of the layer profile (growth rate, composition and doping concentration) in chips either on the same wafer (local effect) or different wafers (global effect). This is related to the difference in the layout and architecture of the wafers. The layout concerns size, shape, and density of the openings over a chip, whereas the wafer architecture refers to the isolation material (SiO_2 or nitride) and its thickness.

As discussed earlier in this chapter, many reports have proposed methods to improve the layer profile uniformity over the wafer but so far there is no remedy to completely eliminate this issue. Recently it has been reported that a better illustration for pattern dependency of the layout is the chip exposed Si coverage (not the size of the openings) [15,16].

3.3.2. The influence of opening size or Si coverage of the chips

Gas depletion theory indicates that chip exposed Si coverage has a direct relation with the amount of gas consumption over a chip. Even if two chips on a wafer have openings with different densities and sizes, they should have a similar layer profile if they have the same area of exposed silicon. In other word, similar exposed Si coverage of two chips with the same size can be written as:

$$\sum_{i=1}^{n} a_i = \sum_{j=1}^{m} b_j$$

where n and m are the number of the openings in chips with opening areas (shapes) a_i and b_j

In this part of the study, the geometry and the density of chip openings were changed, but the Si coverage of the chip was kept constant. Wafers were processed using a mask design containing three pairs of chips with identical coverage (0.83, 2.8 and 8.2 %) but different geometry (see Figure 4.10).

Each chip pair (A and G, B and F, C and E) has one chip with quadratic openings (2×2 μm^2) and one chip with rectangular openings (1×4 μm^2). Epitaxy growth was performed at a total pressure of 20 torr with partial pressure of 60mtorr for SiH_2Cl_2, 20mtorr for HCl and 0.9mtorr for GeH_4. Thickness and Ge content results on these

chips are summarized in Table I. In this table, chips with similar Si coverage show the same Ge content and thickness regardless of geometry.

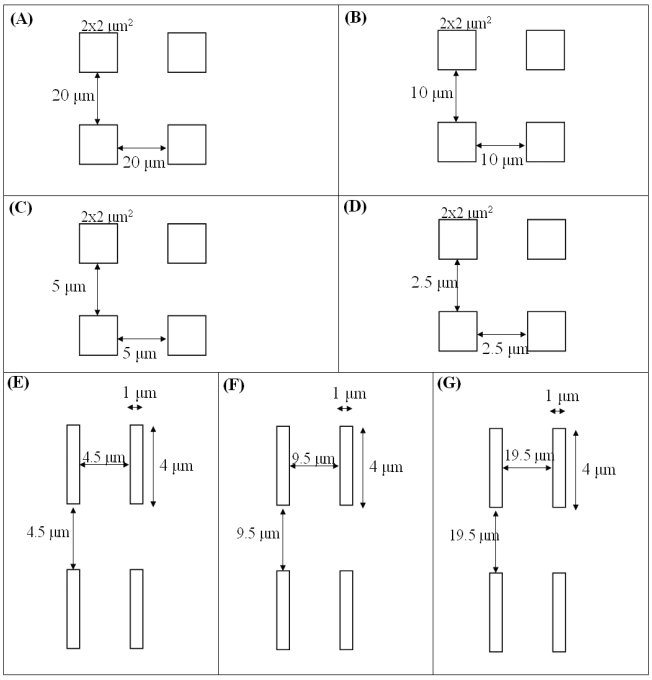

Figure 4.10 Mask design to study the effect of exposed Si coverage of the chip

TABLE I. DEPENDENCY OF THE LAYER PROFILE OF INTRINSIC SIGE ON CHIP COVERAGE (ALL OF THE CHIPS ARE ON THE SAME WAFER)

Chip	Geometry	Coverage (%)	Composition (%)	Growth rate (Å/min)
A	2×2 μm²-20 μm	0.83	26.08	95
G	1×4 μm²-19.5 μm		26.16	96
B	2×2 μm²-10 μm	2.8	24.33	60
F	1×4 μm²-9.5 μm		24.32	63
C	2×2 μm²-5 μm	8.2	22.23	33
E	1×4 μm²-4.5 μm		22.2	32

B incorporation into SiGe is mainly controlled by strain (Ge content) and epitaxial growth rate [39]. B concentration can be maximized by decreasing the growth rate and increasing the Ge content of the layer.

In this study, if the SiGe layers are doped with boron, the amount of incorporated B in SiGe should correlate to the exposed Si coverage of the chip. Values for substitutional B concentration were obtained from the shift of the rocking curve layer peak position of intrinsic and doped layers in x–ray results.

The results from wafers with B–doping are summarized in Table II. As predicted, chip pairs with the same exposed Si area show the same Ge%, growth rate, and B concentration.

TABLE II. DEPENDENCY OF THE LAYER PROFILE OF DOPED SIGE ON CHIP COVERAGE. ALL OF THE CHIPS ARE ON THE SAME WAFER

Chip	Geometry	Coverage (%)	Composition (%)	Growth rate (Å/min)	Active B conc.(cm^{-3})
A	2×2 μm^2-20 µm	0.83	22.5	144	2.38×10^{20}
G	1×4 μm^2-19.5 µm		22.5	144	2.42×10^{20}
B	2×2 μm^2-10 µm	2.8	21	102	2.2×10^{20}
F	1×4 μm^2-9.5 µm		21	102	2.2×10^{20}
C	2×2 μm^2-5 µm	8.2	19.4	73	1.88×10^{20}
E	1×4 μm^2-4.5 µm		19.3	73	1.92×10^{20}

The other factor from gas depletion theory that impacts SiGe growth is the diffusion term. This term is related to how the gas flows and forms boundaries over the wafer and the number of molecules available over the chip which is not derived exactly from the partial pressure in the chamber. These factors are determined by growth pressure during epitaxy.

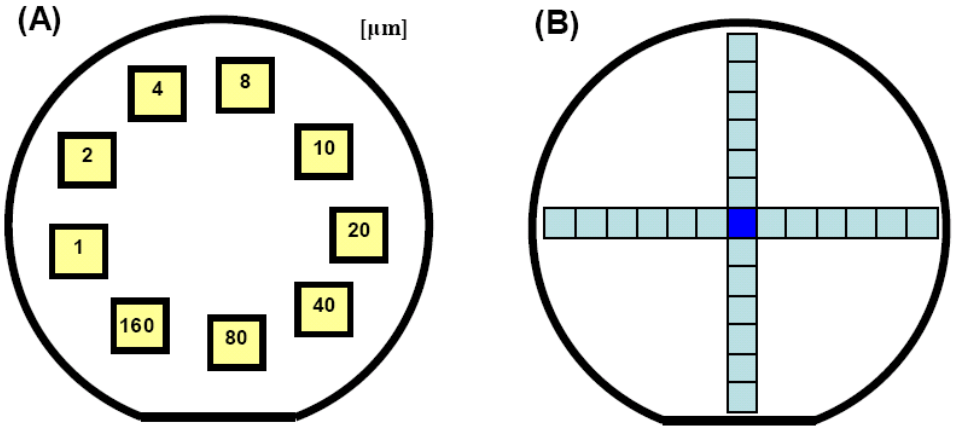

Figure 4.11 Wafer pattern designs used in this study

To examine the impact of diffusion, three samples were processed using a mask design (mask (A) in Figure 4.11) which creates nine chips on a wafer (5×5 mm^2), where each chip contains only one size Si opening. The openings in the chips are either 1×1, 2×2, 4×4, 8×8, 10×10, 20×20, 40×40, 80×80, or 160×160 μm^2 and openings within each chip are spaced 100 µm apart. This mask design creates chips with a wide range of exposed Si coverage that vary between 0.01% and 37.95%. In this test, total pressure was varied from 10 to 40 torr and SiGe layers were deposited with the same dichlorosilane (SiH_2Cl_2) and germane (GeH_4) partial pressure on all wafers. This was performed by compensating the flux of precursors for each total pressure where the carrier gas flow (H_2) was kept constant. Both the Ge content and the growth rate were measured and compared as shown in Figures 4.12a and 4.12b.

There are some missing data in the Figure 4.12b on the sample grown at 40 torr due to strain relaxation.

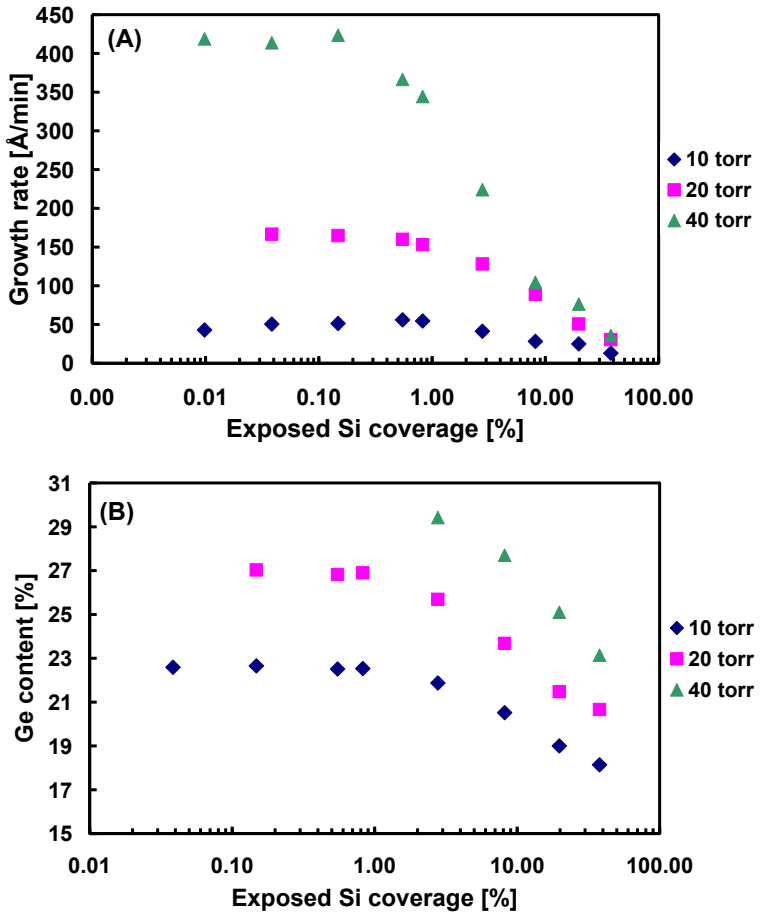

Figure 4.12 a) Growth rate and b) Ge content of intrinsic SiGe selective epitaxy at 650 °C vs. the exposed Si coverage for different total growth pressures but similar precursor partial pressures. (The applied P_{DCS}, P_{HCl} and P_{GeH4} are 60, 20 and 0.9 mtorr, respectively).

The three curves in Figure 4.12a demonstrate that the growth rate increases with increasing growth pressure. For example, for the chip with 1% Si coverage (containing opening sizes of 10×10 μm^2) growth rate values of 50, 160 and 350 Å/min were measured at 10, 20 and 40 torr, respectively. Lowering the pressure leads to slower growth rate because of the relationship between pressure, gas velocity, depletion volume, and the number of molecules diffusing to the wafer surface. By decreasing the growth pressure, the velocity of the gas increases, the formed gas boundary moves closer to the substrate, and the depletion volume becomes smaller. This reduces the number of diffusing molecules.

The curves in Figures 4.12a and 4.12b have two distinguishable regions: a linear region where growth rate and Ge content increase with decreasing exposed Si coverage, and a saturation region where the layer profile is constant. The saturation region shifts to smaller exposed Si coverage for higher growth pressures. For instance, saturation at 20 torr occurs for chips with exposed silicon coverage below 1%, while at 40 torr, it occurs for chips with exposed silicon coverage below 0.65%.

Depicted saturation region is due to very small gas consumption (small as compared to the gas flow).

3.3.3. Interaction among the chips during epitaxy

Testing to this point has revolved around the idealized situation where chips are isolated from one another. In practice, a patterned wafer contains many close–packed chips, and the depletion volume of a chip may overlap and interact with neighboring chips.

A test was performed to estimate the interaction radius around a chip versus its exposed Si coverage. For this study, a wafer was processed with a 5×5 mm^2 chip in the center of the wafer. This center chip had 20% Si coverage and was considered as the 'trap–chip' which depletes reactants from the depletion volume. The center chip (trap–chip) was surrounded by test chips on four sides extending towards the wafer edge. The surrounding chips had 0.83 % exposed Si coverage (mask (B) in Figure 4.11). Figure 4.13a and 4.13b show the impact of the center trap chip on growth rate and Ge content in the surrounding chips. Growth rate was determined with AFM, and Ge content was defined with HRXRD data. In Figure 4.13b, there is no data recorded for Ge content at 40 torr due to strain relaxation.

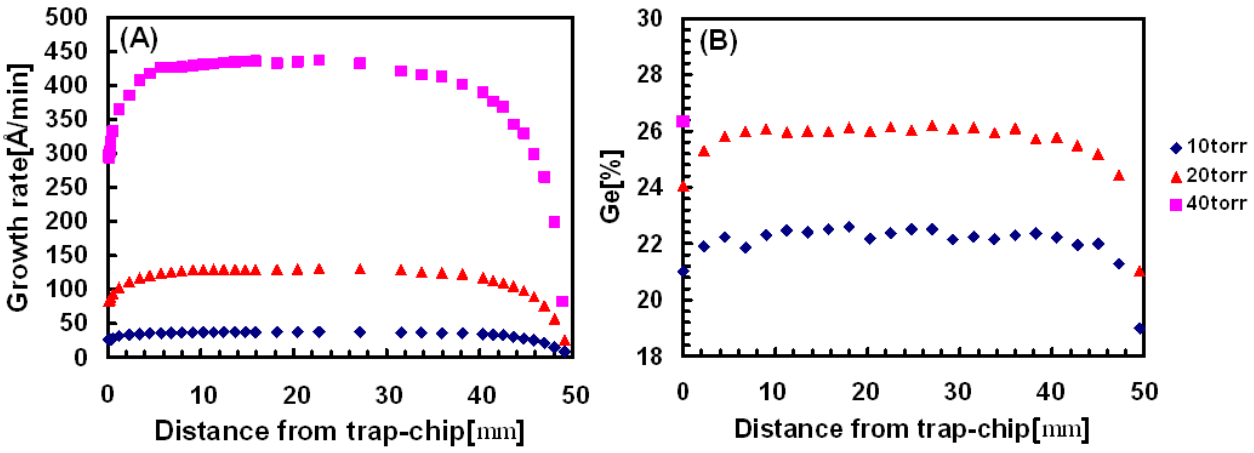

Figure 4.13 Illustration of a) growth rate, and b) composition variation through chips with 20% Si coverage trap-chip in the middle and 2×2 µm^2 openings with 20µm distance (0.83% exposed Si coverage) in the surrounding chips for different growth pressures.

The curves in Figure 4.13 reveal three distinct regions. Within 12 mm of the trap–chip, there is a linear increase in growth rate and Ge content as distance from the trap–chip increases. From 12 mm to 40 mm, the growth rate is saturated and does not vary with distance. Finally, towards the wafer edge, growth rate decreases as distance from the wafer center increases.

The first region involves openings which are impacted by the depletion volume of the trap–chip. In this volume, a significant part of the gas molecules are consumed by the trap–chip and the molecules available for surrounding chips are reduced. When the openings are far enough away from the trap–chip, they are not influenced by the trap; this corresponds to the second region in this figure. Finally, as the edge of the patterned wafer approaches, the susceptor has a chance to deplete reactants. The uniformity of the deposition over a blanket wafer was checked and non–uniformity

was less than 5%. The distribution of layer profile over this wafer reveals a unique picture of the growth and an understanding of pattern dependency of SEG.
Figure 4.13a indicates that the shape of the growth rate curves does not change with decreasing growth pressure, but the width of the linear portion (which determines the radius of depletion volume) becomes smaller. An observation on data points in Figure 4.13 provides a rough estimation for depletion volume radius. This was performed when the relative variation of the growth rate is less than 5% of the saturation value. The extracted radii are approximately 10, 12, and 14 mm for 10, 20 and 40 torr, respectively. These results indicate that the growth kinetics of the gas flux over the chips has been changed, and as a result the depletion volume is decreased. HRXRD results in Figure 4.13b illustrate similar features to 4.13a. Note that the data for Ge content is a mean value over an entire chip. In Figure 4.13b, the layers grown at 40 torr were partially relaxed due to the growth above the critical thickness and were omitted.
In follow–up studies, more complicated cases were tested in which a chip can be impacted by two or more surrounding chips. On the mask for this study, the exposed Si coverages of the surrounding chips (19.75% and 37.85% silicon coverage) were larger than the central chip (0.83% silicon coverage). Four cases were studied as demonstrated in Figure 4.14.

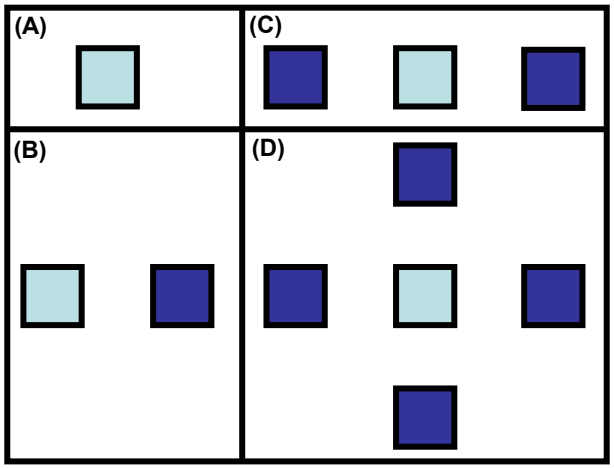

Figure 4.14 Mask design to study the interaction among the chips in a wafer. Surrounding dark blue chips (with exposed Si coverage of 37.85% or 19.75%) are located at 5 mm distance from the central chip (with 0.83% silicon coverage).

A wafer was patterned such that four independent tests could be conducted simultaneously. Each test pattern was more than 15 mm from the wafer edge and from the other test patterns so that results of each pattern can be investigated separately. A reference chip is included (see Figure 4.14a) to determine SiGe growth when there is no interaction with other features. In all cases, the growth rate and Ge content in the central chip were measured. The change of the growth rate in the central chip relative to the reference chip is shown in Figure 4.15. These results reveal that the effects of chips on the central chip are additive. This means that by

knowing the impact of one chip, it is possible to estimate the growth rate in a central chip for any number of surrounding chips.
The above results suggest methods of designing chips with a more uniform layer profile. One approach would be to introduce dummy features on chips to maintain the same exposed Si coverage over the entire wafer. SIMS squares (160×160 μm^2) would be able to deplete all small openings over the chip and lead to more uniform chips over the whole wafer. A second approach would be to calibrate the layer profile by using a calibration sample which contains chips with various Si coverages (similar to Figures 4.12a and 12b). Data from these calibration samples would enable the development of a strategy for chips with complicated layouts (different opening sizes). Each chip can be divided into sub–regions where the Si coverage is kept constant by modifying the density of the openings. This strategy has to be repeated for all the chips of the wafer.

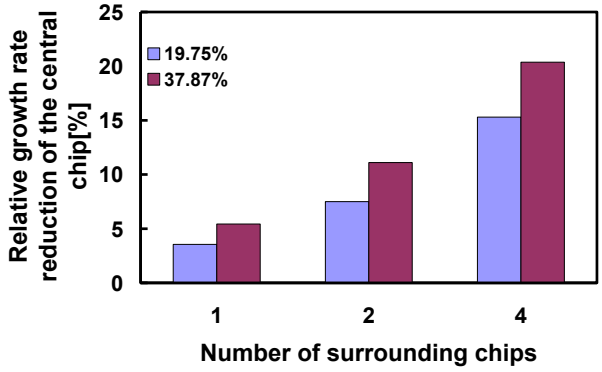

Figure 4.15 Illustration of growth rate reduction compared to the reference opening growth rate on the wafer caused by different numbers of surrounding chips. (The applied P_{DCS}, P_{HCl} and P_{GeH4} are 60, 20 and 0.9 mtorr, respectively)

3.3.4. Global pattern dependency

To examine wafer–to–wafer pattern dependency, two different wafers were processed. The chips on each wafer had the same exposed Si coverage, but the layouts (size and the density of the openings) were different on these wafer. Both patterned Si wafers had an oxide thickness of 0.18 µm, and all chips were positioned in the way to avoid being impacted by other chips and the susceptor. The results are illustrated in Table III. In this table, chips 1, 3 and 5 were located on wafer 1 while chips 2, 4, and 6 were located on wafer 2. The layer profile is unchanged for all chip pairs with the same exposed Si coverage. It means that our results demonstrate a way to control the global pattern dependency by choosing the same chip exposed Si coverage.
The architecture of the samples was studied by evaluating patterned Si wafers with oxide thicknesses of 73, 140, 235 and 340 nm. The variation of the layer profile over different exposed Si coverages and oxide thicknesses is illustrated in Figures 4.16a and 4.16b.

TABLE III. DEPENDENCY OF THE LAYER PROFILE OF SIGE ON CHIP EXPOSED SI COVERAGE WAS INVESTIGATED ON TWO WAFERS WITH SIMILAR GLOBAL AND LOCAL COVERAGES. CHIPS WITH ODD AND EVEN NUMBERS ARE LOCATED ON DIFFERENT WAFERS.

Chip No.	Geometry	Coverage	Composition (%)	Growth rate (Å/min)
1	2×2 μm^2-20 µm	0.83	25.46	112
2	1×4 μm^2-19.5 µm		25.36	118
3	2×2 μm^2-10 µm	2.8	24.22	94
4	1×4 μm^2-9.5 µm		24.16	97
5	2×2 μm^2-5 µm	8.2	22	46
6	1×4 μm^2-4.5 µm		22.2	49

Figure 4.16 can be considered as an illustration of global vs. local emissivity. Ge content decreases with increasing the oxide thickness while the growth rate shows a minor fluctuation. The reason of Ge content variation for different oxide thicknesses is not known yet, however, it may relates to the properties of oxide surface.

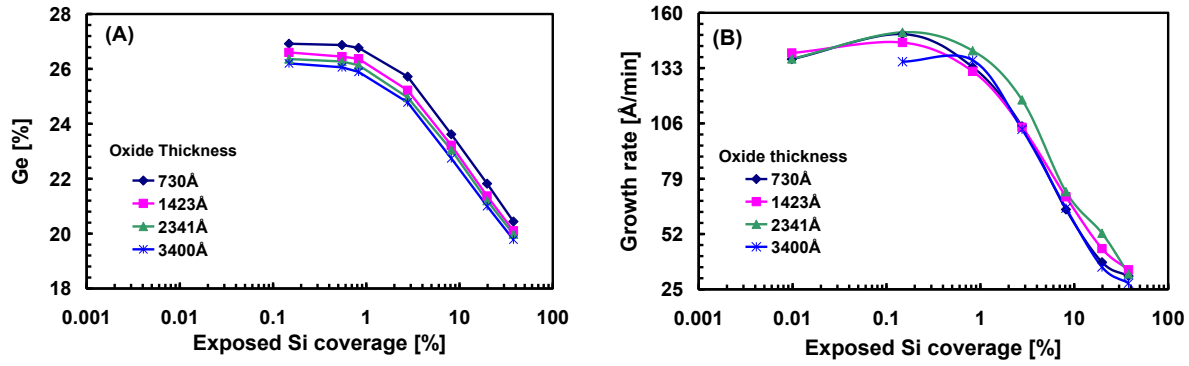

Figure 4.16 Illustration of a) Ge content and b) growth rate variation vs. exposed Si coverage in four different wafers with different oxide thicknesses (The applied P_{DCS}, P_{HCl} and P_{GeH4} are 60, 20 and 0.9 mtorr, respectively)

3.3.5. Pattern dependency of dopant (B and C) concentration

In pMOSFETs, the SiGe layers in S/D regions create uniaxial strain in the channel which improves the hole mobility. Since this improvement depends directly on strain amount, high Ge content SiGe layers are desired. In these transistors, the pattern dependency of the epitaxy growth has a large impact on the amount of strain (and the device performance) but there are also other concerns about these devices as follows: low sheet resistance in S/D junctions, high thermal stability of the silicide layers (formed for low contact resistance) and low dopant out–diffusion from S/D to the channel region [40]. The first two issues can be solved by high boron doping in SiGe epi–layers. Since the presence of boron compensates the compressive strain in SiGe layers [39], high level of both boron and germanium are necessary for such transistors.

An antidote for the out–diffusion of boron in MOSFETs is to implement carbon in S/D junctions. Since the pattern dependency of the growth may result in different

doping profiles in the SiGe layers, having both carbon and boron in S/D regions makes the device process more complicated.

On the other hand, as MOSFET devices are scaled down, the source/drain extension junction depth must be reduced in order to suppress the short–channel effect. However, extremely shallow junctions require a resistivity corresponding to doping levels exceeding the doping atom solid–solubility level in Si. This fundamental limit is connected to ion implantation followed by thermal activation or solid phase epitaxy of amorphous silicon. While ago, Gannavaram et al. proposed a novel method to deceive these issues [41]. It is literally based on forming a recess by selective Si etching and subsequently filling it by *in–situ* doped epitaxial $Si_{1-x}Ge_x$ layers. In this case, the surface solubility governs the dopant incorporation which is several orders of magnitude larger than that of the equilibrium solid solubility.

A more controlled and uniform layer profile enables a more aggressive device design. The original work on pattern dependency mainly focused on selective SiGe epitaxy at rather high temperatures to achieve reasonable growth rates with medium Ge concentrations (i.e., 10%–15% Ge). Advanced devices now require broader composition ranges and *in–situ* doping to enhance their performance. Therefore, more recent publications focus on higher Ge amounts at lower temperatures [42].

Among dopants only B (also C) and Sb have significantly different atomic sizes from Si and induce a measurable strain in the lattice [43]. As mentioned so far in this chapter when dopant atoms are introduced in SiGe matrix, the growth kinetics can be varied and the Ge content in the SiGe layers can be affected.

Figure 4.17 shows the secondary ion mass spectrometry (SIMS) measurement reported by Ghandi et al. [39]. It is clear that the presence of B in SiGe has no effect on the Ge content in these layers. This was a rather surprising result since a significant variation in the growth rate was observed for high B partial pressures. It is usually thought that the change of growth rate affects the Ge content but this is not the case here. This is the validity of the calculated substitutional atomic concentration by measuring the strain compensated amount (comparing the intrinsic and B–doped SiGe layers). In this way, HRXRD can be used also as a feedback to optimize the growth parameters to incorporate maximum boron content in SiGe layers grown in the S/D openings.

It was reported by J. Hallstedt et al. [12] that 1×10^{21} cm^{-3} was the maximum B active concentration in the epitaxially grown layers at 650˚C in the device openings. In this article, SiGe layers with $P(B_2H_6) > 0.1$ mtorr became amorphous in the small openings and the HRXRD layer peak disappeared. It was announced in this article that the maximum active concentration is size dependent so the process has to be calibrated for the opening sizes of interest.

Incorporation of dopants in SiGe is an issue where an accurate estimation of the substitutional dopant concentration is critical. The atomic dopant concentration obtained by SIMS may differ from substitutional (active or incorporated) dopant concentration in the lattice. In case of SiGe, performing the electrical measurements to obtain active dopant concentration of p–type dopant is not quite straight forward

since the induced strain by Ge in Si crystal causes variation in both the hole mass and the warping of the valence band.

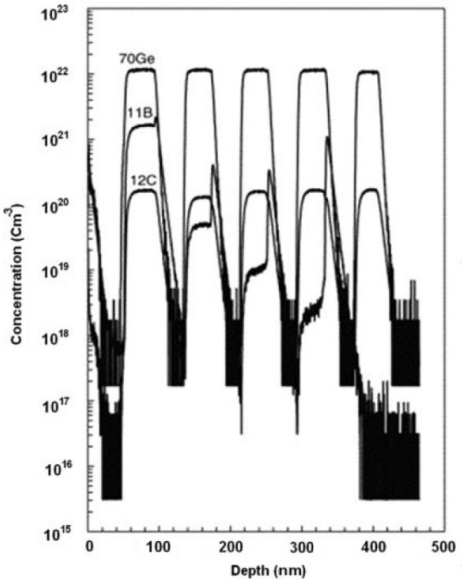

Figure 4.17 SIMS profile for a SiGeC:B multilayer structure capped with 300 Å intrinsic Si layers showing Ge, C and B amount versus depth. The boron partial pressure varied in the range of $5.3 \times 10^{-5} - 4.8 \times 10^{-2}$ mtorr meanwhile for carbon was 0.5 mtorr [39].

The SiGe film composition can be calculated from the mismatch values obtained from ω–2θ rocking curves (ω and 2θ are incident and diffracted angles, respectively) by scanning a focused x–ray beam on a specific chip in high resolution x-ray diffraction (HRXRD) mode. In these rocking curves, the position of the layer relative to the substrate peak provides the lattice mismatch perpendicular to the surface. The Ge content was obtained from simulation of the rocking curves by using the Takagi-Taupin equations. This type of measurement is one dimensional analysis; however, the lattice mismatch parameters can be measured by high–resolution reciprocal lattice maps (HRRLM) around (113) reflection. The low angle of the incident beam in this reflection is about 2.8° which makes this method extra sensitive for revealing the defects in the SiGe layers. The mismatch parameters perpendicular and parallel to the surface are obtained from the following equations:

$$f_{\perp} = \frac{\sin\theta_s \cos(\omega_s - \theta_s)}{\sin\theta_l \cos(\omega_l - \theta_l)} - 1$$

$$f_{\parallel} = \frac{\sin\theta_s \sin(\omega_s - \theta_s)}{\sin\theta_l \sin(\omega_l - \theta_l)} - 1$$

where the indices s and l stand for the substrate and the layer, respectively. The lattice mismatch can be written as:

$$f = (f_{\perp} - f_{\parallel})\frac{1-\nu}{1+\nu} + f_{\parallel}$$

where υ is the Poisson ratio (υ = 0.278) for $Si_{1-x}Ge_x$/Si and the incorporation of B or C in these heterostructures is believed to have only a minor effect on the Poisson value [44].

When the SiGe crystal is doped with B (substitutional dopant concentration), strain compensation occurs since the size of the dopants is smaller than Si and Ge atoms. As a result, a shift of the layer peak towards the substrate peak occurs in ω–2θ rocking curve. The substitutional dopant concentration can be calculated as follows:

$$C_{dopant} = \frac{\Delta f}{\beta}$$

where, Δf is the compensated mismatch (between the intrinsic and doped SiGe) and β is the lattice contraction coefficient which is given by:

$$\beta = \frac{1}{N_{Si}}\left(1 - \frac{r_{dopant}}{r_{Si}}\right)$$

where N_{Si} is the density of Si atoms in a unit volume and r is the atomic radius. In these calculations, the Ge content is assumed to be constant [39]. In selective epitaxial growth, the doped SiGe layers are fully–strained, thus, $f_{\parallel}$ is negligible. This method (HRXRD) has been recognized as a fast, easy and indestructible technique which measures the induced strain in Si or SiGe layers.

Radamson et al. [45] published the feature of B concentration in SiGe layers (shown in Figure 4.18). Since the incorporation of B in SiGe depends strongly on the growth rate and Ge content (or strain), any increase (or saturation) of these parameters may influence the B content in the layers.

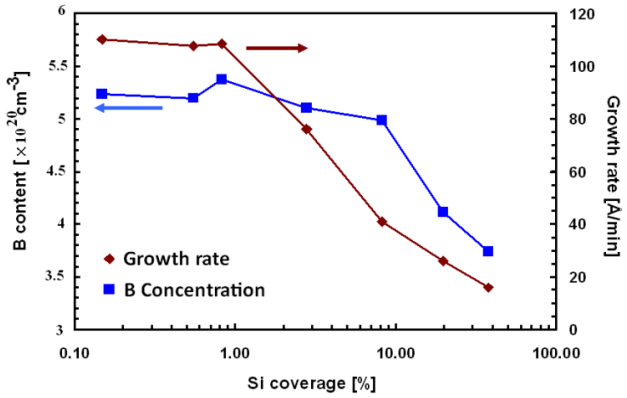

Figure 4.18 Growth rate and active boron concentration for B–doped SiGe layers grown at 650 °C depending on the local exposed Si coverage. (P_{DCS}, P_{HCl} and P_{GeH4} are 60, 20 and 0.5 mtorr, respectively) [45].

All the curves in Figures 4.12, 4.16 and 4.18 illustrate a linear increase of growth rate with decreasing the exposed Si coverage until a saturation region is reached. In epitaxy, the growth rate amount relates to the availability of the molecules and gas consumption rate over a chip [14]. This becomes insensible for low exposed Si coverage which corresponds to values below 1%.

According to the previous report [46], the B–doped SiGe layers have higher growth rate compared to intrinsic layers. The presence of B atoms on the Si surface enhances the growth rate by acting as desorption sites for Cl and H. This increase in

the growth rate of B–doped layers is diminished when carbon is also introduced in SiGe layers.
It is illustrated in Figure 4.19 that carbon doping level follows inversely the Ge content (see also Figure 4.16). C concentration monotonically decreases in SiGe layers grown in smaller exposed Si coverage.

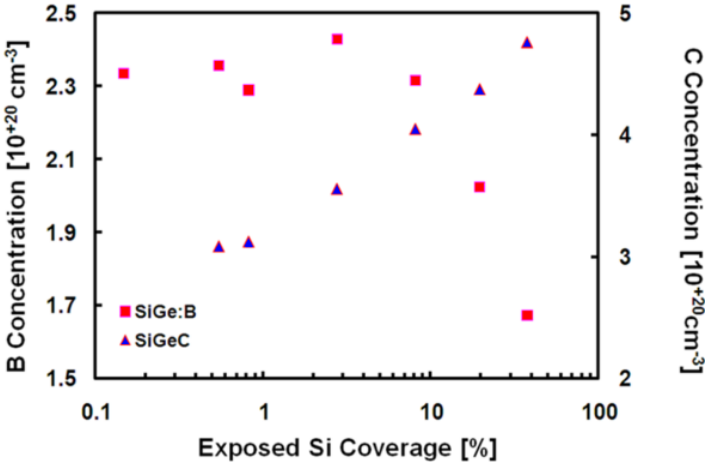

Figure 4.19 Dopant concentration calculated from the shift in the layer peak of HRXRD rocking curves. Identical dots were measures on different chips (different exposed Si coverage) of one wafer. Dichlorosilane, germane, methylsilane, HCl and diborane partial pressures were 60, 1.2, 0.3, 20 and 3.6 mtorr, respectively.

Meanwhile, the boron doping level follows the Ge content and growth rate as expected. The results of this study indicate that the measured strain compensation amount of these dopants (B or C) in SiGe layers are additive. This has been concluded under the assumptions of high epitaxial quality and epi–layers with no strain relaxation.

3.4. Modeling of the SEG of SiGe on the fully–patterned substrate

3.4.1. Lateral components

As mentioned earlier, in selective epitaxy growth there are four different sources which depending on the layout, are either active or not. In order to evaluate a fully–patterned chip design, wafers were processed with a single chip repeatedly patterned over the whole wafer. Nine different fully–patterned wafers were processed; one wafer for each exposed Si coverage ranging from 0.01% to 37.85%. The openings inside chips were either 1×1, 2×2, 4×4, 8×8, 10×10, 20×20, 40×40, 80×80 or 160×160 μm^2 which were spaced 100 µm apart. In these patterns, source c of section 3.1 (surface diffusion from the surrounding oxide) can be excluded from the deposition sources cited before. Thus, for each atom, three sources are available for deposition. For Si selective epitaxy, eq.1 can be rewritten as:

$$R_T = R_{Si}^V + R_{Si}^{LG} + R_{Si}^{SC} - R_E^V - R_E^{LG} - R_E^{SC} \quad (19)$$

LG and SC refer to the lateral gas and surface diffusion from oxide within the chip. In fully–patterned substrates, depletion volumes of the chips are overlapped. However, for a fully–patterned substrate with identical chips, the depletion power of the chips is similar; therefore, in this pattern, the lateral gas–phase diffusion

contribution does not exist (see Figure 4.20). In this case, due to presence of Cl atoms on the oxide, the surface diffusion of Si atoms to the openings is negligible.

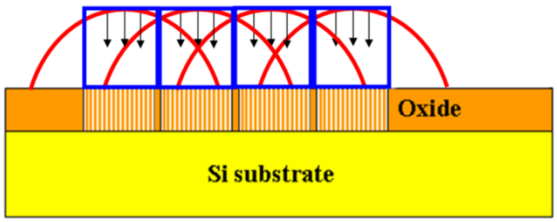

Figure 4.20 Schematic cross-sectional view of the boundary theory and gas diffusion in a fully–patterned substrate; the sources available for deposition are "vertical component" and "diffusion from the oxide within the chip".

The total growth rate equation for a fully–patterned mask is then:

$$R_T = R_{Si}^V - R_E^V - R_E^{SC} \tag{20}$$

This equation is describing a condition in which the selectivity of the growth is guaranteed; which means the HCl partial pressure is high enough to obtain total selectivity against the patterned mask. It has also been reported [47] that migration length of Si on the oxide is very short which may explain the non–selective nature of Si epitaxy from non–chlorine sources. In this case, Si nucleation on the oxide surface is removed by part of the chlorine atoms and the rest migrate towards the openings. Since SiH_2Cl_2 has been used as the Si source and HCl as the etchant, the number of Cl atoms is enough to perform etch both on the oxide surface (to achieve selectivity) and inside the openings. Figure 4.21 illustrates the growth rate results obtained by AFM and the model on five different wafers. Pattern dependency in Si deposition follows the inverse order of SiGe [45,46]. The last point in the chart with 100% exposed Si coverage is in fact the result of the same growth recipe on a blanket substrate (which follows the similar order). As illustrated in the figure, growth rate rises when the exposed Si coverage increases. This is due to the decrease of the third term in eq.20. By decreasing the exposed Si coverage of the chip, which also means increasing its oxide coverage, the number of Cl atoms on the oxide surface increases. This enhances the etch rate inside the opening.

In SEG of Si, P_{HCl}^{SC} is provided through the diffusion of Cl atoms on the oxide surface and has an inverse relation with the exposed Si coverage of the chip. This can be shown as:

$$\Delta P_{HCl}^{SC} = -AP_{HCl}\frac{\Delta c}{c} \tag{21}$$

where c is the exposed Si coverage of the chip and A is a layout factor which can vary depending on the mask type used for isolation. By integrating eq. 21 and using a boundary condition the following equation is achieved:

$$P_{HCl}^{SC} = AP_{HCl}\ln\left(\frac{1}{c}\right) \tag{22}$$

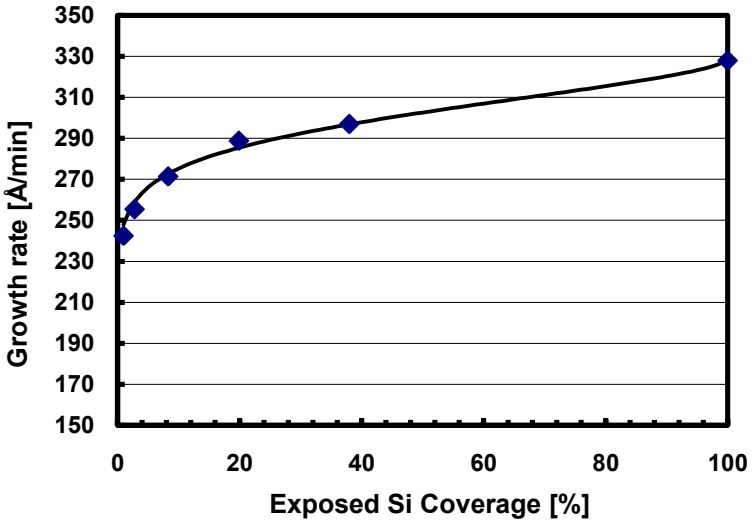

Figure 4.21 Illustration of the growth rate vs. exposed Si coverage of the chip for five different fully–patterned wafers at 20torr total pressure. The applied P_{DCS} and P_{HCl} partial pressures were 120 and 20 mtorr, respectively. The dots are experimental points

Therefore, Eq 20 can be rewritten as follows:

$$R_T = \beta \frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{SiH_2Cl_2}}{\left(2\pi m_{SiH_2Cl_2} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{SiH_2Cl_2 on\ Si}}{k_b T}\right) \quad (23)$$

$$-\frac{\gamma(1-\theta_{H(Si)})}{N_0} \frac{P_{HCl}^{0.596}}{(2\pi m_{HCl} k_b T)^{\frac{1}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right)$$

$$-\frac{\gamma(1-\theta_{H(Si)})}{N_0} \frac{(AP_{HCl}\ln(1/c))_{HCl}^{0.596}}{(2\pi m_{HCl} k_b T)^{\frac{1}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right)$$

3.4.2. SEG of SiGe on a fully–patterned substrate

In this part of the experiment, DCS, GeH_4 and HCl have been introduced for deposition on the patterned wafer. Thus, eq.1 can be rewritten as:

$$R_T = R_{Si}^V + R_{Si}^{LG} + R_{Si}^{SC} + R_{Ge}^V + R_{Ge}^{LG} + R_{Ge}^{SC} - R_E^V - R_E^{LG} - R_E^{SC} \quad (24)$$

In fully–patterned masks with identical chips, lateral gas–phase diffusion of Si, Ge and Cl atoms are vanished (see Figure 4.20). Due to the presence of Ge atoms on the surface of the oxide, Cl desorption occurs from Ge atoms on the oxide surface and therefore, the surface diffusion of Cl becomes insignificant. This has been reported [48] for the epitaxy process and also can be valid for desorption of chlorine from the oxide surface. Eq. 24 can then be rewritten as:

$$R_T = R_{Si}^V + R_{Ge}^V + R_{Ge}^{SC} - R_E^V = R_T^{Blanket} + R_{Ge}^{SC} \quad (25)$$

The Ge surface diffusion from the oxide surface has been written in the same form as that of Cl (eq.22). This can be referred to as the oxide surface contribution in Ge partial pressure (P_{Ge}^{SC}):

$$P_{Ge}^{SC} = BP_{GeH_4} \ln\left(\frac{1}{c}\right) \quad (26)$$

where B is a unit–less constant dependent on the architecture of the mask (oxide or nitride) and c is the exposed Si coverage of the chip. The activation energy for Ge atoms to migrate on the oxide surface is 0.1 eV and must be added to the activation energy of the growth.

Thus, the total growth rate equation will be:

$$R_T = \beta\frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{P_{GeH_4}}{\left(2\pi m_{SiH_2Cl_2}k_bT\right)^{\frac{1}{2}}}\left(\frac{E_{SiH_2Cl_2\,on\,Si}}{k_bT}+1\right)\exp\left(-\frac{E_{SiH_2Cl_2\,on\,Si}}{k_bT}\right)$$
$$+\chi\frac{(1+m)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{P_{GeH_4}}{\left(2\pi m_{GeH_4}k_bT\right)^{\frac{1}{2}}}\left(\frac{E_{GeH_4on\,Si}}{k_bT}+1\right)\exp\left(-\frac{E_{GeH_4on\,Si}}{k_bT}\right)$$
$$+\frac{\chi(1+m)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0}\frac{\left(BP_{GeH_4}\ln\left({}^{1}/_{c}\right)\right)}{\left(2\pi m_{GeH_4}k_bT\right)^{\frac{1}{2}}}\left(\frac{E_{GeH_4on\,Si}+0.1eV}{k_bT}+1\right)\exp\left(-\frac{E_{GeH_4on\,Si}+0.1eV}{k_bT}\right)$$
$$-\frac{\gamma\left(1-\theta_{H(Si)}\right)}{N_0}\frac{P_{HCl}^{0.596}}{\left(2\pi m_{HCl}k_bT\right)^{\frac{1}{2}}}\left(\frac{E_{Etching}}{k_bT}+1\right)\exp\left(-\frac{E_{Etching}}{k_bT}\right) \quad (27)$$

The Ge partial pressure from the oxide surface should be added to the vertical Ge partial pressure to extract the Ge composition. Eq. 17 can then be rewritten as:

$$\frac{x^2}{1-x}=\alpha\exp\left(\frac{0.7eV}{k_bT}\right)\left(\frac{P_{GeH_4}+\left(BP_{GeH_4}\ln\left({}^{1}/_{c}\right)\right)-(1-\lambda)P_{HCl}}{P_{SiH_2Cl_2}-\lambda P_{HCl}}\right) \quad (28)$$

In Figure 4.22, model and experiment results are shown for the proof of sanity. As it is perceived there is a good agreement between the model and the experiment for fully–patterned wafers.

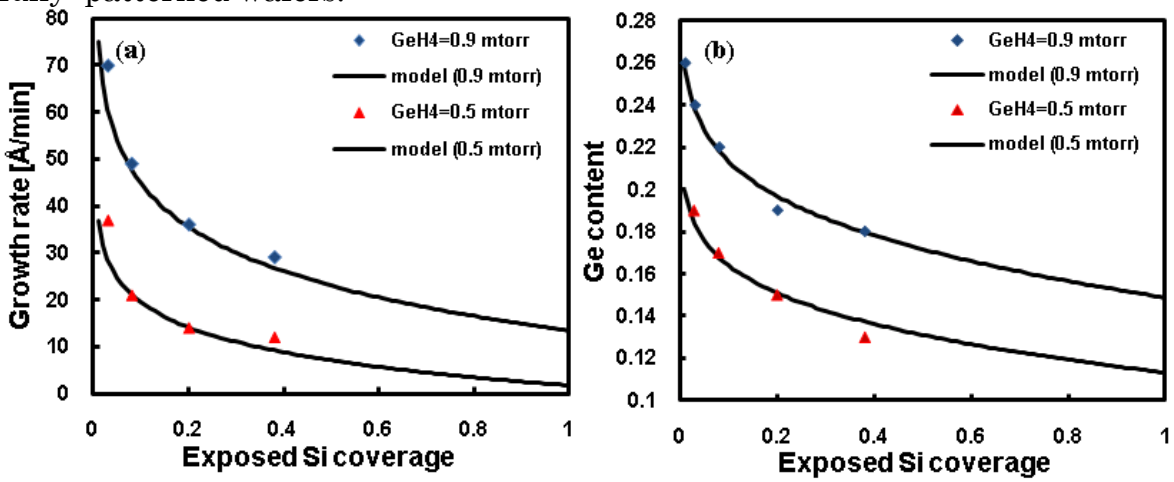

Figure 4.22 a) Growth rate vs. chip exposed Si coverage and b) Ge content vs. chip exposed Si coverage for different fully–patterned wafers at 20torr total pressure. The applied PDCS and PHCl partial pressures were 60 and 20 mtorr, respectively.

As mentioned earlier, the SEG of SiGe has been used recently in the Si industry at 32/20 nm CMOS technologies. In this application, high exposed Si coverage (~10%) with submicron openings has been employed as the substrate [49]. Therefore, in this part of the study a fully–patterned substrate with 10% exposed Si coverage (see Figure 4.23) using 100nm opening was fabricated. Hole Colloidal Lithography (HCL)

was employed to produce a uniform pattern all over the wafer. The experimental and calculated growth rates were 51 and 46 Å/min, respectively. This can simply benchmark the model for 32/20 nm node technology.

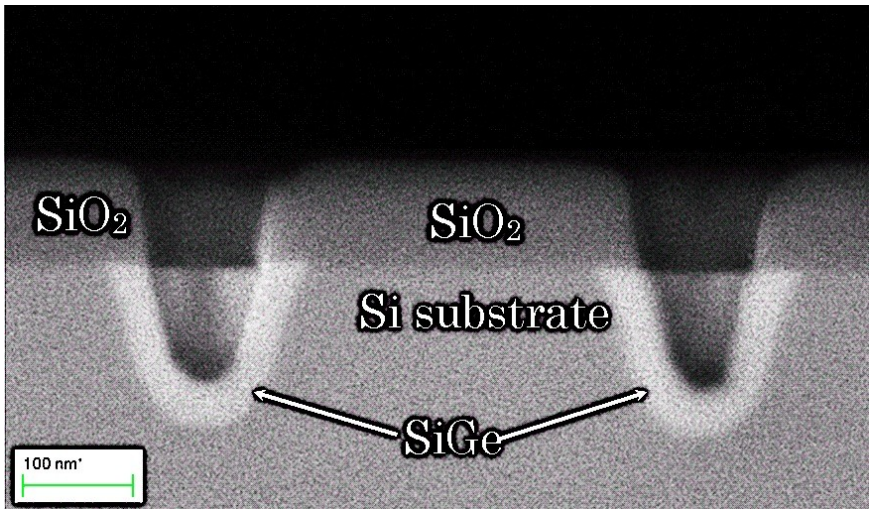

Figure 4.23 The cross-sectional high resolution scanning electron microscopy picture of SiGe epitaxy inside 100nm openings. The applied PDCS, PGeH4 and PHCl partial pressures were 60, 0.9 and 20 mtorr, respectively.

3.5. Modeling of SEG of SiGe on a non-uniform pattern

So far in this study, wafers have been uniformly patterned with same chip repeated all over the wafer. But in reality, the fabrication dies include chips with different exposed Si coverage (different opening sizes and densities). In order to develop the model for a real pattern, the interaction between the openings and chips must be taken into account.

As discussed earlier, there is a driving force *f*, for the species to be attracted to the dangling bonds inside the openings. This attraction force is strong close to an opening and decays gradually further away as an inverse function of distance (estimated by K/r where r is distance and K is a constant). Since a chip contains many openings then the driving force over species will be exerted non–linearly depending on the exposed silicon coverage of the chip, c. In this case, the driving force equation for an array opening in a chip can be expressed by:

$$\iint f(x,y)dxdy = \alpha Kc + \beta K\sqrt{c} \qquad (29)$$

where the linear and non–linear terms are calculated as $\alpha = 0.24649$ and $\beta = 1.1186$. Using this equation, one can calculate the effects of chips on the diffused molecule from the boundary layer. By increasing the exposed Si coverage of the chip, the lateral gas–phase attraction of the diffused molecules increases. These molecules coming laterally in the gas–phase will be consumed by openings located along a distance of 5τ from the edge of the chip. As the exposed Si coverage of the chip increases, the τ value decreases. The chip consumption length (τ) is defined as follows:

$$\tau = \frac{1}{\alpha K c + \beta K \sqrt{c} + \delta} \tag{30}$$

where δ is added to consider the collisions between the species before arriving at the consumption sites. The above equation demonstrates that by increasing the exposed Si coverage on chips with uniform patterns, the migration length of the gas molecules above the chip decreases. These molecules are mostly consumed in openings closer to the edge of the chip. Empirical calculations showed that with the following numbers the best results were achieved for this model:

$$K\alpha = 0.0004\ \mu m^{-1} \quad K\beta = 0.0011\ \mu m^{-1} \quad \delta = 0.00048\ \mu m^{-1}$$

In order to finalize the model for SEG of SiGe, another mask was designed and utilized to establish a model for interaction between the chips (see Figure 4.24). The main idea of the modeling is based on the non–uniform gas consumption among the chips. During growth, the chip with more exposed Si coverage (so–called a trap–chip) attracts the gas molecules from the vertical component of the surrounding chips. On the mask for this study, the Si coverage of the surrounding chips (1%, 2.7% and 8% exposed Si coverage) were smaller than that of the central chip (2.7%, 8%, 19.75% and 37.85% exposed Si coverage).

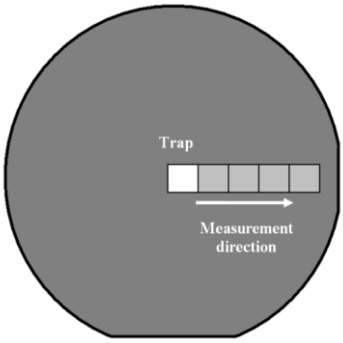

Figure 4.24 The mask design used to establish the interaction model between the chips

The trap–chip has a strong influence on the surrounding chips; however, the chips which are positioned far enough do not feel the presence of the trap. Thus, the growth rate as a function of distance from the trap ($R_T(d)$) is expressed in the following manner:

$$R_T(d) = R_{Trap} + \left(R_{Surr} - R_{Trap}\right)\left(1 - e^{\frac{-d}{\tau(c_{surr})}}\right) \tag{31}$$

where d is the distance from the trap-chip and c_{Surr} is the exposed Si coverage of the surrounding chips. In this equation, the exponential function determines the interaction between the chips; the variable τ is a function of exposed Si coverage (see eq. 30). The input parameters R_{Trap} and R_{Surr} can be obtained from eq. 27 in different cases. The growth rate results of the experiment and the interaction model are demonstrated in Figure 4.25. As it has been shown in Figure 24, the trap-chip is surrounded by chips on the right and by oxide on other directions. Openings close to the trap are significantly impacted by the depletion volume of the trap-chip. In this volume, many of the gas molecules either in the gas-phase or on the surface are consumed by the trap-chip and thus the number of molecules available for the

surrounding chips is reduced considerably. The trap-chip has no influence on the growth rate of openings positioned far away from it.

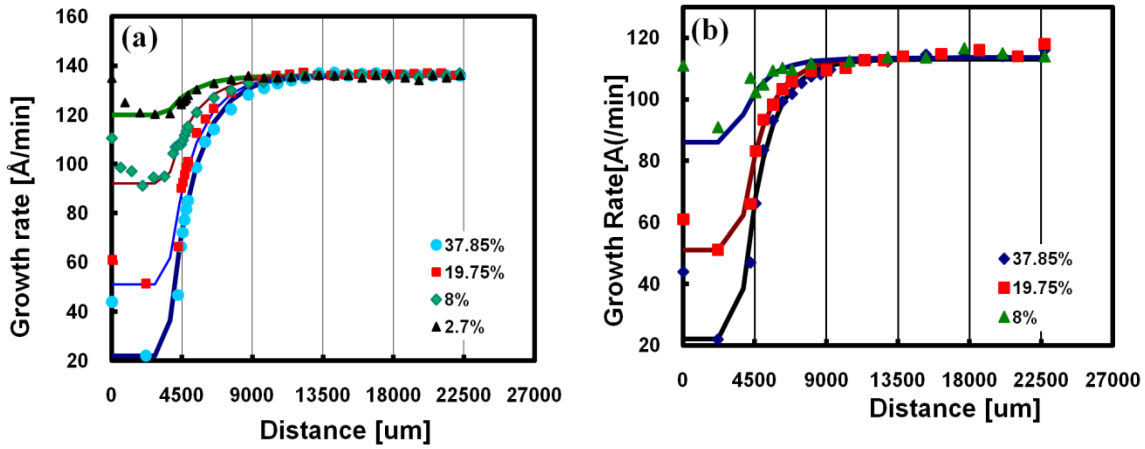

Figure 4.25 The measured (dots) and calculated (lines) growth rate of an array of openings along five chips. a) The trap–chip (first chip from left) has an exposed Si coverage of 2.7, 8, 19.75 and 37.85% where this value is about 1% for the surrounding chips. b) The trap has an exposed Si coverage of 8, 19.75 and 37.85% where this value is 2.7% for the surrounding chips. The applied P_{DCS}, $P_{GeH4}$and P_{HCl} partial pressures were 60, 0.9 and 20 mtorr, respectively.

3.6. Model description

In this part, a guideline to apply the model for advanced designs is presented. This can provide the process designers with the required information to implement this model in a real fabrication line. In most of the chips in production, there are different opening sizes and densities. First step is to spot different exposed Si coverages which are repeated over the wafer. As an example, Figure 4.26a shows an example of a mask with three sub–divisions. The exposed Si coverage, "c", of these sub–divisions are assumed to be 3, 8 and 20% (see Figure 4.26a). In this example, the applied P_{DCS}, P_{GeH4} and P_{HCl} partial pressures were respectively 40, 1.5 and 60 mtorr and the epitaxy growth was performed at 685˚C and 10 torr.

Next step is to calculate the growth rate, Ge content and consumption length (τ) for each sub–division individually using Eq. 27, 28 and 30, respectively (these calculated data are displayed in Figure 4.26a). In this figure, the sub–division with highest exposed Si coverage (20%) is the dominant sinkhole, i.e. most of the coming gas molecules are consumed in this part. In this example, sub–division 1 (20%) does not affect sub–division 2 since they are placed far enough from each other (1 cm which is larger than 5τ for these sub–divisions). Thus, using Eq. 31, one can estimate the interaction of both sub–divisions 1 and 2 with sub–division 3.

As cited before, the interaction model determines the influence of sub–divisions on each other as a function of distance (see Figure 4.26b). Due to the additive nature of these interactions, the final growth rate profile of sub–division 3 can be predicted (shown in red color curve in Figure 4.26b). In this way, this model not only provides the layer profile for specific area, but also calculates the pattern dependency of the epitaxy growth.

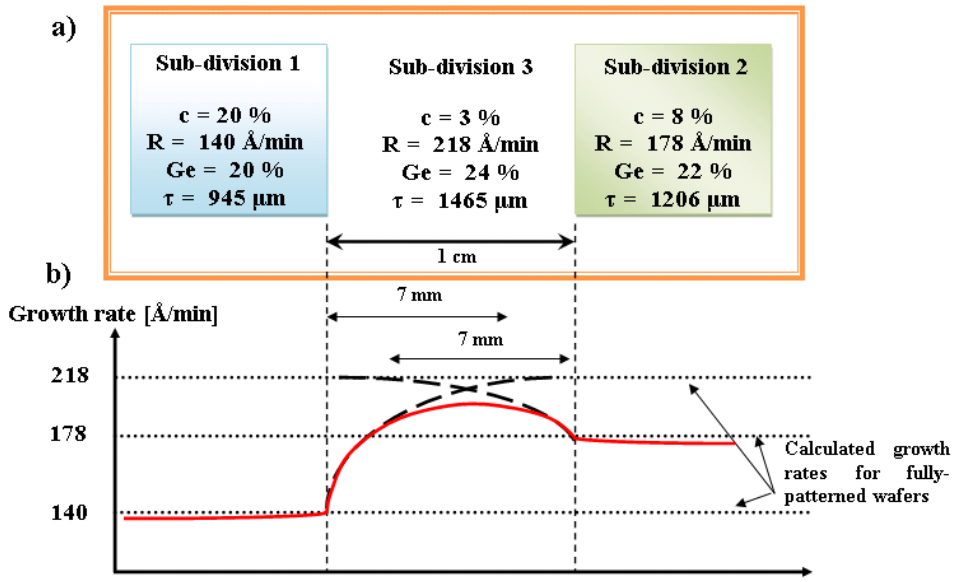

Figure 4.26 Simple demonstration of applying the model for a "real chip"; a) an illustration of a "real chip" layout and b) the instruction of how the interaction model can be used

3.7. Modeling of the SEG of SiGe for recessed openings

In order to prepare samples with recessed openings, reactive ion etching (RIE) was used to create recess inside the fully–patterned oxide mask. CF_4, HBr, and Cl_2 gases were applied to etch Si through the oxide mask.

In order to conform to the empirical model, two different recess depths (100 and 200nm) were examined for this study. A fully–patterned substrate with 8% exposed Si coverage uniformly distributed over the whole wafer (1×1 μm^2 openings placed 2.5 µm from each other) was used for this experiment.

The layer thickness was measured at the center of the openings due to the facets at the edges. These data demonstrate that the growth rate is affected by the recess depth, where deeper openings acquire moderately lower growth rates. An explanation for the growth rate behavior is that the number of dangling bonds on the inclined facets e.g. (113) is more (11.8×10^{14} atom/cm^2) than the facet (100) with 6.8×10^{14} atom/cm^2 available sites.

Another reason can be related to the influence of facets formed at the edges by the recessed etch. The atoms may diffuse from these facets towards the center of the opening. Previous theoretical studies have demonstrated this atomic theory of migration from the inclined planes towards (100) plane [50-52]. As a result, the growth rate of the inclined planes becomes lower than the center.

In principle, the growth rate behavior depends on the gas consumption where the diffusion of the adatoms, chemical reactions and the dangling bonds are the main parameters. For different recessed depths, the number of dangling bonds varies; but since the ratio of Si to Ge flux is still constant, the Ge content is expected to be constant. This means that the recessed depth will not have impact on the Ge

content. Figure 4.27 illustrates the Ge content for the recessed and unprocessed openings.

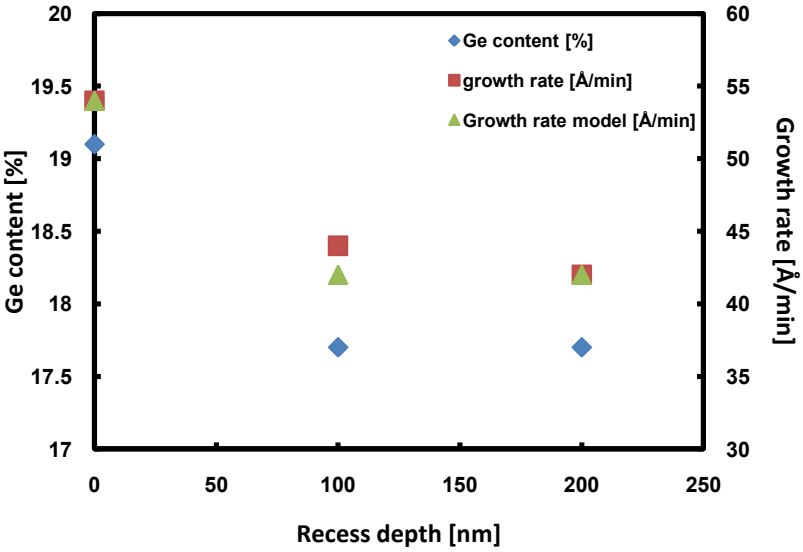

Figure 4.27 The measured and calculated growth rates and Ge contents on fully–patterned wafers with either recessed or unprocessed openings all acquiring 8% exposed Si coverage. The applied P_{DCS}, $P_{GeH4}$and P_{HCl} partial pressures were 60, 0.9 and 20 mtorr, respectively.

The Ge contents are the same for both recessed depths, but are less than the unprocessed openings. This difference of Ge content can be connected to the diffusion of Ge from the oxide surface towards the exposed Si area. Inside the recess, the diffused Ge atoms are engaged with the dangling bonds on the recess walls; this reduces the ratio of the atoms available for incorporation on (100) plane. Therefore, to extract the Ge content value for a recessed opening, one must only change B in eq. 28 to B/2:

$$\frac{x^2}{1-x} = \alpha\, exp\left(\frac{0.7eV}{k_bT}\right)\left(\frac{P_{GeH_4}+(\frac{B}{2}P_{GeH_4}\, ln(1/c)) - (1-\lambda)P_{HCl}}{P_{SiH_2Cl_2} - \lambda P_{HCl}}\right) \quad (32)$$

This change can directly be exerted unto eq.27 for the growth rate calculation. The results of the growth rate model and experiment for selective epitaxy growth on recessed and unprocessed openings are also illustrated in Figure 4.27.

3.8. Time dependency of the growth

More study on the growth rate behavior has been performed by investigating deposition behavior versus time and recess depth. Two different recess depths of 100 and 200nm were considered in this experiment. SiH_2Cl_2, GeH_4 and HCl partial pressures were 60, 0.9 and 20 mtorr, respectively. Figure 4.28 shows the growth rate of SiGe layers in the recessed and unprocessed openings. Since there are facets at the edges, then the layer thickness was measured by AFM at the center of the openings.

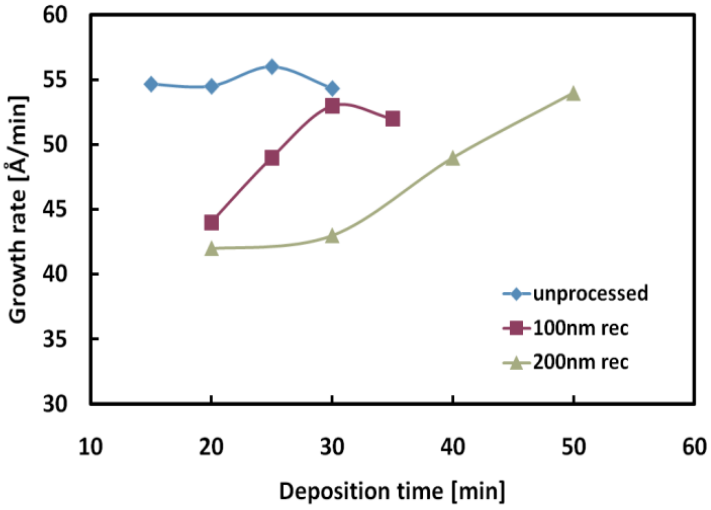

Figure 4.28 Illustrates the momentary growth rate of the recessed and unprocessed openings with 8% exposed Si coverage using 1×1 μm² openings.

Each point in this figure is calculated from the layer thickness divided by the growth time. The growth rate is almost constant for unprocessed openings whereas it increases for recessed ones. These data demonstrate that the growth rate is also affected by the recess depth and lower for deeper one.

This behavior is expected since the number of dangling bonds decreases continuously during the epitaxy. Another reason can be related to the influence of facets formed at the edges by the recess etch. During the epitaxy, the incoming atoms may diffuse from these facets towards the center of the opening. Previous theoretical studies have demonstrated this atomic diffusion theory from the inclined planes towards (100) direction [50-52].

Another explanation for the growth rate behavior is that the number of dangling bonds on the inclined facets e.g. (113) and (111) is higher than the facet (100). As a result, the growth rate on the inclined planes becomes lower than the center.

This theory is difficult to be proved directly, but the layer profiles in the cross–sectional HRSEM micrographs in Figure 4.29 show some evidence about how an opening is filled for different deposition times. During the growth in the unprocessed openings, edge–facets are formed at the initial stage but it becomes flattened afterwards. However, for the recessed openings, the facets have already existed from the beginning and the growth occurs on the facets where the surface recovers after longer time.

Another important issue for the growth of recessed openings is that the SiGe layers exceed the critical thickness earlier than the unprocessed openings [53]. This can be argued when the growth occurs on Si inclined walls (recessed opening) compared to unprocessed openings surrounded with oxide. In the latter case, there is no deposition on the oxide wall and the SiGe grows isolatedly on the center of the opening, however, in the recessed growth, the relaxed SiGe from the surroundings has strong influence on the strain amount in the center. The role of strain relaxation on the growth kinetics is unknown and more investigations are necessary to be executed, but it is predicated that it will increase the growth rate.

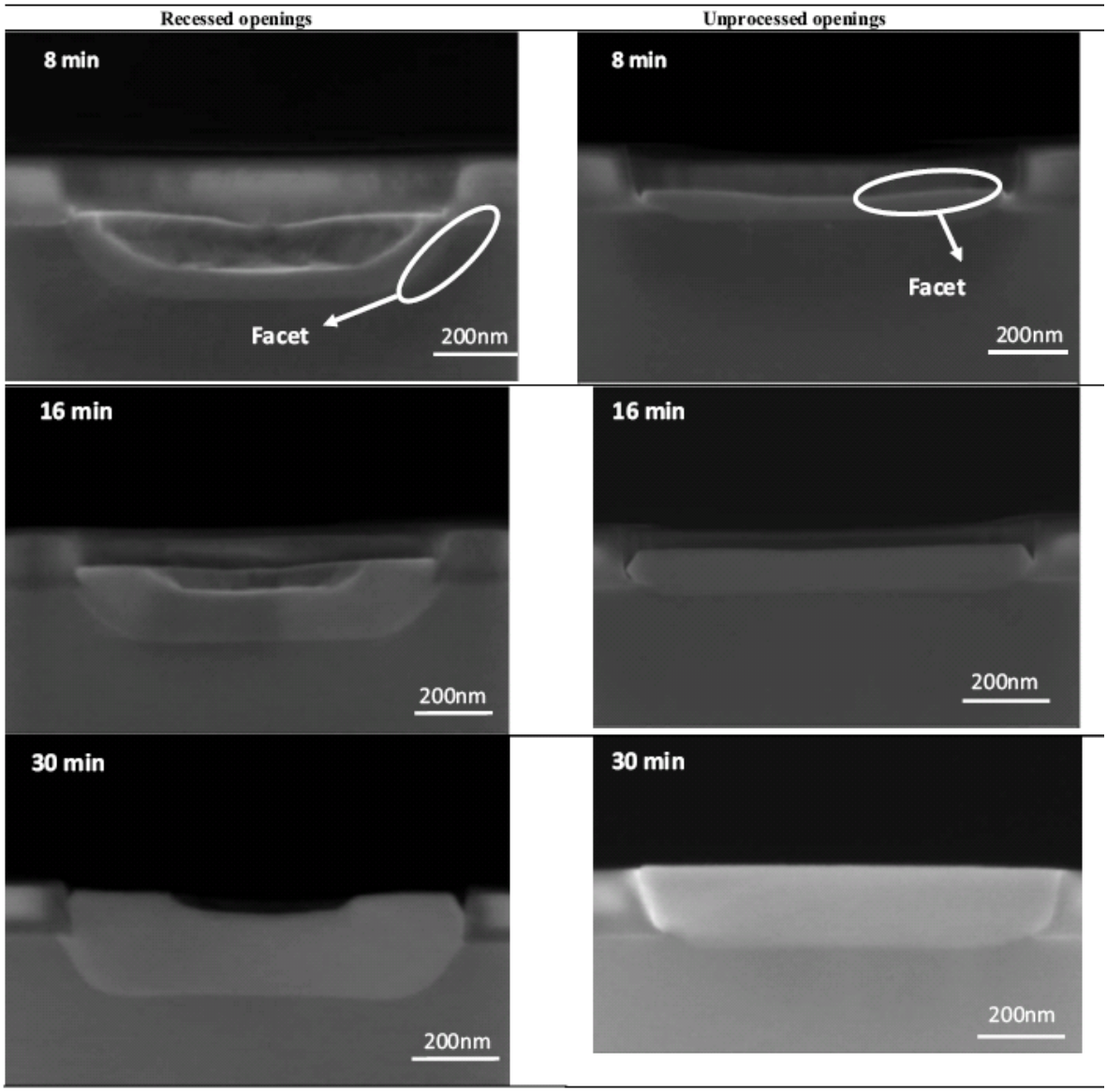

Figure 4.29 Cross–sectional view of SiGe layers inside recessed and unprocessed openings.

As mentioned earlier, for different recessed depths, the number of dangling bonds is varied, but since the ratio of Si to Ge flux is still constant then a constant Ge content for the samples is expected. This means that the recess depth will not have any impact on the Ge content. Figure 4.30 illustrates the Ge content for two recess depths and unprocessed openings shown in Figure 4.28. The Ge contents for the both recess depths are similar, but lower than the unprocessed openings. This difference of Ge content can be related to the diffusion of Ge from the oxide surface towards the exposed Si area. Inside recess, the diffused Ge atoms are engaged with the dangling bonds on the recess walls which results in lower ratio of these atoms available for incorporation on (100) plane. This amount of Ge atoms on the wall leads to even higher etch rate of Si atoms and faster relaxation of these layers.

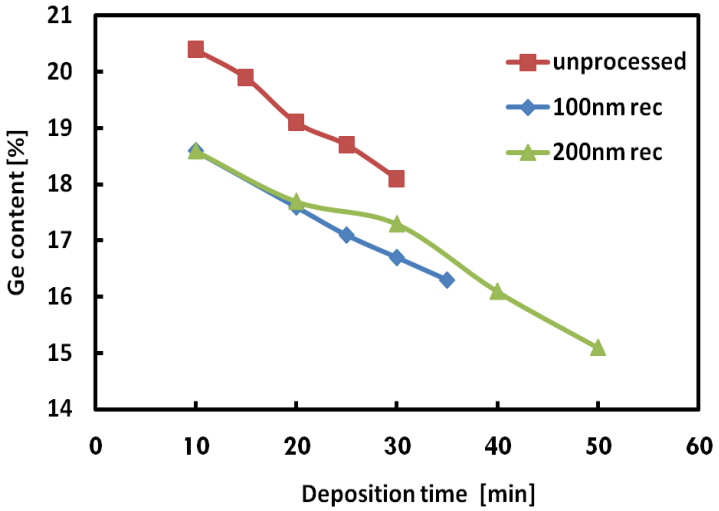

Figure 4.30 Illustrates the Ge content of the recessed and unprocessed openings with 8% exposed Si coverage using 1×1 μm² openings.

Another important issue in this figure is the grading of Ge content (or strain). It was predicated since the SiGe layers experience a strain relaxation during epitaxy when the grown layer becomes thicker. The previous results have reported that the incorporation of dopant depends on the strain and the growth rate [54,55]. Both the higher growth rate and the strain reduction versus time may result in a grading dopant concentration in SiGe layers. The pattern dependency, dopant interaction and non–uniform growth behavior result in a very complicated scenario for the kinetics of selective epitaxy of SiGe layers.

4. Summary

In this chapter, an empirical model to predict the growth rates and compositions of $Si_{1-x}Ge_x$ layers grown on patterned substrates by RPCVD was presented. The model explains the growth kinetics through gas phase processes and related surface reactions.

A good agreement between the model and the experimental data of the growth profile has been achieved. This model can be utilized in its current form in the manufacturing line to predict the pattern dependency and layer profile of CVD deposited layers. It is also capable of providing a 2D layer growth simulation for any provided pattern (deposition mask). This model is based on different input parameters, such as dichlorosilane, germane, hydrochloric acid partial pressures, growth temperature and mask layout. The output parameters consist of the growth rate and Ge content. The interaction between chips (sub–chips) on a wafer was modeled using a new approach.

The pattern dependency of selective epitaxial growth of B– and/or C–doped SiGe layers in recessed and unprocessed openings has been presented. The profile of the grown SiGe layers appeared to be non–uniform versus deposition time in recessed

openings. The Ge content of the SiGe layers grown in the recessed openings is independent of the recess depth when the gas ratio is expected to be consumed constantly. The Ge content or strain is graded vertically due to the fact that the layer thickness usually exceeds above the critical thickness. Finally, the strain compensation amounts due to the C– and B–doping in SiGe matrix are additive.

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CHAPTER 5

GROUP IV-BASED THERMISTORS FOR INFRARED DETECTION

1. Introduction

1.1. Infrared spectra

Infrared (IR) radiation is a part of electromagnetic spectra with a wavelength between 0.7 and 300 μm, corresponding to a frequency range of ~1 and 430 THz. There is a special division of the IR spectra which distinguish the region and the application of the radiation. Here are more details on abbreviations for IR spectra:
Near–infrared (NIR) relates to wavelengths of 0.75–1.4 μm and can be absorbed by water and shows low attenuation losses in the SiO_2 glass (silica) medium. The main application appears in fiber optic telecommunication.
Short–wavelength infrared (SWIR) indicates an interval of 1.4–3 μm where the water absorption is significantly observed at 1450 nm. In this range, wavelengths of 1530 to 1560 nm are dominant for long–distance telecommunications.
Mid–wavelength infrared (MWIR) refers to 3–8 μm wavelengths and has a strong military application in 'heat seeking' in missile's head. The IR signature seeks the exhaust plume of the target aircraft jet engine.
Long–wavelength infrared (LWIR) is 8–15 μm part of the spectra which is used for "thermal imaging". This concept has been employed in night vision cameras especially for the car industry.
Far–infrared (FIR) is a region of the electromagnetic spectra with a wavelengths in range of 15–1000 μm. This group of waves has a close application with THz region. A highly demanded application for this wavelength interval concerns FIR lasers which are used for THz imaging and THz time–domain spectroscopy. The main purpose of manufacturing these equipments is to detect explosive materials and chemical warfare agents for future security applications.

1.2. A Brief overview of thermal detectors

Early 1950s was a period when the first extrinsic photoconductive IR detector using impure Ge was manufactured. The impurity level in Ge material determined the IR spectral window at that time, but a full control of operating wavelength was not fulfilled [1]. The extrinsic Si was the next candidate as an alternative material after about 10 years. A tremendous development towards advanced design detectors was taken in 1973 when both detection and read–out circuit were implemented using the Si platform. The Schottky barrier height in metal/silicide–Si system was used for IR detection by Shepherd and Yang [2]. Simultaneously, narrow bandgap material platform was being developed to extend the detection wavelength range and sensitivity. In 1982, the first thin film–based bolometer with the objectives of robust, low cost, uncooled thermal detection, small element size (< 0.1 mm), fast speed of response (1.0 msec) and a detectivity exceeding 1×10^8 $cmHz^{1/2}W^{-1}$ was manufactured [3,4]. Bolometer is a sensitive thermistor to measure the energy of incident electromagnetic radiation.

Since 1950, many materials have been examined for sensing different IR ranges. The uncooled bolometers have become the technology of choice for LWIR detection. The detector operates through the response of thermistor material to temperature variations. These bolometers are preferred nowadays since they are smaller and cheaper to use. The figure of merit for the thermistor in such devices is that it simultaneously acquires high temperature coefficient of resistance (TCR) and high signal–to–noise (SNR) ratio.

The most widely used approach today for thermal detection is to implement microbolometers using surface micromachined bridges on CMOS read–out processed wafers [5-17]. Currently, there are microbolometer arrays with high performance similar to the cooled photon detectors [5,6]. However, there are issues concerning the fabrication process of these detectors. After CMOS fabrication, thermistor material should be deposited which is followed by a complicated post–CMOS surface micromachining. This consequently limits the use of such detectors for commercial applications. Today's mostly known and widely used thermistor material is vanadium oxide (VO_x) with a high TCR of about 2–3%/K [7] but incompatible with standard Si fabrication and toxic material. The integration of VOx requires a dedicated expensive process line to prevent contamination of the CMOS fabrication line.

The IC compatible thermistor materials are amorphous phase of silicon [8-11], silicon–germanium [12], silicon carbide [13] and poly– [14] or single–crystalline silicon–germanium [15-19] which have also exhibited high TCR values (2–5%/K).

The poly–crystalline materials require a thermal annealing treatment to reduce their residual stress. This step is necessary otherwise the micro–machined membrane of such materials bends up or down depending on the stress type. It is worth mentioning here that any thermal treatment is not suitable for post–CMOS processing. The poly–based thermistor materials exhibit also higher *1/f* noise due to defects and their non–crystalline structure. For high performance bolometers, high signal–to–noise ratio is an important parameter in order to obtain an accurate signal for sensitive IR imaging. For these reasons, the single–crystalline thermistor material is an excellent alternative for high performance thermal detectors [15]. Another high TCR material in the market is YBaCuO which requires complicated and expensive post–CMOS surface micromachining processes [20,21]. The other IC compatible thermistor materials are metal films [22,23] which suffer from low TCR and post–thermistor deposition steps.

1.3. IR detector categories

The research funding has been mainly focused on two IR ranges: MWIR (3–5 μm) and LWIR (8–14 μm). Nowadays, the development in IR detectors has changed its orientation towards semiconductor IR detectors. The IR detectors are categorized in two classes; photon detectors and thermal detectors. In the first class, the electrons' band transition is the result of the radiation absorption. These electrons may be free electrons or bound to a lattice atom or impurity. The observed output signal will be

magnified in a complementary read–out integrated circuit (ROIC). One important issue in these detectors is their selective wavelength response which complicates the design of these detectors. However, high signal–to–noise performance and very fast response are the main advantages of these detectors. A drawback of photon detectors is that their functionality depends on the cryogenic cooling. This is due to the thermal generation of charge carriers which makes the non–cooled devices very noisy. The cryogenic cooler makes them heavy, expensive and inconvenient to use for civil applications. The photon detectors are sub–divided into different groups depending on the nature of the interaction. The most important ones are: intrinsic, extrinsic, photoemissive (metal/silicide Schottky barriers), and quantum well detectors.

In contrast to photon detectors, thermal detectors typically operate at room temperature. This class of detectors has had modest sensitivity and slow response but they are cheap and easy to use. This could be the reason why recently, they have attracted attention for both military and civil applications, especially for car industries. The thermal detectors are also sub–divided to three major categories: bolometers, pyroelectric and thermoelectric detectors. A change in the internal electrical polarization is the physical phenomenon in pyroelectric detectors which converts into an output signal. But in bolometers, the thermistor material absorbs infrared radiation. This changes the resistivity of these pixels which finally turns to an electric signal. The fact that the signal is not dependent on the photonic nature of the radiation makes the thermal detectors generally wavelength independent. However, the output signal depends upon the radiant power or its rate of change.

2. Thermal detection concept

As discussed earlier, thermal detection can be performed through variation of a temperature–dependent mechanism e.g. thermoelectric voltage, resistance, pyroelectric voltage. The detector may be simply represented by a thermal capacitance C_{th} coupled via the thermal conductance G_{th} to a heat sink at the constant temperature T. When the detector is exposed to radiation, the temperature variation can be calculated through the heat balance equation. For any thermistor assuming periodic radiant power, temperature variation is given by [24,25]:

$$\Delta T = \frac{\varepsilon \Phi_0}{(G_{th}^2 + \omega^2 C_{th}^2)^{1/2}} \quad (1)$$

where ΔT is the optically induced temperature variation due to the incident radiation Φ ($\Phi_0 \exp(i\omega t)$) and ε is the emissivity of the detector. The usual procedure employed in bolometer detectors to achieve a good IR absorption is depositing a transparent thin metallic film on top of the device. Free electron absorption in metal films guarantees the absorption of about 50% of the incident IR radiation [4]. In order to further enhance infrared absorbance, the detector architecture employs a resonant cavity. The resonant cavity involves an absorbing membrane suspended at a distance "d" above the cavity reflector metal. The resonant absorbance peaks

correspond to the condition for minimum reflectance. Figure 5.1 [26] shows the first three resonance absorbance peaks including the fundamental λ/4–, 3λ/4– and 5λ/4– resonance spanning the LWIR spectral band.

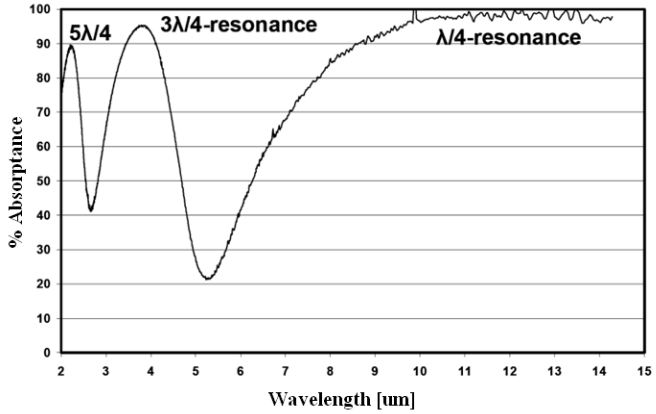

Figure 5.1 Resonant absorbance of a–Si/a–SiGe quarter–wave resonant cavity pixel design exhibiting λ/4– resonance; 3λ/4–resonance; and 5λ/4–resonance [26].

Exploiting this resonant cavity in the detector design allows substantial reduction in the amount of absorbing material to reduce the mass of the pixel [24].

In order to increase the temperature response of the detector, the thermal capacity of the detector (C_{th}) and the thermal coupling to its surroundings (G_{th}) must be as small as possible. The thermal contacts of the detector with surroundings should be reduced while the interaction with the incident beam must be optimized. Thus, the thermal response time (τ_{th}), another important feature of the thermal detection, can be written as:

$$\tau_{th} = \frac{C_{th}}{G_{th}} = C_{th}R_{th} \tag{2}$$

The typical response time for a thermal detector is in millisecond range which is longer than that of photon detectors (microsecond range). Eq.1 can then be rewritten as:

$$\Delta T = \frac{\varepsilon \Phi_0 R_{th}}{(1+\omega^2\tau_{th}^2)^{1/2}} \tag{3}$$

It can be concluded that there is always a compromise between the working frequency range and the sensitivity of the detector. This means that the detector sensitivity is higher for lower frequency range.

The voltage responsivity of the detector is given by the ratio of the output voltage signal (V_s) to the input radiation power (Φ_0):

$$R_V = \frac{V_s}{\Phi_0} = \frac{K\Delta T}{\Phi_0} \tag{4}$$

where the generated output voltage is assumed to be linearly proportional to the temperature difference and K is linearly dependent on the thermistor TCR value. Substituting eq.3 in eq.4 results in the following equation [4]:

$$R_V = \frac{V_s}{\Phi_0} = \frac{|\alpha| V R_b R_L \varepsilon R_{th}}{(R_b+R_L)^2(1+\omega^2\tau_{th}^2)^{1/2}} \tag{5}$$

It can be deduced from the final expression that at low frequencies ($\omega<<1/\tau$), the responsivity is proportional to the thermal resistance of the detector (R_{th}) and not the thermal capacitance. This is exactly the opposite at high frequencies. As the operating frequency increases beyond the cut–off frequency ($f = 1/2\pi\tau$) the responsivity of the detector rapidly declines. Thus, good responsivity can be achieved by using a high TCR thermistor which is a characteristic of semiconductors rather than metals, and by minimizing G_{th} through a good thermal isolation of the bolometer.

Noise is a stochastic random process which limits the IR detectivity of the devices. Noise voltage or noise current of a device is the summation of many contributions from different sources. Noise sources in electronic devices can be divided into two main groups; a) external or extrinsic sources which are in the surrounding of the device and b) Internal or intrinsic sources which generate noise through random fluctuation in the carrier transport.

The thermal noise, so–called Nyquist or Johnson noise, is caused by random thermal motions of the charged carriers in a material which is similar to the Brownian motion of particles. In a conductor material, at non–zero temperature T, electrons vibrate randomly depending on T. This noise in a Δf bandwidth for a resistor R is expressed by:

$$V_J^2 = 4kTR\Delta f \tag{6}$$

where k is the Boltzmann constant. Since Johnson noise is proportional to $(TR\Delta f)^{1/2}$, it can be minimized by the use of lower resistance bolometers, lower operating temperature and narrower bandwidth. However, the actual bolometer application requires a finite limit to the bandwidth through the scanning and read–out of the detectors and ambient operation temperature. This suggests preferred use of low resistance bolometers; however such a solution may not always be the case depending on the bandwidth and the TCR value.

Thermal or temperature fluctuation noise is another source of noise which must be discussed to evaluate the detectivity of the device. An exchange of the heat between the sensitive area of the detector and the surrounding substrate (which is in thermal contact with the detector) introduces a random fluctuation in the temperature and this will transform in the form of an electric noise because of the coupling between the temperature and the resistance. Temperature fluctuation is expressed as follows [24,25]:

$$V_{th}^2 = \frac{4kT^2\Delta f}{(1+\omega^2\tau_{th}^2)^{1/2}}K^2R_{th} \tag{7}$$

The other important source of noise for IR detection is the "background noise". Heat exchange due to radiation between the detector at temperature T_d and the environment at temperature T_b generates voltage noise which is so–called "background noise". The expression is given by [24,25]:

$$V_b^2 = \frac{8k\varepsilon\sigma A(T_d^2+T_b^2)}{1+\omega^2\tau_{th}^2}K^2R_{th}^2 \tag{8}$$

However, *1/f* noise or Flicker Noise is the most predominant noise at low frequency in semiconductor thermal detectors. *1/f* noise can be evaluated by the noise

constant: $K_{1/f} = \gamma/N$ where N is the total number of free charges and γ is known as the Hooge's constant [27]. There is no unique and exhaustive theory to justify the presence of *1/f* noise; nevertheless, the interactions of carriers with defects, surface states and other events (e.g. recombination and trapping–detrapping) are the major causes of *1/f* noise in semiconductors. Because of its uncertain origin, particularly in the bolometer case, a simple expression for voltage power spectrum density (PSD) is as follows:

$$S_V = \frac{K_{1/f} V_{bias}^{\beta}}{f^{\gamma}} \tag{9}$$

where $K_{1/f}$ is a noise constant, which is generally smaller for single–crystalline (sc) materials in comparison to polycrystalline or amorphous ones. The frequency exponent γ is close to 1. The *1/f* noise voltage can be demonstrated as:

$$V_{1/f}^2 = \frac{K_{1/f} I^{\beta}}{f^{\gamma}} \Delta f \tag{10}$$

The parameters γ, ß and $K_{1/f}$ are dependent on the material, processing, metal contacts and surfaces. Thus, it is very difficult to calculate them analytically. The square of total noise voltage (V_n) may be written as:

$$V_n^2 = V_J^2 + V_{th}^2 + V_b^2 + V_{1/f}^2 \tag{11}$$

When a thermal detector absorbs the electromagnetic radiation, both output signal and noise will be generated. High amplitude output signal and low noise level (high signal–to–noise ratio) are desired in IR detectors. To evaluate the performance of the detector, "Detectivity" may be defined as follows:

$$D = \frac{R_V}{\Phi_0} = \frac{V_s}{\Phi_0 \, V_n} \tag{12}$$

The detectivity is proportional to square root of active area and frequency bandwidth. Therefore, the normalized detectivity D* is given by:

$$D^* = D \times A^{1/2} \times \Delta f^{1/2} \tag{13}$$

In a thermal detector, D* can be expressed as:

$$D^* = \frac{K \varepsilon R_{th} A^{1/2}}{(1 + \omega^2 \tau_{th}^2)^{1/2} (V_J^2 + V_{th}^2 + V_b^2 + V_{1/f}^2)^{1/2}} \tag{14}$$

where A is the pixel area. It can be concluded from eq.14 that the detectivity may be enhanced by increasing the responsivity and/or decreasing the noise. The responsivity, like the Flicker noise, increases linearly with voltage, while the Johnson noise is independent of voltage. At small voltages, the noise is mainly Johnson noise. But, at sufficiently high V, noise is dominated by the Flicker noise and thus D* becomes independent of voltage. According to the previous calculations, while viewing a room temperature background, the highest detectivity for a thermal detector at room temperature is about 2×10^{10} $cmHz^{1/2}W^{-1}$; which can be referred to as the thermal detectors theoretical limitation. The published photon detectors have shown higher detectivities as a result of their limited spectral responses. Another fundamental limitation to the sensitivity of a bolometer is determined by fluctuations in the energy transport between the bolometer (with temperature T_d) and the heat sink (with temperature T_s), and is given by [1]:

$$NEP = \sqrt{4k_B T_d^2 G} \tag{15}$$

The sensitivity of the bolometer can be maximized when T_d rises to $2T_s$ in which the sensitivity can be rewritten as:

$$NEP = \gamma \sqrt{4\frac{k_B T_s \Phi_0}{\eta}\ [\mathrm{WHz}^{1/2}]} \tag{16}$$

where γ is determined from choice of material and thermistor (Mather 1984) and η is the optical absorptivity.

3. General theory of thermistor material

Since the birth of thermal bolometers, particular attention has been given to materials and their growth techniques which can maximize the thermal responsivity and minimize the electronic excess noise. As mentioned previously, the main focus of this chapter is on the thermal detectors. Among this class of detectors, the bolometers are chosen to be the technology for low cost IR imaging system. The heart of a bolometer is the "thermistor" material or structure. The word "thermistor" is actually a contraction of "thermal resistor". It is sensitive to temperature variations which result in resistivity changes; in particular, increasing the temperature decreases the resistivity of the thermistor material. The thermistor material can be chosen by several items [26]: 1) a high temperature coefficient of resistance (TCR); 2) a high signal–to–noise ratio (SNR); 3) a sufficiently low thermal response time constant which leads to a high responsivity; 4) the ability to form a thermally isolated optical cavity from the material; 5) the mature material growth technology that is compatible with integration on a substrate containing the VLSI signal processing functions; and 6) the possibility to manipulate a wide range of bolometer resistance.

Temperature Coefficient of Resistance (TCR), a figure of merit for thermal detection, is the parameter used to quantify the temperature sensitivity and is defined as [19]:

$$\alpha = \frac{1}{R}\frac{\partial R(T)}{\partial T}[K^{-1}] \tag{17}$$

The resistivity is the exponential function of thermal activation energy which is expressed by:

$$\rho = \rho_0 \exp\left(\frac{E_a}{kT}\right) \tag{18}$$

where ρ, ρ_0, E_a and k are the resistivity, measured pre–factor, activation energy and the Boltzmann's constant. In semiconductors, α can be expressed by the activation energy derived from Arrhenius plot:

$$\alpha = -\frac{E_a}{kT^2}[K^{-1}] \tag{19}$$

The thermistors must have either large positive temperature coefficient of resistance (PTC thermistors) or large negative temperature coefficient of resistance (NTC thermistors). The first group includes materials like metals in which the resistance increases with increasing the temperature; whereas, the latter group are

composed of semiconductor materials in which the resistance has a negative temperature dependence.
As mentioned earlier, the noise voltage in thermal detector includes Johnson noise due to the thermal agitation of charge carriers, *1/f* noise due to trapping and de–trapping mechanisms and surface state scattering, and temperature fluctuation noise arising from the fluctuations in the heat exchange between active element and heat sink. In thermistor material, *1/f* noise is the main source of noise and can be quantified by $K_{1/f}$.
$K_{1/f}$ is a material parameter that can vary several orders of magnitude for different materials and even small variations of the material composition can dramatically change the *1/f* noise constant [24]. It is well–known that $K_{1/f}$ is generally smaller for single–crystalline materials in comparison to polycrystalline or amorphous ones. Thus, a solution for increasing the D* of a bolometer is to use mono–crystalline temperature sensing materials with a low *1/f* noise constant [17].
In addition to the parameters involved in the thermal sensitivity, the importance of the electrical contacts on thermistor performance needs to be emphasized. The current–voltage characteristics of the thermistors are greatly influenced by the nature of the metal/silicide–semiconductor interface. Ohmic contact with low resistivity and lifetime stability of the device are the requirements for many applications. However, when large electrical current is involved, a low sheet resistance contact is required to spread the current flow uniformly without localized overheating. A metal with low work function forms an ohmic contact with a n–type semiconductor with surface states. The reverse story is true for a p–type semiconductor. In these cases, introducing higher doping concentration reduces the contact resistance near the contact surface (barrier thinning).

4. Fabrication process flow

Resistive bolometers are mainly composed of a temperature sensing resistor and an IR absorber. A good thermal isolation is the requirement to increase the sensitivity of these detectors. This can be achieved by suspending the bolometer structure in the air through either membrane or bridge support as shown in Figure 5.2.
It was reported in 2004 [12] that noise current of the bridge–supported structures is one order magnitude higher than that of the membrane–supported structure. However, the bridge–supported structure process flow enables a precise control on the resonant cavity length which makes it the dominant design for microbolometers.
The process flow of fabricating a bolometer is very dependent on the thermistor material. For thermistors which can be deposited at low temperatures, there is a possibility to directly integrate on the readout integrated circuit (ROIC) without harming its elements. Amorphous Si, SiGe, Ge, $Ge_xSi_{1-x}O_y$ and VOx are a few examples of such thermistors in the market.

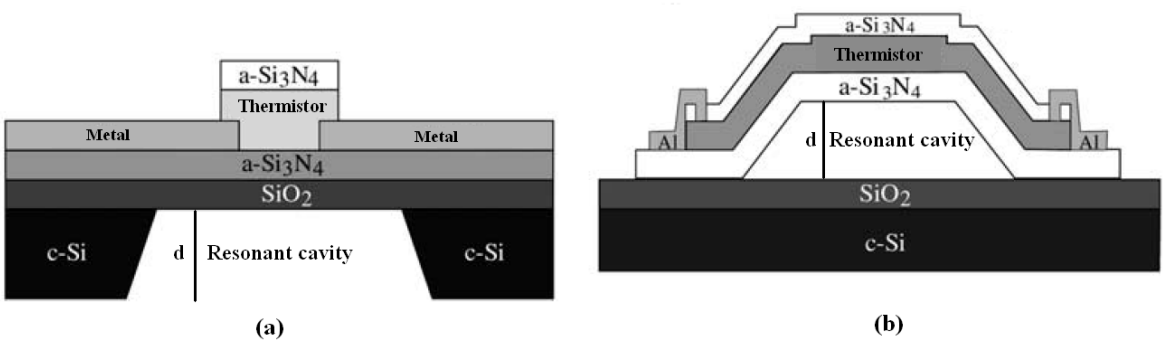

Figure 5.2 Cross-section of a) the membrane-supported and b) the bridge-supported microbolometer [12].

The advantage of mentioned group IV–based materials in this list is the absolute compatibility with the silicon processing line. The process flow is described in Figure 5.3 [28]. The first step is deposition of a thin reflective layer directly on top of the ROIC. A thick sacrificial layer is then spun and cured to form the resonant cavity at the end of the process. The thermistor material is deposited over the sacrificial layer and covered by metallic contact electrodes. The metallic contact deposition and etching enable electrical continuity between the underlying substrate and thermistor on the surface of the sacrificial layer. Finally, the micro–bridge arrays are released by removing the sacrificial layer.

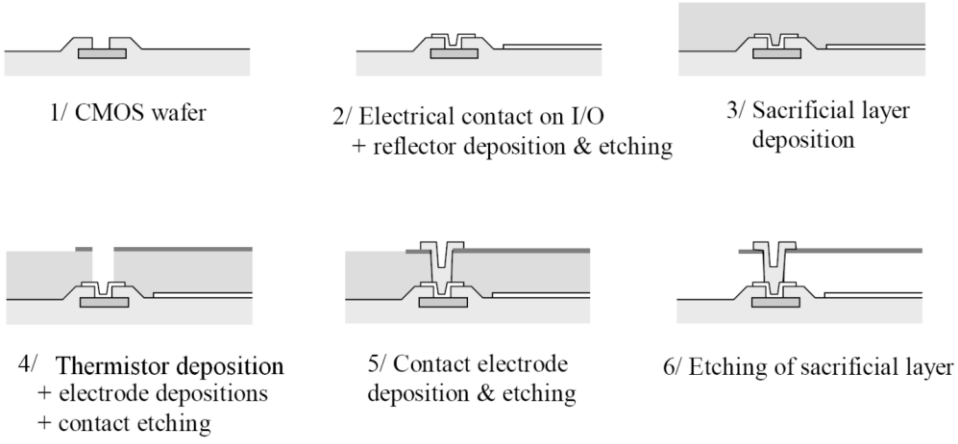

Figure 5.3 Process flow of a bridge–supported microbolometer technology [28].

Another process flow for fabrication of bolometers is through wafer bonding process. Heterogeneous three–dimensional (3D) bolometer integration has been proposed for the integration of high performance mono–crystalline thermistor materials on ROICs [29-31]. In this method, the thermistor material is deposited on a separate carrier wafer. The materials are then transferred from the carrier wafer to the ROIC wafer using low temperature adhesive wafer bonding in combination with sacrificial removing of the carrier wafer as shown in Figure 5.4 [32]. The advantage of 3D bolometer integration is that it allows application of high TCR and SNR mono–crystalline thermistor for imaging application.

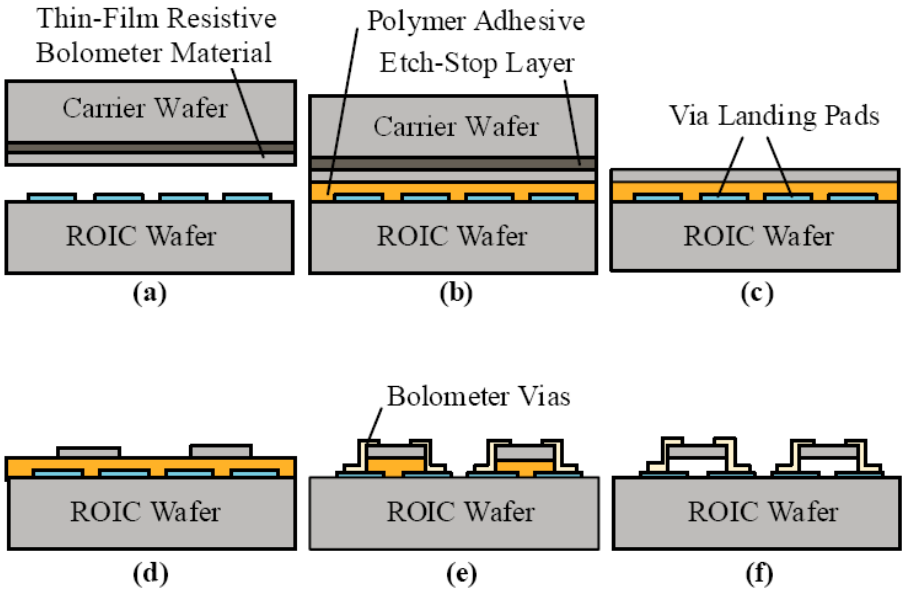

Figure 5.4 Heterogeneous 3D integration for uncooled infrared bolometer arrays: (a) separate fabrication of ROIC wafer and carrier wafer with resistive bolometer material; (b) adhesive wafer bonding; (c) thinning of carrier wafer; (d) bolometer definition; (e) via formation; (f) sacrificial etching of polymer adhesive [32].

5. Thermistor materials

5.1. Amorphous Silicon

In this part, the advantages and drawbacks of bolometers using amorphous Si (a-Si) are presented. The mechanism and characterization results are illustrated and compared to the existing thermistors. This material possesses a number of properties that make it an attractive thermistor material for bolometer application. High TCR values ($1.8 < \beta < 5.5\%K^{-1}$) [33,34] depending on the material growth technique can be achieved (see Figure 5.5 [33]). High TCR comes with high resistance which can be adjusted by doping concentration or hydrogenating the layer. Decreasing the resistance of the thermistor material increases the current and hence the responsivity of the detector. It should be noted here that two–fold extension of TCR from $-2.5\ \%K^{-1}$ to $-5\ \%K^{-1}$ is accompanied by over almost two decades increase in the resistance of the thermistor material. Thus, an appropriate compromise to gain a better responsivity would be the lowest achievable resistivity despite a lesser TCR. Low processing temperature and well–known deposition/etching technologies make this material a competitor for monolithic implementation in bolometers. Its high resistance minimizes pixel array Joule power dissipation and permits continuous sampling/integration of all pixels in the focal plane array (FPA). This can be done using a constant detector bias [26] on the one hand; and decreasing the signal–to–noise ratio on the other.

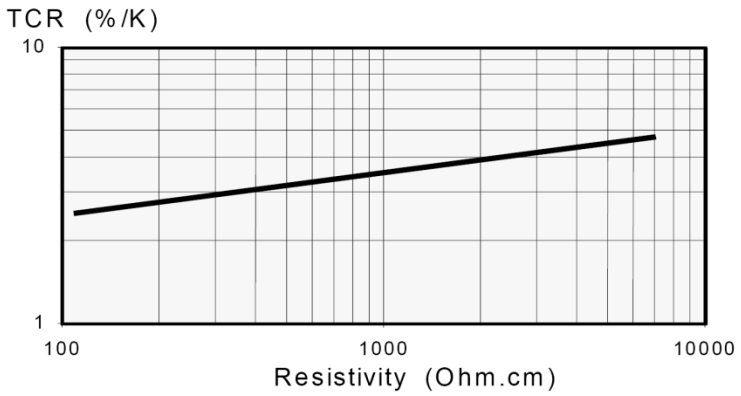

Figure 5.5 Evolution of the TCR as function of the electrical resistivity of amorphous silicon [33].

Amorphous Si can be deposited using either plasma enhanced chemical vapor deposition (PECVD) or sputtering. Amorphous Si deposition can be performed under a high control by PECVD and the layer acquires high uniformity and low stress. Moreover, the resistivity of a–Si can be controlled by the doping level (phosphorous or boron). However, in sputtered a–Si, resistivity is governed by the degree of dangling bond passivation by hydrogen (hydrogenated amorphous Si, a–Si:H). It increases by adding a small portion of H_2 to the argon atmosphere of the sputtering chamber. Precise control of the hydrogen amount deposited can be very difficult and this causes non–uniformity and reproducibility problems [33].

As mentioned earlier, *1/f* noise is the main source of noise in thermistors. The level of *1/f* noise found in the sputtered material is up to 3 orders of magnitude lower than that found in PECVD material [36]. This is due to the higher hydrogen content within PECVD a–Si:H compared to the sputtered one. According to Unewisse et al. [33], unhydrogenated materials exhibit the highest detectivity D* in sputter deposited a–Si (2.2×10^8 $cmHz^{1/2}W^{-1}$ for unhydrogenated compared to 1.08×10^8 $cmHz^{1/2}W^{-1}$ for hydrogenated a–Si), despite lower TCR values (1.8 $\%K^{-1}$ for unhydrogenated compared to 2.1 $\%K^{-1}$ for hydrogenated a–Si). It should be emphasized here that these results are measured in vacuum using 800˚K source. A vacuum packaged sputtered a–Si:H bolometer is found to have performance about 6 to 10 times higher compared to non–packaged ones. Although vacuum packaging is an expensive process, this improvement is essential for imaging applications.

The other problem with a–Si thermistor is the high level of compressive stress. The pixel deformation is a result of significant amount of compressive stress especially in large devices which may break the device in some cases [26]. Pixel thickness governs the stiffness of the pixel membrane and plays an important role in overcoming stress–induced pixel deformation of the suspended microbolometer pixel element [35].

Creation of defects by extended illumination is another effect of temperature on amorphous silicon (a–Si:H) which was discovered in 1977. The solar cell performance made of a–Si was found to get degraded as they were exposed to sunlight for a long time [36]. Thermal history also impacts the conductivity property which is a concern for bolometers as they need to be perfectly adjusted for a given

electrical resistance value. Mastering the cooling rate from above equilibrium temperature is one possible method which needs further investigation [37].

5.2. Amorphous Ge

Another thermistor material with very encouraging results is a–Ge. The detectors using this thermistor are reported to have 4.7×10^8 cmHz$^{1/2}$W^{-1} detectivity for the standard test [26]. This performance enhancement is attributed to the lower resistivity of a–Ge relative to a–Si (22 kΩ for a–Si compared to 1.4 kΩ for a–Ge in a 70×70 μm^2 pixels). The lower resistance offered by Ge allows an increased current to flow through the bolometer resulting in a higher responsivity for a given bias [38]. Although the thermistor temperature is higher and increases faster, since the relative reduction in resistance is much larger than the relative increase in temperature, the Johnson noise is reduced. Thus, the SNR and D* are improved for a–Ge.

M. Garcia et al. [12] in 2004 reported 5 %K^{-1} TCR with 0.4 eV activation energy for a–Ge:H,F grown using low frequency plasma enhanced chemical vapor deposition ((LF)PECVD) with GeF_4 and H_2 precursors.

5.3. Amorphous SiGe

Alloying Si with a material like Ge has also the potential for producing high performance detectors. The bolometers made of a–SiGe benefit from a–Si TCR, low resistance due to a reduced energy band gap of germanium and hence high SNR. Reduction in the intrinsic *1/f* noise properties of the a–SiGe material is the key to maintain low noise in the small pixel design. 5 %K^{-1} TCR has been reported [25] for a–SiGe compared to 3.3 % K^{-1} for a–Si manufactured with the similar condition. Yon et al. [39] has studied the effect of germanium composition on resistivity and TCR as shown in Figure 5.6.

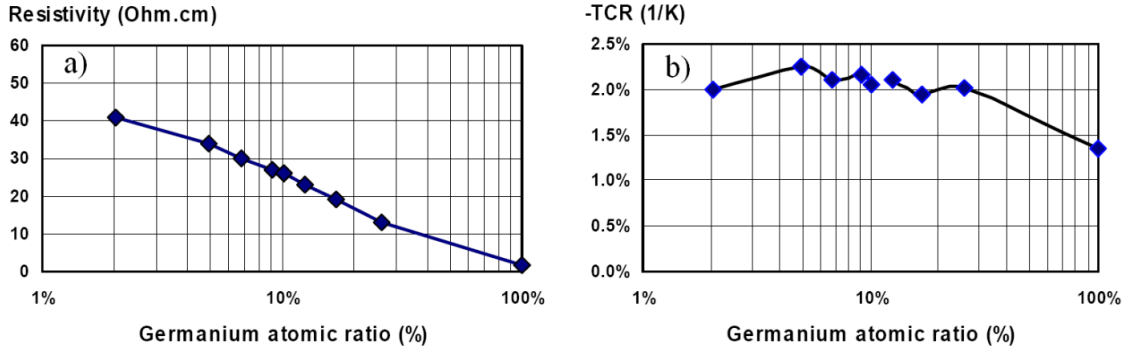

Figure 5.6 a) Thin film resistivity and b) TCR vs. the Ge atomic ratio x of the a–Si_{1-x} Ge_x alloy [39].

They measured the resistivity and TCR at a temperature of 30°C by the direct probing of the thin film itself. This study confirms the relevance of the a–SiGe thin film achievement to dramatically reduce the resistance of the amorphous silicon based microbolometer detectors (see Figure 5.6a). In Figure 5.6b, TCR is shown to be rather constant, close to –2.1 %K^{-1}, for the germanium contents below 25%. For Ge

contents over 25%, TCR decreases significantly down to –1.35 $\%K^{-1}$. This group has also published the device test data of TCR vs. resistivity by integrating a–$Si_{1-x}Ge_x$ with germanium content (x) in the range of 0–25% as shown in Figure 5.7 [39].

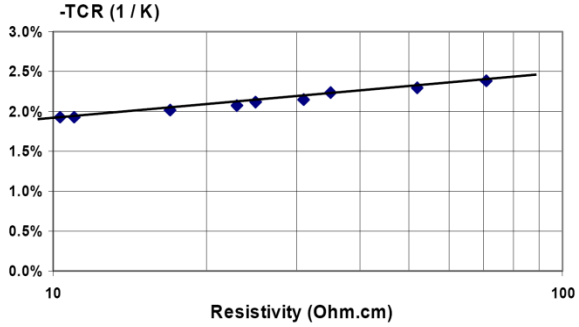

Figure 5.7 TCR vs. resistivity from doped a-Si1-xGex thin films embedded in the test device with x ranging from 0% to 25% [39].

The film resistivities and TCR values extracted from the test device resistance measurements are consistent with the results obtained on the thin film which validates the successful integration of the a–SiGe material into a bolometer design.
The capability of a–SiGe for fabricating a low resistance pixel is fantastic to comply with the voltage lowering trend of advanced CMOS processes which is operating on the produced signal. By comparing Figure 5.5 with 5.7, one can conclude $-2\ \%K^{-1}$ can be achieved using a–$Si_{0.75}Ge_{0.25}$ with almost tenfold reduction in the resistance compared to a–Si. The responsivity of the detectors, as mentioned earlier, is proportional to TCR divided by resistance. The responsivity enhancement of 50% has been reported for introducing only 5% germanium in a–Si [39].
In this case, by decreasing the resistance the Johnson noise becomes negligible and it can be referred to as an improvement in the thermistor statistic. However, the predominant *1/f* noise and responsivity, which is proportional to the current, increase by decreasing resistance value. This will have no harm on the signal–to–noise ratio. The reported $K_{1/f}$ for a–Si and a–$Si_{0.75}Ge_{0.25}$ are 4.2×10^{-6} and 3.6×10^{-6}, respectively [39]. Therefore, a–SiGe is preferred over a–Si for its higher sensitivity, while preserving, similar signal–to–noise ratio as a–Si.

5.4. Amorphous $Si_{1-x}C_x$

This material (a–$Si_{1-x}C_x$:H) was proposed [13] as a thermistor material for its very high TCR, good noise property and the fact that although high TCR values can be achieved in other amorphous semiconductor films, they have significant electronic excess noise problems [27]. The noise properties of this thermistor were investigated in 1997–8. The layers were grown by PECVD reactor using SiH_4, CH_4, B_2H_6 and H_2. Ichihara et al. [13] reported that the noise in a–$Si_{1-x}C_x$:H dramatically decreases as the number of Si–CH_3 and C–H_n bonds in the thin film decrease and as the doping level increases. Although hydrocarbon bonds such as Si–CH_3, and C–H_n have no effect on the activation energy, these bonds degrade the structural uniformity [40] and can be expected to affect conduction mechanisms.

The noise reduction due to the increased doping level was surprising despite an increased structural disorder. Thus, it was concluded that the *1/f* noise does not originate from neither the structural disorder nor neutral dangling bonds which act as recombination centers, but from the structural non–uniformity which causes fluctuation in the carrier conduction [41]. In comparing films with the same activation energy but different doping levels and CH_4/SiH_4 ratios, heavily doped films showed lower *1/f* noise [41]. High doping level reduces the carrier density fluctuation and hence, the noise level decreases. They reported TCR increase from 4 $\%K^{-1}$ to 6.6$\%K^{-1}$ by changing the deposition conditions [13].

5.5. $Ge_xSi_{1-x}O$

As it is known, Si– and Ge–based compounds have proved to be good thermistor materials due to simplicity of integration with the driving electronics. Extrinsic electrical conduction in amorphous semiconductors is a thermally activated process [14] which is due to the activation of carriers from midgap extended levels to the conduction band [42]. The activation energy (E_a) is related to the doping concentration, grain size, and density of defects at the grain boundaries. High activation energies, i.e. high TCR, are achievable for low doping levels which results in very high resistivity of the material. Therefore, a trade–off between large TCR and large resistivity must be reached.

If in an amorphous material the carrier concentration in the midgap levels is high, the resistivity of the material remains in a useful range. In a–Si, the extrinsic conduction mechanism takes place at very low temperatures which is not appropriate for a thermistor material. In a–Ge inferior band gap gives low activation energies, however, adding oxygen to evaporated a–Ge increases the gap which in turn increases TCR form 1.1$\%K^{-1}$ in pure Ge to 4.2$\%K^{-1}$in $GeO_{0.9}$.

Addition of oxygen will increase the number of deep donor levels which results in moderate resistivity values. Moreover, alloying a–Ge with Si will create an extra bonus of higher TCR through increasing the bandgap [43].

In this ternary system, oxygen atoms are preferentially bonded to silicon and not to germanium atoms [44]. This can be elucidated by the fact that the film is growing in a thermodynamic quasi–equilibrium state similar to thermal oxidation [45,46]. However, applying the glow discharge in the sputtering process creates a thermodynamic non–equilibrium state that allows the formation of both Si–O and Ge–O bonds in the growing film [43]. Clement et al. [43] reported that film parameters (e.g. electrical resistivity, optical gap and the activation energy) depend only on the total oxygen content and not on the particular values of RF power and gas composition used to achieve that composition. This feature offers a large flexibility to optimize any process parameter.

In 1971 [42], it was found that the band structure of amorphous semiconductors is determined by a smooth variation of the density of states with energy in the band–edge zones, called band tails, and a high density of states in the midgap region. If the mobility of carriers in the band tails is high enough, the conduction mechanism

is dominated by carriers activated from the midgap states to these band tails. In this case, the activation energy of the electrical resistivity is smaller than half of the optical gap (as shown in Figure 5.8 [43]).

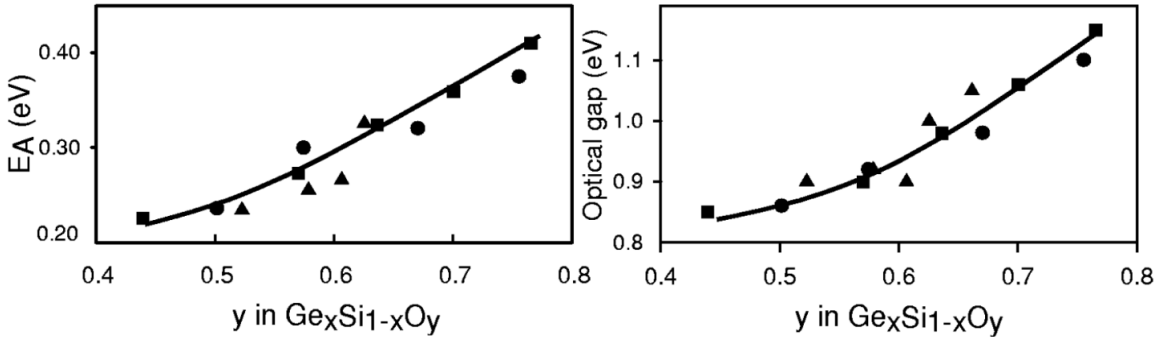

Figure 5.8 The activation energy (Ea) and optical gap vs. the oxygen content (y) in films deposited without substrate bias at various O_2 contents in the gas discharge and various rf power levels, (●) 500 W, (■) 800 W, and (▲) 1500 W [43].

In 2002, Iborra et al. presented $Ge_xSi_{1-x}O_y$ with moderate resistivity (<10^5 Ω.cm) and very high TCR of –4.5 $\%K^{-1}$. The bolometer made of this thermistor illustrated a response time of 1.8ms [47]. They claimed that the reproducibility of the electrical properties of the $Ge_xSi_{1-x}O_y$ resistive layers is very successful.

5.6. Polycrystalline Si

Polycrystalline Si as a thermistor material was offered as a response to the demand of a sensor which could prevent damage to high speed electronic systems. Supadech at al. [48] thermally characterized the LPCVD grown layer after various boron ion implantation doses. They have reported a critical point where the polarity of TCR changes which is so–called "saturation range" [49,50] (see Figure 5.9).
At low temperatures, the resistance decreases with increasing temperature because the impurity atoms (acceptor atoms) are ionized. The resistance then remains constant over the specified temperature range ("saturation range"). After the critical temperature, the lattice scatterings have more effect than the acceptor atom ionization effect which may explain the resistance rising up in the material [48]. The critical point, as it is shown in Figure 5.9, can be tuned by doping concentration.

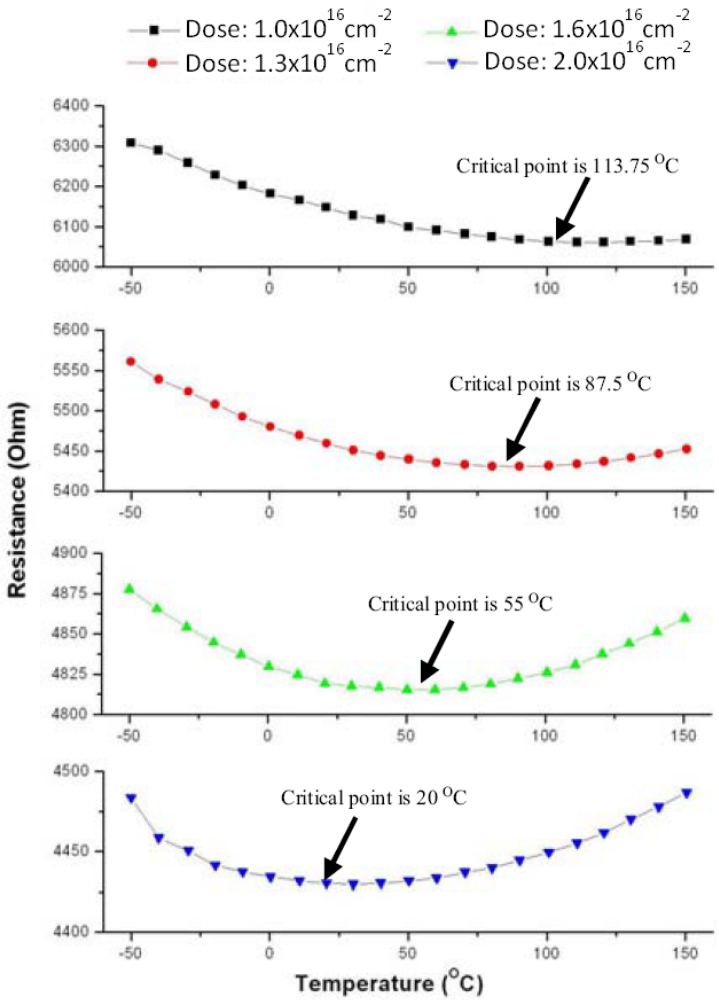

Figure 5.9 Resistance of poly–Si thermistor vs. temperature for different implanted doses [48].

5.7. Polycrystalline SiGe

In this area of electronics, many research groups are devoted to find the material with optimum characteristics, but none have yet completely succeeded. Vanadium oxide (VOx) suffers the fact that it is not a standard material in IC technology, metals have very low TCRs and a–Si (SiGe) has demonstrated a large low frequency (*1/f*) noise [33].

Although a–SiC with a high TCR of 4–6 $\%K^{-1}$ is an IC compatible material [13], a high temperature post–annealing (about 1000 ˚C) is required to obtain stable microstructure. This treatment will damage the ROIC. Another candidate is a–Si:B which has shown TCR of 2–8 $\%K^{-1}$ but its excessive *1/f* noise badly compromises the TCR. This makes it unsuitable to use for high performance thermal detectors [51].

Due to compatibility with standard Si processing and lower *1/f* noise compared to amorphous prototypes, polycrystalline Si (poly Si) was suggested to become the next thermistor for bolometer realization. According to reports [52,53], the concern about this material is the mechanical stability of the bolometer. A solution to this problem

is a high temperature annealing [54] which can damage the ROIC electronics. However, the presence of Ge atoms reduces the deposition temperature which leads to a more ordered structure and lower stress in the layer [55,56]. Thus, employing polycrystalline SiGe instead of polycrystalline Si with at least a factor of four lower thermal conductivity than polycrystalline Si [57,58], easily micromachining property and a TCR comparable with other available materials [59] can be a good solution for mass production. Altering the growth condition (temperature and pressure) is a way to adjust the stress in the grown layer [57]. Reduced pressure chemical vapor deposition (RPCVD) and atmospheric pressure chemical vapor deposition (APCVD) are tools which have been utilized for the growth of such layers. Stability at high temperature annealing and high stress uniformity along the deposited layers are the advantages of RPCVD compared to APCVD grown layers [57].
Due to low resistance of this material, Flicker noise always dominates over the Johnson noise; thus, improving the performance of the device depends mainly on reducing this noise component. As cited before in other thermistors, the parameters such as TCR, resistivity and *1/f* noise are dependent and all need to be considered for optimizing the processing. Doping level of the thermistor is in charge of the resistivity and resistivity determines the TCR and noise level (see Figure 5.10 [14]).

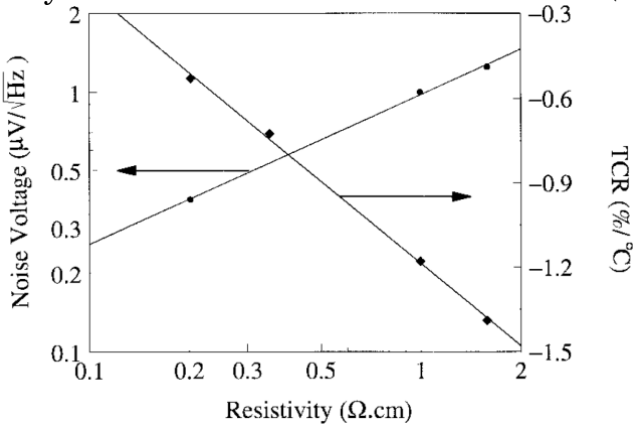

Figure 5.10 dependence of TCR and noise voltage on resistivity of in–situ doped RPCVD polycrystalline SiGe, 1 μm thick [14].

In this case, to obtain the maximum effective detectivity D*, the effect of resistivity on D* must be well–understood. At large bias, after linear increase of detectivity with bias voltage, it reaches saturation due to linear increase of *1/f* noise (D* is the product of TCR times ($1/V_{1/f}$)). As shown in Figure 5.10, TCR and $1/(V_{1/f})$ are respectively an increasing and decreasing function of resistivity. Therefore, their product maximum should be chosen to achieve optimum performance [14].
TCR values as large as of –2% and –1% have been reported for polycrystalline SiGe grown by APCVD and RPCVD, respectively [14]. Despite lower TCR of RPCVD samples, they exhibit smaller resistance and $V_{1/f}$ compared to those grown by APCVD which makes them favorable for this application [14].
In 2003, d. Liong et al. reported ultra high vacuum chemical vapor deposition grown (UHVCVD) polycrystalline SiGe with $-1.91\%K^{-1}$ TCR and 0.145 eV activation

energy. This group exhibited that the *1/f* noise of polycrystalline SiGe is much lower than that of a–Si:B [60].

5.8. Single–crystalline SiGeC

Single–crystalline SiGeC is claimed to enable better thermal isolation by using MEMS technology for health–care applications. This thermistor material offers low heat dissipation and results in a high responsivity [61]. The SiGe layers with high Ge content usually contain a large amount of strain which deforms the mono–crystalline structure to polycrystalline. This stored strain reduces the thermal stability of the SiGe layers. This limitation mostly belongs to the application of binary systems which can be surmounted by using ternary systems (SiGeC). By compensating the strain using C atoms, the crystalline SiGeC film can be formed directly on the silicon substrate without the concern of the critical thickness. This system enables the growth of thermistor at even higher temperature than SiGe [62]. In 2006, Hsieh et al. [63] reported a TCR value of –2.74 $\%K^{-1}$ and an activation energy of 0.21eV for $Si_{0.68}Ge_{0.31}C_{0.01}$ ternary system.

5.9. Hydrogenated nanocrystalline silicon-carbide (p-nc-SiC:H)

Back in 2002, due to further increase in the demand for optimum thermistors, photo–assisted CVD boron–doped hydrogenated nano–crystalline silicon-carbide (p–nc–SiC:H) films were proposed by H. Lee et al [64]. The p–nc–SiC:H is composed of nano–sized crystal silicon (c–Si) grains embedded in amorphous SiC:H (a–SiC:H) matrix [65]. The maximum achieved TCR value was 2.3 $\%K^{-1}$. This material is also a wide bandgap material and TCR can be determined by controlling the bandgap through the carbon content of the deposited layer. What made their work significant compared to others was using photo–assisted CVD which can grow films with small powers (~10 mW/cm^2) at low substrate temperature (≤ 250˚C). This eliminates the ion damage during the film deposition using PECVD and thus, the grown films are expected to have smaller *1/f* noise.
In p-nc-SiC:H, the correlation between resistivity and TCR is shown in Figure 5.11 [65-67].
As the C_2H_4/SiH_4 increases, TCR and *1/f* noise are decreased. High carbon content prohibits the nano–crystallization of SiC:H films and decreases the non–uniformity of the material structure. This reduces the fluctuation in the carrier concentration [41] which decreases TCR and noise level simultaneously [64].

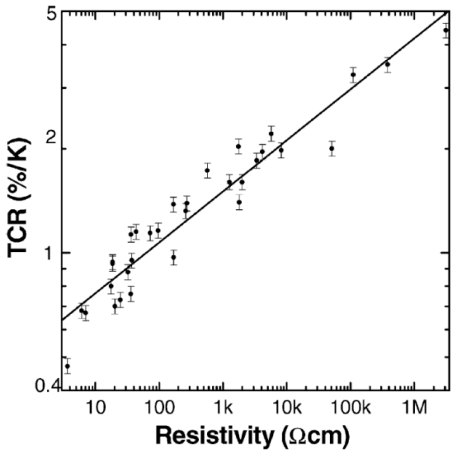

Figure 5.11 Correlation between the resistivity and TCR of various p-nc-SiC:H films [65-67].

5.10. Schottky-diodes

Schottky barrier diodes were introduced for the first time as a micro–electromechanical systems (MEMS) processing method for fabrication of microbolometers at Bell Labs for air–bridge isolation in ICs [68]. The thermistor element is a differential pair of PtSi/p–Si, NiSi/p–Si and RhSi/p–Si Schottky barrier diodes. The operating principle is the log–linear temperature dependence of Richardson thermionic emission currents in reverse biased Schottky diodes [69,70]. Such designs demonstrate very high TCR values in range of 6–7% [69] and independency to Flicker noise proposes them as good candidates for IR detection. High resistance due to the potential barrier at the interface of the metal and semiconductor (Si) results in low current in these detectors. Since *1/f* noise is proportional to the current, Johnson noise is the dominant noise source in this case. Thus, by optimizing the resistance through improving the contacts, the resistance and in turn Johnson noise will be reduced [69].

In these detectors, thermal detection occurs through the changes in the emission current of a reverse biased Schottky diode. The diode has very high impedance and acts as a current source. The magnitude of the saturation current will be proportional to the electrically active area of the Schottky junction. For a well–fabricated diode, thermionic emission is the dominant mechanism in producing the saturation current [69]. The saturation current density can be written as:

$$J_s = A_r T^2 \exp\left(-\frac{\varphi_{bn}}{kT}\right) \quad (21)$$

where A_r is Richardson's constant, k is Boltzmann's constant, and T is the absolute temperature. φ_{bn} is the Schottky barrier potential which can be calculated by an activation energy analysis of the variation of diode current with temperature. Eq.21 demonstrates the saturation current dependency on the temperature. For bolometer application, the variation of the detector temperature changes the total distribution of electron energies in the Schottky electrode which in turn changes the detector saturation current. The final expression for the temperature coefficient of resistance (current) is given by:

$$\alpha = \frac{1}{J_R}\frac{\partial J_R(T)}{\partial T}[K^{-1}] = \frac{1}{T}(\frac{q\varphi_{bn}}{kT} + 2) \quad (22)$$

Thus, the Schottky barrier based thermal emission sensors have the potential (high temperature response) to improve significantly for IR applications.

5.11. Single-crystalline Si/SiGe multilayer structures

This section briefly reviews our detectors made of single–crystalline material. A novel design on the basis of the dark noise in the photon detectors has been suggested for the first time in 2001 [71]. The initiative behind this thermistor was that the single–crystalline (sc) material exhibits very low *1/f* noise which is the main source of noise in these detectors [72]. For high performance bolometers, high signal–to–noise ratio is an important parameter to obtain accurate signal for sensitive IR imaging. The *1/f* noise in sc–Si/SiGe (Si barrier layer/SiGe quantum well) bolometers is attributed to the quality of epi–layers, interfacial roughness (or unevenness) and the contact resistances [17,73]. By optimizing parameters such as the barrier height (with changing the Ge content) and the fermi level (E_f) (by variation of the quantum well width and doping level), this system will provide the potential to design structures with higher TCR and SNR as compared with today's thermistor materials.

According to the reports, the noise level measured in this system was two orders of magnitude lower than VOx [5,74]. This thermistor material is therefore very promising for future mass market applications.

Technically, to maximize the thermal response in this system, highest barrier potential must be exerted in the valence band to confine holes. This can be achieved by introducing highest strain in the quantum wells of the structure through increasing the Ge amount. This means that further increase of the Ge content and the well thickness leads to higher number of quantized energy levels and enhanced temperature response. However, for Ge contents more than 30%, the thermistor will strain–relax due to a large lattice mismatch between Si and SiGe. This phenomenon generates dislocations in the lattice structure giving rise to the generation–recombination noise level which in turn reduces the signal–to–noise ratio. This happens when a certain critical thickness is reached. Consequently, the possibilities to change the composition and thickness of the materials are limited by lattice mismatch [17,73].

In this case, TCR can be estimated through the difference between the bandgap of Si and embedded $Si_{1-x}Ge_x$ [19]. Figure 5.12 illustrates a schematic diagram of the valence band in a single quantum well structure.

In semiconductors, conductance (1/R) is proportional to the amount of free carriers, p_{exc} [m^{-3}] (or n_{exc} in case of n–doping), hence eq.17 for TCR can be calculated as [74]:

$$\alpha = -\frac{1}{kT^2}[\frac{3}{2}k_BT + E_f - V] \quad (20)$$

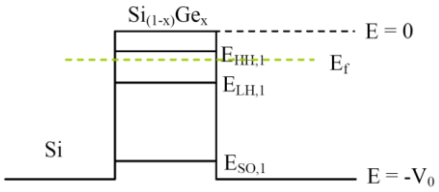

Figure 5.12 Valence band structure of a Si/SiGe/Si quantum well [19].

where k_B, V and T are Boltzmann's constant, barrier height and temperature, respectively. When the thermistor material is heated, thermal excitations generate carriers (holes in this case) which have energies high enough to overcome the potential barrier of the quantum well. If a voltage is applied across the active region, these excited carriers move in the direction of the applied field, thus resulting in a current (see Figure 5.13). This current will increase at higher temperatures by increasing the number of the carriers in the current stream.

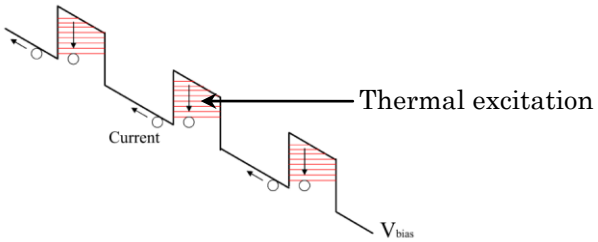

Figure 5.13 The tilt of the valence band after applying a biased voltage across the SiGe/Si stack. The thermally excited holes move towards the negative potential.

The thermistor structures in this study consist of an intrinsic stack of multi quantum dot (MQD) or well (MQW) structures sandwiched with two highly boron–doped contact layers both on the top and bottom (see Figure 5.14).

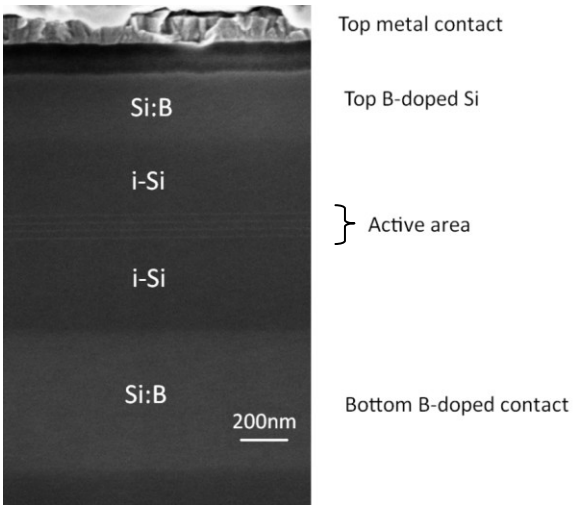

Figure 5.14 The cross–sectional view of the stack and the active area.

The presence of two intrinsic Si layer at top and bottom of the stack suppress the boron auto–doping from the contact layer to quantum wells. B–doping of the active area impacts directly on E_f value of the structure which decreases the thermal response of the detector [19].

We have studied the application of Ge quantum dots instead of quantum wells to maximize the barrier height. However, the Ge quantum dots are not pure Ge and are in fact SiGe due to the intermixing of Si with Ge at the growth temperature range. In this case, ~47% Ge content was achieved which improved the TCR values compared to the MQWs (3.4 $\%K^{-1}$ for multi quantum dots compared to 2.7 $\%K^{-1}$ for MQWs) [17]. However, a remarkable shift (3 order of magnitude) in the $K_{1/f}$ for MQDs compared to MQWs was observed. This shift can be explained through the strain fluctuation in the QD structures compared to uniform profile in QWs.
Integration of C in the Si/SiGe stack [75] (SiGe(C)/Si(C) multi quantum wells) was also examined which exhibited an outstanding TCR of 4.5%/K for 100×100µm² pixel sizes and low noise constant ($K_{1/f}$) value of 4.4×10^{-15}. The outstanding performance of the devices was believed to be due to low contact resistance in the presence of Ni silicide, smooth interfaces, and high quality multi quantum wells (MQWs) containing high Ge content. For these detectors, Ni silicide was used as the absorbent [76,77]. This is due to its simple preparation and the fact that it has a strong absorption of about 90% in wavelength range between 7–13 µm [78]. The main idea is to create SiGe layers through the intermixing of Si into the Ge thin layers (grown by introducing GeH_4 without SiH_4). The intermixing of Si and Ge can be controlled by the growth temperature and the carbon doping in the Si barrier layer [79]. Thus, growth of the Ge–delta layers at low temperature embedded in $Si_{1-y}C_y$ will be an ideal solution to create SiGe(C) quantum wells with very high TCRs and high SNRs.
The difference in integration of this thermistor material compared to the previously mentioned ones is that, this material must be transferred from the carrier wafer to the ROIC by wafer bonding. Materials like VOx and a–Si are benefiting from simplicity of the monolithic processing but on the other hand, they suffer from the limitation of processes which has to be compatible with the ROIC. Temperatures above 400–450°C are prohibited and therefore the choices for thermistor material are limited to materials that can be optimized by processing at such temperatures.
After optimization, the sc–SiGe/Si multilayer stack is transferred to the ROIC by low temperature adhesive wafer bonding and subsequent removal of the carrier. In 2010, Lapadatu et al. [80] proposed a novel approach to increase the fill factor. In their design the legs, which support the bolometer membrane and connect it to the ROIC, are built underneath the membrane as shown in Figure 5.15.

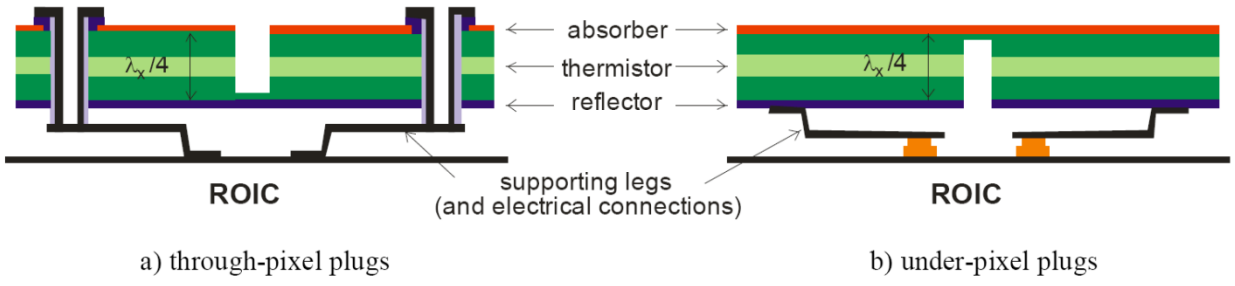

Figure 5.15 Schematic representation of the bolometer pixel illustrating two schemes for electrical connection [80].

It was also reported that the detectors composed of Si/SiGe quantum wells have presented a TCR around 3.1 $\%K^{-1}$ and 5×10^{-13} for $K_{1/f}$ [80].

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CHAPTER 6

SUMMARY, CONCLUSIONS AND FUTURE PERSPECTIVES

Heteroepitaxial SiGe(C) has uncovered many exclusive opportunities by enabling strain and bandgap engineering. This thesis presents a comprehensive experimental and theoretical study of the selective growth of SiGeC layers for CMOS and infrared (IR) applications. The CVD deposited layers were analyzed, calibrated and subsequently integrated in the devices. Major outcomes of this work are summarized below.

1. Selective epitaxy growth demonstrates a pattern dependency which leads to a variation of Ge content and growth rate for chips with different exposed Si coverages. This behavior is saturated for chips with exposed Si coverage below 1%. On the patterned wafer, the interaction between chips originates from the amount of gas consumed by the chips and the distance of the chips from each other (radius of gas depletion). An estimation of the radius of gas depletion for the chips in this study is 8 mm at 10 torr and 15 mm at 40 torr. Using thicker oxide in the pattern led to lower Ge content, but had no significant influence on the growth rate. The impact of oxide thickness originates from less heat conduction for thicker oxides, which impacts the kinetics of gases over the chip.

2. The interaction between chips on a patterned wafer was estimated using various approaches and mask designs. The effect of neighboring chips on a particular chip was found to be independent and additive. This suggests a method of designing chips with a more uniform layer profile. One approach would be to introduce dummy features to maintain the same exposed Si coverage over the entire chip. This will lead to more uniform layer profile over the whole wafer.

3. The pattern dependency of the selective epitaxial growth of B- and C-doped SiGe layers in recessed and unprocessed openings has been studied. The SiGe layer profile was not constant during deposition in recessed openings. The facets have an impact on the growth where the diffusion of adatoms toward the center of the opening occurs. The Ge content in SiGe layers grown on the recessed openings is independent of the recess depth when the gas ratio of Si and Ge is expected to be consumed constantly. The Ge content or strain is graded vertically because the layer thickness usually exceeds the critical thickness. The strain compensation amount due to C and B doping in the SiGe matrix is additive.

4. The first detailed empirical model to predict the growth rates and compositions of $Si_{1-x}Ge_x$ layers grown on patterned substrates by RPCVD was developed. This model is published in the Journal of Electrochemical Society and received the following comment:"This is a very nice paper, which will make an important contribution to the field and it has the potential to become a classic". The model is able to explain the growth kinetics through gas phase processes and related surface reactions. The

diffusion of reactant molecules from the formed stationary boundary layer has been calculated using Fick's law. The gas consumption was modeled by estimating the available sites on the Si surface. A good agreement between the model and the experimental data of the growth profile has been achieved. This model can be utilized in its current form in the manufacturing line to predict the layer profile on any patterned substrate. The input parameters are dichlorosilane, germane, hydrochloric acid partial pressures, growth temperature and mask layout. The interaction between chips (sub-chips) on a wafer was modeled using a new approach.

5. Carbon was integrated in SiGe/Si multilayer structure for the first time and the devices demonstrated a satisfactory thermistor material for future thermal detectors. The performance of the detectors has been very sensitive to the layer quality and the interfacial roughness. These terms are strain-related and become more critical for Ge contents over 30% (SiGe grown at 600-650˚C). Multi quantum dots (MQDs) have shown higher TCR (3.4 %/K) but also higher $K_{1/f}$ (2×10^{-9}) compared to MQWs. These IR detectors have shown low resistance and not very high signal-to-noise ratio. Using Ni silicide as an absorber for this thermistor material decreases the contact resistance and the noise level in this detector. Due to better IR absorption of Ni silicide layers, the thermal response of the detectors is slightly improved. The SiGeC/SiC structures with Ni silicide contacts demonstrated TCR value of 4.5% and remarkably low $K_{1/f}$ (4.4×10^{-15}). In this work, the factorial method has been applied to evaluate the effect of each individual factor in the experiment. Statistical analysis can quantify the importance of different design parameters for improvements in IR detectors.

In the future, the requirement for strain and bandgap engineering in advanced device designs increases and the vitality of alloying group IV-based materials reveals itself. Emerging applications of group IV materials in optoelectronics and also scalability of CMOS device are examples manifesting the necessity of uniform, reproducible and high quality SiGeC(Sn) layers using CVD technique. Successfully alloying Si(GeC) with Sn to make direct bandgap materials extends group IV application to photonic area. Moreover, epitaxial growth has recently entered a new era of low temperature epitaxy (<400˚C) using precursors (e.g. Si_2H_6, Ge_2H_6 and Si_3H_8). Therefore, exploring the new precursor generations is required to fully understand the kinetics and control the epitaxy growth quality. This is especially challenging due to the interest in continuously decreasing the thermal budget of advanced epi-processes for CMOS and BiCMOS applications.