Heterogeneous Integration for Optical MEMS

A. Fischer¹, F. Forsberg¹, M.A. Lapisa¹, N. Roxhed¹, G. Stemme¹, F. Zimmer², F. Niklaus¹

¹ Microsystem Technology Laboratory, School of Electrical Engineering
KTH - Royal Institute of Technology, Stockholm, Sweden

² Fraunhofer Institut für Photonische Mikrosysteme (IPMS), Dresden, Germany

(Invited Paper)

Abstract—In this paper we present different large-scale heterogeneous integration technologies for optical MEMS that enable the integration of optical MEMS with standard CMOS-based ICs. Examples that are presented include various mono-crystalline silicon micro-mirror arrays and infrared bolometer arrays.

Index Terms— MEMS, micro-opto-electromechanical system, MOEMS, More-than-Moore, photonics integration, self assembly, wafer-level heterogeneous integration, wafer-scale IC integration

I. HETEROGENEOUS INTEGRATION TECHNOLOGIES AND IMPLEMENTED OPTICAL MEMS DEVICES

With heterogeneous integration we refer to wafer-to-wafer and chip-to-wafer joining, processing and interconnecting materials and components that are prepared with different technologies including micro-electromechanical systems (MEMS), micro-opto-electromechanical systems (MOEMS), photonics, electronic integrated circuits (ICs) and emerging nano-electromechanical systems (NEMS). Fig. 1 and 2 show examples of schematic process schemes for wafer-to-wafer heterogeneous integration using a via-first and a via-last process respectively. One of the early heterogeneously integrated MOEMS devices using metal bump bonding (via-first) is the mono-crystalline silicon mirror array shown in Fig. 3 [1]. The first mono-silicon mirror array that was fully integrated with functional CMOS ICs was manufactured with a variation of the process illustrated in Fig. 1 and is shown in Fig. 4. Each mirror pixel is 1 mm x 1 mm in size [2].

Fig. 1. Schematic of heterogeneous integration process using partly processed MOEMS or MEMS devices that are wafer-level metal bump-bonded to the target wafer (e.g. a CMOS IC wafer) and subsequently post-processed.

Fig. 2. Schematic of heterogeneous integration process in which a MOEMS, MEMS or NEMS device layer is transferred from a handle wafer to a target wafer (e.g. a CMOS IC wafer). Therefore the device layer can be released from the handle wafer or the handle wafer can be sacrificially removed. Thereafter the MOEMS devices are defined and connected to the target wafer and the bond layer is sacrificially etched to obtain suspended MOEMS, MEMS or NEMS devices [3].

Fig. 3. Mono-crystalline silicon mirror array manufactured with CMOS compatible heterogeneous integration process using metal bump bonding [1].

Fig. 4. Mono-crystalline silicon mirror integrated on top of IC electronics using the heterogeneous integration process illustrated in Fig. 1. Each mirror pixel is 1 mm x 1 mm in size [2].

General advantages of via-last heterogeneous integration processes such as the one shown in Fig. 2 are that vias with extremely small dimensions of below 2-3 μm can be implemented. In case of the transfer of unpatterned layers no accurate wafer-to-wafer alignment is needed during bonding.

This enables extremely accurate positioning of the MOEMS components on the target wafer, which is limited only by the overlay accuracy of the used lithographical processes. Via-last heterogeneous integration processes based on adhesive wafer bonding [3, 4] have been implemented for a number of MOEMS and MEMS devices, including infrared bolometer arrays [5, 6], mono-crystalline silicon micro-mirror arrays [7-9] and radio frequency meta-material surfaces [10]. Fig. 5 shows an infrared bolometer array with a pixel size of $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$ and vias with a diameter of $3\text{ }\mu\text{m}$ [5]. Fig. 6 shows piston-type mono-crystalline silicon micro-mirrors with a pixel size of $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$ [8]. Fig. 7 shows an array of tilting mono-crystalline silicon micro-mirrors with a pixel size of $16\text{ }\mu\text{m} \times 16\text{ }\mu\text{m}$ and with $2\text{ }\mu\text{m}$ diameter vias.

Fig. 5. Infrared bolometer array manufactured with wafer-level via-first heterogeneous integration platform illustrated in Fig. 2 [5].

Fig. 6. Piston-type single-crystalline silicon mirrors manufactured with a variation of the heterogeneous integration process shown in Fig. 2 [8].

Fig. 7. Tilting single-crystalline silicon mirrors manufactured with a variation of the heterogeneous integration process shown in Fig. 2 [9].

For some applications wafer-to-wafer heterogeneous integration technologies are not a cost-efficient solution. This

is for example the case in situations where the manufacturing yield of one or both components to be integrated is low, where the components are very different in size and/or where both components are complex and expensive. Also, some materials such as silicon and more expensive photonic III-V materials may not be available in identical standard wafer sizes. These problems are being addressed by modified or new heterogeneous integration techniques such as localized material placement [11] and selective device distribution [12]. Fig. 8 shows an elegant and cost-efficient process using die-to-wafer placement with subsequent wafer-level device and via processing, enabling extremely high integration densities.

Fig. 8. Die-to-wafer placement of device materials and subsequent wafer-level via formation, processing and release etch of the MOEMS, MEMS or NEMS components [11].

ACKNOWLEDGMENT

This work was supported in part by the European project ICU and sponsored by the EU through its 7th Framework Program.

REFERENCES

- [1] M.A. Michalick, V.M. Bright, *Sensors and Actuators A: Physical*, Vol.95, No.2-3, pp.152-167, 2002.
- [2] J. Bryzek, S. Nasiri, A. Flannery, H. Kwon, M. Novack, D. Marx, E. Sigari, E. Chen, J. Garate, *Nanotech*, Vol.2, pp. 428-431, 2003.
- [3] F. Niklaus, G. Stemme, J.-Q. Lu, R.J. Gutmann, *Journal of Applied Physics*, Vol.99, No.1, pp.031101.1-031101.28, 2006.
- [4] F. Niklaus, R.J. Kumar, J.J. McMahon, J. Yu, J.-Q. Lu, T.S. Cale, R.J. Gutmann, *Journal of The Electrochemical Society*, Vol.153, No.4, pp.G291-G295, 2006.
- [5] F. Niklaus, J. Pejnefors, M. Dainese, M. Haggblad, P.-E. Hellström, U.J. Wallgren, G. Stemme, *Proc. SPIE 2004*, Vol.5406, pp.521-530, Orlando, USA.
- [6] F. Niklaus, A. Decharat, C. Jansson, G. Stemme, *Infrared Physics and Technology*, Vol.51, No.3, pp.168-177, 2008.
- [7] F. Niklaus, S. Haas, G. Stemme, *Journal of Microelectromechanical Systems*, Vol.12, No.4, pp.465-469, 2003.
- [8] M.A. Lapis, F. Zimmer, F. Niklaus, A. Gehner, G. Stemme, *Proc. MEMS 2009*, pp.1007-1010, Sorrento, Italy.
- [9] T. Bakke, B. Völker, D. Rudloff, M. Friedrichs, H. Schenk, H. Lakner, *Proc. SPIE 2006*, Vol.6114, pp.02.1-02.7.
- [10] M. Sterner, D. Chicherin, A.V. Räisänen, G. Stemme, J. Oberhammer, *Proc. MEMS 2009*, pp. 896-899, Sorrento, Italy.
- [11] G. Roelkens, D. Van Thourhout, R. Baets, *Electronics Letters*, Vol.41, No.9, pp.561-562, 2005.
- [12] R. Guerre, U. Drechsler, D. Jubin, M. Despont, *Journal of Microelectromechanical Systems*, Vol.17, No.1, pp.157-165, 2008.