Fabrication and Characterization of 3C- and 4H-SiC MOSFETs

Romain Estève

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Fabrication and Characterization of 3C- and 4H-SiC MOSFETs

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À ma famille
Abstract

During the last decades, a global effort has been started towards the implementation of energy efficient electronics. Silicon carbide (SiC), a wide band-gap semiconductor is one of the potential candidates to replace the widespread silicon (Si) which enabled and dominates today’s world of electronics. It has been demonstrated that devices based on SiC lead to a drastic reduction of energy losses in electronic systems. This will help to limit the global energy consumption and the introduction of renewable energy generation systems to a competitive price. Active research has been dedicated to SiC since the 1980’s. As a result, a mature SiC growth technology has been developed and 4 inch SiC wafers are today commercially available. Research and development activities on the fabrication of SiC devices have also been carried out and resulted in the commercialization of SiC devices. In 2011, Schottky barrier diodes, bipolar junction transistors, and junction field effect transistors can be purchased from several electronic component manufacturers.

However, the device mostly used in electronics, the metal-oxide-semiconductor field effect transistor (MOSFET) is only recently commercially available in SiC. This delay is due to critical technology issues related to reliability and stability of the device, which still challenge many researchers all over the world.

This thesis summarizes the main challenges of the SiC MOSFET fabrication process. State of the art technology modules like the gate stack formation, the drain/source ohmic contact formation, and the passivation layer deposition are considered and contributions of this work to the development of these technology modules is reported.

The investigated technology modules are integrated into the complete fabrication process of vertical MOSFET devices. This MOSFET process was tested using cubic SiC (3C-SiC) and hexagonal SiC (4H-SiC) wafers and achieved results will be discussed.
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List of included papers

A. **Comparative study of thermally grown oxides on n-type free standing 3C-SiC (001).**
   R. Esteve, A. Schöner, S. A. Reshanov, C.-M. Zetterling and H. Nagasawa,
   Contribution: design of the experiment; implementation of the oxidation recipes; fabrication and characterization of the MOS capacitors; writing of the manuscript.

B. **Advanced oxidation process combining oxide deposition and short post-oxidation step for N-type 3C- and 4H-SiC.**
   R. Esteve, A. Schöner, S. A. Reshanov, C.-M. Zetterling and H. Nagasawa,
   Contribution: design of the experiment; implementation of the oxidation recipes; fabrication and characterization of the MOS capacitors; writing of the manuscript.

C. **Electrical properties of MOS structures based on 3C-SiC(111) epilayers grown by Vapor-Liquid-Solid and Chemical-Vapor-Deposition mechanisms on 6H-SiC(0001).**
   R. Esteve, J. Lorenzzi, S.A. Reshanov, N. Jegenyes, A. Schöner, G. Ferro and C.-M. Zetterling,
   Contribution: design of the experiment; implementation of the oxidation recipes; fabrication and characterization of the MOS capacitors; writing of the manuscript.

D. **Comparative Study of Thermal Oxides and Post-Oxidized Deposited Oxides on n-Type Free Standing 3C-SiC.**
   R. Esteve, A. Schöner, S. A. Reshanov, C.-M. Zetterling and H. Nagasawa,
   Contribution: design of the experiment; implementation of the oxidation recipes; fabrication and characterization of the MOS capacitors; writing of the manuscript.
E. Towards 4H-SiC MISFETs devices based on ONO (SiO$_2$-Si$_3$N$_4$-SiO$_2$) structures.
Contribution: design of the experiment; implementation of the oxidation recipes; fabrication and characterization of the MIS capacitors; writing of the manuscript.

F. Surface Passivation Effects on the Performance of 4H-SiC BJTs.
Contribution: implementation of the passivation layers processes; fabrication and characterization of the MOS test structures; participation in the writing of the manuscript.

G. Optimization of Poly-Silicon Process for 3C-SiC Based MOS Devices.
Contribution: design of the experiment; implementation of oxidation and poly-Si activation recipes; fabrication and characterization of the MOS capacitors; writing of the manuscript.

H. 3C-SiC MOSFET with High Channel Mobility and CVD Gate Oxide.
Contribution: implementation of the gate oxide and gate contact formation processes; fabrication and characterization of the MOS test structures; monitoring of the fabrication of the MOSFETs.
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My family and Laetitia for their constant support all along these years and journeys.
## List of symbols and acronyms

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<th>Description</th>
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<tr>
<td>$A$</td>
<td>Area (cm$^2$)</td>
</tr>
<tr>
<td>$A^{**}$</td>
<td>Richardson's constant</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic force microscope</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar junction transistor</td>
</tr>
<tr>
<td>$C_{ACD-DCD}$</td>
<td>Capacitance measured from accumulation to depletion regimes (F)</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer aided design</td>
</tr>
<tr>
<td>$C_{DEP-ACD}$</td>
<td>Capacitance measured from depletion to accumulation regimes (F)</td>
</tr>
<tr>
<td>$C_{INV}$</td>
<td>Capacitance of the insulator in inversion regime (F)</td>
</tr>
<tr>
<td>$C_{NIT}$</td>
<td>Capacitance related to the presence of near-interface traps (F)</td>
</tr>
<tr>
<td>$C_{OX}$</td>
<td>Oxide capacitance (F)</td>
</tr>
<tr>
<td>C-V</td>
<td>Capacitance – voltage measurement</td>
</tr>
<tr>
<td>$D_{IT}$</td>
<td>Density of interface traps (cm$^{-2}$eV$^{-1}$)</td>
</tr>
<tr>
<td>$D_{NIT}$</td>
<td>Density of near-interface traps (cm$^{-2}$)</td>
</tr>
<tr>
<td>$d_{OX}$</td>
<td>Oxide thickness (cm)</td>
</tr>
<tr>
<td>$E_B$</td>
<td>Breakdown electric field (MV/cm)</td>
</tr>
<tr>
<td>$E_C$</td>
<td>Critical field (MV/cm)</td>
</tr>
<tr>
<td>$E_{C_{3C-SiC}}$</td>
<td>Conduction band edge of 3C-SiC (eV)</td>
</tr>
<tr>
<td>$E_{C_{4H-SiC}}$</td>
<td>Conduction band edge of 4H-SiC (eV)</td>
</tr>
<tr>
<td>$E_{C_{SiC}}$</td>
<td>Conduction band edge of SiC (eV)</td>
</tr>
<tr>
<td>$E_F$</td>
<td>Fermi level (eV)</td>
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<tr>
<td>$E_G$</td>
<td>Energy band gap (eV)</td>
</tr>
<tr>
<td>$E_V$</td>
<td>Valence band edge energy (eV)</td>
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<tr>
<td>FGR</td>
<td>Field guard ring</td>
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<td>$G_D$</td>
<td>Drain conductance (S)</td>
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<td>$G_M$</td>
<td>Transconductance (S)</td>
</tr>
<tr>
<td>G-V</td>
<td>Conductance – voltage measurement</td>
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<tr>
<td>$h$</td>
<td>Planck's constant ($6.626068 \times 10^{-34}$ m$^2$kg/s)</td>
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<td>$I_{DS}$</td>
<td>Drain-source current (A)</td>
</tr>
<tr>
<td>$I_{DS_SAT}$</td>
<td>Saturation drain-source current (A)</td>
</tr>
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<td>$I_L$</td>
<td>Leakage current (A)</td>
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<tr>
<td>Acronym</td>
<td>Definition</td>
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<td>I-V</td>
<td>Current – voltage measurement</td>
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<td>$L_{CH}$</td>
<td>Length of the MOSFET channel (cm)</td>
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<td>$L_D$</td>
<td>Debye length (cm)</td>
</tr>
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<td>LPCVD</td>
<td>Low-pressure chemical vapor deposition</td>
</tr>
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<td>LTO</td>
<td>Low temperature oxide</td>
</tr>
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<td>$m$</td>
<td>Effective mass</td>
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<tr>
<td>MIS</td>
<td>Metal insulator semiconductor</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal oxide semiconductor</td>
</tr>
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<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
</tr>
<tr>
<td>MISFET</td>
<td>Metal insulator semiconductor field effect transistor</td>
</tr>
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<td>$N$</td>
<td>Doping concentration ($\text{cm}^{-3}$)</td>
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<td>$N_A$</td>
<td>Acceptor doping concentration ($\text{cm}^{-3}$)</td>
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<tr>
<td>$N_D$</td>
<td>Donor doping concentration ($\text{cm}^{-3}$)</td>
</tr>
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<td>ONO</td>
<td>SiO$_2$-$\text{Si}_3\text{N}_4$-SiO$_2$ stack</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma-enhanced chemical vapor deposition</td>
</tr>
<tr>
<td>$q$</td>
<td>Fundamental electronic charge ($1.6 \times 10^{-19} \text{ C}$)</td>
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<td>$Q_{\text{EFF}}$</td>
<td>Effective oxide charge (C)</td>
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<td>$Q_{\text{EFF}}/q$</td>
<td>Fixed oxide charges concentration ($\text{cm}^{-2}$)</td>
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<td>$Q_{\text{NIT}}/q$</td>
<td>Density of near-interface traps ($\text{cm}^{-2}$)</td>
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<td>$q\Phi_B$</td>
<td>Schottky barrier (eV)</td>
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<td>$q\Phi_{FI}$</td>
<td>Difference between the Fermi level in the bulk and the intrinsic Fermi level in the bulk (eV)</td>
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<td>$q\Phi_{MSC}$</td>
<td>Difference between metal and semiconductor workfunctions (eV)</td>
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<td>$q\Phi_M$</td>
<td>Metal workfunction (eV)</td>
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<td>$q\Phi_{SC}$</td>
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<td>$R_{CP}$</td>
<td>Probe contact resistance ($\Omega$)</td>
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<td>RMS</td>
<td>Root mean square</td>
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<td>$R_p$</td>
<td>Probe resistance ($\Omega$)</td>
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<td>$R_s$</td>
<td>Sheet resistance ($\Omega/$sqr)</td>
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<td>$R_{SER}$</td>
<td>Bias dependent series resistance ($\Omega$)</td>
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<td>$R_{SP}$</td>
<td>Probe spreading resistance ($\Omega$)</td>
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<td>RTA</td>
<td>Rapid thermal annealing</td>
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<td>SEM</td>
<td>Scanning electron microscope</td>
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<tr>
<td>$T$</td>
<td>Temperature ($^\circ\text{C}$)</td>
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<td>TA</td>
<td>Thermal annealing</td>
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<td>TEM</td>
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<td>TLM</td>
<td>Transfer length method</td>
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<td>TO</td>
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<td>$V_D$</td>
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<td>$V_{DS}$</td>
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<td>$V_{FB}$</td>
<td>Flatband voltage (V)</td>
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<tr>
<td>$V_{FB\text{ IDEAL}}$</td>
<td>Ideal flatband voltage (no oxide traps) (V)</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
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<tr>
<td>$V_{FB\ MEASURED}$</td>
<td>Measured flatband voltage (V)</td>
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<td>$V_{GS}$</td>
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<td>$V_L$</td>
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<td>$V_{TH}$</td>
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<td>$V_{TH\ ideal}$</td>
<td>Ideal threshold voltage (V)</td>
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<td>$W_{CH}$</td>
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<td>Width of the depletion region (cm)</td>
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<td>$\varepsilon_0$</td>
<td>Vacuum permittivity ($8.85 \times 10^{-14}$ F/cm)</td>
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<td>$\varepsilon_{SC}$</td>
<td>Dielectric constant of the semiconductor</td>
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<td>$\mu_{EFF}$</td>
<td>Effective mobility (cm$^2$/Vs)</td>
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<td>$\mu_{FE}$</td>
<td>Field effect mobility (cm$^2$/Vs)</td>
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<td>$\mu_N$</td>
<td>Electron mobility (cm$^2$/Vs)</td>
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<td>$\mu_P$</td>
<td>Hole mobility (cm$^2$/Vs)</td>
</tr>
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<td>$\rho$</td>
<td>Resistivity (Ωcm)</td>
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<td>$\rho_C$</td>
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<td>$\chi$</td>
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In our life today we are using more and more electronic equipment needing more and more electrical energy. Electronic equipment is based on different semiconductor devices and the number of such devices is constantly increasing. Hence, the energy consumption of semiconductor devices becomes one of the main concerns for the environment. The energy consumption and losses of semiconductor devices have to be reduced drastically in order to prevent the construction of many new electricity generation plants consuming more and more of earth’s resources.

Today, the electronics world is dominated by the silicon (Si) technology. Using Si technology in power electronics applications, for example, gives energy losses typically in the 4-5% range. Improvements in microelectronic design of Si devices can slightly decrease the energy losses, but will not result in a major reduction of the total wasted electricity in the world. To achieve that, the energy losses in power systems need to be reduced to less than 2%. Innovative solutions and the usage of more suitable materials are needed to increase the performance of electronic devices, which then results in a decrease of the power consumption in the power system. Silicon carbide (SiC) is one of such promising materials. During the last decade, the SiC growth technology has been significantly improved, and device grade 100 mm SiC wafers are commercially available in larger volumes enabling the cost effective production of SiC electronic devices.

In the early stage of the SiC device development, it was thought that SiC devices can be basically processed in similar way as Si devices. But it was very fast realized that the intrinsic SiC material properties and the 50% carbon in the material makes it difficult to use standard Si technology. Many process steps had to be refined and/or new innovative techniques had to be invented.

The semiconductor device mostly used in electronic applications is the Metal-Oxide-Field-Effect-Transistor (MOSFET). Today MOSFETs exist in many designs called DMOSFET, UMOSFET or VMOSFET depending on the way the MOS structure is formed. The main advantages of MOSFET devices can be described as the following:
The MOSFET is a voltage driven device with a rather simple control circuit that results in reduced current consumption.

- High switching frequency capability (up to 1 MHz in Si technology) due to the absence of reverse recovery currents associated with minority carrier recombination.
- High breakdown voltage and current handling capability (up to 1500 V and 10 A in Si technology) due to the use of the substrate and epilayer as the body of the transistor.

During the last two decades, intensive research to fabricate SiC MOSFETs has been done. In 1992, Cree Research reported the fabrication of the first SiC power transistors, which were vertical U-shape trench MOSFETs (UMOSFETs) [1]. Since that time, a wide variety of SiC MOSFETs has been developed, including planar Double-implanted MOSFETs (DMOSFETs) [2]. From these early investigations the MOSFET process technology challenges like the remaining carbon close to the or at the MOS interface have been identified. Alternative solutions were developed to overcome the MOSFET fabrication issues. However, despite intense interest from many research groups and the persistent announcements of device manufacturers, SiC MOSFETs have only been recently commercially available. One of the main reasons for this delay is related to reliability concerns. These concerns are still present and despite promising R&D results, the MOSFET process suitable for mass production is not yet established.

After a brief introduction to the potential of 3C- and 4H-SiC based power MOSFETs, this thesis will review the investigated challenges for fabricating commercial and reliable SiC MOSFET devices. For each of these modules, state-of-the-art considerations and models are presented and the contribution of this work to these technology modules is reported:

- The gate oxide formation: after evaluating state-of-the-art oxidation processes for 3C- and 4H-SiC, an advanced oxidation process combining oxide deposition and short post-oxidation steps in various ambient atmospheres was developed and high quality 3C- and 4H-SiC based oxides could be fabricated. Parallel to these investigations, the potential of ONO ($\text{SiO}_2$-$\text{Si}_3\text{N}_4$-$\text{SiO}_2$) dielectric structures for high temperature MOSFET applications was evaluated.
- The gate electrode elaboration: an optimization of the poly-Si process for 3C-SiC based MOS devices was proposed and significant improvement of the MOS structure reliability has been reported.
- The drain/source ohmic contact formation: low temperature Ni based ohmic contacts fabrication process for n- and p-type 3C-SiC has been demonstrated.
- The passivation layer fabrication: bottom and top parts passivation layer technologies for SiC MOSFETs were investigated and efficient device shielding could be achieved.
The process integration of the developed fabrication modules is demonstrated on a complete SiC MOSFET process and vertical and lateral SiC MOSFETs were fabricated on 3C- and 4H-SiC wafers. The achieved results will be described and discussed.
Chapter 1: SiC MOSFET technology

1.1. Potential and promises

Limitations of Si-MOSFET applications in high power range and the overcoming of advanced materials based technologies were predicted by pioneers of microelectronics [3]. Next generation of power devices is expected to be based on wide band gaps semiconductors. Those materials demonstrate four main intrinsic advantages:

- High electric field operation: because of the wide band gap, the impact ionization energy is high in wide band gap semiconductors. This means the electric field can become very high without avalanche multiplications of ionized carriers. Thus the electric field to accelerate carriers is several times greater in wide band gap semiconductors than in silicon. The breakdown voltage of the wide band gap semiconductor based devices is several times greater than in silicon devices.

- High temperature operation: the intrinsic carrier concentration is inversely related to the energy gap of the semiconductor. A wider gap gives a lower intrinsic carrier concentration. Consequently, unlike silicon, the temperature for the transition from extrinsic conduction dominated by the doping to intrinsic conduction is higher for wide bandgap semiconductors and devices based on wide band gap material offer the advantage of high temperature operation.

- High frequency operation: the size of wide bandgap semiconductor devices can be decreased due to the high electric field strength allowing the use of higher doping concentrations in the active part of devices. Hence, the input and output capacitances are reduced for wide band gap semiconductor devices giving the possibility for higher frequency operation.

- High current density operation: due to high electron drift velocity and thermal conductivity, wide band gap semiconductors offer the possibility of handling high current densities while demonstrating minimal resistances.
Chapter 1: SiC MOSFET technology

The commercial availability of electronic devices based on wide band gap semiconductors would impact application industries like energy distribution, transport, telecommunication and security. The implementation of advanced electronic devices minimizing energy losses, offering superior electrical properties, and capable to operate in hostile environment can overcome technology limitations that industries are currently facing. Figure 1.1.a shows application segments in power electronics positioned with respect to their required power ratings, where wide band gap semiconductor based components and industries can have an impact.

![Voltage and current rating for different power electronics application industries](image)

Figure 1.1.a: Voltage and current rating for different power electronics application industries [4].

One of the most promising materials for various applications in the electronic industry is silicon carbide (SiC). Its physical properties such as high electric field strength, high saturation drift velocity and high thermal conductivity (see Table 1.1.a) have made SiC at the centre of a renewed focus of semiconductor material and device research amongst the other wide energy gap semiconductors. Its remarkable electrical and physical properties make SiC a semiconductor of choice for the following applications fields:

- High power switches
- High temperature and/or hostile environments components
- High power radio frequency components

In comparison with other wide energy gap semiconductors such as III/V Nitrides, SiC has notable advantages such as its rapidly maturing technology for making single crystal substrates. In addition, the ability to form a layer of SiO₂ on SiC in a similar way to silicon enhances the potential of SiC MOS-based devices for
applications like high/temperature electronics [5, 6]. SiC is perceived to be the semiconductor of choice with potential to revolutionize the way the electronic systems are designed.

In view of the research in power switching devices, by far the largest effort has concentrated on unipolar devices. These include Field Effect Transistors that exist in many types: JFET, MOSFET and MESFET. In low power electronic applications that require high switching speed, the silicon MOSFETs have become the dominant technology for many reasons. However, the relatively low breakdown of Si and the resistance of the drift region that increases with increasing blocking voltage generally limit the use of silicon MOSFETs to 500V and below.

![Figure 1.1.b: Specific On-resistance as function of the blocking voltage of DMOSFETs based on Si, 3C- and 4H-SiC [7].](image)

The advantage of SiC material properties, in particular the high breakdown field, makes SiC MOSFETs a very promising candidate for high power switching devices. Its wide band gap and superior drift electron velocity imply the possibility of achieving low specific on-resistance and high blocking voltage capability devices (see Figure 1.1.b). On the other hand, wide band gap structure results in minimal thermal minority carrier generation and consequently reduced leakage current and device operation at high temperature. Moreover, the thermal conductivity of SiC which is three times higher than Si (see Table 1.1.a) and even higher than copper at room temperature provides a higher efficiency of heat extraction from the device and a further reduction in the requirements for device cooling.

Of the numerous crystallographic different polytypes of SiC, initial work focused on the cubic 3C-SiC material due to the superior transport properties: electron
Chapter 1: SiC MOSFET technology

mobility $\mu_N$, electron drift velocity $v$, thermal conductivity $\theta_K$ (see Table 1.1.a). Nowadays, the technologies for growing 3C-SiC bulk crystals are limited and the material quality of 3C-SiC heteroepitaxially grown on silicon is comparably poor due to the large lattice mismatch. The insufficient material quality has hindered the advancement in 3C-SiC device technology. However, the 3C-SiC polytype would be the most promising for direct integration on silicon wafers. Such integration would drastically decrease the price of 3C-SiC electronics and makes it a world leader material for electronic applications.

The availability and reproducible quality of single crystal 4H- and 6H-SiC favors these polytypes for electronic SiC devices. The physical and electrical properties at room temperature for 3C-, 6H- and 4H-SiC polytypes and silicon for reference are listed in Table 1.1.a.

Table 1.1.a: Material properties of Si, 3C-SiC, 6H-SiC and 4H-SiC at room temperature [8].

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>3C-SiC</th>
<th>6H-SiC</th>
<th>4H-SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant $\varepsilon$</td>
<td>11.8</td>
<td>9.7</td>
<td>9.7</td>
<td>9.7</td>
</tr>
<tr>
<td>Energy gap $E_G$ (eV)</td>
<td>1.12</td>
<td>2.39</td>
<td>3.03</td>
<td>3.26</td>
</tr>
<tr>
<td>Critical field $E_C$ (MV/cm)</td>
<td>0.3</td>
<td>1.5</td>
<td>3.2</td>
<td>3</td>
</tr>
<tr>
<td>Electron mobility $\mu_N$ (cm$^2$/Vs)</td>
<td>1400</td>
<td>1000</td>
<td>370$^1$, 100$^2$</td>
<td>800$^1$, 950$^2$</td>
</tr>
<tr>
<td>Hole mobility $\mu_P$ (cm$^2$/Vs)</td>
<td>600</td>
<td>40</td>
<td>90</td>
<td>115</td>
</tr>
<tr>
<td>Electron drift velocity $v$ ($\times 10^7$ cm/s)</td>
<td>1</td>
<td>2.5</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Thermal conductivity $\theta_K$ (W/cmK)</td>
<td>1.5</td>
<td>5</td>
<td>4.9</td>
<td>4.9</td>
</tr>
</tbody>
</table>

$^1$: perpendicular to c-axis; $^2$: parallel to c-axis

4H- and 3C-SiC have substantially higher carrier mobilities than 6H-SiC. Furthermore, the electron mobility anisotropy in 6H-SiC degrades conduction parallel to the crystallographic c-axis. The electron mobility drops from 370 cm$^2$/Vs perpendicular to the c-axis to 100 cm$^2$/Vs parallel to the c-axis. The electron mobility anisotropy is much less in 4H-SiC (see Table 1.1.a) and does not exist in 3C-SiC (cubic crystal structure). These advantages makes 4H-SiC and 3C-SiC the polytypes of choice for SiC electronic devices and especially for vertical devices due to the low mobility anisotropy.

The emergence of higher mobility 4H-SiC MOSFETs has overshadowed significant progress made in obtaining improved 3C-SiC material through heteroepitaxy on low-tilt-angle 6H-SiC substrates [9]. Still, this 3C-SiC material improvement has to be demonstrated with MOSFET performance.
1.2. Challenges

Even though the crystal quality of mainly 4H-SiC substrates and epilayers has been improved during the last decades, the fabrication of SiC power MOSFETs remains rather complex and many issues and challenges stay unsolved (see Figure 1.2.a). The next paragraphs will summarize the current challenges regarding SiC MOSFET technology like gate oxide, gate contact, passivation layer, and source-drain ohmic contact formation. More detailed discussions will follow in the next chapters.

Figure 1.2.a: Scheme of the cross section of a DMOSFET cell. Present issues of SiC DMOSFET technology such as the gate oxide formation, gate contact fabrication, passivation layer construction and source-drain ohmic contacts manufacture are highlighted by the red arrows.

1.2.1. Gate oxide

The most critical issue that regards the SiC MOSFET device concerns the gate stack formation. Thermally grown oxide on SiC results in high densities of oxide/near-interface/interface states which degrade the channel mobility and reliability of the MOSFET. Thermal oxidation of the SiC material induces defects in the oxide/near-interface/interface regions, which are electrically active and contain mostly remaining carbon. This carbon cluster formation deteriorates the electrical characteristics of the fabricated MOSFET channel.

Efforts in reducing the densities of states at the SiC-SiO₂ interface have been carried out during the last ten years and new oxidation processes achieving the passivation of traps to a large extent were demonstrated [10]. However, the channel mobility of MOSFET devices remains rather low compared to bulk mobility values (see Table 1.2.1.a) and the implementation of alternative oxidation techniques remains an issue.
Table 1.2.1.a: Reviewing of state of the art channel mobility achieved in 3C- and 4H-SiC MOSFETs.

<table>
<thead>
<tr>
<th>MOSFET Type</th>
<th>Authors</th>
<th>Year</th>
<th>Channel Mobility ( \mu_{\text{EFF}} ) (cm(^2)/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3C-SiC ( (\mu_N = 1000 , \text{cm}^2/\text{Vs}) )</td>
<td>K.K. Lee et al., 2003 [11]</td>
<td>Normally-Off, LMOSFET</td>
<td>220</td>
</tr>
<tr>
<td></td>
<td>W. Jianwei et al., 2002 [12]</td>
<td>Normally-Off, LMOSFET</td>
<td>170</td>
</tr>
<tr>
<td></td>
<td>A. Schöner et al., 2006 [13]</td>
<td>Normally-Off, DMOSFET</td>
<td>20</td>
</tr>
<tr>
<td>4H-SiC ( (\mu_N = 800 , \text{cm}^2/\text{Vs}) )</td>
<td>H. Yano et al., 1999 [14]</td>
<td>Normally-Off, LMOSFET</td>
<td>96</td>
</tr>
<tr>
<td></td>
<td>E. Ö. Sveinbjörnsson et al., 2006 [15]</td>
<td>Normally-Off, DMOSFET</td>
<td>150*</td>
</tr>
<tr>
<td></td>
<td>D. Okamoto et al., 2010 [16]</td>
<td>Normally-Off, DMOSFET</td>
<td>90</td>
</tr>
</tbody>
</table>

*Severe reliability concerns (sodium contamination)

1.2.2. Passivation layer

The availability of an efficient passivation technology for SiC power devices is essential for their performance. SiC power MOSFETs should operate at blocking voltages of 1500 V and on-state currents of 100 A. Consequently, efficient shielding of the semiconductor surface is required to minimize device leakage currents and prevent surface recombination (see Figure 1.2.a). The implementation of an efficient passivation layer would lead to superior operability and reliability of the device.

During the last ten years, passivation techniques derived from gate oxide formation processes [17] were investigated but complete and efficient solutions have not yet been demonstrated.

1.2.3. Low resistance gate contact

The MOSFET gate contact formation is one of the major challenges that SiC researchers have to face. High operation frequency of power switches require low resistance of the gate contact [18]. In conventional silicon technology the gate contact of power devices is most commonly formed by low-pressure chemical vapor deposition (LPCVD) of poly-Si layers highly doped with phosphorous. Post-deposition high temperature anneal is performed to form the poly-Si layer and
activate the phosphorous dopant. This process results in low resistivity poly-Si films, which are suitable as gate contact. Unfortunately, this standard Si process cannot be implemented directly into the SiC MOSFET fabrication. The high temperature annealing step damages the gate oxide by destabilizing the passivation of the interface traps. For this reason, an alternative gate electrode describing low contact resistance and low formation temperature should be developed to preserve the gate oxide quality.

1.2.4. Drain and source ohmic contacts

The drain and source ohmic contact formation is a current issue in the fabrication of SiC power MOSFETs. Ohmic contacts serve the purpose of carrying electrical current into and out of the semiconductor, ideally with no parasitic resistance. Low resistivity ohmic contacts are essential for high-frequency/high power operation [18]. Additionally, high device operating temperatures and high power handling require that ohmic contacts be reliable under extreme conditions. In SiC technology, the fabrication of low resistance ohmic contacts is rather complex:

- In the case of 4H-SiC, as deposited metals will form mainly Schottky barrier contacts due to the difference in their work function and the SiC electron affinity. Crofton et al. [19] reported that Ni films annealed at temperatures in the range of 900-1000°C give ohmic contacts on n-type 4H-SiC. For p-type 4H-SiC material, due to the higher height of the Schottky barrier, ohmic contact formation is even more difficult. Research activities have focused on Al/Ti contacts, which give a specific contact resistance in the $\sim 10^{-4} \Omega \text{cm}^2$ range. The possible mechanisms of ohmic contact formation of Al/Ti alloys on SiC were especially of interest. However, the reduction of the ohmic contact resistance on p-type SiC is still an issue.

- Due to the lack of commercially available 3C-SiC material, informations about ohmic contacts for 3C-SiC remain limited. However, early work [20] demonstrated similarities of the ohmic contact formation process to the ones for 4H-SiC.

The control of the thermal budget required for the ohmic contact formation is a critical parameter to achieve reasonable process compatibility. As described earlier, post-gate formation high temperature annealing can degrade the electrical properties of the gate oxide enhancing the creation of extra densities of oxide/near-interface/interface states. As a result, innovative low temperature ohmic contact formation processes should be developed.
Chapter 2: Gate oxide

Like silicon, SiC demonstrates the considerable advantage to have a native oxide: the SiO$_2$. Silicon dioxide is the most popular dielectric applied in Si power microelectronic technology and therefore has been developed for decades. Despite its remarkable electrical properties, this dielectric being the native oxide of silicon offers the possibility to be grown by simple thermal oxidation. Unfortunately, Si oxidation technologies are not suitable for SiC. As briefly described earlier in the first chapter of this report, the thermal oxidation of SiC material results in the formation of SiO$_2$ and carbon-silicon-oxygen complexes. Indeed, the SiO$_2$/SiC interface system is much more complex than the SiO$_2$/Si interface system. In order to highlight the complexity of the SiO$_2$/SiC interface system, possible species formed during the oxidation of SiC have been described below [21]:

\[
\begin{align*}
\text{SiC}(s) + O_2(g) &\rightarrow \text{SiO}_2(s) + C(s) \\
4 \text{SiC}(s) + 6 O_2(g) &\rightarrow 4 \text{SiO}_2(s) + 4 \text{CO}(g) \\
\text{SiC}(s) + 2 O_2(g) &\rightarrow \text{SiO}_2(s) + \text{CO}_2(g) \\
\text{SiC}(s) + O_2(g) &\rightarrow \text{Si}(s) + \text{CO}_2(g) \\
2 \text{SiC}(s) + 3 O_2(g) &\rightarrow 2 \text{SiO}(s) + 2 \text{CO}_2(g) \\
\text{SiC}(s) + O_2(g) &\rightarrow \text{SiO}(g) + \text{CO}(g) \\
2 \text{SiC}(s) + O_2(g) &\rightarrow 2 \text{Si}(s) + 2 \text{CO}(g) \\
2 \text{SiC}(s) + O_2(g) &\rightarrow 2 \text{SiO}(g) + 2 \text{C}(s)
\end{align*}
\]

(2.a)

Carbon related complexes/defects are present at the interface, near-interface and in the oxide layer degrading the electrical characteristics of the MOS structure (see interface SiC/SiO$_2$ part).

During the last decades, great efforts to understand the SiO$_2$/SiC interface system were made by many researchers [22]. Much progress in the identification of oxide/near-interface/interface traps was achieved and traps passivation techniques
were developed. However, high concentrations of electrically active defects remain present in SiC based oxides and degrade the performance and reliability of MOSFET devices.

Interface and near-interface traps are considered to be the killer defects of the effective MOSFETs channel mobility $\mu_{EFF}$, scattering and trapping electrons and holes flowing between source and drain via the gate oxide channel. The effective channel mobility $\mu_{EFF}$ is a key parameter of the MOSFET device directly influencing the output drain-source current $I_{DS}$ (see Figure 2.a).

![Figure 2.a](image-url)

Figure 2.a: Transfer characteristics of a simulated MOSFET demonstrating the effect of 50% decrease of the mobility on the drain-source current $I_{DS}$.

For an n-MOSFET device, the drain-source current $I_{DS}$ can be described by the following Equation [23]:

$$I_{DS} = \frac{W_{CH} \mu_{EFF} C_{INV}}{L_{CH}} \left[ (V_{GS} - 2\Phi_{FI} - \frac{V_{DS}}{2}) - \frac{2}{3} \sqrt{2qN_A \varepsilon_0 \varepsilon_{SC}} \frac{C_{INV}}{(V_{DS} + 2\Phi_{FI})^{3/2} - (2\Phi_{FI})^{3/2}} \right],$$

(2.b)

where $W_{CH}$ is the width of the channel, $L_{CH}$ the length of the channel, $C_{INV}$ the capacitance of the insulator in inversion, $V_{GS}$ the gate-source voltage, $\Phi_{FI}$ the
difference between Fermi level $E_F$ in the bulk and the intrinsic Fermi level $E_{FI}$ in the bulk, $V_{DS}$ the drain-source voltage, $q$ the fundamental electronic charge, $N_A$ the acceptor doping concentration, $\varepsilon_{SC}$ the dielectric constant of the semiconductor and $\varepsilon_0$ the vacuum permittivity.

The decrease of the effective channel mobility $\mu_{\text{EFF}}$ directly reduces the drain-source current $I_{DS}$ minimizing the transfer characteristics slope and saturation drain-source current $I_{DS\text{sat}}$.

Fixed charges present in the oxide layer affect the performance of the MOSFET by shifting the threshold voltage $V_{TH}$ of the device towards the positive or negative range depending on the polarity of the dominant oxide states (see Figure 2.b).

![Figure 2.b: Influence of the positive and negative oxide traps on the transfer characteristics of a simulated MOSFET device.](image)

The threshold voltage of an n-MOSFET can be described by the Equation (2.c) [23]:

$$V_{TH} = V_{TH\text{\,ideal}} - \frac{Q_{\text{EFF}}}{C_{\text{INV}}} = \Phi_{\text{MSC}} + 2\Phi_{FI} + \frac{\sqrt{4eN_A\varepsilon_0\varepsilon_{SC}\Phi_{FI}}} {C_{\text{INV}}} - \frac{Q_{\text{EFF}}}{C_{\text{INV}}},$$

(2.c)

where $V_{TH}$ represents the threshold voltage, $V_{TH\text{\,ideal}}$ the ideal threshold voltage (without oxide charges), $Q_{\text{EFF}}$ the effective oxide charge and $\Phi_{\text{MSC}}$ the difference between the metal and semiconductor workfunctions.

From the Equation 2.c, a clear dependency of the fixed oxide traps charge $Q_{\text{EFF}}$ on the threshold voltage of the device $V_{TH}$ appears. Excess of negatively charged
Chapter 2: Gate oxide

oxide traps in the oxide layer shifts the threshold voltage of MOSFET towards the positive range, while excess of positively charged oxide defects shifts $V_{TH}$ towards the negative range. Presence of defects in the oxide/near-interface/interface degrades the reliability of MOSFETs. Defects and states may migrate through the MOS structure while applying voltage on the gate. Traps discharge therefore enhances leakage current through the dielectric layer and early extrinsic oxide breakdown occurs [24].

This chapter will describe the state-of-the-art of the understanding of the SiO$_2$/SiC interface system and present the solutions for passivating oxide/near-interface/interface traps which have been brought out so far.

2.1. Interface SiC/SiO$_2$

The state-of-the-art of the understanding of the SiC/SiO$_2$ interface system can be described and summarized by Figure 2.1.a.

![Figure 2.1.a: “Carbon cluster model” for interface states in SiC/SiO$_2$ MOS structures. The interface states are governed by wide energy gap sp$^2$-bonded carbon clusters and graphite-like (π-bonded) carbon clusters. In this schematic representation the near-interface traps* correspond to the Afanasev-like near-interface traps while near-interface traps** represent the slow oxide traps present in the SiO$_2$ near-interface (adapted from [22] and [25]).](image-url)
That schematic representation of the SiC/SiO$_2$ interface exhibits the nature and energy positions of the main defects/states present at the SiC/SiO$_2$ interface, SiC near interface, SiO$_2$ near interface and bulk. Energy positions of the conduction bands of 4H- and 3C-SiC are described on the energy axis of Figure 2.1.a. The wider band gaps of 3C and 4H-SiC with respect to silicon result in increased sensitivity of these material to oxide defects. As described in Figure 2.1.a, most of critical defects present for SiC/SiO$_2$ interface are positioned in the conduction and valence bands of silicon and consequently do not affect the charge transport at the SiO$_2$/Si interface.

SiC near-interface is mostly populated by the $\pi$-bonded carbon clusters. $\pi$-bonds are covalent chemical bonds where two lobes of one involved electron orbital overlap two lobes of the other involved electron orbital. Such orbital disposition can be described as in Figure 2.1.b. $\pi$-bonded carbon clusters (see Figure 2.1.b) are electrically active and can be either donor-like if they are positioned between 0 and 3.6 eV below the conduction band edge of the SiO$_2$ either acceptor-like when they are localized below (see Figure 2.1.a).

\[
2 \times p_z \text{orbitals} + 1 \sigma_x \text{orbital} = 1 \times \pi_{xz} \text{orbital}
\]

Figure 2.1.b: $\pi$-bonding orbital disposition. The $\pi$-bonding is formed of two parallel $p$-orbitals and one $\sigma$-orbital.

At the SiC/SiO$_2$ interface, the dominant defects are the sp$^2$-bonded carbon clusters (see Figure 2.1.c). As described in Figure 2.1.a, those clusters are localized between 0 and 1.5 eV below the SiO$_2$ conduction band edge and above the SiO$_2$ valence band energy level. Sp$^2$-bounded carbon related defects can be acceptor- and donor-like (see Figure 2.1.a).
Chapter 2: Gate oxide

The SiO$_2$ near-interface is populated by at least two main kinds of states:

- Near-interface traps*: the first type was reported by Afanasev et al. [22] and called near-interface traps. These traps are rather fast, acceptor-like and localized at 2.77 eV of the SiO$_2$ conduction band edge. Because of their high concentrations and fast trapping abilities, they are expected to be at the origin of the low channel mobility of MOSFETs [22].

- Near-interface traps**: the second type of defects is named slow oxide traps or near-interface traps by researchers characterizing the SiC/SiO$_2$ interface using photoelectric characterization techniques [22]. The nature, energy position and electric charge of these slow oxide traps/near-interface traps are not clear yet. These slow charges degrade the stability of MOS based devices limiting their switching abilities.

![sp$^2$-bonding orbital disposition](image)

Figure 2.1.c: sp$^2$-bonding orbital disposition. The sp$^2$-bonding is formed by hybridization of two p-orbitals with one s-orbital.

Finally, the silicon dioxide layer demonstrates high densities of fixed oxide states which are not influencing the charge transport at the SiC/SiO$_2$ interface but affecting the reliability of SiC oxide based devices. Those defects are called fixed because of the impossibility of charging or discharging them. Their charge remains constant while driving the device.

2.2. States passivation techniques

Power SiC MOSFETs are most commonly based on an n-channel due to fact that no p-type substrates are available and the hole mobility in 3C- and 4H-SiC is
limited. For that reason this part will focus on the case of n-channel inversion mode MOSFETs.

When the MOSFET device is switched ON, the MOS structure is in the strong inversion regime. In inversion mode the Fermi level of the semiconductor is close to the conduction band edge of the semiconductor (in case of an n-channel MOSFET). Consequently, the most critical interface states which degrade the transport of electron at the SiC/SiO$_2$ interface are the ones localized close to the conduction band edge of the SiC $E_C$ SiC. On the other hand, conduction band edges of 3C- and 4H-SiC $E_C$ 3C-SiC and $E_C$ 4H-SiC are located at different energies therefore leading to different sensitivities of these polytypes to interface/near-interface/oxide defects (see Figure 2.2.a):

![Diagram showing interface traps densities as functions of the energy position.](image)

**Figure 2.2.a:** Schematic representation of the interface traps densities as functions of the energy position (adapted from [26]).

### 2.2.1. 4H-SiC polytype

The 4H-SiC/SiO$_2$ interface is mostly concerned by the acceptor-like $\pi$-bonded carbon clusters and near-interface traps*. Of these, dominating defects are the near-interface traps*. As mentioned earlier these defects demonstrate fast scattering abilities and high concentrations. As described in the Figure 2.2.a, recent investigations [26] demonstrated that the near-interface traps concentration could be equal to $10^{14}$ cm$^{-2}$eV$^{-1}$ close to $E_C$ 4H-SiC. This density is 100 times higher than the one of $\pi$-bonded carbon clusters. Consequently, the main efforts in 4H-SiC oxidation process development aim to passivate near-interface traps*.
4H-SiC thermal oxidations carried out in dry oxygen ambient at various temperatures result in poor electrical quality of the SiO$_2$ layer/interface demonstrating high densities of near-interface traps* $D_{NIT*}$. Variation of the oxidation temperature and implementation of post-oxidation anneals were considered but no significant improvement could be achieved.

Further studies considering state-of-the-art of silicon MOSFET gate oxide formation techniques such as the use of wet oxygen (H$_2$O:O$_2$ or H$_2$:O$_2$) [27] as ambient gas during the oxidation process were demonstrating slight improvement of the quality of the SiO$_2$ layer properties but no drastic decrease of $D_{NIT*}$ could be demonstrated.

In 1997, Li et al. [28] reported new efficient technique to passivate defects localized close to $E_{C,4H-SiC}$. This method using nitrogen-rich atmosphere (NO) as oxidation ambient described efficient passivation of interface carbon clusters and near-interface traps as well. During the last decade, researchers considered the possible causes of this drastic reduction of the interface defects densities $D_{NIT*}$ marked close to $E_{C,4H-SiC}$. One of the most supported explanations states that nitridation of carbon clusters/near-interface traps does not passivate them. Instead, while changing their atomic compositions the nitridation modifies the energy positions of those defects shifting those towards the middle of the semiconductor band gap [29]. As described earlier in this chapter, the critical interface states affecting the charge transport at the SiC/SiO$_2$ interface are the ones positioned close to the conduction band. Consequently, even if the near-interface traps*/carbon clusters nitridation does not result in a complete passivation of those states that technique remains valuable for gate oxide process.

Few examples of the gate formation processes targeting efficient nitridation of near-interface traps/carbon clusters which were developed are described below:

- Jamet et al. [30] was developing a gate oxide formation process combining dry oxidation and NO post-oxidation step.
- Ciobanu et al. [31] was proving the potential of pre-implanting the SiC surface with nitrogen before dry oxidation.
- Constant et al. [32] was investigating the potential of the rapid thermal oxidation of SiC under nitrogen-rich atmosphere.
- Kimoto et al. [33] was evaluating processes combining SiO$_2$/Si$_3$N$_4$ deposition and post-oxidation steps carried out in N$_2$O atmosphere.

Recently, Okamoto et al. [34] reported a systematic study investigating the potential of elements like B, N, F, Al, P and Cl to reduce defects densities at the 4H-SiC/SiO$_2$ near-interface/interface. This work highlighted the possibility to significantly decrease the concentrations of interface and near-interface states by using phosphorous. Complementary investigations are under consideration but preliminary results demonstrate similarities of the defects phosphorisation with respect to the nitridation of near-interface/interface states.
2.2.2. 3C-SiC polytype

The 3C-SiC/SiO₂ interface presents the main advantage not to be concerned by near-interface states*. Instead, the dominating defects are donor-like π-bonded carbon clusters. Unfortunately, due to the absence of commercial supplier of 3C-SiC material, the number of investigations concerning the 3C-SiC/SiO₂ interface is reduced.

In 1994, De Meo et al. [35] reported on some early works on the thermal oxidation kinetics of 3C-SiC in N₂O at 1050 and 1150 °C. It has been found that the limiting mechanism for the 3C-SiC oxidation is the diffusion of CO complex in the oxy-nitride layer. In 2006, Krieger et al. [36] analyzed the interface trap parameters from double-peak conductance spectra taken on N-implanted 3C-SiC MOS capacitors. 3C-SiC/SiO₂ capacitors were fabricated by thermal over-oxidation of an implanted Gaussian N- or for comparison an implanted Ne-profile. The conductance spectra taken on N-implanted capacitors showed a double peak structure corresponding to two different types of interfaces traps which have identical time constants but are located at different energy positions. While the first type of interface states was demonstrated to be related to carbon clusters, the second kind of traps was directly correlated to the incorporation of N-atom during the oxidation process. This last type of states was so called nitrogener carbon clusters.

Schöner et al. [13] reported on the fabrication and characterization of 3C-SiC MOSFETs. The gate oxide was formed by thermally oxidation for 90 min at 1100 °C in dry oxygen followed by a 3-hour post-oxidation anneal in wet oxygen at 950 °C. 3C-SiC MOS capacitors were fabricated parallel to the process of the MOSFETs and the determination of the density of traps $D_{IT}$ was carried out. $D_{IT}$ evaluation resulted in concentrations in the range of $10^{12}$-$10^{13}$ cm⁻²eV⁻¹ at 0.63 eV from the 3C-SiC conduction band edge $E_{C,3C-SiC}$.

More recently, Im et al. [37] discussed of the potential of nitric acid oxidation method to form SiO₂/3C-SiC structure at 120 °C. Process combining two-step nitric acid (HNO₃) oxidation performed after the hydrogen treatment oxidized 3C-SiC at extremely low temperature of 120 °C, forming thin SiO₂ layers (21 nm). Fabricated nitric oxides were electrically characterized and demonstrated $D_{IT}$ of $5 \times 10^{12}$ cm⁻²eV⁻¹ and fixed oxide charge concentration $Q_{EFF}/q$ equal to $1.7 \times 10^{13}$ cm⁻².

2.3. Characterization techniques

In order to judge on the electrical properties and reliability of investigated oxides, MOS (Metal-Oxide-Semiconductor) capacitors are commonly fabricated and characterized.
2.3.1. Electrical properties

The most commonly used measurement to highlight interface/oxide defects is the capacitance-voltage measurement. This measurement demonstrates the variation of electric charges stored in the dielectric layer and semiconductor for a given electric potential.

![Schematic representation of accumulation, deep depletion and flatband modes](image)

Figure 2.3.1.a: Schematic representation of the accumulation, deep depletion and flatband modes of an ideal n-type SiC based MOS structure. In this scheme, we assume that $\Phi_{MSC}$ is null and no oxide defects exist.

The Figure 2.3.1.a describes the three regimes of an ideal n-type SiC based MOS structure which can be observed under tight light environment:

- Flatband regime: when the conduction and valence band edges are not bent the structure is in the flatband condition.
- Deep depletion regime: while applying a negative voltage on the gate metal, the structure turns to deep depletion mode. The negative charge of the gate metal repulses the electrons from SiC to the substrate and a depletion layer appears. Because of the formation of the depletion layer the capacitance is drastically reduced. The SiC capacitance is proportional to the doping concentration of the material.
Accumulation regime: while applying positive voltage of the gate metal, the structure turns to accumulation mode. The positive charge of the gate metal attracts electrons from the SiC to the SiC/SiO$_2$ interface. In this band structure configuration, most of the potential variation is within the oxide. Due to the accumulation charge close to the interface, the capacitance increases up to reach a saturation level which defines the oxide capacitance. The oxide capacitance is proportional to the thickness of the oxide layer.

Unlike silicon, the inversion regime is not seen for SiC based MOS capacitors under tight-light environment, deep depletion is observed instead. In SiC, high generation time for minority carriers makes it difficult to observe inversion in MOS structures. The high generation time for minority carriers is due to the absence/extremely low concentration of minority carriers in SiC [38]. In order to observe inversion regime in SiC MOS structures, an external source of minority carriers has to be implemented as in the case of MOSFET, or UV-light stimulation has to be performed before and during the C-V measurement.

From capacitance measurements fixed oxide charges, near-interface states** and interface traps can be detected. The Figure 2.3.1.b describes the different deformations induced by those defects on the capacitance curve of an n-type SiC based MOS capacitor.

Figure 2.3.1.b: Schematic representation of the distinct deformations induced by fixed oxide charges, near-interface states (slow oxide traps) and interface traps on the capacitance curve of an n-type SiC based MOS capacitor.
2.3.1.1. Fixed oxide traps

The flatband voltage of the capacitance curve is ideally equal to the difference of the metal and semiconductor workfunctions $\Phi_{MSC}$. In reality, the presence of fixed oxide traps shifts the flatband voltage of the capacitance towards the positive voltage range if the traps are positively charged or towards the negative voltage range if the traps are negatively charged. From the difference between the ideal flatband voltage $V_{FB\, ideal}$ and the measured one $V_{FB\, measured}$ it is possible to estimate the effective fixed oxide traps densities $Q_{EFF}/q^*$:

$$\frac{Q_{EFF}}{q} = \frac{(V_{FB\, measured} - V_{FB\, ideal}) \times C_OX}{A \times q},$$

(2.3.1.1.a)

where $C_{OX}$ represents the oxide capacitance, $A$ the contact area of the MOS capacitor, $q$ the elementary charge of an electron.

2.3.1.2. Near-interface traps** (slow oxide traps)

The presence of near-interface traps** creates a hysteresis between both sweeps of the capacitance (from deep depletion to accumulation and vice versa). From the measured hysteresis a quantitative estimation of the near-interface traps concentration $D_{NIT^*}$ can be done.

The capacitance related to the near-interface states $C_{NIT^*}$ is equal to the difference of capacitance measured from deep depletion to accumulation $C_{DEP-ACC}$ and the capacitance measured from accumulation to deep depletion $C_{ACC-DEP}$:

$$C_{NIT^*} = C_{DEP-ACC} - C_{ACC-DEP}$$

(2.3.1.2.a)

The derivative of the charge induced by the near interface traps $dQ_{NIT^*}$ can consequently be expressed as

$$dQ_{NIT^*} = C_{NIT^*} \times dV = (C_{DEP-ACC} - C_{ACC-DEP}) \times dV$$

(2.3.1.2.b)

Then the density of near interface traps $D_{NIT^*}$ can be described as the induced charge $Q_{NIT^*}$ divided by the electron charge $q^*$:

$$D_{NIT^*} = \frac{Q_{NIT^*}}{q} = \frac{1}{q} \int_{V_{MIN}}^{V_{MAX}} C_{NIT^*} \, dV$$

(2.3.1.2.c)

This approximation is only valuable for fixed frequency and temperature capacitance measurement. Also this method does not take into account the nature or energy position of the near interface states.
2.3.1.3. Interface traps

The presence of interface traps creates a stretch-out of the capacitance curve close to the accumulation region. Interface traps scatter electrons accumulating close to the SiC/SiO$_2$ interface thus screening applied bias therefore resulting in the slowing of the transition to accumulation mode. The quantification of the interface traps density $D_{IT}$ can be achieved from capacitance measurements via the Terman and Hi-Lo methods. However, those techniques demonstrate the drawback to underestimate $D_{IT}$ [24]. In order to provide a reliable evaluation of the interface traps concentration, the conductance method was developed by Nicollian and Brews [39]. This method based on both capacitance and conductance measurements permits to evaluate accurately $D_{IT}$ and distinguish distinct types of traps/defects. The calculation procedure of $D_{IT}$ using the conductance method is described in the Appendix A.1.

2.3.2. Reliability

The reliability of fabricated oxides is commonly judged by current-voltage measurements I-V. Multiple I-V measurement configurations highlighting the presence of various oxide defects and instabilities of the structure are possible. Recently, reliability studies became important as MOSFETs are coming closer to commercialization. In the reported works focused on gate oxide reliability concerns, we consider two main oxide stress-induced methods: current measurements I-V and time zero dielectric breakdown TZDB measurements.

2.3.2.1. I-V characteristics

At first one can judge of the reliability of the MOS capacitors by looking at the shapes of the I-V characteristics. As described in Figure 2.3.2.1.a, the typical curve of an I-V characteristic is composed of three main regions:

- The blocking region: at low applied voltage, low/no current is measured. That implies no charge flow through the MOS structure.
- The Fowler-Nordheim tunneling region: while the applied voltage increases and becomes rather high, the intense applied electric field stimulates the charge tunneling across the oxide layer and the current therefore increases. This tunneling phenomenon is called Fowler-Nordheim tunneling.
- The breakdown region: while the applied voltage and electric field increase, the charge tunneling phenomenon exponentially increases. This results in the exponential augmentation of the current and finally the breakdown of the oxide.

Oxide defects induce three typical deformations on I-V characteristics (see Figure 2.3.2.1.b):

- Increase of the leakage current of the device $I_{LK}$ in the blocking region.
- Random current peaks due to point defect discharges.
Chapter 2: Gate oxide

- Early breakdown of the oxide $E_B$.

Figure 2.3.2.1.a: Typical I-V characteristic of an MOS capacitor. Three main regions can be described: the blocking, Fowler- Nordheim tunneling and breakdown regions.

Figure 2.3.2.1.b: I-V characteristics of MOS capacitors with and without oxide defects.

Consequently, one can obtain a first evaluation of the reliability of a fabricated oxide looking at the breakdown, leakage current and amount of peaks of current displayed on I-V characteristics.
TZDB measurements

The second considered approach for judging of the reliability of the oxide is so called Time Zero Dielectric Breakdown (TZDB) [40]. This test consists of measuring the breakdown electric field values of numerous MOS capacitors and plotting the collected results. TZDB measurements are commonly used for the estimation of the average oxide breakdown $E_B$ value and displaying the distribution of the oxide breakdown results.

When a large number of oxide breakdown values can be measured (wafer-scale analysis), one can apply the Weibull distribution function to the collected results. An example of the application of the Weibull distribution function to collected oxide breakdown electric field values taken on MOS capacitors is shown in the Figure 2.3.2.2.a below.

Figure 2.3.2.2.a: Weibull distribution function applied to collected oxide breakdown electric field values taken on MOS capacitors.

Two main parameters can be extracted from such a plot:
- The distribution of the breakdown electric field values: the steepness of the slope of the distribution defines the sharpness of the distribution profile of the collected breakdown electric fields. Steeper is the slope, sharper is the distribution profile.
- The type of breakdown of the oxide. The presence of different slopes indicates the existence of different breakdown modes of the oxide structure. From that point the identification of extrinsic breakdown modes reducing the performance and lifetime of the MOS capacitors can be achieved.
2.4. Results

2.4.1. Thermally grown oxides

As described earlier in this report (section 2.2.1.), it was shown the quality of 4H-SiC based thermally grown oxides can be improved (a) by post-oxidation annealing [41], (b) by hydrogen passivation [27], or (c) by implementation of nitrogen in oxidation processes [42]. The aim of our work focused on thermally grown oxides was to apply these techniques to the 3C-SiC(001) polytype.

Table 2.4.1.a: Oxidation and post-oxidation annealing parameters of investigated 3C-SiC(001) MOS capacitors.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Oxidation</th>
<th>Post-oxidation annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>gas species</td>
<td>T (°C)</td>
</tr>
<tr>
<td>#1</td>
<td>O\textsubscript{2}</td>
<td>1100</td>
</tr>
<tr>
<td>#2</td>
<td>O\textsubscript{2}</td>
<td>1200</td>
</tr>
<tr>
<td>#3</td>
<td>O\textsubscript{2}</td>
<td>1100</td>
</tr>
<tr>
<td>#4</td>
<td>O\textsubscript{2}</td>
<td>1100</td>
</tr>
<tr>
<td>#5</td>
<td>N\textsubscript{2}O:N\textsubscript{2} (1:4)</td>
<td>1200</td>
</tr>
<tr>
<td>#6</td>
<td>N\textsubscript{2}O:N\textsubscript{2} (1:4)</td>
<td>1250</td>
</tr>
<tr>
<td>#7</td>
<td>N\textsubscript{2}O:N\textsubscript{2} (1:4)</td>
<td>1250</td>
</tr>
</tbody>
</table>

Table 2.4.1.b: Oxide thickness ($d_{\text{OX}}$), flat band voltage ($V_{\text{FB}}$), density of interface traps ($D_{\text{IT}}$) and effective oxide charge ($Q_{\text{EFF}}/q$) of investigated 3C-SiC(001) MOS capacitors.

<table>
<thead>
<tr>
<th>Sample</th>
<th>$d_{\text{OX}}$ (nm)</th>
<th>$V_{\text{FB}}$ (V)</th>
<th>$D_{\text{IT}}$ $^{*}$ ($\times10^{12}$ cm$^{-2}$eV$^{-1}$)</th>
<th>$Q_{\text{EFF}}/q$ $^{*}$ ($\times10^{12}$ cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>74.5 ± 3.0</td>
<td>-30.9 ± 1.5</td>
<td>42.7</td>
<td>9.3</td>
</tr>
<tr>
<td>#2</td>
<td>72.0 ± 6.7</td>
<td>-25.0 ± 1.2</td>
<td>65.9</td>
<td>7.1</td>
</tr>
<tr>
<td>#3</td>
<td>71.1 ± 3.7</td>
<td>-4.5 ± 0.3</td>
<td>7.1</td>
<td>1.3</td>
</tr>
<tr>
<td>#4</td>
<td>61.6 ± 7.3</td>
<td>-3.0 ± 1.3</td>
<td>5.2</td>
<td>0.9</td>
</tr>
<tr>
<td>#5</td>
<td>17.0 ± 1.1</td>
<td>-3.0 ± 1.1</td>
<td>11.5</td>
<td>3.0</td>
</tr>
<tr>
<td>#6</td>
<td>29.9 ± 1.3</td>
<td>-5.4 ± 0.7</td>
<td>9.1</td>
<td>3.1</td>
</tr>
<tr>
<td>#7</td>
<td>23.9 ± 0.9</td>
<td>-2.1 ± 0.2</td>
<td>9.4</td>
<td>1.6</td>
</tr>
</tbody>
</table>

$^{*}D_{\text{IT}}$ determined at $E_{\text{C}}-E_{\text{IT}} \approx 0.52$ eV

In paper A, we evaluate and compare three different ways to improve the oxidation process of 3C-SiC(001) in order to reduce the fixed and mobile charge...
densities in the grown oxide and at the interface. At first, we study the dry oxidation performed at elevated temperature. The second approach assesses improvements of the oxide quality implementing low temperature post-oxidation steps. Thermal oxides have been post-oxidized in wet and dry oxygen in order to bring out impacts of the stabilization of the oxide and the hydrogen passivation on 3C-SiC(001) material. Finally, we examine the efficiency of nitridation in the case of 3C-SiC(001) by using N₂O oxidation.

The standard dry oxidation at 1100 °C results in a high negative flat band voltage of 31 V and in a high $D_{IT} = 4.3 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$. The increase of the oxidation temperature up to 1200 °C slightly reduces the fixed charge in the oxide at the cost of $D_{IT}$ and surface potential fluctuation increase, thus not resulting in the oxide improvement. A strong reduction in both the fixed charge and the $D_{IT}$ can be achieved by the post-oxidation annealing step. The wet post-oxidation process H₂+O₂ is a superior one. Finally, we have discussed the inefficiency of the use of nitridation in the case of 3C-SiC(001). MOS capacitors, which were fabricated by N₂O oxidation, revealed the huge hysteresis in depletion due to near-interface traps and the creation of nitrogen related deep interface states, while the flat band voltage was comparable with the post-oxidized MOS capacitors. The wet post-oxidation annealing applied to N₂O grown oxides does not result in the improvement of the $D_{IT}$ either. Another disadvantage of the N₂O oxidation is the low oxidation rate which leads to longer processing time and high thermal budget.

2.4.2. Post-oxidized deposited oxides

Lee et al. [11] demonstrated that thermal oxides grown on SiC material preserve high quality and low concentration of interface traps until the oxide thickness does not exceed 5 nm. Up to this critical thickness interface states density stays rather low and no flatband voltage shift is observed. Recently, it has been demonstrated that also the reliability of thermal oxide on 4H-SiC(0001) is comparable to that of thermal oxides on Si, for SiO₂ thickness in this range [43]. However, for the fabrication of MOS structures usable in power device applications an oxide thickness of at least 50 nm is required.

Consequently, an advanced oxidation process combining thermal and deposited oxide can be a superior one. The present oxidation issue proposes to deposit 55 nm of silicon dioxide using plasma enhanced chemical vapor deposition PECVD and to post-oxidize it. The post-oxidation steps perform first a densification of the deposited oxide and second a thermal oxidation of a 3-5 nm thin layer of SiC.

In paper B, we evaluate the potential of advanced oxidation processes combining plasma-enhanced chemical vapor deposition PECVD of SiO₂ and short post-oxidation at low temperature. Three gas atmospheres have been investigated for the post-oxidation anneals: dry oxygen, wet oxygen H₂O:O₂, and N₂O, compared to the densification in pure nitrogen. The differences in the electrical properties of oxides fabricated on 3C-SiC(001) and 4H-SiC(0001) are discussed based on the
model of the energetic distribution of interface and near-interface states. Our study demonstrates the efficiency of the advanced oxidation process combining SiO$_2$ deposition and post-oxidation steps.

Table 2.4.2.a: Deposition and post-oxidation parameters of investigated MOS capacitors.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Deposition time (s)</th>
<th>Deposition thickness (nm)</th>
<th>Post-oxidation annealing</th>
<th>Gas species</th>
<th>T (°C)</th>
<th>time (h)</th>
<th>Gas flow (slm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>45</td>
<td>55</td>
<td></td>
<td>N$_2$O:N$_2$ (1:4)</td>
<td>1100</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>#2</td>
<td>45</td>
<td>55</td>
<td></td>
<td>H$_2$O:O$_2$</td>
<td>950</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>#3</td>
<td>45</td>
<td>55</td>
<td></td>
<td>O$_2$</td>
<td>950</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>#4</td>
<td>45</td>
<td>55</td>
<td></td>
<td>N$_2$</td>
<td>1100</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>#5</td>
<td>45</td>
<td>55</td>
<td></td>
<td>N$_2$</td>
<td>950</td>
<td>3</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 2.4.2.b: Oxide thickness ($d_{OX}$), flat band voltage ($V_{FB}$), effective oxide charge ($Q_{EFF}/q$) and breakdown field ($E_B$) of investigated 4H-SiC(0001) MOS capacitors.

<table>
<thead>
<tr>
<th>4H-SiC(0001) sample</th>
<th>$d_{OX}$ (nm)</th>
<th>$V_{FB}$ (V)</th>
<th>$Q_{EFF}/q$ ($\times 10^{11}$ cm$^{-2}$)</th>
<th>$E_B$ (MV·cm$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>53.2 ± 4.7</td>
<td>-0.6 ± 0.5</td>
<td>4.6</td>
<td>8.2</td>
</tr>
<tr>
<td>#2</td>
<td>57.5 ± 3.2</td>
<td>-3.0 ± 0.4</td>
<td>13.2</td>
<td>7.9</td>
</tr>
<tr>
<td>#3</td>
<td>55.0 ± 4.1</td>
<td>-0.5 ± 0.7</td>
<td>4.1</td>
<td>1.6</td>
</tr>
<tr>
<td>#4</td>
<td>46.8 ± 8.5</td>
<td>-0.9 ± 0.3</td>
<td>6.8</td>
<td>9.0</td>
</tr>
<tr>
<td>#5</td>
<td>49.5 ± 9.1</td>
<td>12 ± 2.2</td>
<td>-50.5</td>
<td>7.5</td>
</tr>
</tbody>
</table>

In the case of 4H-SiC(0001) MOS capacitors, the N$_2$O post-oxidation process is the superior one. Nitrogened atmosphere provides to MOS capacitors small flatband voltage of 0.6 V and a drastic reduction of interface traps concentration. Measurements of the oxide breakdown field revealed $E_B$ equal to 8.2 MVcm$^{-1}$. 4H-SiC(0001) MOS capacitors fabricated by wet H$_2$O:O$_2$ or dry oxygen post-anneals revealed higher concentrations of interface states and poor electrical properties. In the case of 3C-SiC(001) benefits of the wet H$_2$O:O$_2$ oxygen atmosphere for the post-deposition anneal has been demonstrated. MOS capacitors fabricated using wet oxidation step brought out superior properties than ones annealed in N$_2$O, dry oxygen, or N$_2$. They have shown significant improvements in terms of flatband voltage shift, effective oxide charge and density of interface traps, as well as the highest oxide breakdown field $E_B$ of 9.1 MVcm$^{-1}$. We have also demonstrated the inefficiency of the use of nitridation in the case of 3C-SiC(001). MOS capacitors,
which were fabricated by N\textsubscript{2}O post-oxidation, revealed the creation of nitrogen related deep interface states, while the flatband voltage was comparable with the dry oxygen post-oxidized MOS capacitors.

Table 2.4.2.c: Oxide thickness ($d_{OX}$), flat band voltage ($V_{FB}$), effective oxide charge ($Q_{EFF}/q$) and breakdown field ($E_{B}$) of investigated 3C-SiC(001) MOS capacitors.

<table>
<thead>
<tr>
<th>3C-SiC(001) sample</th>
<th>$d_{OX}$ (nm)</th>
<th>$V_{FB}$ (V)</th>
<th>$Q_{EFF}/q$ ($\times10^{11}$ cm\textsuperscript{-2})</th>
<th>$E_{B}$ (MV·cm\textsuperscript{-1})</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>52.8 ± 3.1</td>
<td>-5.4 ± 1.3</td>
<td>20.1</td>
<td>8.2</td>
</tr>
<tr>
<td>#2</td>
<td>56.2 ± 2.3</td>
<td>-0.8 ± 0.2</td>
<td>1.7</td>
<td>9.1</td>
</tr>
<tr>
<td>#3</td>
<td>64.0 ± 4.6</td>
<td>-5.5 ± 1.7</td>
<td>17.6</td>
<td>5.9</td>
</tr>
<tr>
<td>#4</td>
<td>46.8 ± 5.9</td>
<td>-10.2 ± 1.3</td>
<td>46.5</td>
<td>6.3</td>
</tr>
<tr>
<td>#5</td>
<td>51.2 ± 4.7</td>
<td>-6.5 ± 2.1</td>
<td>26.3</td>
<td>6.2</td>
</tr>
</tbody>
</table>

In 1999, Yano et al. [14] investigated the impact of the crystal orientation of 4H-SiC material on the electrical properties of fabricated oxides. In that way oxides grown on 4H-SiC(11-20) could exhibit reduction of interface states densities with respect to oxides grown on 4H-SiC(0001). In case of 3C-SiC, such information has never been reported.

In paper C, the electrical properties of post-oxidized PECVD oxides in wet oxygen based on 3C-SiC(111) epilayers grown by vapor-liquid-solid (VLS) and chemical-vapor-deposition (CVD) mechanisms on 6H-SiC(0001) have been studied in. Different 6H-SiC(0001) samples exhibiting diverse crystal orientations (on-axis, 2° off-axis) and growth conditions were compared. A comparative study of oxide qualities has been carried out via capacitance and conductance measurements (C-G-V). Achieved interface traps densities and effective oxide charges were compared for the different samples. Reliability issues have been considered via current measurements (I-V and TZDB) and statistical data treatment techniques (Weibull plots).

Our study reports on the possibility of achieving high quality oxides based on 3C-SiC (111). MOS devices based on 3C-SiC layer grown via a process mixing VLS and CVD techniques demonstrated low interface states densities $D_{IT}$ of $1.2\times10^{10}$ eV\textsuperscript{-1}cm\textsuperscript{-2} at 0.63 eV below the conduction band and fixed oxide defects concentrations $Q_{EFF}/q$ of $-0.1\times10^{11}$ cm\textsuperscript{-2}. On the other hand, the reliability study has assessed low oxide breakdown field $E_{B}$ of 5.5 MVcm\textsuperscript{-1}. The Weibull analysis of TZDB measurements has brought out a dominating extrinsic breakdown mode which could be caused by material defects, probably double-positioning boundary (DPB) or stacking faults (SF).
2.4.3. Comparison thermal oxides/post-oxidized deposited oxides

The electrical properties of oxides fabricated on n-type 3C-SiC(001) using wet oxidation and an advanced oxidation process combining SiO\textsubscript{2} deposition with rapid post oxidation steps have been compared in paper D. Two alternative SiO\textsubscript{2} deposition techniques have been studied: the plasma enhanced chemical vapor deposition (PECVD) and the low pressure chemical vapor deposition (LPCVD). Our study reports on the benefits in terms of electrical properties and reliability of a gate oxidation process combining PECVD oxide with a post-oxidation step in wet oxygen compared to state-of-the-art thermally grown oxides. It was shown that post-oxidized PECVD deposited oxide exhibit the lowest concentrations of fixed charges \( \frac{Q_{\text{EFF}}}{q} = 1.7 \times 10^{11} \text{ cm}^{-2} \) and interface states \( D_{\text{IT}} = 1.9 \times 10^{12} \text{ eV}^{-1}\text{ cm}^{-2} \). Reliability studies highlighted the superiority of the post-oxidized PECVD deposited oxide, resulting in a high breakdown electric field of 9.1 MV cm\(^{-1}\) and a steep Weibull function. The LPCVD deposited oxides show comparably low reliability caused probably by the use of carbon containing TEOS gas.

Table 2.4.3.a: Processing parameters, oxide thickness \( d_{\text{OX}} \), effective oxide charge \( \frac{Q_{\text{EFF}}}{q} \) and average breakdown electric field \( E_B \) of investigated 3C-SiC(001) MOS capacitors.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Oxidation/Deposition</th>
<th>Annealing</th>
<th>( d_{\text{OX}} ) (nm)</th>
<th>( \frac{Q_{\text{EFF}}}{q} ) ( \times 10^{11} \text{ cm}^{-2} )</th>
<th>( E_B ) (MV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>H\textsubscript{2}O:O\textsubscript{2}</td>
<td>1150</td>
<td>-</td>
<td>53</td>
<td>-3.0</td>
</tr>
<tr>
<td>#2</td>
<td>SiH\textsubscript{4}:N\textsubscript{2}O</td>
<td>300</td>
<td>H\textsubscript{2}O:O\textsubscript{2}</td>
<td>950</td>
<td>56</td>
</tr>
<tr>
<td>#3</td>
<td>Si(OC\textsubscript{2}H\textsubscript{5})\textsubscript{4}</td>
<td>680</td>
<td>H\textsubscript{2}O:O\textsubscript{2}</td>
<td>950</td>
<td>54</td>
</tr>
</tbody>
</table>

Additionally to the electrical characterization work presented in the paper D, further morphological investigations have been carried out. The root mean square RMS surface roughness of post-oxidized PECVD oxide and wet thermally grown oxides were characterized by atomic force microscopy in contact and tapping modes.

The analysis of the initial 3C-SiC(001) surface, the SiO\textsubscript{2} layer surface after oxide deposition (in case of the PECVD post-oxidized oxide) and after oxidation/post-oxidation was carried out (see Figure 2.4.3.a). Each surface characterization was composed of five atomic force microscope (AFM) scans of 50×50 µm\(^{2}\) area. From the AFM scans (contact mode) the surface RMS roughness of the post-oxidized PECVD oxide and the wet thermally grown oxide at the different steps of the fabrication were extracted and summarized in the Figure 2.4.3.b.
Figure 2.4.3.a: AFM pictures (tapping mode) of the initial 3C-SiC(001) surface, the SiO₂ layer surface after oxide deposition (in case of the PECVD post-oxidized oxide) and after oxidation/post-oxidation of the post-oxidized PECVD oxide and the wet thermally grown oxide.

Figure 2.4.3.b: Average RMS roughness of the initial 3C-SiC surface, the SiO₂ layer surface after oxide deposition (in case of the PECVD post-oxidized oxide) and after oxidation/post-oxidation of the post-oxidized PECVD oxide a) and the wet thermally grown oxide b).

From the Figure 2.4.3.b, several informations can be extracted. At first, the RMS roughness of the SiO₂ layer surface appears to be clearly dependent of the initial SiC surface roughness for both samples. Then, no significant increase or decrease (high standard deviation) of the SiO₂ surface roughness compared to the initial SiC surface roughness can be demonstrated for the post-oxidized PECVD oxide and
Chapter 2: Gate oxide

wet thermally grown oxide. Finally, one can observe the minimal RMS standard deviation achieved for the post-oxidized PECVD oxide. Such reduced standard deviation demonstrates the superior reliability of this process permitting the fabrication of highly homogeneous gate oxide.

On the other hand, interesting features are exhibited on the AFM picture of the SiO$_2$ layer surface of the wet thermally grown oxide: oxide bumps/peaks are present at the SiO$_2$ surface layer.

In 2010, Hosoia et al. [44] reported some investigation of surface and interface morphology of thermally grown SiO$_2$ dielectrics on 4H-SiC(0001) substrates. This work presented the significant enhancement of the 4H-SiC oxidation rate at location facing step bunching. In that way the oxide formed by dry O$_2$ oxidation at 1100 °C for 12 hours describes thickness on the step terrace and at the face of the step of 35 and 80 nm, respectively. The AFM images and, cross sectional profiles and of 4H-SiC(0001) surface (a) and SiO$_2$ surface (b) are shown in Figure 2.4.3.c. In addition, cross sectional transmission electron microscope (TEM) image of SiO$_2$/SiC structure was included (c).

Figure 2.4.3.c: AFM images and, cross sectional profiles and of 4H-SiC(0001) surface (a) and SiO$_2$ surface (b) are shown in Figure 2.4.3.c. In addition, cross sectional TEM image of SiO$_2$/SiC structure was included (c). [44]
The oxide thickness fluctuation was found to be leading to local electric field concentration around the step bunching thus resulting in early breakdown of MOS devices. In case of 3C-SiC(001), because of the on-axis crystal growth, no step bunching exists. However, high concentration of extended defects such as carbon stacking faults $SF_C$, silicon stacking faults $SF_{Si}$ and silicon-carbon stacking faults $SF_{Si-C}$, are present at the 3C-SiC surface. Those defects are electrically active and might lead to local fluctuations of the 3C-SiC oxidation rate resulting in oxide bumps described in Figure 2.4.3.b. In order to prevent the formation of such oxide bumps, one should minimize the oxidation temperature and reduce the quantity of SiC consumed during the oxidation process. From that point, the use of the post-oxidized PECVD oxide as gate oxide becomes significant: the oxide formation process of the post-oxidized PECVD oxide combines PECVD of SiO$_2$ and short post-oxidation step at low temperature oxide.

2.4.4. ONO (SiO$_2$-Si$_3$N$_4$-SiO$_2$) dielectric structures

In paper E, we evaluate the potential of ONO (SiO$_2$-Si$_3$N$_4$-SiO$_2$) structures for 4H-SiC power MOSFET gate dielectric. The electrical properties of metal-insulator-semiconductor (MIS) devices based of ONO structures fabricated on n-type 4H-SiC (0001) epilayers have been investigated. Three different combinations of low-pressure chemical vapor deposition (LPCVD), plasma-enhanced chemical vapor deposition (PECVD) and thermal oxidations (TO) in N$_2$O and wet oxygen H$_2$O:O$_2$ were studied for the formation of the ONO stack. In addition, the influence of the thickness of SiO$_2$ and Si$_3$N$_4$ layers were considered and recommendations for optimal ONO structure were given. Oxide characterization tests and reliability investigations have been performed at room and high temperatures.

4H-SiC MIS devices based on ONO stack formed via a process mixing plasma-enhanced and low pressure chemical vapor deposition techniques (PECVD + LPCVD) demonstrated superior electrical properties and reliability both at room and high temperatures. Capacitance and conductance measurements (C-G-V) carried out at room temperature were describing low interface states densities of $D_{IT}$ of $5.45 \times 10^{10}$ eV$^{-1}$cm$^{-2}$ at 0.35 eV below the conduction band and minimal effective oxide charges $Q_{EFF}$/q of $-0.15 \times 10^{10}$ cm$^{-2}$. The evaluation of the electrical properties at high temperature brought out reduced variation of the flatband voltage shift. The investigation considering the variation of the density of near interface traps $D_{NIT}$ as a function of the temperature exhibited the stability of the structure with $D_{NIT}$ values bounded between 2.9 and $14.4 \times 10^{10}$ cm$^{-2}$. 4H-SiC ONO MIS capacitors fabricated by complete PECVD technology resulted in poor electrical properties exhibiting high concentrations of oxide/interface/near-interface traps, even at room temperature.
Figure 2.4.4.a: Experimental procedure for the formation of investigated ONO structures. Three main technology combinations (TO+LPCVD, PECVD+LPCVD and PECVD) involving low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) and thermal oxidations (TO) in N₂O and wet oxygen H₂O:O₂ were regarded.
Chapter 3: Passivation layer

In power electronics, two main issuing parameters (see Figure 3.a) drastically degrade the performance and reliability of the components:
- Surface recombination current which is at the origin of early breakdowns
- Source/gate contacts short that destabilizes the device structure, performance and reliability

Figure 3.a: Scheme of the cross section of DMOSFET cells of two DMOSFETs presenting the main issues of passivation layer technology. In the Figure the abbreviation FGR corresponds to field guard ring.

3.1. Surface recombination current

The surface recombination current which is at the origin of early breakdowns of the SiC-MOSFET device is mainly due to the presence of Si- and C-dangling
bonds at the SiC surface. These dangling bonds cause electric potentials which lead to surface current. In conventional Si-technology, the passivation of the semiconductor surface (Si-dangling bonds) is commonly performed by growing a thermal oxide layer. In the particular case of the MOSFET technology post-gate oxide thermal oxidation process is not possible. For that reason, an alternative technique exists. This consists of the conservation of the gate oxide at the surface of the semiconductor. As described in the Figure 3.1.a, the remaining gate oxide layer achieving the passivation of the surface states composes the base of the passivation layer structure.

![Figure 3.1.a: Scheme of the cross section of the DMOSFET cells presenting the bottom part of the passivation layer made of remaining gate oxide layer. In the Figure the abbreviation FGR corresponds to field guard ring.](image)

In case of SiC MOSFET technology, the same technique is used. The main difference between Si- and SiC-MOSFET technologies is the nature the dangling bonds. As mentioned in chapter 2, SiC technology has to face the passivation C-dangling bonds that do not exist in case of Si. Consequently, the oxide formation processes developed for SiC-MOSFET gate oxide have to be evaluated for being used in bottom part passivation layer application.

### 3.2. Source/gate contacts short

Cracks, voids and pores present into the passivation layer short the gate and source contacts. Those contact shorts therefore lead to parasite currents and the
uncontrollability of the MOSFET. Scanning electron microscope (SEM) images of observed source/gate contacts shorts implied by voids/cracks into the passivation layer are described in Figure 3.2.a:

![SEM image of the cross section of DMOSFETs cell presenting cracks a) and voids b) into the passivation layer.](image)

As seen in Figure 3.2.a, voids and cracks start to appear at the base of the top part of the passivation layer. This part of the passivation layer is commonly made by SiO₂ deposition. The sharpness of the edge of the gate contact structure induces stress in the oxide/passivation layer during the deposition process. SiO₂ cracks appearing at the edge of the gate contact propagate across the passivation layer up to the surface leading to the formation of micro-holes. Deposited source metal pad fills SiO₂ micro-pipes and consequently contacts the gate metal. This results to the gate/source contacts short.

During the last decades, a wide range of oxide deposition technologies were developed for Si based device process. The two most commonly used technologies for passivation layer formation are: plasma-enhanced chemical vapor deposition (PECVD) and low-pressure chemical vapor deposition (LPCVD). PECVD technique demonstrates two great advantages: high deposition rate and low temperature of the deposition (200-300 °C). As drawback the deposited SiO₂ layer describes low physical and electrical properties. Unlike PECVD, the SiO₂ material formed by LPCVD achieves high physical and electrical properties. However, this technique implies low deposition rate and requires high temperature during the deposition (500-800 °C).

In SiC MOSFET technology, high temperature post gate formation processes damage the gate oxide destabilizing passivating species and creating extra densities of oxide/near-interface/interface states. For this reason, a trade-off between passivation layer quality and gate oxide preservation should be considered. Oxide deposition techniques and etching processes smoothing the gate contact edges are
nowadays investigated to minimize the creation of voids/cracks into the passivation layer.

3.3. Characterization techniques

Different characterization techniques are used to investigate the bottom and top parts of the fabricated passivation layers.

3.3.1. Bottom passivation layer part

The electrical properties and reliability of the bottom part insuring the passivation of surface states and therefore reducing the surface recombination current can be characterized in the same way as the gate oxide. Capacitance and conductance measurements (C-G-V) judge the electrical properties while current measurements (I-V) investigate the reliability. Those characterization methods are described in the gate oxide related part of this report in chapter 2. On the other hand, one can implement investigated passivation layers on devices directly impacted by the presence of surface recombination current to judge their efficiencies. Paper F demonstrates the possibility of evaluating the efficiency of studied passivation layers by implementing them on a Bipolar Junction Transistor (BJT) and measuring the current gain of these devices.

3.3.2. Top passivation layer part

As described before, the main issue for the top part of the passivation layer is the formation of cracks/voids during the deposition process. Consequently, TEM and SEM images of the cross section of passivation layers deposited on top of the gate contact structures can be used to judge of the integrity of the top passivation layer parts.

3.4. Results

3.4.1. Surface passivation effects on the performance of 4H-SiC BJTs

In paper F, the electrical performance in terms of maximum current gain and breakdown voltage has been compared experimentally and by device simulation for 4H-SiC BJTs passivated with different surface passivation layers. Variation in BJT performance has been correlated to densities of interface traps and fixed oxide charge, as evaluated through MOS capacitors. As described in Table 3.4.1.a, six different methods were used to fabricate SiO₂ surface passivation on BJT samples from the same wafer. Our study reports that 4H-SiC BJTs performance can be related to the interface traps and effective oxide charges that were evaluated
through MOS structures. Our results indicate that around 60% higher maximum current gain can be achieved by a new surface passivation layer with low interface trap density. This layer consists of a PECVD deposited SiO$_2$ layer followed by post-anneal in N$_2$O ambient. However, this passivation can provide different effective oxide charge compared to conventional passivation layers and this can affect the optimum doses of implanted dopants in JTE area, resulting in reduced breakdown voltage. Therefore, modification of JTE implantation dose may be needed when applying new passivation layers to high voltage SiC devices.

Table 3.4.1.a: Processing parameters of investigated passivation layers technologies.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Oxidation/Deposition</th>
<th>Annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>gas species</td>
<td>T(°C)</td>
</tr>
<tr>
<td>1</td>
<td>N$_2$O</td>
<td>1250</td>
</tr>
<tr>
<td>2</td>
<td>NO</td>
<td>1200</td>
</tr>
<tr>
<td>3</td>
<td>O$_2$</td>
<td>1100</td>
</tr>
<tr>
<td>4</td>
<td>TEOS-N$_2$O</td>
<td>680</td>
</tr>
<tr>
<td>5</td>
<td>TEOS-Wet</td>
<td>680</td>
</tr>
<tr>
<td>6</td>
<td>PECVD-N$_2$O</td>
<td>300</td>
</tr>
</tbody>
</table>

3.4.2. Top passivation layer part for 3C- and 4H-SiC MOSFETs

Three different alternative methods to form top part of passivation layer for power MOSFET devices applications were investigated: PECVD, low-stress PECVD and LPCVD low-temperature oxide LTO. In the Table 3.4.2.a, process parameters of considered deposition methods are described.

Table 3.4.2.a: Process parameters of PECVD, low-stress PECVD and LPCVD LTO.

<table>
<thead>
<tr>
<th>Deposition process</th>
<th>Gases (sccm)</th>
<th>Pressure (mTorr)</th>
<th>HF Power (W)</th>
<th>Temperature (°C)</th>
<th>Dep. rate (nm/min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PECVD</td>
<td>SiH$_4$:N$_2$O (710:425)</td>
<td>800</td>
<td>20</td>
<td>300</td>
<td>67</td>
</tr>
<tr>
<td>Low-stress PECVD</td>
<td>SiH$_4$:N$_2$O (75:700)</td>
<td>400</td>
<td>10</td>
<td>300</td>
<td>14</td>
</tr>
<tr>
<td>LPCVD LTO</td>
<td>SiH$_4$:O$_2$ (2.8:21.9)</td>
<td>300</td>
<td>-</td>
<td>400</td>
<td>4.2</td>
</tr>
</tbody>
</table>
Passivation layers of 1 µm thickness were deposited on top of DMOSFETs gate contact structures processed on 3 inch SiC and Si wafers. The gate electrode is formed of 400 nm of LPCVD poly-Si and 100 nm of TiW. The integrity of deposited SiO$_2$ passivation layers was characterized via cross sectional SEM pictures and by current measurements. From the wafer scale electrical measurements, the failure rate of DMOSFETs was estimated. The failure rate corresponds in that particular case to the number of gate/source shorted devices divided by the total number of analyzed devices. Deposited oxide passivation layers morphological and electrical characteristics have been listed in Table 3.4.2.b.

Figure 3.4.2.a, b and c show cross sections of DMOSFET cell structures based on PECVD, low-stress PECVD and LPCVD LTO technologies for the passivation layer formation.

Figure 3.4.2.a: SEM image of the cross section of DMOSFET cell presenting voids into the PECVD based passivation layer.

Figure 3.4.2.b: SEM image of the cross section of DMOSFET cell presenting cracks into the low-stress PECVD based passivation layer.
Cross sectional SEM image of the deposited PECVD SiO$_2$ passivation layer displays wide voids close to gate contact edges (see Figure 3.4.2.a). These voids propagate up to the source contact and metal pad leading to gate/source shortcut. Electrical measurements highlight a failure rate of 64.5%.

Low-stress PECVD oxide sample results in the formation of cracks propagating from the gate contact edges to the surface of the deposited oxide layer (see Figure 3.4.2.b). The electrical characterization of devices results in a failure rate of 12.1%. The creation of cracks and not voids (as in the case of PECVD oxide) indicates the achievement of a significant reduction of the stress of the deposited SiO$_2$ film.

![Cross sectional SEM image of the deposited PECVD SiO$_2$ passivation layer](image)

Figure 3.4.2.c: SEM image of the cross section of DMOSFET cell presenting voids into the LPCVD LTO based passivation layer.

LPCVD LTO sample demonstrates the presence of minimal cracks at the gate electrode edge which do not propagate through the oxide layer (see Figure 3.4.2.c). Current measurement describes that no source/gate shortcuts are present over the three inch wafer.

Table 3.4.2.b: Morphological and electrical characterization results of PECVD, low-stress PECVD and LPCVD LTO.

<table>
<thead>
<tr>
<th>Deposition Process</th>
<th>Crack/Void</th>
<th>Failure rate (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PECVD</td>
<td>Void</td>
<td>65.5</td>
</tr>
<tr>
<td>Low-stress PECVD</td>
<td>Crack</td>
<td>12.1</td>
</tr>
<tr>
<td>LPCVD LTO</td>
<td>-</td>
<td>0</td>
</tr>
</tbody>
</table>
Chapter 4: Gate contact

As briefly described in the first chapter of this report, SiC power MOSFETs would be components of choice for high frequency power switches. For this reason, development of low resistance gate electrode should be considered [18]. In conventional silicon technology the gate contact of power devices is most commonly formed by low-pressure chemical vapor deposition (LPCVD) of poly-Si layer highly doped with phosphorous. Post-deposition high temperature anneal is performed to form the poly-Si and activate the phosphorous dopant. This results in the achievement of the low resistivity of the poly-Si film and consequently the gate contact.

Apart from its low resistivity, poly-Si material demonstrates remarkable benefits when it is used as gate electrode for MOS devices:

- Because poly-Si is a semiconductor, its workfunction can be modulated by adjusting its doping concentration. Therefore that results in the possibility of tuning the threshold voltage of the MOS devices. By contrast, metals’ workfunctions cannot easily be modified, so tuning the work function to obtain low threshold voltages becomes a significant challenge. Furthermore, in CMOS technology, obtaining low-threshold voltage devices on both PMOS and NMOS devices would likely require the use of different metals for each device type, introducing additional complexity to the fabrication process.

- Unlike the metal/SiO$_2$ interface, the poly-Si/SiO$_2$ interface demonstrates rather low concentration of defects. Most of metal/insulator interfaces describe significant levels of defects which can lead to Fermi-level pinning, charging, or other phenomena that degrade device performances.

- In the MOSFET IC fabrication process, it is preferable to deposit the gate electrode material prior to certain high-temperature steps in order to make better-performing transistors. Such high temperature steps would melt some metals, limiting the types of metal that can be used in a metal-gate-based process.
The use of poly-Si as gate electrode improves significantly the reliability of the gate oxide [45] with respect to metal gate contact: while metal gate electrodes induce ions to the oxide layer degrading the reliability of the devices, Poly-Si based electrode does not affect the quality of the gate oxide.

For all these reasons, poly-Si technology has been standard for the last twenty years in Si power electronics technology.

In SiC MOSFET technology, because of using passivating species during the gate oxide formation process, the post-gate oxide formation thermal budget should remain rather low. The case of the 3C-SiC MOSFET represents the most challenging issue. As described in the gate oxide related part of this report (chapter 2), optimal oxide quality for 3C-SiC is achieved when using wet oxygen conditions ($H_2O:O_2$) during the oxidation/post-oxidation process. Hydrogen passivation of oxide and interface defects demonstrates significant improvement of the electrical properties of the formed 3C-SiC based oxide. However, desorption of hydrogen atoms is rather intense at temperatures higher than 800 °C. Such a phenomenon would lead to the degradation of the oxide quality. From that point, the deposition and activation processes of poly-Si for 3C-SiC MOS devices should describe a minimal thermal budget. Such reduced thermal budget should help to preserve the high electrical properties of the oxide.

4.1. Formation of low resistance gate electrode

In order to minimize the thermal budget of the deposition step, the formation of the Poly-Silicon layer is achieved by low-pressure chemical vapor deposition LPCVD mixing $SiH_6$ and $PH_3:H_2$ precursors at 380 °C. That results in achieving amorphous poly-Si (before activation) describing a phosphorous doping concentration in the range of $10^{20} \text{ cm}^{-3}$.

4.1.1. Bi-layer gate contact structure for 3C-SiC

To prevent and avoid the hydrogen desorption from the 3C-SiC based oxide, poly-Si activation process should not be carried out at temperatures higher than 800 °C. After annealing at that temperature, poly-Si layers demonstrate typical resistivity $\rho$ values of about 1.5-1.8 m$\Omega$cm. Correspondingly, the sheet resistance $R_s$ of films of 300 nm thickness is estimated to 50-60 $\Omega$/sqr. That rather high resistivity of the Poly-Si film is mainly due to the incomplete activation of the phosphorous dopant. In order to reduce the gate electrode resistance the implementation of a metal layer on top of the poly-Si layer (after activation) can be used, which results in achieving more than 50% decrease of the gate stack sheet resistance. However one has to take into account of the compatibility of this process with the complete SiC MOSFET fabrication process. Post-gate electrode formation high temperature treatment such as the one for the ohmic contacts formation (silicidation process...
carried out at 950 °C) might lead to the intense reaction of the top gate contact metal layer with the poly-Silicon film.

4.1.2. Single layer gate contact structure for 4H-SiC

The oxide and interface states passivation of 4H-SiC based oxides is commonly achieved by using nitrogenated atmospheres (N₂O, NO) during the oxidation/post-oxidation steps (see chapter 2). With respect to hydrogen atoms, nitrogen demonstrates superior stability and can stand higher temperature before diffusing from the oxide.

One the other hand, in case of 4H-SiC MOSFET technology, silicidation processes carried out at temperature of 950 °C have to be performed in order to create low resistance source/drain ohmic contacts. Consequently, one can combine the activation of the poly-Si film with the contacts silicidation annealing. That results in the minimization of the oxide thermal budget and achieving typical poly-Si layer resistivity of 1.0 mΩcm. As described in the case of 3C-SiC the implementation of an extra metal layer on top of the poly-Si film cannot be performed for 4H-SiC: annealing at 950 °C would lead to the intense reaction of the top gate contact metal layer with the poly-silicon film.

4.2. Characterization techniques

In order to evaluate the potential of a gate electrode process formation, two main parameters have to be considered:

- The gate electrode resistance. This parameter is most commonly characterized by measuring the value of the sheet resistance $R_s$ and resistivity $\rho$ of the gate contact structure using the four-point probe method.
- The gate oxide quality. In order to judge of the preservation of the gate oxide quality, MOS capacitors are manufactured and electrically characterized.

4.2.1. Four-point probe method

The four-point probe method developed by Van der Pauw, permits the measurement of the sheet resistance of a thin conductive film. That characterization technique consists in applying current through two probes placed at a distance $D$ of each other and sensing the resulting voltage between two other probes placed at a reduced distance $d$ (see Figure 4.2.1.a section a)). As described in Figure 4.2.1.a section b), several resistances have to be taken into account for measuring accurately the sheet resistance. Each probe demonstrates an associated resistance $R_P$ which can be determined by shorting two probes and measuring their resistances. At the interface between the probe tip and the semiconductor, there is
also a probe contact resistance named $R_{CP}$ (see Figure 4.2.1.a section b)). Finally, when the current flows from the small tip into the semiconductor and spreads out in the semiconductor, there will be a spreading resistance, $R_{SP}$. Finally the thin conductive film itself describes a sheet resistance $R_S$.

The equivalent circuit for the measurement of sheet resistance is shown in Figure 4.2.1.a section c). Exhibited parasitic resistances can be neglected for the two voltage probes ($R_P$, $R_{CP}$, $R_{SP}$) because the voltage is measured with a high impedance voltmeter, which draws very little current.

Thus the voltage drops across these parasitic resistances are insignificant. The measured voltage from the voltmeter is approximately equal to the voltage drop across the thin conductive film sheet resistance. By using the four-point probe method, the thin film sheet resistance can be calculated using the following Equation 4.2.1.a:

$$R_S = F \frac{V}{I},$$

(4.2.1.a)

where $V$ is the measured voltage, $I$ is the applied current by the two current carrying probes (1 and 4), and $F$ is a correction factor. For collinear or in-line probes with equal probe spacing configuration, the correction factor $F$ can be written as a product of three separate correction factors:
Fabrication and Characterization of 3C- and 4H-SiC MOSFETs

\[ F = F_1 F_2 F_3, \]

(4.2.1.b)

where \( F_1 \) takes into account the non-homogeneity of the sample thickness, \( F_2 \) corrects for finite lateral sample dimensions, and \( F_3 \) corrects for placement of the probes with finite distances from the sample edges. For very thin samples with the probes being far from the sample edge, \( F_2 \) and \( F_3 \) are approximately equal to 1, and the expression of the thin film sheet resistance becomes:

\[ R_S = \frac{\pi V}{\ln(2) I} \]

(4.2.1.c)

Finally, the value of the resistivity \( \rho \) can be estimated via the Equation 4.2.1.d:

\[ \rho = R_S \times t, \]

(4.2.1.d)

where \( t \) represents the thickness of the considered deposited layer. The four-point probe method can eliminate the effect introduced by the probe resistance, probe contact resistance and spreading resistance. Therefore it has more accuracy than the two probes measurement method.

4.2.2. Gate oxide characterization

Capacitance and conductance measurements (C-G-V) judge of the electrical properties while current measurements (I-V) investigate the reliability. Those characterization methods are described in the gate oxide related part of this report.

4.3. Results

4.3.1. Optimization of poly-Si process for 3C-SiC based MOS devices

The benefits of the implementation of an advanced oxidation process combining PECVD (Plasma Enhanced Chemical Vapor Deposition) SiO\(_2\) deposition and short post-oxidation steps in wet oxygen has been previously demonstrated (see Paper G). The concentrations of fixed and mobile charges in the oxide and at the SiO\(_2\)/SiC interface were significantly reduced. Silicon technologies have indicated earlier the benefits of poly-silicon gate for MOS devices. Significant improvements in terms of gate oxide reliability were achieved [46-48]. Because of the desorption of hydrogen atoms used for the passivation of defects in 3C-SiC based oxides, the deposition and activation processes of poly-Si for 3C-SiC MOS devices should describe a minimal thermal
budget. Such reduced thermal budget should help to preserve the high electrical properties of the oxide.

In this study we report on the influence of the poly-silicon activation process on the electrical properties of 3C-SiC MOS structures. The poly-Silicon activation has been carried out by five different processes. The influence of two main parameters has been considered: the type of the process (Thermal Annealing and Rapid Thermal Annealing) and the gas species composing the annealing atmosphere (argon, dry and wet oxygen).

Our study demonstrates the efficiency of the minimization of the thermal budget during the activation of the poly-silicon layer on the preservation of the oxide quality. 3C-SiC MOS capacitors fabricated using rapid thermal annealing under argon atmosphere describe superior electrical properties of the oxide, describing low defects densities and oxide charges $Q_{\text{EFF}}/q$ equal to $2.9 \times 10^{11} \text{ cm}^{-2}$. The interface traps density $D_{\text{IT}}$ has been estimated to $7.4 \times 10^{10} \text{ eV}^{-1}\text{ cm}^{-2}$ at 0.63 eV below the conduction band. The reliability study has assessed high oxide breakdown field $E_B$ of 9.4 MVcm$^{-1}$. The Weibull analysis of TZDB measurements has brought out the sharp distribution of these oxide breakdown field values.

Table 4.3.1.a.: Poly-Si activation process parameters, sheet resistance of the poly-Silicon layer after activation $R_S$, oxide thickness $d_{\text{OX}}$, effective oxide charge ($Q_{\text{EFF}}/q$), and average breakdown electric field ($E_B$) of MOS capacitors.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Gas species</th>
<th>$T$ (°C)</th>
<th>Technology</th>
<th>$R_S$ (Ω/sqr)</th>
<th>$d_{\text{OX}}$ (nm)</th>
<th>$Q_{\text{EFF}}/q$ ($\times 10^{11}$ cm$^{-2}$)</th>
<th>$E_B$ (MV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>H$_2$O:O$_2$</td>
<td>800</td>
<td>TA</td>
<td>67.3</td>
<td>58</td>
<td>16.7</td>
<td>5.8</td>
</tr>
<tr>
<td>#2</td>
<td>O$_2$</td>
<td>800</td>
<td>TA</td>
<td>64.2</td>
<td>53</td>
<td>9.1</td>
<td>8.9</td>
</tr>
<tr>
<td>#3</td>
<td>Ar</td>
<td>800</td>
<td>TA</td>
<td>38.7</td>
<td>55</td>
<td>2.9</td>
<td>5.9</td>
</tr>
<tr>
<td>#4</td>
<td>O$_2$</td>
<td>800</td>
<td>RTA</td>
<td>52.5</td>
<td>55</td>
<td>3.2</td>
<td>8.7</td>
</tr>
<tr>
<td>#5</td>
<td>Ar</td>
<td>800</td>
<td>RTA</td>
<td>50.2</td>
<td>52</td>
<td>3.9</td>
<td>9.4</td>
</tr>
</tbody>
</table>
Chapter 5: Source-drain contacts

As stated in Chapter 1, SiC power devices are expected to have higher efficiency and lower on-state resistance in comparison to Si power devices. The on-state resistance is characterized by the serial connection of the resistances of the metal connections and the semiconductor plus the resistance of the metal to semiconductor contacts. Hence, the resistance of the ohmic contacts to source and drain can contribute significantly to the total on-state resistance of a MOSFET device. Ohmic contacts are commonly characterized by the specific contact resistance $\rho_C$, which is a contact geometry independent, intrinsic interface property. An ohmic contact formation process is therefore needed, which minimizes the voltage drop over the contact interface. High-frequency and high-power SiC electronic devices require ohmic contacts with contact resistance values in the range of $10^{-5}$-$10^{-6}$ $\Omega \text{cm}^2$ [24]. In addition, as SiC devices should in some applications also be able to operate in harsh environments and at elevated temperatures, the ohmic contacts should have a high reliability and resistance to environment related degradation (oxidation, chemical attacks, exposure to radiation, etc…).

The ohmic contact between a metal and a semiconductor allows charge carriers to flow in and out of the semiconductor without any large barrier or threshold (resistance). Two different methods can be used to form an ohmic contact system. One method consists of band alignment, where the difference $\Phi_{MSC}$ of the metal and semiconductor workfunctions is negative for n-type semiconductors and positive for p-type semiconductors (see Figure 5.a). Another approach to form ohmic contacts is to minimize the space charge depletion region formed by the metal-semiconductor contact (Schottky barrier contact) to enable tunneling of charge carriers through the barrier. The space charge region can be minimized by introducing high doping concentrations in the vicinity of the contact area. The band diagram of a deposited metal on heavily n- and p-doped semiconductors is shown in figure 5.b. When a metal is deposited on top of a heavily doped ($N > 1 \times 10^{19} \text{ cm}^{-3}$) semiconductor layer, the Schottky barrier will have the same height as in the case of low doped material, but the depletion region width $W_{DEP}$
will be reduced. If the depletion region is thin enough, electrons or holes can tunnel through the thin energy barrier forming tunnel ohmic contacts.

![Figure 5.a](image)

Figure 5.a: Scheme of the energy band diagram of metal/semiconductor ohmic contact by band alignment for n- and p-type semiconductor, respectively. In this schematic representation $VL$ corresponds to the vacuum level, $E_C$ to the conduction band edge, $E_V$ to the valence band edge, $E_F$ to the Fermi level, $\chi$ to the electron affinity, $\Phi_{SC}$ to the semiconductor workfunction and $\Phi_M$ to the metal workfunction.

Conduction mechanisms relevant for charge carriers in metal semiconductor contacts are thermionic emission, thermionic field emission, and tunneling. Different carrier conduction mechanisms dominate depending on the semiconductor doping concentration. The parameter which determines the dominant conduction mechanism can be described as in Equation 5.a [49]:

$$E_{00} = \frac{h}{4\pi} \left( \frac{N}{m\varepsilon} \right)^{\frac{1}{2}},$$

(5.a)

where $h$ is the Planck's constant, $N$ the doping concentration, $m$ the effective mass and $\varepsilon$ the dielectric constant.

$E_{00}$ describes the relationship between the semiconductor doping $N$ and temperature $T$. $kT/qE_{00}$ indicates which conduction mechanisms should dominate:

- For lightly doped semiconductors ($N < 1\times10^{17}$ cm$^{-3}$), $kT/qE_{00} \gg 1$ and thermionic emission is dominant. In that configuration, carriers having sufficient thermal energy to surmount the Schottky barrier can pass from the semiconductor to the metal and vice versa.
- For intermediate doping levels ($1\times10^{17} < N < 1\times10^{19}$ cm$^{-3}$), $kT/qE_{00} \approx 1$, the thermionic field emission process is dominant.
For heavily doped semiconductors \((N > 1 \times 10^{19} \text{ cm}^{-3})\), \(kT/qE_{00} \ll 1\) and tunneling dominates.

The expression of specific contact resistance \(\rho_c\) depends also on the doping concentration of the semiconductor and can be described as in the Equations 5.b, c and d for light, intermediate and high doping concentrations \(N\), respectively.

\[
\rho_c = \frac{k}{qTA^*} \exp \left( \frac{q\Phi_B}{kT} \right),
\]

\[
\rho_c \propto \exp \left( \frac{\Phi_B}{\sqrt{N}} \right),
\]

\[
\rho_c \propto \exp \left( \frac{\Phi_B}{E_{00} \coth \left( \frac{E_{00}}{kT} \right)} \right),
\]

\(5.0\)
Chapter 5: Source-drain contacts

where $T$ corresponds to the temperature, $A^{**}$ to the Richardson’s constant, $q\Phi_B$ ($= q\Phi_M - q\chi$) to the Schottky barrier, $N$ the doping concentration of the semiconductor and $k$ to the Boltzmann’s constant.

As described earlier in Chapter 1, the fabrication of low resistance ohmic contacts is rather complex in SiC technology. A scheme representing the band diagrams of 3C-, 4H-SiC and Si (for reference) and the workfunctions of the most commonly used metals in microelectronics is shown in Figure 5.c.

N- and p-type 4H-SiC do not demonstrate ohmic structure by band alignment with any of the presented metals. The Fermi levels in the metals are positioned in the band gap of 4H-SiC. As a result, Schottky barrier $q\Phi_B$ heights on n- and p-type 4H-SiC are larger than 1 eV, which exhibits the complexity of achieving low specific contact resistance ohmic contacts.

In case of 3C-SiC, the complexity of achieving low resistance ohmic contacts is not related to a concern of workfunction (at least for n-type 3C-SiC). As described earlier in this report, even if remarkable efforts were made to improve the crystal quality of 3C-SiC, densities of defects/states present at the surface of 3C-SiC material remain rather high. Extended crystal defects such as carbon stacking faults $SF_C$, silicon stacking faults $SF_{Si}$ and silicon-carbon stacking faults $SF_{Si-C}$ are electrically active and pin the Fermi level $E_F$ of the semiconductor [51]. This pinning induces deformations of the conduction and valence band edges resulting in the degradation of the ohmic contact quality or leading to the formation of leaky Schottky contacts.

![Figure 5.c: Scheme describing the band diagrams of 3C-, 4H-SiC and Si (for reference) and the workfunctions of the most commonly used metal in microelectronics (Al, Ti, Ag, Cu, W, Ni and Au) [50].](image-url)
A great deal of effort has been spent to study the physics of metal contacts on SiC and to achieve low resistivity reliable ohmic contacts. The interest of the scientific community has resulted in a large number of review papers dealing with ohmic contacts [19, 52-55].

5.1. Ohmic contacts to 4H-SiC

5.1.1. Ohmic contacts to n-type 4H-SiC

Ohmic contacts to n-type 4H-SiC are essential for vertical device structures as n-type substrate material is typically used and the substrate contact should have perfect ohmic characteristics. The material quality and doping technology improvements realized during the last decade resulted in the availability of high quality and highly doped substrates, as well as epitaxial layers. But the ohmic contact formation to high doped material was already studied from the beginning of the SiC device development. A variety of reports have demonstrated that ohmic contacts with \( \rho_C \) in the range of \( 10^{-6} \Omega \text{cm}^2 \) can be formed on heavily doped n-type SiC material (\( > 10^{19} \text{cm}^{-3} \)). Table 5.1.1.a lists ohmic contact systems reported in the literature and the achieved values of the specific contact resistance \( \rho_C \). A wide range of doping concentrations obtained either by epitaxial growth or by ion-implantation have been used for the contact studies and the metal contacts were heat treated to form the desired low resistive metal semiconductor interface. A variety of different annealing conditions were investigated, including change in temperature, anneal duration, and anneal atmosphere. The \( \rho_C \)-values were determined by means of the transfer length method (TLM).

The Schottky barrier height \( q\Phi_B \) determines the current transport in metal semiconductor contacts. For the fabrication of ohmic contacts, metals with low Schottky barriers are preferred and the ideal case would be a Schottky barrier close to 0 V. In n-type 4H-SiC, all as-deposited metals have a Schottky barrier of more than 0.5 V. As indicated in Table 5.1.1.a, annealed Ni has been the most widely used metal for ohmic contact formation to n-type 4H-SiC. The Schottky barrier height \( q\Phi_B \) for Ni/SiC contacts depends on the surface preparation prior to the metal deposition. \( q\Phi_B \) ranges from 1.40 V to 1.59 eV for as-deposited and unannealed Ni contacts [56-58]. Therefore, post-deposition annealing at temperatures in the range of 900-1000°C is required to form low resistive ohmic contacts.

The first papers reporting on the Ni/4H-SiC system focused on the structural characterization of the Ni/4H-SiC interface. Pai et al. [59] reported structural investigations of annealed Ni-films carried out by combining Rutherford backscattering spectrometry (RBS) with x-ray diffraction (XRD). No reaction of the Ni film with the SiC surface could be detected after annealing at temperatures up to 400°C. The Ni-film reacted completely with SiC at a temperature of 500°C.
and Ni silicide phases with a thin carbon rich layer beneath the silicided contact were formed. Recently it has been shown by chemical analysis that Ni becomes mobile at temperatures above 400°C and reacts with Si to form Ni silicides [60]. However, ohmic behavior is typically not observed at temperatures below 900-1000°C. Such high temperatures enhance the dissociation of Si and carbon bonds at the interface and hence enforce the formation of Ni$_x$Si$_y$. The remaining carbon agglomerates in large carbon clusters down to a depth of about 20 nm from the silicide/SiC interface. These carbon clusters might enable the formation of low resistive ohmic contacts.

Table 5.1.1.a: Reported ohmic contacts to n-type 4H-SiC material. Adapted from [55].

<table>
<thead>
<tr>
<th>Metal</th>
<th>Annealing conditions</th>
<th>N_D (at/cm$^3$)</th>
<th>(\rho_C) ((\Omega)cm$^2$) (TLM)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>-</td>
<td>(&gt;10^{20}) P-impl.</td>
<td>0.54-1.2(\times)10^{-6}</td>
<td>[61]</td>
</tr>
<tr>
<td>Al/Ni</td>
<td>1000 °C, 2 min, Ar</td>
<td>(2\times10^{20}) P-impl.</td>
<td>4.8(\times)10^{-5}</td>
<td>[62]</td>
</tr>
<tr>
<td>Co/Si/Co</td>
<td>500 °C, 5 min + 800 °C, 2 min, vacuum</td>
<td>1.1(\times)10^{19} epi.</td>
<td>1.8(\times)10^{-6}</td>
<td>[63]</td>
</tr>
<tr>
<td>Mo</td>
<td>-</td>
<td>(&gt;10^{20}) P-impl.</td>
<td>2(\times)10^{-6}</td>
<td>[61]</td>
</tr>
<tr>
<td>Nb</td>
<td>1100 °C, 10 min, atm</td>
<td>1.3(\times)10^{19} epi.</td>
<td>&lt;1(\times)10^{-6}</td>
<td>[64]</td>
</tr>
<tr>
<td>Ni</td>
<td>-</td>
<td>(&gt;10^{20}) P-impl.</td>
<td>3(\times)10^{-6}</td>
<td>[61]</td>
</tr>
<tr>
<td>Ni</td>
<td>1000 °C, 1 min, atm</td>
<td>4.2(\times)10^{15} epi.</td>
<td>2.8(\times)10^{-3}</td>
<td>[65]</td>
</tr>
<tr>
<td>Ni</td>
<td>1000 °C, 2 min, Ar</td>
<td>(&gt;10^{20}) P-impl.</td>
<td>1.2(\times)10^{-6}</td>
<td>[66]</td>
</tr>
<tr>
<td>Ni</td>
<td>950 °C, 10 min, Ar</td>
<td>l(\times)10^{19} epi.</td>
<td>2.8(\times)10^{-6}</td>
<td>[67]</td>
</tr>
<tr>
<td>Ni</td>
<td>1000 °C, 2 min, Ar</td>
<td>(2\times10^{20}) P-impl.</td>
<td>6(\times)10^{-6}</td>
<td>[68]</td>
</tr>
<tr>
<td>Ni/Si</td>
<td>950 °C, 10 min, Ar</td>
<td>l(\times)10^{19} epi.</td>
<td>2.7(\times)10^{-5}</td>
<td>[67]</td>
</tr>
<tr>
<td>NiCr</td>
<td>1100 °C, 3 min, vacuum</td>
<td>1.3(\times)10^{19} epi.</td>
<td>1.2(\times)10^{-5}</td>
<td>[69]</td>
</tr>
<tr>
<td>Si/Ni</td>
<td>900 °C, 10 min, Ar</td>
<td>2(\times)10 epi.</td>
<td>1.9(\times)10^{-6}</td>
<td>[70]</td>
</tr>
<tr>
<td>Ti</td>
<td>-</td>
<td>(&gt;10^{20}) P-impl.</td>
<td>2.7(\times)10^{-7}</td>
<td>[61]</td>
</tr>
<tr>
<td>Pt/TaSi$_2$/Ti</td>
<td>600 °C, 30 min, N$_2$</td>
<td>2(\times)10^{19} epi.</td>
<td>4.7(\times)10^{-4}</td>
<td>[71]</td>
</tr>
<tr>
<td>TiC</td>
<td>-</td>
<td>1.3(\times)10^{19} epi.</td>
<td>9.2(\times)10^{-6}</td>
<td>[72]</td>
</tr>
<tr>
<td>TiC</td>
<td>950 °C, 2 min, H$_2$/Ar</td>
<td>1.3(\times)10^{19} epi.</td>
<td>4.0(\times)10^{-5}</td>
<td>[72]</td>
</tr>
</tbody>
</table>

The mechanism of ohmic contact formation in the nickel silicide/SiC system is still widely discussed. Two possible reasons are favored:

- A first hypothesis discusses the possibility of reducing the Schottky barrier height of metals by silicidation. Different silicide phases might result in different Schottky barrier heights. For example, Han et al.[73] discovered the effective Schottky barrier height of nickel silicide contacts on lightly doped 4H-SiC increases from 1.55 to 1.81 eV after annealing at 600°C, but decreases again to 1.25 eV after annealing at 800°C.
A second theory attributes the formation of ohmic contacts to the presence of carbon vacancies due to the agglomeration of carbon clusters at the edge of the nickel silicide region. Carbon vacancies below the contact act as donors for electrons resulting in a reduction of the depletion layer width [73].

5.1.2. Ohmic contacts to p-type 4H-SiC

Due to the wide band gap of 4H-SiC low Schottky barrier height values of commonly available contact metals are difficult to obtain. The large band gap of 4H-SiC (3.2 eV) together with the electron affinity of the material (around 4 eV) leads to a position of the valence band more than 6 eV away from the vacuum level (see Figure 5.b). Since most of the metals have workfunctions in the range of 4-5.5 eV, a significantly high energy difference arises between the conducting carriers of the metal and the Fermi level in the p-type 4H-SiC material.

The reports on ohmic contacts to p-type 4H-SiC are less extensive than for n-type material. Table 5.1.2.a summarizes reported ohmic contacts to p-type 4H-SiC including the used metals and annealing conditions.

Because of the possibility of increasing the Al doping concentration of SiC material by Al diffusion during the contact annealing process, leading to the reduction of the Schottky barrier width and enhancing the tunneling probability of holes, Al-based alloyed contacts received much attention for ohmic contacts to p-type 4H-SiC. Many investigations have been reported on Al-based ohmic contacts, and in particular on mixed Al/Ti contacts.

Al/Ti contacts are generally not ohmic after deposition. Annealing temperatures above 900°C are required to obtain ohmic behavior. The first quantitative investigation on the electrical properties of Al/Ti contacts on p-type 4H-SiC was reported by Crofton et al. [74] in 1997. In this investigation, a wide doping concentration range of 4H-SiC epitaxial layers was considered and $\rho_C$ was measured by means of circular TLM structures. Al/Ti contacts annealed at 1000°C could demonstrate ohmic behavior with a low value of $\rho_C$ estimated to $5\times10^{-6}\ \Omega\text{cm}^2$.

A number of studies investigated the correlation between the structural and electrical properties of Al/Ti contacts on p-type SiC. Possible mechanisms describing the ohmic contact formation have been suggested. One interesting report was submitted by Crofton et al. [75] in 2002. Al/Ti alloys annealed at 1000°C were characterized. By etching away the annealed metal layer, the presence of many pits on the SiC surface was revealed. It was suggested that these pits might be intrusions enhancing the field emission at the metal/SiC interface, thus lowering the contact resistivity. This interpretation does not confirm the hypothesis of increased p-type doping by Al-diffusion into the SiC material. After observing that the binary Al-Ti phase diagram exhibits multiple phases prior to any
Chapter 5: Source-drain contacts

The reaction of the metal with SiC, the ohmic behavior was correlated to the presence of a liquid phase appearing at the annealing temperature of 1000°C. Despite progress in the determination of the optimized Al/Ti composition, technical challenges remain. Reactions produced in the SiC substrate lead to contact degradation limiting the degree of spiking and the reproducibility of the contact resistance. Transition metals such as Ni were also considered and investigated as ohmic contacts to p-type SiC, since they react with SiC forming silicides. In addition, metal silicides demonstrate low resistivity, and high thermal stability, thus making them promising for the high temperature operation.

Table 5.1.2.a: Reported ohmic contacts to p-type 4H-SiC material. Adapted from [55].

<table>
<thead>
<tr>
<th>Metal</th>
<th>Annealing conditions</th>
<th>(N_A) (at/cm(^3))</th>
<th>(\rho_C) ((\Omega\cdot\text{cm}^2)) (TLM)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>1000 °C, 2 min, vacuum</td>
<td>4.8×10(^{18}) epi.</td>
<td>4.2×10(^{-4})</td>
<td>[76, 77]</td>
</tr>
<tr>
<td>Al/Ni</td>
<td>1000 °C, 2 min, Ar</td>
<td>7×10(^{20}) Al-impl.</td>
<td></td>
<td>[62]</td>
</tr>
<tr>
<td>Al/Ti</td>
<td>900 °C, 3 min, vacuum</td>
<td>1×10(^{19}) epi.</td>
<td>6.4×10(^{4})</td>
<td>[78]</td>
</tr>
<tr>
<td>Al/Ti/Al</td>
<td>1000 °C, 2 min, vacuum</td>
<td>4.8×10(^{18}) epi.</td>
<td>3.3×10(^{-4})</td>
<td>[76, 77]</td>
</tr>
<tr>
<td>Al/Ti/Pt/Ni</td>
<td>1000 °C, 2 min, vacuum</td>
<td>6-8×10(^{18}) epi.</td>
<td>9×10(^{-5})</td>
<td>[79]</td>
</tr>
<tr>
<td>Al-Si/Ti</td>
<td>950 °C, 5 min, Ar</td>
<td>3-5×10(^{19}) epi.</td>
<td>9.6×10(^{5})</td>
<td>[80]</td>
</tr>
<tr>
<td>Al/Ti</td>
<td>1000 °C, 2 min</td>
<td>1.3×10(^{19}) epi.</td>
<td>5×10(^{6})</td>
<td>[75]</td>
</tr>
<tr>
<td>CoAl</td>
<td>900 °C, 5 min, vacuum</td>
<td>9×10(^{18}) epi.</td>
<td>4×10(^{-4})</td>
<td>[81]</td>
</tr>
<tr>
<td>Al/Ti/Ge</td>
<td>600 °C, vacuum</td>
<td>4.5×10(^{18}) epi.</td>
<td>1×10(^{-4})</td>
<td>[82]</td>
</tr>
<tr>
<td>Ni</td>
<td>1000 °C, 2 min, Ar</td>
<td>2×10(^{20}) Al-impl.</td>
<td>7×10(^{-5})</td>
<td>[68]</td>
</tr>
<tr>
<td>Ni/Al</td>
<td>1000 °C, 30 min, vacuum</td>
<td>3-9×10(^{18}) epi.</td>
<td>9.5×10(^{-5})</td>
<td>[83]</td>
</tr>
<tr>
<td>Ni/Ti/Al</td>
<td>800 °C, 30 min, vacuum</td>
<td>3-9×10(^{19}) epi.</td>
<td>6.6×10(^{-5})</td>
<td>[83]</td>
</tr>
<tr>
<td>Pd</td>
<td>700 °C, 5-40 min, N(_2)</td>
<td>5×10(^{19}) epi.</td>
<td>5.5×10(^{-5})</td>
<td>[84]</td>
</tr>
<tr>
<td>Si/Al</td>
<td>700 °C, 5-40 min, N(_2)</td>
<td>5×10(^{19}) epi.</td>
<td>3.8×10(^{-5})</td>
<td>[78]</td>
</tr>
<tr>
<td>Si/Pt</td>
<td>1100 °C, 3 min, vacuum</td>
<td>l×10(^{19}) epi.</td>
<td>5.8×10(^{-4})</td>
<td>[78]</td>
</tr>
<tr>
<td>Ti</td>
<td>800 °C, 1 min, vacuum</td>
<td>1.3×10(^{19}) epi.</td>
<td>2-4×10(^{-5})</td>
<td>[75]</td>
</tr>
</tbody>
</table>

5.2. Ohmic contacts to 3C-SiC

Ohmic contact formation on 3C-SiC has not been as extensively investigated as in the case of 4H-SiC material. Tables 5.2.a and b report ohmic contacts to n- and p-type 3C-SiC achieved, using different metals and annealing conditions. In 1994, Dmitriev et al. [85] reported on the fabrication of ohmic contacts to 3C-SiC. To form ohmic contacts on n- and p-type 3C-SiC, Ni and Al/Ti metals were employed, respectively. Deposited Ni was annealed at 1000 °C for 30 seconds in forming gas while Al/Ti stack was sintered at 950 °C for 2 minutes in N\(_2\). The
measured specific contact resistance $\rho_C$ of the ohmic contacts to n-type 3C-SiC was found to be less than 1.7×10^{-5} and 2×10^{-5} $\Omega \text{cm}^2$ for contacts to p-type 3C-SiC. In 1995, Moki et al. [86] could demonstrate the possibility of achieving ohmic behavior on n-type 3C-SiC ($N_D = 3\times10^{20} \text{cm}^{-3}$) of as-deposited Al and Ti contacts. The contact resistivities of Al and Ti ohmic contacts to n-type 3C-SiC were measured using the circular TLM method. The surface doping concentration under the contact was increased by ion-implantation of nitrogen into SiC. The contact resistivity was observed to decrease with increasing surface doping concentration for both Al and Ti contacts. For 3C-SiC surface doping concentration of $3\times10^{20} \text{cm}^{-3}$ minimum contact resistivities of $1.4\times10^{-5}$ and $1.5\times10^{-5} \Omega \text{cm}^2$ were measured for Al and Ti, respectively, without any post-metallization anneal. However, considerable spreading in the contact resistivity was observed and attributed to the presence of extended crystal defects (stacking faults).

**Table 5.2.a: Reported ohmic contacts to n-type 3C-SiC material.**

<table>
<thead>
<tr>
<th>Metal</th>
<th>Annealing conditions</th>
<th>$N_D$ (at/cm$^3$)</th>
<th>$\rho_C$ ($\Omega \text{cm}^2$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>1000 °C, 30 sec, H$_2$</td>
<td>1-3×10$^{19}$ epi.</td>
<td>&lt;1.7×10$^{-5}$</td>
<td>[85]</td>
</tr>
<tr>
<td>Al</td>
<td>-</td>
<td>3×10$^{20}$ N-impl.</td>
<td>1.7×10$^{-5}$</td>
<td>[86]</td>
</tr>
<tr>
<td>Ti</td>
<td>-</td>
<td>3×10$^{20}$ N-impl.</td>
<td>2×10$^{-5}$</td>
<td>[86]</td>
</tr>
<tr>
<td>Ni</td>
<td>950 °C, 1 min, Ar</td>
<td>3×10$^{19}$ epi.</td>
<td>1.2×10$^{-5}$</td>
<td>[87]</td>
</tr>
<tr>
<td>Ni/Ti</td>
<td>1050 °C, 1 min, Ar</td>
<td>&gt;10$^{20}$ N-impl.</td>
<td>2×10$^{-5}$</td>
<td>[87]</td>
</tr>
<tr>
<td>Al</td>
<td>300 °C, 1 min, Ar</td>
<td>6×10$^{18}$ N-impl.</td>
<td>5×10$^{-7}$</td>
<td>[87]</td>
</tr>
<tr>
<td>Au/Ti</td>
<td>600 °C, 1 min, Ar</td>
<td>3×10$^{20}$ N-impl.</td>
<td>1.2×10$^{-5}$</td>
<td>[87]</td>
</tr>
</tbody>
</table>

**Table 5.2.b: Reported ohmic contacts to p-type 3C-SiC material.**

<table>
<thead>
<tr>
<th>Metal</th>
<th>Annealing conditions</th>
<th>$N_A$ (at/cm$^3$)</th>
<th>$\rho_C$ ($\Omega \text{cm}^2$)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al/Ti</td>
<td>950 °C, 2 min, N$_2$</td>
<td>1-3×10$^{19}$ epi.</td>
<td>2×10$^{-5}$</td>
<td>[85]</td>
</tr>
</tbody>
</table>

More recently, Bazin et al. [87] investigated the potential of annealed Ni, Ti, Al and Au contacts for ohmic contact formation on n-type 3C-SiC epilayers grown on (100) silicon substrates. Classical circular TLM structures were prepared to evaluate the specific contact resistance. Ni and Ni/Ti contacts were annealed between 950° C and 1050° C while Al and Au/Ti contacts were annealed between 300° C and 600° C. For each investigated contact, the best specific contact resistance values obtained is lower than 2×10$^{-5}$ $\Omega \text{cm}^2$, even consecutively to a low temperature annealing.
Chapter 5: Source-drain contacts

5.3. Problems with silicides for contacts bonding

Apart from the specific metal resistance, the good bonding ability of the ohmic contacts is one of the key parameters for direct integration to complete device system. This bonding should ensure the connection between the ohmic contact and the die package. As described earlier in this chapter, nickel silicide \((\text{Ni}_x\text{Si}_y)\) contacts are generally formed by annealing Ni films at temperatures around 950 °C using RTA technology. As a consequence of the silicidation, two main problems occur:

- At first the resulting nickel silicide surface demonstrates high roughness leading to practical problems of bonding while depositing extra metal systems on top of \(\text{Ni}_x\text{Si}_y\). In order to solve this problem, one can remove the untreated Ni from the silicide and deposit an extra layer of interdiffusion barrier metal such as Ti, TiN or TiW ensuring the adhesion of the bonding metal commonly made of Al or Au. On the other hand, the presence of such an interdiffusion barrier metal may prevent the diffusion of free carbon present of the silicide contacts to the cap metal layer.

- The use of RTA technology for silicidation processes may induce the formation of a nickel oxide layer on top of the nickel silicide, thus resulting in the drastic increase of the contact resistance while depositing interconnect metal on top of the nickel silicide contact. Apart from the increase of the contact resistance, the adhesion of the interconnect metal can be drastically reduced due to the presence of the oxide layer, therefore resulting in the occurrence of peeling-off of the interconnect metal. To solve this problem, the etching of the oxide layer by Ar aching using RIE technology can be envisaged.

5.4. Characterization technique

In order to characterize ohmic contacts quality and estimate their specific contact resistance \(\rho_C\), the four probe Transfer Length Method (TLM) is commonly used.

5.4.1. Transfer Length Method (TLM)

The TLM measurement of a metal-semiconductor specific contact resistance can be described by the Figure 5.4.1.a section a). In this configuration several different resistances have to be taken into account (see Figure 5.4.1.a section b)): the probe resistance \(R_P\), the probe-to-metal contact resistance \(R_{CP}\), the metal-to-semiconductor contact resistance \(R_{CS}\) and the semiconductor sheet resistance \(R_S\). The equivalent circuit for the measurement of metal-semiconductor contact resistance by using four-point TLM is shown in Figure 5.4.1.a section c).
Figure 5.4.1.a: Four-point measurement of metal-semiconductor specific contact resistance.

Figure 5.4.1.b: Transfer Length Method pattern for the four-point measurement of metal-semiconductor specific contact resistance. In this representation $L$ and $W$ correspond to the length and width of the metal contacts.

The advantage of using the four-point method is that it can eliminate the parasitic resistance introduced by the probes. If the metal-to-semiconductor contact resistance $R_{CS}$ is very small (comparable to the probe resistance $R_P$), one should use four-point instead of two-point for the measurement. This is important when the specific contact resistance is less than about $10^{-4} \Omega \text{cm}^2$. 
Chapter 5: Source-drain contacts

The total resistance $R_T$ can be calculated using the Equation 5.4.1.a:

$$R_T = 2R_{CS} + \left( \frac{R_S}{W} \right) D = \frac{V}{I},$$

(5.4.1.a)

where $W$ is the width of the contact, $D$ is the contacts spacing (see Figure 5.4.1.b), $V$ is the voltage reading from the voltmeter and $I$ is the current carried by the two current-carrying probes.

In order to estimate the values of $R_{CS}$, $R_S$, and $\rho_C$, one should repeat the measurement of $R_T$ using different contacts spacing distances $D$ (see Figure 5.4.1.b and c). Collected values of $R_T$ are then plotted as function of the contacts spacing $D$ (see Figure 5.4.1.c). From the plotting of the collected total resistance $R_T$ values measured at different contacts spacing, one can estimate the values of the metal-to-semiconductor contact resistance $R_{CS}$ and the transfer length $L_T$.

![Figure 5.4.1.c: Plot of the total resistance $R_T$ as a function of the distance between the metal contacts $D$. In this representation $L_T$ corresponds to transfer length.](image)

The specific contact resistance $\rho_C$ is deduced via the Equation 5.4.1.b:

$$\rho_C = R_{CS}WL_Ttgh\left(\frac{L}{L_T}\right)$$

(5.4.1.b)

In order to avoid the contribution of parasitic resistances and of the current propagating from around the metal contacts, contacts doped regions should be
isolated by the formation of mesas structures or local implantation profiles for epitaxial and implanted configurations, respectively (see Figure 5.4.1.b).

5.5. Results

5.5.1. Low temperature ohmic contacts formation process for n- and p-type 3C-SiC(001)

The present study reports on the fabrication and characterization of n- and p-type 3C-SiC(001) ohmic contacts based on annealed Ni contacts. Ni ohmic contacts were fabricated on 3C-SiC(001) free standing 3” wafers with a lightly doped ($5 \times 10^{15} \text{ cm}^{-3}$) n-type epitaxial region of 5 µm in thickness. A scheme of the cross-section of the n-type and p-type contacts regions is described in Figure 5.5.1.a. Contacts were formed to ion-implanted n- and p-type regions of $N_D = 5 \times 10^{19} \text{ cm}^{-3}$ and $N_A = 3 \times 10^{20} \text{ cm}^{-3}$, respectively.

![Schematic representation of the n-type and p-type contacts regions used for TLM measurements and the determination of the specific contact resistance $\rho_C$ of investigated Ni contacts on 3C-SiC(001).](image)

Positive-type photoresist was deposited on the cleaned 3C-SiC(001) material, and transfer length method (TLM) patterns were created using lift-off photolithography. Rectangular TLM structures were formed by ion beam sputtering of 100 nm of Ni and using lift-off photolithography process. TLM contact pads were 100 µm by 50 µm and contacts spacings were 5, 10, 15, 20, 25 µm. Subsequent metal post-deposition annealings were carried out at 500, 600, 700, 800, 850 and 900 °C for 1 min using rapid thermal annealing (RTA). In order to accurately control the annealing process temperature, a silicon container was used. After the annealing, contacts were electrically characterized by current-voltage (I-V) measurements carried out using a Keithley 237 High Voltage Source Measure Unit. The specific contacts resistance $\rho_C$ was extracted using TLM method described in the section 5.4.1. of this chapter.
Chapter 5: Source-drain contacts

The specific contact resistances of n- and p-type 3C-SiC(001) based ohmic contacts are plotted as a function of the annealing temperature in the Figure 5.5.1.b and c, respectively. As reference, the initial value of $\rho_C$ of as-deposited Ni contacts on both materials was added.

Figure 5.5.1.b: Specific contact resistance of Ni based ohmic contacts to n-type 3C-SiC(001) plotted as a function of the annealing temperature.

Figure 5.5.1.c: Specific contact resistance of Ni based ohmic contacts to p-type 3C-SiC(001) plotted as a function of the annealing temperature.
As described on Figure 5.5.1.b, the contact resistance of n-type 3C-SiC(001) based ohmic contacts demonstrates at first an increase after annealing at 500 °C, then reduces, reaching a minimum of $2 \times 10^{-7} \text{Ωcm}^2$ at 700 °C and finally increases a second time up to $2 \times 10^{-5} \text{Ωcm}^2$ at 900 °C. At 500 °C the formation of a thin nickel silicide layer is achieved but no significant reaction between nickel and the SiC material can be generated. The workfunction of nickel silicide being higher than the one of nickel, the Ni$_x$Si$_y$/3C-SiC(n-type) Schottky barrier is therefore higher than the one of Ni/SiC. The augmentation of $q\Phi_B$ naturally leads to the increase of the specific contact resistance. Contacts annealed at 600 and 700 °C demonstrate significant reaction between SiC material and nickel contacts, which result in the drastic decrease of $\rho_C$. Contacts annealed at temperatures superior to 700 °C describe an increase of the specific contact resistance which might be related to the degradation of the ohmic contacts.

The evolution of the specific contact resistance of p-type 3C-SiC(001) based Ni contacts demonstrates different behavior. As-deposited Ni contacts describe maximum value of $\rho_C$ in the range of $2 \times 10^{-2} \text{Ωcm}^2$. After annealing at 500°C, $\rho_C$ slightly reduces exhibiting a value of $3 \times 10^{-2} \text{Ωcm}^2$. This slight reduction of $\rho_C$ might be again related to the formation of nickel silicide: the workfunction of the nickel silicide being superior than the one of Ni, the Ni$_x$Si$_y$/3C-SiC(p-type) Schottky barrier is thus reduced. Metals annealed at temperatures of 700°C and above exhibit specific contact resistances in the range of $8 \times 10^{-4} \text{Ωcm}^2$ that demonstrate the reaction between the Ni and the SiC material and the formation of the ohmic contacts.

Figure 5.5.1.d: Specific contact resistance of Ni based ohmic contacts to p-type 3C-SiC(001) plotted as a function of the annealing temperature.
In order to assess the ohmicity of the nickel based ohmic contacts on p-type 3C-SiC(001), typical measured I-V curves have been plotted in the Figure 5.5.1.d. Contacts spacing $D$ of presented I-V curves is 10 µm. I-V curves demonstrate linear behavior which proves the ohmic character of the contacts.
Chapter 6: 3C- & 4H-SiC MOSFETs

The fabrication of 3C- and 4H-SiC DMOSFETS has been performed based on technology modules presented in previous chapters of this report. This chapter aims to describe the integration of those process modules into the fabrication of practical devices and to evaluate their electrical characteristics.

6.1. Design and process description

6.1.1. Design

The design of the fabricated 3C- and 4H-SiC MOSFETs was based on the computer-aided design (CAD) work made by an external project partner.

Figure 6.1.1.a: CAD pictures of 7000 cells power 3C- and 4H-SiC DMOSFETs illustrating principal aspects of these devices.
Device grade 3C-SiC(001) and 4H-SiC(0001) substrates with 13 and 12 µm, respectively thick epitaxial layers lightly doped with nitrogen ($7 \times 10^{15} \text{ cm}^{-3}$) were prepared by HOYA Corporation and ACREO AB. Target devices were 3C- and 4H-SiC DMOSFETs with 600 and 1200 V blocking voltage and 10 A drain current handling capabilities. Figure 6.1.1.a describes the design of the devices. The gate and JFET lengths were based on 1.0 and 3.0 µm designs, respectively. The unit cell size pitch was defined to 13 µm. 10 A MOSFET structure consists of 7000 cells with an active device area of 1.1 mm$^2$. MOSFETs were fabricated using g-line steppers for all lithography processes and dry etching to define the contacts and cell interconnections. Patterns of 1.0 µm line width were achieved.

6.1.2. Process description

In order to describe the fabrication process of 3C-SiC(001) and 4H-SiC(0001) MOSFETs, the process flow of those devices has been schematically illustrated in the appendix A.2. The MOSFETs fabrication process consists of 15 major steps:

1. Plasma-enhanced chemical vapor deposition (PECVD) of 100 nm oxide on top of the SiC wafer.
2. Photolithography and room temperature ion implantation of the P-well region.
3. Photolithography and room-temperature ion implantation of the N+ region.
4. Photolithography and room-temperature ion implantation of the P+ region.
5. RCA cleaning of the wafer and activation annealing of the dopants at 1600 and 1650 °C for 3C- and 4H-SiC, respectively.
6. Gate oxide fabrication: deposition of 55 nm of PECVD oxide and post-oxidation annealing, performed in wet oxygen (950 °C, 3h) for 3C- and N$_2$O (1100 °C,3h) for 4H-SiC MOSFETs, respectively.
7. Deposition of the gate contact based on Poly-Si/TiW (300/100 nm) for 3C- and Poly-Si (500 nm) for 4H-SiC MOSFETs, respectively. Subsequent post-deposition activation annealing of the poly-Si (800 °C, Ar, 1min, RTA) is performed in case of 3C-SiC MOSFETs.
8. Dry etching of the gate contact structure.
9. Deposition of low temperature oxide LTO (1 µm) for the top part passivation layer.
10. Dry etching of the passivation layer and gate oxide: opening the source contact.
11. Deposition of the source and drain ohmic contacts composed of Ti/TiN for 3C-SiC MOSFETs and Ni for 4H-SiC MOSFETs, respectively.
13. Only in case of 4H-SiC MOSFETs: silicidation of the source and drain contacts (950 °C, Ar, 1min, RTA).
14. Deposition of the source metal pad composed of Ti/Al.
15. Dry etching of the source metal pad.
6.2. Characterization techniques

The electrical properties of MOSFET devices are commonly judged by analyzing transfer and output characteristics in on-state and blocking characteristics in off-state.

6.2.1. Transfer characteristics

The transfer characteristic of a MOSFET corresponds to the plot of the drain-source current $I_{DS}$ (linear or logarithmic scaled) as a function of the gate-source voltage $V_{GS}$ for a fixed drain-source voltage $V_{DS}$. An example of such a characteristic is shown in Figure 6.2.1.a.

![Figure 6.2.1.a: Typical transfer characteristics (linear a) and logarithmic b) scaled gate-source current $I_{DS}$ as a function of the gate-source voltage $V_{GS}$ for a fixed drain-source voltage $V_{DS}$) of a normally-off DMOSFET.](image-url)
From the output characteristic, one can estimate three device parameters: the threshold voltage $V_{TH}$, the subthreshold slope and the leakage current $I_{LK}$. The threshold voltage corresponds to the gate-source voltage $V_{GS}$ for which the channel of the MOSFET is switched on (conducting) and defines the normally-off ($V_{TH} < 0 \text{ V}$) or normally-on ($V_{TH} > 0 \text{ V}$) character of the device. The steepness of the subthreshold slope characterized the transition speed between the off state (low output current) and on state (high output current). The leakage current $I_{LK}$ of the device is defined by the drain-source current $I_{DS}$ while no voltage is applied to the gate-source ($V_{GS} = 0 \text{ V}$).

From transfer characteristic measurements, one can deduce the value of the transconductance $G_M$ which can be estimated according to the Equation 6.2.1.a:

$$G_M = \frac{\partial I_{DS}}{\partial V_{GS}}$$

(6.2.1.a)

Figure 6.2.1.b presents typical plot of the transconductance $G_M$ as a function of the gate-source voltage $V_{GS}$. $G_M$ typically demonstrates an increase in the subthreshold region, reaches maximum level when the device is turning on ($V_{TH}$), and finally decreases in the saturation regime of the device.

![Typical transconductance characteristics](image)

Figure 6.2.1.b: Typical transconductance characteristics ($G_M$ as a function of the gate-source voltage $V_{GS}$ for a fixed drain-source voltage $V_{DS}$) of a normally-off DMOSFET.
6.2.2. Output characteristics

The output characteristic of a MOSFET is the plot of the drain-source current $I_{DS}$ as a function of the drain-source voltage $V_{DS}$ for different constant gate-source voltages $V_{GS}$. An example of such a plot is shown in Figure 6.2.2.a.

![Figure 6.2.2.a: Typical output characteristics (gate-source current $I_{DS}$ as a function of the drain-source voltage $V_{DS}$ for a fixed gate-source voltage $V_{GS}$) of a DMOSFET.]

Three different regimes of the MOSFET can be distinguished [23]:

- The linear regime: the drain-source voltage $V_{DS}$ is rather low and the variation of the channel conductance is negligible. The drain-source current $I_{DS}$ proportionally increases with $V_{DS}$.
- The quadratic regime: when the drain-source voltage $V_{DS}$ increases, the variation of the bias voltage of the MOS capacitor along the channel becomes significant, the electron density and consequently the channel conductivity decrease. As a result, $I_{DS}$ demonstrates an under-linear variation with $V_{DS}$ and starts saturating.
- The saturation regime: when the drain-source voltage $V_{DS}$ increases over the saturation voltage $V_{DS\, SAT}$, the region close to the drain is not anymore in inversion mode. The pinching point, where the potential stays constant, moves towards the source.

From the output characteristics, one can estimate the value of the drain conductance $G_D$ which can be described as in the Equation 6.2.2.a:

$$G_D = \frac{\partial I_{DS}}{\partial V_{DS}}$$

(6.2.2.a)
Figure 6.2.2.b presents typical plot of the drain conductance $G_D$ as a function of the drain-source voltage $V_{DS}$. Being equal to the slope of the transfer characteristics, $G_D$ naturally describes a first plateau before decreasing and reaching a minimum corresponding to the linear, quadratic and saturation regimes of the device, respectively.

Figure 6.2.2.b: Typical drain conductance characteristics ($G_D$ as a function of the drain-source voltage $V_{DS}$ for a fixed gate-source voltage $V_{GS}$) of a normally-off MOSFET.

6.2.3. Channel mobility estimation

From the output and transfer characteristics, the electron mobility in the channel of the MOSFET can be estimated. Two different definitions of the channel mobility exist and are commonly used: the field effect mobility $\mu_{FE}$ and the effective mobility $\mu_{EFF}$.

6.2.3.1. Field effect mobility

The field effect mobility $\mu_{FE}$ is evaluated via the consideration of the device design (width of the channel $W_{CH}$, length of the channel $L_{CH}$ and oxide capacitance $C_{OX}$) and the measurement of the transconductance $G_M$. The Equation 6.2.3.1.a defines $\mu_{FE}$.

$$\mu_{FE} = \frac{L_{CH}G_M}{V_{DS}W_{CH}C_{OX}}$$  (6.2.3.1.a)
6.2.3.2. Effective mobility

The effective mobility \( \mu_{\text{EFF}} \) is evaluated via the consideration of the device design (width of the channel \( W_{\text{CH}} \), length of the channel \( L_{\text{CH}} \) and oxide capacitance \( C_{\text{OX}} \)) and the measurement of the drain conductance \( G_D \). The Equation 6.2.3.2.a defines \( \mu_{\text{EFF}} \).

\[
\mu_{\text{EFF}} = \frac{L_{\text{CH}} G_D}{W_{\text{CH}} C_{\text{OX}} (V_{\text{GS}} - V_{\text{TH}})}
\]

(6.2.3.2.a)

6.2.4. Blocking characteristics

The blocking characteristic refers to the plot of the drain-source current \( I_{DS} \) as a function of the drain-source voltage \( V_{DS} \) for a fixed gate-source voltage \( V_{GS} \) which should be inferior to the threshold voltage \( V_{\text{TH}} \) of the device (see Figure 6.2.4.a). In the forward blocking mode of the DMOSFET, the voltage is supported by a depletion region formed on both sides of the p-well/n-drift region. The maximum blocking voltage is determined by the electric field at this junction becoming equal to the critical electric field for breakdown if the parasitic n+/p/n bipolar transistor is completely suppressed. This suppression is accomplished by short-circuiting the n+ source and p-well regions. However, a large leakage current can occur when the depletion region in the p-well region reaches the n+ zone.

Figure 6.2.4.a: Simulated blocking characteristics (drain-source current \( I_{DS} \) as a function of the drain-source voltage \( V_{DS} \) for a fixed gate-source voltage \( V_{GS} < V_{\text{TH}} \)) of a 1200V DMOSFET.
Chapter 6: 3C- & 4H-SiC MOSFETs

The doping concentration and thickness of the p-well region must be designed to prevent the reach-through phenomenon from limiting the breakdown voltage. This problem becomes critical in SiC based devices due to the high electric field at the blocking junction [5].

6.3. Results

6.3.1. High Channel Mobility 3C-SiC(001) MOSFETs

Paper G reports on the fabrication and characterization of 3C-SiC(001) MOSFETs based on post-oxidized PECVD gate oxide. MOSFETs with 140 cm²/Vs of channel mobility were fabricated. High performance fabrication processes were adopted, including room temperature implantation with photoresist mask, (poly-silicon)-metal gate contacts, aluminium interconnects with titanium and titanium nitride and a specially developed activation anneal at 1600 °C in Ar to get a smooth 3C-SiC(001) surface and hence the expected high channel mobility. PECVD deposited oxide with post-oxidation annealing (POA) was utilized to reduce unwanted oxide charges and hence to get a better reliability compared to thermally grown gate oxides.

Figure 6.3.1.a presents the cross-section TEM image of the post-oxidized PECVD gate oxide under polysilicon gate electrode (a) and the lattice image of the SiO₂/SiC interface (b).

Figure 6.3.1.a: Cross-section TEM image of the post-oxidized PECVD gate oxide under gate polysilicon gate electrode (a) and lattice image of the SiO₂/SiC interface (b).

The roughness of the SiO₂/SiC interface has been estimated to less than 3 nm. Reliability investigations demonstrated that post-oxidized PECVD oxide has a breakdown electric field of over 9 MV/cm.

Figure 6.3.1.b describes typical output characteristics of a fabricated 3C-SiC(001) MOSFET with 600 V blocking voltage and 10 A drain current assembled in TO-220 packaging. The present MOSFET exhibits drain-source current $I_{DS}$ of 6.4 A.
and 9.7 A for drain-source voltages $V_{DS}$ of 5 and 10 V, respectively. Several fabricated MOSFETs achieved specific on-resistance of less than 5 mΩcm$^2$ at $V_{DS}$ 1 V. The evaluation of test patterns included in the layout close to the MOSFETs gave a sheet resistance of the TiW/Poly-Si gate of 5.2 Ω/sqr and a contact resistance to the n+ and p+ regions of $10^{-4}$ and $10^{-2}$ Ωcm$^2$, respectively. These values are considered acceptable for practical use of 3C-SiC MOSFETs. For a 64 nm thick gate oxide and 3 µm channel length, the maximum channel mobility is 140 cm$^2$/Vs, which is 2-3 times higher than for similar 4H-SiC MOSFETs.

![Figure 6.3.1.b: Output characteristics of 3C-SiC(00 1) MOSFET with 600 V blocking voltage and 10 A drain current assembled in TO-220 (I: 1A/div, V: 1V/div).](image)

**6.3.2. 4H-SiC(0001) MOSFETs based on post-ox. PECVD gate oxide**

This section is devoted to the fabrication and characterization of 4H-SiC(0001) MOSFETs based on post-oxidized PECVD gate oxide. Room temperature implantation with photoresist mask, poly-Silicon gate contact, LTO passivation layer, nickel silicide based ohmic contacts and aluminium interconnects with titanium were implemented for the fabrication process of 4H-SiC(0001) MOSFETs. PECVD oxide post-oxidized in N$_2$O ambient at 1150 °C for 3 hours was used for the gate oxide formation in order to minimize oxide/interface/near-interface charges and thus obtain high channel mobility and oxide reliability. MOSFETs characterization was carried out on wafer-scale (about 200 components per wafer) at room temperature, 100, 200 and 300 °C using Keithley 237 High Voltage Source Measure Units. In parallel, n-type MOS structures with an area of $200 \times 100$ µm$^2$ were characterized by capacitance-voltage (C-V) and conductance-voltage (G-V) measurements (using HP4284A LCR meter at the frequency range
of 10 kHz) to judge of the quality and reliability of the gate oxide. TLM structures processed on n+ and p+ contacts regions have been used to evaluate the specific contact resistance of source and drain contacts.

Typical C-G-V characteristics taken on n-type 4H-SiC(0001) MOS structures at room temperature, 100, 200 and 300 °C are presented in Figure 6.3.2.a sections a) and b). The oxide thickness $d_{ox}$ calculated from the measured oxide capacitance $C_{ox}$ was estimated to 57 nm. MOS capacitors demonstrated positive flatband voltages of around 0.36, 0.31, 0.29 and 0.02 V for room temperature, 100, 200 and 300 °C measurements, respectively.

Figure 6.3.2.a: Typical C-V a) and G-V b) characteristics taken on n-type 4H-SiC(0001) MOS structures at room temperature, 100, 200 and 300 °C and at a probe frequency $f = 10$ kHz.
Practically no hysteresis between both sweeps of capacitance (from deep depletion to accumulation and vice versa) are observed up to 200 °C, highlighting the reduced concentrations of slow oxide charges ($D_{NIT^*}$). While increasing the temperature up to 300 °C, drastic widening of the C-V curves hysteresis appeared thus leading to the augmentation of $D_{NIT^*}$. Conductance-voltage measurements presented in Figure 6.3.2.a section b) exhibit low intensity and sharp peak, therefore assessing of low $D_{IT}$ and surface potential fluctuations, respectively. The evaluation of $D_{IT}$ at RT using the conductance method (see appendix A.1) revealed an interface traps concentration of $1.1 \times 10^{11}$ eV$^{-1}$ cm$^{-2}$ at 0.35 eV of the conduction band edge.

Typical output characteristics of 7000 cells power 4H-SiC(0001) DMOSFET taken at room temperature (RT) are shown in Figure 6.3.2.b. Drain-source current $I_{DS}$ of 0.4 A was achieved for drain-source voltage $V_{DS}$ of 5 V and gate-source voltage $V_{GS}$ equal to 25 V. Minimal linear regime could be detected on vertical MOSFET devices thus leading to the unfeasibility of the specific on-resistance and effective mobility evaluations. The present quadratic increase of the drain-source current $I_{DS}$ might be related to intense drift region and contacts resistances.

![Figure 6.3.2.b](image.png)

Figure 6.3.2.b: Typical output characteristics of 7000 cells power 4H-SiC(0001) DMOSFET taken at room temperature.

In order to study the evolution of 7000 cells DMOSFET's output characteristics with increasing the temperature, output measurements were done at 100, 200 and 300 °C. Collected results have been plotted in Figure 6.3.2.c. The increase of the temperature resulted in the significant augmentation of the source-drain current $I_{DS}$. In that way, $I_{DS}$ increases by a factor of 2 at temperatures of 200 and 300 °C.
reaching values exceeding 1 A (measurement limit of SMU) at $V_{DS}$ equal to 4.2 V. Complying with the output characteristics results, typical transfer characteristics measured at RT, 100, 200 and 300 °C (see Figure 6.3.2.d) also highlight the drastic augmentation of $I_{DS}$ and the subthreshold slope when increasing the temperature.

Figure 6.3.2.c: Output characteristics of 7000 cells power 4H-SiC(0001) DMOSFET taken at RT, 100, 200 and 300 °C (gate-source voltage $V_{GS}$ fixed at 25 V).

Figure 6.3.2.d: Transfer characteristics of 7000 cells power 4H-SiC(0001) DMOSFET taken at RT, 100, 200 and 300 °C (drain-source voltage $V_{DS}$ fixed at 0.2 V).
Subthreshold slope values were evaluated to 4.4, 5.4, 21.6 and $25.6 \times 10^{-4}$ A/V at RT, 100, 200 and 300 °C, respectively. On the other hand, transfer characteristics assess the normally-on character of the power DMOSFETs and exhibit drain-source leakage current inferior than $10^{-11}$ A. Threshold voltages of 7.9, 7.4, 7.2 and 7.1 V were determined at RT, 100, 200 and 300 °C, respectively.

![Figure 6.3.2.e: Field effect mobility of 7000 cells power 4H-SiC(0001) DMOSFET taken at room temperature, 100, 200 and 300 °C (drain-source voltage $V_{DS}$ fixed at 0.2 V).](image)

From transfer measurements, the field effect mobility $\mu_{FE}$ of the channel has been extracted and plotted as a function of the gate-source voltage $V_{GS}$ in Figure 6.3.2.e. At RT, 7000 cells DMOSFET demonstrates $\mu_{FE}$ equal to 0.18 cm$^2$/Vs. While increasing the temperature to 300 °C, $\mu_{FE}$ raises to 1.08 cm$^2$/Vs that corresponds to an increase by a factor of 5.7. Apart from this augmentation at high temperature, the channel mobility remains rather low. One can suggest several reasons explaining the minimal values of $\mu_{FE}$. At first, one can suppose all 7000 cells are not effectively working thus leading to the reduction of effective output drain-voltage current $I_{DS}$ and therefore measured $\mu_{FE}$. Then, considering output characteristics results one can point out the presence of an intense resistance which might be related to the lowly doped thick drift region and drain/source contacts resistances. The evaluation of the specific contact resistance on TLM structures designed parallel to MOSFET devices resulted in $\rho_C$ of $9 \times 10^{-4}$ and $2 \times 10^{-2}$ Ωcm$^2$ to the n+ and p+ regions, respectively. Those values are rather high and comply with achieved electrical characteristics of the MOSFETs.
In order to remove the contribution of the drift region resistance and not working MOSFET cells during the evaluation of $\mu_{FE}$, the field effect mobility of single cell planar devices ($W_{CH} = 10 \ \mu m$ and $L_{CH} = 2 \ \mu m$) has been carried out and plotted in Figure 6.3.2.f. As in case of vertical structures a clear increase of $\mu_{FE}$ is demonstrated while raising the temperature of the measurements. At RT, $\mu_{FE}$ was estimated to 20 cm$^2$/Vs that corresponds to 100 times $\mu_{FE}$ of 7000 cells DMOSFETs. The maximum of the field effect mobility was estimated to 55 cm$^2$/Vs and achieved at the temperature of 300 °C. Hence, $\mu_{FE}$ increases by a factor of 2.7 while measuring at RT and 300 °C.

![Figure 6.3.2.f: Field effect mobility of single cell 4H-SiC(0001) LMOSFET taken at room temperature, 100, 200 and 300 °C (drain-source voltage $V_{DS}$ fixed at 0.2V).](image)

In order to understand the increase of $I_{DS}$ and consequently $\mu_{FE}$ when raising the temperature, one can speculate on the impact of the temperature on the source/drain ohmic contacts resistance. As described in chapter 5, in case of n+ 4H-SiC(0001) ohmic structure, the dominant current transport mechanism is the direct tunneling through the Schottky barrier $q\Phi_B$. The raising of the temperature leads to the increase of the energy of the electrons and holes at the metal/semiconductor interface thus enhancing the flow of electrons/holes traveling between the semiconductor and the metal. In that way, the ohmicity of the structure is increased and the contact resistance is therefore decreased.
Conclusions and future outlook

The present thesis explores several technology modules related to the fabrication of 3C- and 4H-SiC power MOSFETs. The gate stack formation, drain/source ohmic contacts fabrication and passivation layer elaboration were discussed and generated results were presented. Then, the last chapter of the report introduces the implementation of the technology modules to the complete devices process and describes the achieved results.

Investigations on the gate oxide formation revealed the superiority of an advanced oxidation process combining oxide deposition by PECVD and short low-temperature post-oxidation steps in wet oxygen and N\textsubscript{2}O for 3C-SiC(001) and 4H-SiC(0001), respectively. High electrical properties and reliability of fabricated oxides could be demonstrated. Since significant improvements of the oxide quality while using phosphorous-rich atmosphere during the oxidation process of 4H-SiC(0001) has been recently demonstrated [16], one might found interesting to evaluate the potential of post-oxidized PECVD oxides in phosphorous-rich atmosphere and compare them with post-oxidized PECVD samples in N\textsubscript{2}O ambient.

The development activities on the gate contact highlighted the benefits of using poly-Si. Preservation of the quality and improvements of the reliability of the gate oxide could be described. On the other hand, the use of RTA technology for the poly-Si activation process could achieve minimization of the thermal budget and superior conservation of the gate oxide quality.

Studies on the passivation layer formation demonstrated the possibility of combining thin thermally grown oxide and LTO deposited oxide for ensuring efficient passivation of the devices and reducing the surface recombination current. In some future studies, one might be interested in considering the possibility of using PECVD phosphorous-doped oxide as top passivation layer part. This material, well known for its superior elasticity, could describe reduced stress (minimal cracks) around the sharp edges of the gate contact structures and drastic reduction of the total thermal budget of MOSFET devices process.
Conclusions and future outlook

Research on the elaboration of ohmic contacts to n+ and p+ doped 3C-SiC material highlighted the possibility of achieving ohmic contacts using single metal layer of nickel and low temperature annealing process. Other metals such as Ti, TiW and W might be interesting to be tested and compared with results achieved with Ni. Finally, the implementation of developed technology modules demonstrated the possibility of fabricating normally-off power 3C- and 4H-SiC MOSFETs. Power 3C-SiC devices composed of 7000 cells could demonstrate 600 V blocking voltage and 10 A drain current handling capabilities. High field effect mobility of 140 cm$^2$/Vs and minimal specific on-resistance of less than 5 mΩcm$^2$ at $V_{DS}$ 1 V were shown. In case of 4H-SiC, fabricated power MOSFETs could demonstrate high temperature operating ability. 7000 cells devices exhibited drain-source current of more than 1 A at 300 °C at $V_{GS}$ 25 V and $V_{DS}$ 5V.
Appendix

A.1. Conductance method

A.1.1. Interface traps density calculation procedure

The contribution of interface traps distributed over the semiconductor band gap to the admittance $Y_{IT}$ is given by [88]:

$$Y_{IT} = \frac{q^2 D_{IT}}{2} \omega \ln(1 + \omega^2 \tau^2) + i\omega \frac{q^2 D_{IT}}{2} \arctan(\omega \tau)$$  \hspace{1cm} (A.1.1.a)

As described in the Equation A.1.1.b, the admittance related to interface traps $Y_{IT}$ is composed of a real part, the conductance $G_{IT}$ and an imaginary part, the capacitance $C_{IT}$.

$$G_{IT} = \frac{q^2 D_{IT}}{2} \omega \ln(1 + \omega^2 \tau^2)$$  \hspace{1cm} (A.1.1.b)

$$C_{IT} = \frac{q^2 D_{IT}}{2} \frac{\arctan(\omega \tau)}{\omega \tau}$$  \hspace{1cm} (A.1.1.c)

Because of the inhomogeneous distribution of the semiconductor and oxide traps, the roughness and imperfections of the semiconductor/oxide interface, surface potential fluctuations have to be taken into account in the case of real MOS capacitor. Nicollian et al. [39] associated the surface potential fluctuations to a statistical Gaussian fluctuation describing a standard deviation $\sigma_s$. The convolution of the admittance with this Gaussian distribution transforms leads to:
where:

\[
\tau(\varphi_S) = \frac{\exp(-\beta \varphi_S)}{\sigma_N V_{T,N} N_D}
\]  

(A.1.1.f)

In the three Equations A.1.1.d, e and f, \(\tau\) corresponds to the time constant, \(\omega\) the radial frequency of the measurement, \(\sigma_N\) the capture cross section of the traps, \(v_{T,N}\) the thermal velocity of the traps, \(\varphi_S\) the applied surface potential and \(\beta = kT/q\).

In order to link the measured admittance \(G_M\) to the admittance related to interface traps \(G_{IT}\), a model of the admittance measurement has to be described.

Figure A.1.1.a: Equivalent circuit of a MOS device. The capacitance of the dielectric \(C_{OX}\) is connected in series with the semiconductor and \(R_S\) a). The semiconductor consists of a parallel circuit if the interface traps capacitance \(C_{IT}\), the space charge region capacitance \(C_{SC}\) and the interface traps conductance \(G_{IT}\). Simplified circuit considering the transformations of the Equation A.1.1.g b). Scheme of the measured capacitance \(C_M\) and admittance \(G_M\) c).

The Figure A.1.1.a exhibits the equivalent circuit of a MOS device and the series connection between the oxide and semiconductor capacitances (see Figure A.1.1.a
section a)). Considering separately the capacitance and conductance (see Figure A.1.1.a section b)) one obtains:

\[ C_P = C_{SC} + C_{IT} \]
\[ G_P = G_{IT} \]  
(A.1.1.g)

The Figure A.1.1.a section c) presents the equivalent parallel circuit of the measured admittance \( Y_M \) providing the imaginary part \( C_M \) and the real part \( G_M \):

\[ C_M = \frac{\omega^2 C_P}{|Y_P|} + \frac{1}{C_{OX}} \]
\[ G_M = \frac{\omega^2 \left( \frac{G_P}{|Y_P|} + R_{SER} \right)^2 + \left( \frac{\omega^2 C_P}{|Y_P|} + \frac{1}{C_{OX}} \right)^2}{\omega^2 \left( \frac{G_P}{|Y_P|} + R_{SER} \right)^2 + \left( \frac{\omega^2 C_P}{|Y_P|} + \frac{1}{C_{OX}} \right)^2} \]

where \(|Y_P| = G_P^2 + \omega^2 C_P^2\)  
(A.1.1.h)

As described in Figure A.1.1.a and Equations A.1.1.h, five main factors contribute to the measured admittance \( G_M \):

- the interface traps capacitance \( C_{IT} \) and admittance \( G_{IT} \)
- the oxide capacitance \( C_{OX} \)
- the surface potential \( \varphi_S \)
- the space charge region capacitance \( C_{SC} \)
- the bias-dependent resistance \( R_{SER} \) which describes the deformation effects of the substrate, ohmic back-side contact, cables etc.

The estimation of the series resistance \( R_{SER} \) and the capacitance of the oxide \( C_{OX} \) are obtained using the Equations A.1.1.i and j described below:

\[ R_{SER} = \frac{G_{M,ACC}}{G_{M,ACC}^2 + \omega^2 C_{M,ACC}^2} \]
(A.1.1.i)

\[ C_{OX} = \frac{G_{M,ACC}^2 + \omega^2 C_{M,ACC}^2}{\omega^2 C_{M,ACC}} \]
(A.1.1.j)

where \( G_{M,ACC} \) and \( C_{M,ACC} \) correspond to the measured capacitance and conductance in accumulation mode, respectively.
The value of the surface potential $\phi_S$ can be calculated from the expression of the applied gate voltage $V_G$ described below in the Equation A.1.1.k:

$$V_G = \frac{\varepsilon_{SC}\sqrt{2}}{\beta L_D C_{OX}} \text{sign}(\phi_S) \left( \sqrt{e^{\beta \phi_S} - \beta \phi_S - 1} \right) + \phi_S + V_{FB}$$

(A.1.1.k)

Knowing $V_G$, $C_{OX}$, $\beta$, $\varepsilon_{SC}$, $V_{FB}$ one can deduced the value of $\phi_S$ by calculating when the function $f$ (see Equation A.1.1.i) is equal to 0:

$$f = V_G - \frac{\varepsilon_{SC}\sqrt{2}}{\beta L_D C_{OX}} \text{sign}(\phi_S) \left( \sqrt{e^{\beta \phi_S} - \beta \phi_S - 1} \right) + \phi_S + V_{FB}$$

(A.1.1.i)

### A.1.2. Traps energy position procedure

The $G_{IT}/\omega$ curve describes an asymmetric peak shape. The peak of the curve is reached at $\omega \tau = 1.98$. The conductance peak maximum is attained when the Fermi level $E_F$ gets close to the interface traps energy position $E_{IT}$. At that point, interface traps describing time constants in the range of the probe frequency resonate (get charged/discharged).

The energy position of the interface traps can be evaluated from the Equation A.1.2.a described below:

$$E_{C\_SURFACE} - E_{IT} = E_{C\_BULK} - E_F - q\phi_S\_PEAK\_MAX$$

(A.1.2.a)

A schematic representation of the interface traps energy position is proposed by the Figure A.1.2.a:

![Figure A.1.2.a: Determination of the energy position of interface traps close to the Fermi level.](image-url)
A.2. 3C- and 4H-SiC MOSFETs fabrication process

Table A.2.a: Schematic diagrams of 3C- and 4H-SiC MOSFETs process flow.

1. Plasma-enhanced chemical vapor deposition (PECVD) of 100 nm oxide.

<table>
<thead>
<tr>
<th>Process</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Plasma-enhanced chemical vapor deposition (PECVD) of 100 nm oxide.</td>
<td><img src="image1.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

2. Photolithography and room-temperature ion implantation of the P-well region.

<table>
<thead>
<tr>
<th>Process</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. Photolithography and room-temperature ion implantation of the P-well region.</td>
<td><img src="image2.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

3. Photolithography and room-temperature ion implantation of the N+ region.

<table>
<thead>
<tr>
<th>Process</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>3. Photolithography and room-temperature ion implantation of the N+ region.</td>
<td><img src="image3.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

4. Photolithography and room-temperature ion implantation of the P+ region.

<table>
<thead>
<tr>
<th>Process</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>4. Photolithography and room-temperature ion implantation of the P+ region.</td>
<td><img src="image4.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

5. RCA cleaning of the wafer and activation annealing of the dopant at 1600 and 1650 °C for 3C- and 4H-SiC MOSFETs, respectively.

<table>
<thead>
<tr>
<th>Process</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>5. RCA cleaning of the wafer and activation annealing of the dopant at 1600 and 1650 °C for 3C- and 4H-SiC MOSFETs, respectively.</td>
<td><img src="image5.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>
Appendix

6. Gate oxide fabrication: deposition of 55 nm of PECVD oxide and post-oxidation annealing is performed in wet oxygen (950 °C, 3h) for 3C- and N₂O (1100 °C, 3h) for 4H-SiC MOSFETs, respectively.

7. Deposition of the gate contact based on poly-Si/TiW (300/100 nm) for 3C- and poly-Si (500 nm) for 4H-SiC MOSFETs, respectively. Subsequent post-deposition activation annealing of the poly-Si (800 °C, Ar, 1 min, RTA) is performed in case of 3C-SiC MOSFETs.

8. Dry etching of the gate contact.

9. Deposition of LPCVD low temperature oxide LTO (1 µm) for the top part passivation layer.

10. Dry etching of the passivation layer and gate oxide: opening the source contact.
11. Deposition of the source and drain ohmic contacts composed of Ti/TiN for 3C-SiC MOSFETs and Ni for 4H-SiC MOSFETs


13. Only in case of 4H-SiC MOSFETs: silicidation of the source and drain contacts (950 °C, Ar, 1min, RTA).

14. Deposition of the source metal pad composed of Ti/Al for 3C-SiC a) with as-deposited ohmic contacts and 4H-SiC MOSFETs b) with annealed ohmic contacts.
Appendix

15. Dry etching of the source metal pad for 3C-SiC a) with as-deposited ohmic contacts and 4H-SiC MOSFETs b) with silicided nickel ohmic contacts.
References


References


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