Design of an Analog Front-end for Ambulatory Biopotential Measurement Systems

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摘要

在医疗诊断中,一个比较重要和关键的部分就是生物电势信号的监护.通常情况下,病人被连接到非常巨大和由交流电驱动的电子设备.这不仅限制了病人的自由移动而且给病人带来了不舒适的感觉.同时,在这样的情况下,监护通常不能维持非常长的时间,这也影响到了对病情的诊断效果.因此,非常有必要设计实现一种可移动式生物电势检测系统,这种系统必须是低功耗的,而且尺寸非常小.另外,系统最好能够具有可配置性,可适合应用于不同的生物信号.当然,最终目的是希望能够实现一个尺寸小到不可见,而且使用非常舒适的系统.此类系统的实现不仅可以提高人们的生活质量,而且大大降低了医疗服务的成本.

在本篇论文中,我们实现了一个可应用于移动式生物电势测量系统的模拟前端电路.系统的带宽和增益都可以在一个连续的范围内调节.模拟前端电路可以对不同的生物电势信号进行放大和整形.为了优化系统的功耗和电路结构,模拟前端仅仅采用了两级放大的结构.除此之外,对于关键晶体管的优化和设计使我们能够避免使用传统的斩波电路.模拟前端电路由于是纯模拟电路,因此不会受到数字电路如斩波电路和开关电容电路噪声的影响.

模拟前端在中芯国际0.18微米的工艺中进行了流片,等效输入噪声(从0.48Hz到-2000Hz)仅仅有1.19 μ Vrms.虽然在电源电压3V的情况下,系统的功耗只有32.1 μ W,测试结果表明,系统可以成功地抓取到生物电势信号.

关键词: 模拟前端电路,生物电势测量,低功耗,低噪声

Abstract

A critical and important part of the medical diagnosis is the monitoring of the biopotential signals. Patients are always connected to a bulky and mains-powered instrument. This not only restricts the mobility of the patients but also brings discomfort to them. Meanwhile, the measuring time can not last long thus affecting the effects of the diagnosis. Therefore, there is a high demand for low-power and small size factor ambulatory biopotential measurement systems. In addition, the system can be configured for different biopotential applications. The ultimate goal is to implement a system that is both invisible and comfortable. The systems not only increase the quality of life, but also sharply decrease the cost of healthcare delivery.

In this paper, a continuously tunable gain and bandwidth analog front-end for ambulatory biopotential measurement systems is presented. The front-end circuit is capable of amplifying and conditioning different biopotentials. To optimize the power consumption and simplify the system architecture, the front-end only adopts two-stage amplifiers. In addition, careful design of the critical transistors eliminates the need of chopping circuits. The front-end is pure analog without interference from digital parts like chopping and switch capacitor circuits.

The chip is fabricated under SMIC 0.18 μm CMOS process. The input-referred noise of the system is only 1.19 μV_{rms} (0.48-2000Hz). Although the power consumption is only 32.1 μW under 3V voltage supply, test results show that the chip can successfully extract biopotential signals.

Keywords: Analog front-end, biopotential measurement system, low-power, low-noise

Chapter 1 Introduction

1.1 Background of the research

It is difficult to put a price tag on human life. This is especially true after the attack of the World Trade Center on September 11, 2001. A new notion has emerged for people around the world and our way of life [1]. People become more and more realized to focus on the health care delivery. Yet, some evident challenges are dramatically affecting this delivery. Let's consider the following facts [2-4]

According to many reference, the cost of healthcare delivery is on a sharp upward trend, causing a lot of business and families to cut on operations and household expenses respectively. In the US alone, for example, the total national healthcare spending in 2008 has increased by 6.7%. It is anticipated that the total expenses will double in dollars by the end of 2019, consuming around 21% of the GDP of USA (Fig.1.1).

Fig 1.1 Projections of expenditure and their share of GDP

Another challenge is the medical errors occur in the process of health care delivery. As the experts indicate, more than 98000 people die in hospitals for the fault treatment and diagnostics that could have been prevented. That's more than die from motor vehicle accidents, breast cancer, or AIDS, which receive more attention from public. Not apparently, these medical errors are often caused by faulty conditions and systems that lead people to make wrong decisions other than people themselves.

The third challenge is the lack of wide access to healthcare. Seven major diseases accounted for around 80% of deaths in the world: chronic bronchitis, influenza, heart

disease, arthritis, cancer, asthma and diabetes. If early systematic inspection could be introduced, the death rate will be largely improved.

Therefore, the three significant challenges can be concluded: cost of healthcare, quality of healthcare and availability of healthcare. The healthcare professionals are trying to meet these growing challenges now. They hope to reduce healthcare cost while still giving high quality care. Providing wide access to care for as many people as possible and easy access to medical professionals anytime and anywhere are also what they concern. Meanwhile, they are trying to shift the focus from treatment to prevention via fitness programs and shorten the length of hospital stay by decentralizing the healthcare provision. In a word, balance must be kept between cost containment and patient outcomes.

Technology is indeed a good assistant for medical personals. It serves as the catalyst that can accelerate the transformation of healthcare and medical practice. Whether it is the care and safe delivery of undernourished or extending the life of a senior citizen, any technology that can lower the loss of human life or enhance the quality of life has a value that is priceless.

1.2 Cutting-edge technology in biomedical applications

In recent years, a possible solution to the mentioned challenges can be the ambulatory biopotential measurement systems [5]. As shown in Fig1.2, several sensor nodes are attached to the human body, with each having enough intelligence to implement its own operation. For instance, the top sensor node can extract the EEG (electroencephalograph) signal while the sensor node attached to the chest is capable of getting the electrocardiogram (ECG) signal. The sensor nodes should be able to communicate with one another or with a central node, and then the central node communicates with the outer world through a WLAN or mobile network. In this way, patients are no longer required to stay at hospitals with connection to bulky and mains-powered instrument, which creates discomfort and reduces mobility. The whole ambulatory system can not only enable personalized healthcare or deliver remote health service, but also substantially increase the efficiency of first-aid in case of emergency. Since less human force and time are involved in the whole process, the potential medical cost is for sure to be reduced. As for the healthcare quality, since the weak biopotential signals are amplified and digitized locally, less interference is

introduced. Medical errors can also be reduced to some extent.

However, the realization of such a system puts very stringent constraints on the system design, especially for sensor nodes, in two aspects: (1) How to use innovative integration and packaging techniques to reduce the size and weight of the nodes to make them reconcile with the human body for invisibility and comfort. (2) How to

Fig 1.2 Technology vision for Body Sensor Networks

implement an electrical system that can be embedded in the node in order to successfully acquire high-quality bio-potential signals from the human body? This thesis focuses on giving partial answers to the second issue.

According to the signal chain, the electrical system can be divided into the following parts as shown in Fig 1.3. The biopotential signals extracted from sensors are fed into the analog front-end. The analog-front implements the function of amplifying and conditioning the weak signals. The signal should be large and clear enough to be recognized by the analog-to-digital (AD) converters embedded in the microcontrollers. After the signal is digitized, the micro-controller can further processing the signal or control the work flow of the ambulatory systems. If necessary, information will be sent outside or received from outside via the radio transceiver.

Fig 1.3: System division of ambulatory biopotential systems

Since the analog front-end directly interfaces with real biopotential signals, it can be the most crucial part of the whole ambulatory biopotential measurement system. The design of the front-end circuits almost defines the performance of the whole system. To successfully implement such an biopotential system, the designer is required not only a solid understanding of analog design technique, but also the characteristics of the biopotential signals and their clinical use.

1.3 Organization of the paper

The analog front-end for the biopotential measurement system has to cope with various challenges when extracting the biopotential signals. These problems are not only due to the characteristics of the signals but also due to the apparatus and environment used. Chapter 2 gives a brief introduction of about these aspects: genesis of the biopotential signals , chemistry of the electrodes and interference theory related to the process of measuring.

Chapter 3 discusses different architectures of amplifier to implement such an analog front-end. The advantages and disadvantages are both compared. Then we propose a modified version of the current feedback amplifier. The front-end we implement is able to acquiring good quality biopotential signals without sacrificing the power consumption.

In chapter 4, we focus on the presentation of the critical points in layout designing and PCB designing. In addition, test results are given in this chapter. Of course, there are still some problems in the testing process; some useful solutions are presents for further testing.

Chapter 5 give a conclusion of the whole thesis and what we should do for the future work.

Chapter 2 Introduction of Biopotential Measuring

The bio-signal front-end system has to deal with several problems when extracting the signals from the body. The problems are not only close related with the extremely weak characteristics of the bio-potential signals but also with the environment and the equipment used during the signal acquisition. Therefore, designing such an analog front-end circuit requires the designer both a solid understanding of mixed-signal design techniques and a good grasp of the origin and characteristics of the bio-potential signals.

In this chapter, we will focus on the challenges encountered during the process of extracting biopotential signals. We will introduce the genesis of the biosignals, the frequency and amplitude of the ECG, EEG and EMG signals and chemistry of the electrodes which brings non-ideal effects when measuring. In addition, some interference theory that is closely related with the ECG measuring is also presented. Last but not least; the state-of-the-art ambulatory biopotential measurement system is reviewed, which is the basic of our analog front-end design.

2.1 Brief introduction of the biopotential signals

Biopotential signal are created because of the electro-chemical activity of certain class of cells which are components of muscular, nervous or glandular tissue. Normally, these cells exhibit a resting potential. When stimulated, they create an action potential. Electrically, the activity of each cell is expressed by the exchanging of the ion through the cell membrane. An inactive cell's membrane potential is called the resting potential. When in the rest state, the cell's membrane is more permeable to K^+ than Na^+ , so the inner concentration of the cell is much high than outer concentration. In this way, a diffusion gradient of K^+ appears from the interior to the exterior of the cell, making the exterior more positive relative to the interior. In steady condition, the electrical field balances the diffusion gradient of the K^+ ions. A polarization voltage of nearly -70mv is reached when equilibrium is reached. When the central nervous system electrically stimulates the cell, the condition inverses. The membrane becomes more permeable to Na ions. Therefore, Na ions diffuse to the interior of the cell from the exterior. This leads to an increase in potential of the cell. When this potential is as high as +40mv, the permeability of the membrane to

K^+ ions increases and Na^+ ions decreases. The variation of the permeability induces a sharp decrease in the membrane potential towards its rest state. We always call the action potential of this cycle the cellular potential. The bio-signals like ECG (or EKG) and EEG are often the result of some action potentials produced by a mixture of different cells [7].

EEG is the measure of the electrical activity of the brain created by a group of neurons. Electrodes are placed on certain locations of the scalp. Similarly, ECG is the measure of the electrical activity of the heart. It is extracted from the electrodes on the chest and is characterized by its P-wave, QRS-complex and T-wave. Finally, EMG is the electrical potential of the skeletal muscle cells, which is contracted during the contraction of the muscle.

2.2 Introduction of Biosignal electrodes

To measure potentials and hence currents in the body, it is necessary to offer some interfaces between the body and the analog front-end circuit [7]. The bio-current is carried by ions in the body, whereas it is carried by electrons on the wires connecting the electrodes to the front-end circuits. Therefore, a transducer interface is necessary between the body and the readout circuit that converts the ionic current into electronic current, or vice versa. This interface function is always implemented by biopotential electrodes. . We shall briefly review the basic mechanisms involved in the transduction process.

The operation principle of a biopotential electrode can be described by an electrode–electrolyte interface. The electrode/electrolyte interface is illustrated in Figure 2.1. In order to allow the current flow between the electrolyte, which has no free electrons, and the electrode, which has no free cations or anions, a chemical reaction has to occur at the interface that can be represented by the following general equations:

In this equation, C and A stands for the cations and anions in the electrolyte, respectively, and it has been assumed that the electrode is made up of the cations of the electrolyte. Therefore, the cations in the electrode can oxidize at the interface, and the anions coming to the interface can be oxidized to a neutral atom, both resulting in

a free electron in the electrode. Thus, current can pass from the electrode to the electrolyte. Similarly, the reduction reactions create current in the reverse direction.

Fig 2.1 Electrode/electrolyte interface

Therefore, if a metal is inserted in a solution, which has the ions of the same metal and some anions to preserve the neutrality of the solution, the reactions start to occur depending on the concentration of the cations in the solution. This disturbs the neutrality of the solution, and a charge gradient builds up at the electrode–electrolyte interface, resulting in a potential difference that is called the half-cell potential. The mismatch of the half-cell potential between the reference electrode and the recording electrode is responsible for the differential DC electrode offset voltage.

2.2.1 Polarizable and nonpolarizable Electrodes

In theory, there are two kinds of electrodes: those that are perfectly polarizable and those that are perfectly nonpolarizable. The perfectly polarizable electrodes have no actual charge transfer between the electrode–electrolyte interface. Thus, such electrodes behave as capacitors and the current is due to the displacement current. On the other hand, the current passes freely across the electrode–electrolyte interface of the non-polarizable electrodes, thus these electrodes behave as a resistor. However, neither of the two types can be fabricated. Thus, practical electrodes are something between these two types.

We can describe the equivalent circuit of the electrodes as shown in Figure 2.2. R_d and C_d represent the resistive and reactive components that are closely related with the electrode–electrolyte interface and R_s is the resistance of the electrolyte solution. The half-cell potential of the interface is represented with a voltage source, E_{hc} .

Fig 2.2 Equivalent models of electrodes

In conventional electrodes, the electrolyte represents the gel that is used in between the tissue and the electrode. Since the biopotential signals are generally extracted differentially from two electrodes, there is always a mismatch between the half-cell potentials due to the difference in the gel–tissue interface. Therefore, there appears a DC potential between the two electrodes, which is much larger than the μV level biopotential signals. This DC potential will be referred as differential DC electrode offset voltage in the rest of the text. Hence, the biopotential analog front-end circuit should exhibit high-pass filter (HPF) characteristics to prevent the saturation of the readout circuit.

2.2.2 Categories of electrode

Over the years, many different types of electrode for recording bio-potential signals have been developed. They always can be classified as the following three types.

Wet electrodes are always coated with gel type electrolyte between the interface of the skin and electrode. The most common type of a wet electrode is the Ag/AgCl electrode. The electrode is often fabricated from a disk of Ag that may or may not have an electrolytically disposition layer of AgCl on its contacting surface. Its characteristics approach the characteristics of a perfect nonpolarizable electrode. Since the Ag/AgCl electrodes have the advantages of low impedance and low artifact low artifact due to the motion of artifact, they are popular for recording the ECG or in cardiac monitoring for long-term recordings. However the gel used brings discomfort and increase the time of preparation before measuring.

Dry electrodes [8] are those do not use any kind of gel at the interface of the electrode and body. Compared to the wet electrodes, they brings more comfort and

decrease preparation time. Without electrolyte, they are more like polarizable electrodes or a leaky capacitor. The analog front-end matches the dry electrode must have ultra-high impedance. Therefore, the front-end should be placed closed to the electrode to prevent the electromagnetic interference. Of course, this can be accomplished by using active electrodes (the electrodes embedded with the analog front-end amplifiers). However, active electrodes are not easy to get high CMRR in standard CMOS process. Of course, the performances of dry electrodes are not that poor. It has been demonstrated that with the introducing of MEMS technology, dry electrodes can also achieve low impedance and low dc offset variance comparable to wet electrodes.

In addition to the dry and wet electrodes, non-contact electrodes are also an emerging kind of electrodes. They serve as a pure capacitor between the body and the analog front-end allowing remote measuring of the signals. The most evident advantage of non-contact electrodes is safe, for no DC current is drawn from the body. But two disadvantages are the input impedance of the analog front-end should be very large and any relative motion between the electrode and body will lead the change of capacitance, thus degrade the signal.

2.3 Interference in biosignal measuring

Bio-signal recordings are often disturbed by a high level of interference [10]. Though its origin is clear, the mains power supply, the cause of the disturbance is not that obvious. Because in many cases, very complicated equipment is used, it's not easy to identify which equipment is the main contributor. Sometimes the use of equipment with very good specifications does not assure interference-free recordings. In most measurement conditions, an interference level of 1-10 μV peak-to-peak, which is less than 1% of the peak-to-peak value of an ECG, is acceptable. In addition, the noise of an electrode is also in the magnitude of several μV peak-to-peak. In a word, 10 μV peak-to-peak interference is the maximum level that can be accepted. The common mechanism of electrical mains interference is explained in this part.

2.3.1 Interference from the body and amplifier

Common-mode interference is one major source of interference in bio-potential signals measurement. The basic mechanism (shown in Figure 2.3) is that the capacitance between the human body, the mains power supply and the ground of the

earth cause a small current interference to flow through the body.

When modeling the practical measurement situation, the typical capacitance between the body and earth C_{body} is always set to be 300pF and the typical capacitance between the body and the mains power supply C_{pow} is set to be 3pF. These capacitance cause an interference current i_1 of $0.5\mu A$ (peak-to-peak) to pass from the power supply (220V, 50Hz) through the body to earth. It is regularly found that C_{pow} and C_{body} show large variations and interference current sometimes ten times as high as $0.5\mu A$. If an amplifier is connected to the human body, some of the current from the mains to patient i_1 will flow to earth through Z_{rl} , which is the impedance of the electrode/skin interface of the electrode. The portion of i_1 that flows through Z_{rl} causes the average potential of the body and amplifier common to be different, which equivalently creates a common-mode voltage.

Fig 2.3 Basic mechanism of interference

The capacitances between the amplifier common and mains C_{sup} and between amplifier common and earth C_{iso} should also be considered. C_{sup} causes an additional current interference i_2 to flow from the amplifier to earth. Some of the current i_2 flows through C_{iso} and some of the current flows through Z_{rl} and C_{body} . The portion of i_2 flows through Z_{rl} contributes to the common-mode voltage.

The interference current i_1 and i_2 demand a very high CMRR of the amplifier. It is always accepted that the CMRR is greater than 90dB. Of course, high CMRR alone is not enough for front-end amplifiers. When there is difference in electrode impedance or input impedance, the common mode voltage will be converted into

differential input voltage. This mechanism called “the potential divider” effect is the main reason why it is important to reduce the common-mode voltage as much as possible. This differential interference input voltage created this way is given by equation 2.3.1.

$$V_{ab} = V_{cm} \left\{ \frac{Z_{ia}}{Z_{ia} + Z_{ea}} - \frac{Z_{ib}}{Z_{ib} + Z_{eb}} \right\} \quad (2-3-1)$$

where $Z_{ia,b}$ are input impedances, $Z_{ea,b}$ are electrode impedances.

Assuming the input impedance is much larger than the electrode impedance, rewriting this equation can be more instructive

$$V_{ab} = V_{cm} \frac{Z_e}{Z_i} \left\{ \frac{\Delta Z_e}{Z_e} + \frac{\Delta Z_i}{Z_i} \right\} \quad (2-3-2)$$

$$\text{where } Z_e = \frac{1}{2}(Z_{ea} + Z_{eb}), \quad Z_i = \frac{1}{2}(Z_{ia} + Z_{ib})$$

It is clear that the level of inference generated by the potential divider effect depends on the magnitude of the common-mode voltage, the ratio of the input impedance and electrode impedance, and the relative difference in these two impedances. Surely, impedance should be large and matching of the amplifier should also be carefully designed.

2.3.2 Interference from the measurement cables

Another major source of interference in bio-potential measurements results from the capacitive coupling of the measurement cables with the mains (Cca and Ccb shown in Fig2.3.1). The currents induced in the wires (ia and ib) flow to the body via the electrodes and from the body to earth via Cbody and via Zrl in series with Ciso. Since the currents induced in the wires and the electrode impedances usually differ significantly, a relatively large differential voltage is produced between the inputs of the amplifier. The voltage can be calculated by the following equation:

$$V_{ab} = i_a Z_{ea} - i_b Z_{eb} \quad (2-3-3)$$

It is instructive to rewrite this equation as:

$$V_{ab} = i * Z_e * \left(\frac{\Delta Z_e}{Z_e} + \frac{\Delta i}{i} \right) \quad (2-3-4)$$

where $i = \frac{1}{2}(i_a + i_b)$, $Z_e = \frac{1}{2}(Z_{ea} + Z_{eb})$

One situation can be a mean current of 10nA peak-to-peak in the wires, mean electrode impedance around $20k\Omega$. Assuming the relative variation in current interference and electrode impedance are 50%, then the differential voltage:

$$V_{ab} = 10\text{nA} * 20k\Omega * (50\% + 50\%) = 200\mu\text{V} \quad (2-3-5)$$

It is a high interference level for bio-signals, shielding should be taken into consideration when in practical measuring.

2.3.3 Magnetically induced interference

In addition to the interference mentioned above, another interference disturb the system is called the electromagnetic interference [11]. The magnetic field made by the changeable mains current cuts the loop enclosed by the body, the lead of the system and the amplifier. This introduces an electromotive force (EMF), which creates an AC potential at the input of the circuit. This disturbance is easily distinguished from other types of interference because it varies with the area and the orientation of the loop formed by the cables. In theory, suppression is easy by means of reducing the loop area as much as possible (twisting of cables). It is not always feasible in practical use. For example, the normal electrode configuration in ECG measurements with electrodes placed at the foot of the human body may lead a quite big area between the input cables. Shielding of the patient with a material of high magnetic permeability is too complicated in most situations. Therefore it is often necessary to keep all magnetic sources far from the human body or use miniaturized portable biomedical acquisition systems that can be placed much closer to the electrodes, which in turn reduces the cable length.

2.4 State-of-the-art biopotential measurement systems

In recent years, a few attempts have been made to implement some chips for ambulatory biopotential measurement systems. We will give two best examples of the world up till now here:

(1) Fig 2.4 shows a wireless ambulatory biopotential measurement system fabricated by IMEC research centre. The system consists of IMEC's ExG ASICS and commercial products. As commercial components it uses a Nordic nRF24L01 radio chip set and a TI MSP430f1611 micro-controller as well as a 160mAh Lion battery. The dedicated Exg ASIC is able to amplify and condition different biopotential

signals. The experimental results show that the systems can work well and consumes a power consumption of only 1.16mW [26].

Fig 2.4 IMEC biopotential measurement system

(2) Fig 2.5 is a micro-power System-on-Chip for vital-sign monitoring in wireless body sensor networks [27], which is almost the best solutions in the world until now. The encapsulated wireless sensor node is in the form of a thin and flexible patch, comprising sensors, Sensium SoC, battery and antenna as shown in Fig2.5. The system is powered by a 1V environmentally-friendly materials such that it can be recycled or safely disposed of, and provides typically 3mAh/cm² at 1.4V, dropping to 0.9V at end of battery life.

Fig 2.5 Flexible patch for body worn wireless vital sign monitoring

The SOC is designed to support a number of different types for monitoring applications. The SOC block diagram can be shown in Fig2.6. The analog front-end provides gain, filtering, biasing and buffering of the sensor inputs. The embedded digital processor may be used for sensor calibration to ensure excellent offset and gain accuracy. A 10b $\Delta\Sigma$ analogue-to-digital converter samples sensor input signals within a dc to 250Hz bandwidth.

Fig 2.6 Block diagram of the SENSIIUM SOC

2.5 Challenges in design of a biopotential analog front-end

It is clear that even in the state-of-the-art biopotential measurement systems, the analog front-end is the most important part. The critical purpose of a biopotential front-end is to amplify and filter the weak biopotential signals. However, the design of such an amplifier is not that easy. The amplifier should tackle with different challenges in order to successfully extract the biopotential signals. Meanwhile, the power consumption of the amplifier must be minimized for long-term power anatomy. Fig 2.7 shows the characteristics and relevant interferences in the biopotential signals measuring. Combining with Fig 2.4.1, we will summarize the essential challenges:

- (1) For the low frequency and micro-V amplitude of the signal, the bandwidth we interest is dominated by $1/f$ noise. The analog front we design should be of low noise to get high quality signal.
- (2) 50/60 Hz coupling from the mains appears as a common-mode signal in the input of the whole circuitry system, which demands the system an ultra-high common-mode

rejection ratio

(3) The dc electrode offset generated at the skin-electrode interface should be put into consideration. It is a must the system can implement high-pass filter function to eliminate the dc electrode offset.

(4) The amplitude and bandwidth of the analog front-end can be varied for different biopotential signals.

(5) The ultimate goal of this thesis is to get high-quality bio-potential signals without sacrificing the power dissipation. A good trade of should be achieved between quality and power.

Fig 2.7 Characteristics and interference in biopotential signals

Chapter 3 Designing of Analog Front-end Circuits

3.1 Comparison of different architectures

The most critical part of the analog front-end circuits is the first stage instrumentation amplifier (IA). It defines the signal quality, the noise level, the CMRR and filters the DC electrodes off. So much attention should be placed in the designing and optimization of this stage.

3.1.1 Three-opamp Instrumentation Amplifier

The three-opamp [12-13] IA is able to accurately amplify a low-level signal in the presence of a large common-mode component and can offer ultra-high input impedance/very low output impedance. For this reason, IA finds wide application in the measurement instrumentation and test. Of course, it can also be used in the field of biopotential signal amplification.

Fig 3.1 shows a very typical topology of three-opamp IA. OA₁ and OA₂ form what is often called as the input stage, and OA₃ forms the output stage. Since the constraint of the input voltage, the voltage across R_G is v₁-v₂. For the input current constraints, the current through R₃ is the same as R_G. It is easy to get the equation:

$$v_{o1} - v_{o2} = \left(1 + \frac{2R_3}{R_G}\right)(v_1 - v_2) \quad (3-1-1)$$

It is quite clear the input stage serves as a difference-input, difference output amplifier. For the output stage, we find that OA3 is a difference amplifier, so

$$v_o = \frac{R_2}{R_1}(v_{o1} - v_{o2}) \quad (3-1-2)$$

Combing these two equations together gives

$$v_o = \left(\frac{R_2}{R_1}\right)\left(1 + \frac{2R_3}{R_G}\right)(v_1 - v_2) \quad (3-1-3)$$

If R₁=R₂, the gain can be further simplified to $1 + \frac{2R_3}{R_G}$

Resistor R_G sets the overall gain of this amplifier. It may be implemented internally, externally, or programmed by software or switches. The resistor is always

made of good quality thus the gain of the IA is quite accurate and stable. Since OA_1 and OA_2 are working in the non-inverting configuration, the closed-loop input resistance is ultra-high. For the same reason, the closed-loop output resistance of OA_3 is quite low.

Fig 3.1 Topology of three-opamp instrumentation amplifier

However the three-opamp IA has two very evident disadvantages:

(1) The CMRR of the IA is highly depends on the matching of the resistors. It can be concluded:

$$CMRR \leq 20 \log \left[\frac{1 + \frac{2R_1}{R_G}}{Mismatch\%} \right] \quad (3-1-4)$$

In a typical CMOS process technology, thin film laser trimmed resistors are required to offer excellent matching between the three internal op-amps. This special technology is for sure to increase the cost of circuits and introduces additional difficulties for the integration of following circuits.

(2) The output stage of the three-opamp has quite low output impedance. But this low impedance drives the feedback resistors leads to additional current consumption. Therefore, the power dissipation of the three-opamp is not that satisfactory according to many references.

The three-opamp IA is a very good choice for discrete component circuits. But for its relatively high dissipation and laser trimming technology required, this topology is not quite suitable for ambulatory biopotential measurement system.

3.1.2 Chopper stabilized Instrumentation Amplifier

Since noise is quite a big issue in the instrumentation amplifier for biopotential applications, chopper stabilized amplifier are also a common practice in this field.

We give a brief introduction of the chopping techniques here [14-15]. The low frequency input signal is multiplied with a rectangular signal $m(t)$ with unity amplitude and 50% duty-circle. This shifts the frequency spectrum of the input signal to the odd harmonics of f_{chop} . Then, the modulated input signal is magnified via amplifier $A(f)$ and re-amplifying with $m(t)$. This can reconstruct the signal while leaving replicas at the odd harmonics of f_{chop} . LPF can eliminate this replica. Fig 3.2 shows the basic principal of the chopper modulation technique.

Fig 3.2 Principal of the chopper modulation technique

As for the output noise and DC offset of the amplifier, they are denoted as v_n and v_{off} . The DC offset and noises are only modulated by output modulator. From the view of spectrum, the baseband is free of DC offset. But in terms of noise, there are still some of them remains in the baseband. This can be handled this way:

The input referred voltage noise PSD of the amplifier can be written as, which include both thermal noise and flicker noise.

$$S_{in}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{n=-\infty}^{\infty} \frac{1}{n^2} S_{vn}(f - nf_{chop}) \quad (3-1-5)$$

Assuming $f \gg f_{chop}$ and $f < 0.5f_{chop}$, the thermal noise can be approximately written as:

$$S_{in,thermal}(f) \cong S_{in,thermal}(0) \cong S_o \quad (3-1-6)$$

According to the equation, we can find the thermal noise is not affected by the chopper at all. Indeed, the chopping modulator only periodically changes the sign of the thermal noise.

Continue to consider the flicker noise, it can be approximately written as

$$S_{in,flicker}(f) \cong S_o \frac{f_{c,1/f}}{f} \quad (3-1-7)$$

Inserting equation 3.1.6 to 3.1.5, equation 3.1.7 can be expressed as:

$$S_{in,flicker}(f) \cong 0.85 S_o \frac{f_{c,1/f}}{f_{chop}} \quad (3-1-8)$$

Combining equation 3.17 and 3.18, we can easily get the magnitude of the baseband noise:

$$S_{in}(f) \cong 0.85 S_o \frac{f_{c,1/f}}{f_{chop}} + S_o \quad (3-1-9)$$

It can be concluded that the chopper technique can effectively eliminate the flicker noise while do not affect the thermal noise.

Admittedly, the chopper stabilization can be an effective option in applications for biomedical instrumentation. But this topology still suffers from two problems:

(1)The finite bandwidth of choppers creates significant signal distortion. This is especially true when the power is low. The excess settling time creates even harmonics that lead to sensitivity errors and distortion. Techniques to eliminate this distortion have been explored, but this result in addition current thus dissipation and complicates the circuits.

(2)Another problem is the limited headroom from the amplified offset prior to chopping and low pass filtering. Low headroom can artificially limit the front-end gain in low-power amplifiers, and deteriorate the performance for the existing of second-stage noise.

Therefore, these problems still prevented the chopper-stabilized instrumentation amplifier not an enough good choice for biopotential measurement systems.

3.1.3 Current Feedback Instrumentation Amplifier

Another instrumentation amplifier topology is shown in Fig 3.3. It is called the

current feedback amplifier [16-17].

Fig 3.3 Current Feedback Instrumentation Amplifier

Analyzing the input stage, if two buffers are implemented, the current I_1 can be calculated as:

$$I_1 = (V_{in1} - V_{in2}) / R_1 \quad (3-1-10)$$

Meanwhile, the output stage voltage is:

$$V_{out} = R_2 * I_2 + V_{ref} \quad (3-1-11)$$

The input stage serves as a transconductance amplifier and the output stage serves as a transresistance amplifier. If the current in the input stage is mirrored to the output stage, equation (3-1-11) is obtained:

$$V_{out} = \frac{R_2}{R_1} (V_{in1} - V_{in2}) + V_{ref} \quad (3-1-12)$$

Two evident advantages of the current-feedback amplifier should be mentioned here:

(1) In contrast to the three-opamp architecture, there is no feedback from the output to the input and only one high impedance node is adopted. This simplifies the circuits and frequency compensation.

(2) The CMRR of the current-feedback do not depend on the matching of the resistor any more. The number of the resistor is reduced thus saving chip area.

Table 3.1 gives a conclusion of the performance comparison of the three-opamp, chopper stabilized, and current feedback topology.

Topology	Three-opamp	Chopper Stabilized	Current Feedback
Low Power	No	No	Yes
Noise Fold-over	Yes	No	Yes
High Input Impedance	Yes	No	Yes
CMRR independent from matching resistor	No	No	Yes

3.2 Modified architecture implemented

A typical analog front-end for biopotential measurement system always implement two main functions: amplifying and conditioning. It is a common practice to embed the band-pass filter within such a low noise and low power amplifier.

Fig. 3.4 shows the proposed system architecture of the analog front-end circuits. The front-end mainly consists of two stages. The first stage is a high-pass current feedback amplifier (HPCFA). The weak biosignals fed into the system is amplified and AC coupled in this stage. So the DC offset voltage can be effectively eliminated. Meanwhile, a continuously tunable gain function is also implemented in this stage. The second stage is a variable bandwidth and gain amplifier (VBGA), which offers enough gain and conditions the signal with low-pass filtering. Variable gain and bandwidth make the system suitable for different biopotential signals. If necessary, a buffer can be inserted to drive the sampling capacitors of the following ADC for further digital processing.

Fig 3.4 System architecture of analog front-end

3.2.1 Circuit Implementation of the current feedback amplifier

There are a variety of possibilities to design a current feedback instrumentation amplifier. Most of the reported amplifiers are implemented in bipolar and CMOS technology. A possible version [17] is shown in Figure 3.5. This version adopts a reduced number of stacked transistors, thus improving DC behavior at low power voltage.

With no signal applied, the circuit is balanced and all currents are equal, $V_{out}=V_{ref}$. When a differential signal is applied, the output current of the transconductance stage G_m become unbalanced in order to maintain the currents

systems.

3.2.2 Modified Current-feedback instrumentation amplifier

We modify the architecture in Figure 2 to a fully differential architecture as shown in Fig 3.6. The theory behind the circuits can be understood in an intuitional way. When differential signals are applied, small current signal can only pass through resistor R_1 for the constant current source I_1 and I_2 . With the same reason, current source I_3 and I_4 lead the small current flowing through R_2 instead of I_3 and I_4 . In this way, the same current through resistor R_1 and R_2 make the gain of the circuits still defined by the ratio of R_1 and R_2 . Transistor M_3 and M_4 serve not only as Gm stage in Figure 3.2.2.1, but also as the current mirrors and transresistance stage to recreate the output stage.

Fig 3.6 Modified current feedback amplifier

Also the gain of the circuit can be calculated from the small-signal half-circuit model. The circuit in Fig 3.6 can be expressed as the model in Fig 3.7.

Using the KLV theory, we can derive from the small signal model

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1} \frac{1}{\left(1 + \frac{1}{g_{m1}R_1}\right)\left(1 + \frac{1}{g_{m2}R_2}\right)R_2} \quad (3-2-4)$$

$$1 + \frac{R_{ds1} // R_{out2}}{R_1}$$

If $\frac{(1 + \frac{1}{g_{m1}R_1})(1 + \frac{1}{g_{m2}R_2})R_2}{R_{ds1} // R_{out2}} \ll 1$, $A_v = \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$. The derivation is

the same as the result we understand from an intuitional way.

Fig 3.7 Small-signal half-circuit model

This total differential architecture improves the CMRR of the system. Meanwhile, the circuit is simplified by reducing the parallel current pairs. Current in I_7 and I_8 are shared by the M_1 , M_2 , M_3 and M_4 . Thus, the system dissipation dramatically reduced compared to that in Figure 3.5.

3.2.3 HP characteristic implementation

Considering the high-pass characteristic of the system, we do not design additional high-pass filters to save power. Instead, Gm-C filter is introduced to feedback circuit. A low-pass filter combined with a feedback circuit can make a high-pass filter. The transfer function of the low pass filter can be written as:

$$f_{GM-C} = \frac{g_m}{1 + s / 2\pi f_c} \quad (3-2-5)$$

Figure 3.8 shows the equivalent diagram of the fully differential current-feedback instrumentation amplifier we have designed. It's easy to get the equation (3-1-18), which can be rewritten as the transfer function, (3-1-19).

$$\left(\frac{V_{in}}{R_1} - V_{out} \frac{g_m}{1 + s / 2\pi f_c} \right) R_2 = V_{out} \quad (3-2-6)$$

$$\frac{V_{out}}{V_{in}} = \frac{s + 2\pi f_c}{s + 2\pi f_c(1 + g_m R_2)} \frac{R_2}{R_1} \quad (3-2-7)$$

Fig 3.8 Block diagram of HP filter

If $g_m R_2 \gg 1$, equation 3-2-7 is a typical high-pass-filter function. Therefore, the low-pass cutoff frequency is $g_m R_2 f_c$. Intutionally, the feedback low-pass filter blocks the current component higher than f_c , current lower than f_c is subtracted at the input adder. Thus, the output is zero and current component higher than $g_m R_2 f_c$ passes. The filter achieves the function of elimnating dc offset voltage.

3.2.4 Circuit Implementation of the HPCFA stage

The first stage of analog front-end is shown in Fig3.9. The Gm stage actually consists of OTA- C_{ext} stage (transistor M_5 - M_{11}) and g_m stage (transistor M_{15} - M_{18}). If open-loop gain of OTA is $A_{v,ota}$, the equivalent gm of the Gm stage is $A_{v,ota} * g_{m17}$. This assures $g_m R_2 \gg 1$ in equation (3-1-19). It is easy to get the G_m - C low pass filter composed of OTA- C_{ext} stage has a cut-off frequency f_c of $g_{m,ota} / A_{v,ota} * C_{ext}$. Substitute equivalent gm and f_c to equation (3-1-19), the high cut-off frequency f_h is:

$$f_h = g_{m17} * R_2 * g_{m,ota} / 2\pi * C_{ext} \quad (3-2-8)$$

For ECG signals, f_h is as low as 0.5Hz, either lowering the value of $g_{m,ota}$ or increase C_{ext} can reduce the cut-off frequency. We parallel the transistor pair M_{11}, M_{12} and M_{13}, M_{14} as the output stage of OTA. For $g_m \propto L^{-1/2}$, increase in equivalent L will minimize $g_{m,ota}$. In addition, we define C_{ext} around 1 μ F. This capacitor consumes two much room in the chip, so it is still implemented off the chip.

The implementation of high-pass filter relies on the maximum current differnce of transistor M_{15} and M_{16} in gm stage. When input dc offset generate current in R_1 , if

M_{15} and M_{16} could offer enough current to compensate this current, output will be zero. So we could adjust R_1 and tail current source I_8 in g_m stage to define the maximum dc offset the system could rule out. Of course, it is a trade-off between dc offset and power consumption. We set $R_1=50\text{ k}\Omega$ and $I_8=1\text{ }\mu\text{A}$, thus the maximum dc offset is around 100 mV, much bigger than the offset voltage induced by different electrodes with same type.

Fig 3.9 Circuit implementation of HPCFA stage

The HPCFA stage is fully differential architecture, so common mode feedback circuit is needed. Gates of M_{19} and M_{22} sense the output voltage and gates of M_{20} and M_{21} are connected to common-mode input voltage 1.2V. When the output common-mode voltage is different from V_{cm} , differential pairs M_{19} - M_{22} will adjust the current through M_1 and M_2 in Figure 5 by transistors M_{23} and M_{25} . In this way, the drain voltage of M_1 and M_2 is changed. For M_3 and M_4 act as source follower to M_1

and M_2 drain voltage, common mode output voltage is adjusted. When common mode feedback circuit is in steady condition, the output voltage of first stage is as high as V_{cm} .

Fig 3.10 Current Feedback circuits

We hope the resistor $R1$ that directly define the voltage gain of first stage could be continuously adjusted. The resistor is implemented by two NMOS transistors work in linear region. As shown in Figure 3.11, when common mode output voltage is 1.2V and V_R is set to 3V, scaling the dimension of the transistor to make it equivalent resistance $500k\Omega$. The gain of first stage will be around 10. Voltage gain can be changed by adjusting V_r so as to alter the equivalent resistance.

Fig 3.11 Continuously varied resistors

As for the current sources in the system, we implement it with current mirrors

shown in Figure 3.12. I_{in} injected externally generates bias voltage through M_{p1} and M_{p2} . V_{b1} and V_{b2} are DC bias applied to the gate of M_{p1} and M_{n2} . Thus, all the current sources in the system could be copied from M_{p1} , M_{p2} , M_{n1} , M_{n2}

Fig 3.12 Implementation of current source

3.2.5 Simulation of HPCFA stage

(1) AC response of the HPCFA stage

Fig 3.13 shows the AC response of the HPCFA stage. The simulation results were achieved in the TT process corner under 25C degree. The open loop gain of this stage is around 10.

Fig 3.13 AC response of the HPCFA stage

(2) Transient Simulation of HPCFA stage

We simulate the transient response of the HPCFA stage in TT process corner. Fig 3.14 shows the simulation results. It can be seen that the differential output gain is around 10:

Fig 3.14 Transient response of the HPCFA stage

(3) DC offset voltage

Normally for the electrodes made of same material, Ag/AgCl electrodes, the offset of this kind of electrode is always relatively low. Fig 3.15 shows differential DC electrode offset measurements from several electrode pairs on two different subjects. The maximum measured differential electrode offset voltage is smaller than 20 mV [18].

Fig 3.15 DC offset voltage from different electrodes

The HPCFA stage we design can eliminate around 50mV DC offset, which is enough big for offset voltage to saturate the HPCFA stage, as shown in Fig 3.16. The DC offset voltage can be as high as $\pm 55\text{mV}$, while the output voltage is around zero.

Fig 3.16 DC offset voltage the system can overcome

3.3 Discussion on CMRR

Differing from a general-purpose opamp, the instrumentation amplifier must be capable of rejecting common mode signals at rates of approximately -90dB [19]. Common clients for the instrumentation amplifier marked are signal conditioners for energy-supply plants and biopotential measurements. Both cases are examples in which common-mode signals are so much higher than the signal to be measured that they may jeopardizes the whole signal measuring process, unless measures are taken to reject them. So it is necessary for us to consider how to optimize the CMRR of the circuits. This is exactly the role that the instrumentation amplifier must play.

We divide the analysis of the CMRR into two groups. The first one is the systematic CMRR of the circuit which restrict the CMRR for the sake of topology. Another one is the reduction of the CMRR due to the mismatches caused by the DC electrode offset.

The systematic CMRR is not finite unless the instrumentation amplifier is fully-differential. We can analyze the CMRR from the current-feedback model shown

in Fig 3.3.1. If the transistors are perfectly matched, the common-mode gain of the transconductance is:

$$A_{cm} = \frac{I_1}{V_{in}} = \frac{g_{ds,M5} g_{ds,I1} (2g_1 + g_{m,M1})}{2g_{m,M1} g_{m,M3}} \quad (3-3-1)$$

where $g_{ds,M5}$, $g_{ds,I1}$ are the output resistance of the transistors M_5 and current source I_1 and $g_{m,M1}$ and $g_{m,M3}$ are the transconductance of transistor M_1 and M_3

The same as the transconductance stage, the differential gain of the transisresistance stage is:

$$A_{diff} = \frac{1}{2g_2} \quad (3-3-2)$$

Combining equation (3-3-1) and (3-3-2) with the differential gain of the current feedback amplifier, we got:

$$CMRR_{struct} = \frac{2g_{m,M1} g_{m,M3} g_1}{g_{ds,M5} g_{ds,I1} (2g_1 + g_{m,M1})} \quad (3-3-3)$$

Equation (3-3-3) states that we can decrease the resistor R_1 in first stage or increase the transconductance of the input transistors to increase the CMRR of the instrumentation amplifier. In addition, the output resistance of currents source I_1 - I_6 should also be as high as possible, which has been demonstrated by [19]. The CMRR we derived is just an ideal condition. In realty, it is further reduced by other mismatches.

Though the transistors are perfectly matched, the DC offset induced by electrodes also bring the operating mismatches. If the common-mode gain of the first stage is ultra small, mismatches can still be divided into two parts:

First one is the V_{gs} mismatch of the input transistors. Because the current feedback topology forces the input pair transistors to operate at the same DC current, V_{gs} of the two input transistors are the same. In this way, any DC offset of the electrode will create a mismatch at the source voltages of the input transistors thus a mismatch of the output transconductance of these two transistors. It can be concluded that CMRR caused by this kind of mismatch is:

$$CMRR_{in} = \frac{g_{m,M1}}{I_{ds}} \frac{V_E^2}{(1 + g_1 / g_{mi}) \Delta V_{in}} \frac{1}{\Delta V_{in}} \quad (3-3-4)$$

three mechanisms just discussed.

$$\frac{1}{CMRR_{all}} = \frac{1}{CMRR_{struct}} + \frac{1}{CMRR_{iout}} + \frac{1}{CMRR_{in}} \quad (3-3-6)$$

where $CMRR_{all}$ is the total equivalent CMRR, $CMRR_{struct}$ is the maximum CMRR defined by system topology, $CMRR_{iout}$ is the maximum CMRR restricted by the limited output resistance of current source I_5 and I_6 and $CMRR_{in}$ is the maximum CMRR restricted by the V_{ds} difference induced by DC input offset at transistor M_1 and M_2 .

The topology in Figure 3.17 is fully differential, so $CMRR_{struct}$ is close to infinity, the first item in equation (3-3-6) can be ignored. For the second item, we increase the output resistance of current source to optimize $CMRR_{iout}$. In order to get greater output resistance than cascade current source, we adopt active current source. Replacing transistor M_{15} and M_{16} with current source in Figure 3.18 gives an output resistance:

$$R_{out} = (r_{o, Mc1} * g_{Mc2} * r_{o, Mc2}) * A \quad (3-3-7)$$

which is A times greater than that of cascade current source (A is the gain of the amplifier). Greater output resistance means greater $CMRR_{iout}$.

Fig 3.18 Active current source

For the third item in equation(3-3-6), we introduce a dedicated input stage to overcome the V_{ds} difference between M_1 and M_2 . Assuming M_{i1}, M_{i2} and M_{i3} in Figure 3.19 all work in saturation region with fixed current, the V_{gs} of these three

transistors will be constant. Obviously, V_{ds} of M_{i1} is the difference of other two transistors, i.e. $V_{gs,M_{i2}} - V_{gs,M_{i3}}$. So V_{ds} of M_{i1} does vary with input voltage at the gate of M_{i1} . Therefore, the introduction of the input stage assures the V_{ds} of input transistors no longer affected by dc offset, which dramatically increase $CMRR_{in}$.

Fig 3.19 Dedicated input stage

Fig.3.20 shows the simulated $CMRR$ of the HPCFA stage. The $CMRR$ is as high as 137dB, which is much greater than 90dB demanded by the clinical use [3].

Fig 3.20 Simulated $CMRR$ of HPCFA

Fig 3.21 shows the simulated $CMRR$ with different DC offset. It can be seen that even the DC offset voltage is as high as 50mV, the $CMRR$ of the HPCFA stage is still higher than 115dB, which is also much greater than 90dB demanded by clinical

document

Fig 3.21 CMRR changed with DC offset voltage

3.4 Discussion on input-referred noise

The input-referred noise of the system is another important issue we concern. Since the first stage has a gain of 10, the noise of the whole system is almost defined by this stage. We divide the circuit into two parts: the current feedback amplifier consists of M_1 - M_4 and equivalent Gm stage composed of M_5 - M_{18} . P_{IA} and P_{GM} are used to express the input-referred noise of these two parts. The systematic input-referred noise can be expressed as:

$$P_{ALL} = P_{IA} + P_{GM} * G_m * R_l \quad (3-4-1)$$

In terms of Gm stage, the equivalent input referred noise is filtered by its own transfer function Gm in the bio-potential frequency we interest (e.g. ECG signal from 0.5 Hz-150 Hz). Since the low-pass filter cut off frequency for the input referred noise of the GM stage is $g_m R_2$ times lower than the cut-off frequency of the instrumentation, the noise contributed by Gm stage is small enough to be omitted. In the designing process, we focus on the optimization of noise performance of the current feedback IA.

Using the small-signal half-circuit model to express noises of all transistors and

current sources, the equivalent input referred noise can be derived as:

Fig 3.22 Small signal noise analysis

$$\overline{V^2_{IA}} = \overline{V^2_{M1}} + \frac{1}{2} \overline{V^2_{R1}} + \frac{R_1^2}{R_2^2} \left(\overline{V^2_{M2}} + \frac{1}{2} \overline{V^2_{R2}} \right) + g_{mI5}^2 R_1^2 \overline{V^2_{I5}} + g_{mI3}^2 R_1^2 \overline{V^2_{I3}} + g_{mI1}^2 \left(R_1 + \frac{1}{g_{mM1}} \right)^2 \overline{V^2_{I1}} \quad (3-4-1)$$

Where g_{mI1} , g_{mI3} , g_{mI5} are the transconductance of current source I_1 , I_3 and I_5 . For $R_1/R_2 \gg 1$, equation 10 can be simplified to

$$\overline{V^2_{IA}} = \overline{V^2_{M1}} + \frac{1}{2} \overline{V^2_{R1}} + g_{mI5}^2 R_1^2 \overline{V^2_{I5}} + g_{mI3}^2 R_1^2 \overline{V^2_{I3}} + g_{mI1}^2 \left(R_1 + \frac{1}{g_{mM1}} \right)^2 \overline{V^2_{I1}} \quad (3-4-2)$$

Firstly, we consider thermal noise. For single transistors, thermal noise can be expressed as $4KT\gamma/g_m$. Equation(3-4-2) can be rewritten as:

$$\overline{V^2_{IA}} = 4KT \left[\frac{\gamma}{g_{mM1}} + \frac{1}{2} R_1 + \gamma R_1^2 g_{mI5} + \gamma R_1^2 g_{mI3} + \gamma g_{mI1} \left(R_1 + \frac{1}{g_{mM1}} \right)^2 \right] \quad (3-4-3)$$

Either increasing g_{mM1} or decreasing R_1 lower the input-referred noise. Transconductance g_{mM1} can be maximized when transistor M_1 works in sub-threshold region given the fixed current. However, for the resistor R_1 , it can not be reduced arbitrarily. Decreasing in R_1 will lead current caused by input dc offset to increase. If

current in Gm stage do not increase proportionally, dc offset the system can overcome will reduce. Raising the current can overcome this problem but sacrificing the consumption. So trade-off between dc offset and consumption should be taken into consideration when designing R_1 .

Since the $1/f$ noise is in inverse proportional to the gate area, we should enlarge the transistor as much as possible with the given die area. Of course, additional parasitic capacitor is worthwhile to be attention. When designing, more focus is put into the dimension of input transistor pair. Large W/L ratio PMOS transistor is used as input transistors. In this way, we get not only big gate area, but also big g_{mM1} for the input transistors work in sub-threshold region with the given current.

3.5 Design of VBGA stage

3.5.1 Implementation of VBGA stage

Because voltage gain of first stage is not big enough for weak bio-potential signal, we introduce second stage amplifier circuits [21]. In this stage, we design a variable gain and bandwidth amplifier, which is suitable for different amplitude and frequency bio-signals, like EMG and EEG signals. This stage also serves as a differential to single-end converter. It should be mentioned here, the low CMRR of this stage is not that important, since it is just used as a second stage in the system, and the CMRR is only set by the first stage. The amplifier architecture is shown in Fig 3.23

Fig 3.23 Architecture of VBGA stage

Fig 3.24 Circuit Implementation of VBGA stage

Amplifier composed of transistor M29—M39 is shown in Figure 3.24. Capacitor C1 and C2 form negative feedback circuit while resistor R sets the DC operating point. When $C_1, C_L \gg C_2$, gain of the circuit is decided by the ratio of C1 and C2:

$$A_v = \frac{C_1}{C_2} \quad (3-5-1)$$

The high cut-off frequency and low cut-off frequency are:

$$f_h = 1/(2\pi C_2 R) \quad (3-5-2)$$

$$f_l = g_m C_2 / 2\pi C_1 C_L \quad (3-5-3)$$

High cut-off frequency is as low as 1Hz. If C_2 is set as 1pF, the resistor R should be higher than $10^{11} \Omega$. Obviously, it is almost impossible to implement this resistor in-chip.

A pseudo-resistor made up by MOS-Bipolar devices can be a substitution for this resistor, as shown in Fig 3.24. We will give a detail explanation of the pseudo-resistor [21].

Fig 3.25 shows a negative biased PMOS transistor. Since $V_o > V_f$, the MOS transistor is turned on and the bipolar transistor is turned off. The devices functions as a diode-connected PMOS transistor.

Fig 3.25 Negative biased pseudo-resistor

For opposite polarity, the MOS transistor is turned off and the parasitic source–well–drain p-n-p bipolar junction transistor (BJT) is activated. The device acts as a diode-connected BJT.

Fig 3.26 Positive biased pseudo-resistor

So whenever V_{gs} is positive or negative, for small voltage across the pseudo-resistor, the current passing this device is ultra-low and its equivalent resistance is extremely high. Fig 3.27 shows the measured current-voltage relationship of MOS-bipolar relationship.

Fig 3.27 Current-voltage relationship of pseudo resistor

It is always that the magnitude of this resistor is greater than $10^{12} \Omega$. Fig 3.28 shows the measured resistance of the pseudo-resistor, which is out of the measurement scope.

Fig 3.28 Measured resistance of pseudo-resistor

C1 is designed as a configurable capacitor. To save area in the chip, we implement this capacitor with 10pF in the chip and 10 to 80pF off-the-chip. Off-the-chip capacitor is in parallel with the in-chip capacitor and can be adjusted by the switches externally.

High cut-off frequency relies on the C_L and transconductance of the OTA. For bio-potential signal extracted from human body is always in the magnitude of several hundred hertz, increasing C_L alone to lower the frequency consumes a large portion of the in-chip area. We utilize the change of transconductance to alter the bandwidth. Varying the gate voltage of transistor M_{39} leads to the alternation of OTA bias current, thus affecting transconductance G_m . Since G_m is in direct proportional to the current in transistor M_{39} , reducing in G_m makes the transconductance qualified for the amplifier. In addition, the power dissipation decreases.

3.5.2 Discussion on the noise of VBGA stage

Although the circuit topology of VBGA stage is a typical topology for driving capacitive loads, the sizing of the transistors is critical for such a low-power low noise

amplifier. Let us discuss how to optimize the noise performance of the amplifier.

The input transistor M29 and M30 are designed with the same sized, and we designate their transconductance as g_{m29} and their width-to-length ration as $(W/L)_{29}$. Similarly, transistors M31-M34 and M38 are the same size $(W/L)_{31}$ and have transconductance g_{m31} . The PMOS current sources M33 and M35 have size $(W/L)_{33}$ and transconductance g_{m33} .

The input referred thermal noise can be expressed as:

$$\overline{V_{in,thermal}} = \frac{16kT}{3g_{m29}} \left(1 + 2 \frac{g_{m31}}{g_{m29}} + \frac{g_{m33}}{g_{m29}} \right) \quad (3-5-4)$$

If we make the devices such that $g_{m31}, g_{m33} \ll g_{m29}$, we can minimize the noise contributions of transistors M31-M35 (and M38). This can be easily accomplished by making $(W/L)_{31}, (W/L)_{33} \ll (W/L)_{29}$. In this way, the transistors M31-M35 (and M38) are pushed into strong inversion. By operating M29 and M30 in the subthreshold region, we achieve a relatively high g_{m29} , which is much greater than g_{m31}, g_{m33} .

However, we can not decrease g_{m31} and g_{m33} arbitrarily without danger of instability. If the total capacitance seen by the gate of M31(or M32) is designated as C_{31} , then the OTA has two poles at g_{m31}/C_{31} . In the same way, there is a pole at g_{m33}/C_{33} caused by the PMOS current sources. To ensure stability, these poles must be several times greater than the dominant pole, g_{m29}/C_L (C_L is the equivalent load capacitance). This demands becomes easier to meet if only C_L is made larger, so it is a must to consider area limitations and bandwidth requirements. In the VBGA stage, we decrease $(W/L)_{31}, (W/L)_{33}$ as much as possible to make a trade of between phase margin and lower input-referred noise. We designed out amplifier to have a phase margin of 52° . Transistors M31-M35 (and M38) are narrow devices that require relative large gate overdrive voltage, so output signal swing or finite power-supply voltages still limit the designer's ability to decrease gm.

Flicker noise is another major concern for such a VBGA stage. The same as in the HPCFA stage, we minimize the effects of the flicker noise by using PMOS transistors as input devices or by using devices with large gate areas. Flicker noise in PMOS transistors is always one to two orders of magnitude lower than flicker noise in NMOS transistors. All transistors should be made as large as possible to minimize $1/f$ noise. However, when devices M31-M35 (and M38) are made larger, C_{31} and C_{33}

increase, leading a reduce in phase margin again. When M1 and M2 are made larger, the input capacitance C_{in} increases. The input-referred noise of the VBGA stage can be related to the OTA input-referred noise by:

$$\overline{V^2_{in,VBGA}} = \left(\frac{C_1 + C_2 + C_{in}}{C_1} \right)^2 \overline{V^2_{ota}} \quad (3-5-5)$$

Where C_1 and C_2 are the feedback network capacitors shown in Fig 3.24. Since C_{in} contributes to the capacitive divider that attenuates the input signal, any increase in C_{in} increase the input referred noise of the overall circuit. An optimum gate area for M1 and M2 can be found to minimize the flicker noise.

3.6 Simulation of the analog front-end

We have done several simulations of the analog front-end. We shows some simulations results here.

(1) Transient Simulation

The ECG stimulating signal is generated by MATLAB codes. Meanwhile, we add a 500mV common-mode interference and 50mV DC offset voltage to imitate the real testing conditions. Fig 3.29 shows the testing circuits we simulated. Fig 3.30 shows the simulated results. It can be seen that the interference can be effectively reduced. The P,Q,R,S,T of the ECG signal can be clearly displayed.

Fig 3.29 Testing circuits simulated

Fig 3.30 Simulated ECG signal after amplification

(2) AC response of different gain

(a) Varying the gain of the front-end from *100. We give 4 simulations results here: *100, *200, *300, *400, as shown in Fig 3.31.

(b) Varying the bandwidth of the front-end, as shown in Fig 3.32.

Fig 3.31 AC response of different gain

Fig 3.32 AC response of different bandwidth

Chapter 4 Layout and Testing of the Front-end

In this chapter, we will discuss some important points in the layout designing of such an analog front-end circuits. Also, how to implement the PCB board for testing is also introduced. Finally, we will give the testing results of the analog front-end, including some problems encountered in the process of testing and modifications for future work.

4.1 Layout Design

In addition to the circuit design, front-end layout design plays an even more important role in the success implementation of the front-end circuits. Since the parasitic capacitor, line resistance, noise, offset and mismatch dramatically affect the post-layout simulation, thus the final performance of the chip. We will discuss some critical points in designing such an analog front-end for ambulatory applications.

4.1.1 Analysis of the parasitic resistor and capacitor

In the process of layout design, the parasitic resistors are often induced by metal lines and via contacts. Normally, the resistances of metal lines are small, only about 0.5 ohms per unit area, while the contact resistance between first layer metals and gates is 10ohms. The parasitic resistance can be reduced by increasing the width of metal lines and paralleling via contacts. Since there are a lot of via contacts in the layout design, the parasitic resistance it induced still affects the overall resistance of the whole system.

Parasitic capacitors are induced among multiple metal lines and between metal lines and transistor gates. The parasitic capacitor of unit metal lines is in the magnitude of fF. This can be effectively reduced by the length and width of metal lines. But in the layout design, it is not inevitably to use many long metal lines, thus increased some capacitor load.

The combination of parasitic capacitors and resistors affects the performance of layout circuits. For sampling circuits, considering the circuits shown in Fig xx. It is clear that the parasitic resistor R_{pa} and parasitic C_{pa} affect the RC bandwidth. In terms of high frequency signals, the parasitic components affect the accuracy and speed of sampling circuits.

Fig 4.1 Effects of parasitic capacitors and resistors

For an amplifier, the new pole is:

$$\omega = \frac{1}{2\pi \cdot (R + R_{pa}) \cdot (C + C_{pa})} \quad (4-1-1)$$

Therefore, the parasitic effects affect the position of poles. In addition, the parasitic resistance affects the position of zeros. For miller-compensation twp-stage amplifiers, the change of poles and zeros make the amplifiers not be wholly compensated. In this way the frequency response is not that good, thus decrease the settling speed and linearity error.

Additionally, parasitic resistances and capacitors also deteriorate the matching of fully differential circuits. For such analog front-end circuits, the CMRR highly depends on the matching.

4.1.2 Analysis of symmetry

In the designing of analog circuits, the fully differential circuits that can overcome the mismatch and offset are widely used. Therefore, when drawing the layout, the matching of negative and positive half-circuits is the most important.

Consider the following aspects for symmetrical circuits: (1) the symmetry of signal path (2) the symmetry of vias (3) the symmetry of input and load transistors. (4) the symmetry of capacitors.

The symmetry of signal path mainly decides the parasitic capacitors while the symmetry of vias defines the parasitic resistors. If the parasitic capacitors and vias are not that symmetrical, a deviation of poles and zeros happens. This makes the speed and accuracy of positive and negative sides of the circuits different, thus dramatically influence the performance.

The input and load transistors also demand matching. The mismatch of these

critical transistors causes the variance of g_m and r_o , also the gain and settling accuracy. For MOS transistors, we always introduce cross-quading techniques. For example, if M1 and M2 are the critical input transistors of the amplifier (shown in Fig 4.2), this kind of configuration makes these two transistors both affected by undesired effects of the process instead of only one transistors. Therefore, the matching of these two transistors is highly improved.

The symmetry of capacitors is another important issue we must concern. All the capacitors we draw in the layout are configured in the way shown in Fig 4.3. We not only introduce the cross-quading technique, but also implement dummy capacitors around the capacitors we need. These additional capacitors assure the environment around the capacitors is the same, which can also increase the matching of the capacitors.

Fig 4.2 Matching of transistors with cross-quading

Fig 4.3 Cross-quading capacitors with dummy configuration

4.1.3 Isolation and shielding

In such an ambulatory biopotential system, the amplified analog signal must be digitized before further processing. Therefore, when ADC is introduced in the whole system, the digital signal in the chip interfere the weak analog signal through substrate coupling or crosstalk.

To prevent this noise, we use two means in the layout designing: (1) We implement a NPN guard ring around the analog part and digital part. Meanwhile the analog part and digital part should keep enough distance. (2) Shield the sensitive analog signal path to make it escape from the near interference. Another way is to wrap the interference source; we can implement a bottom and top ground plane around it. For example, we use multiple metal planes to wrap the input signal path, which is the most important signal path for this layout design, as can be shown in Fig 4.4

Fig 4.4 A 360 degree wrap up of input signal path

4.2 Layout Implementation

According to the important points we have just mentioned the in previous part, we configure every part of the layout shown in Fig 4.5.

Fig 4.5 Component configuration on the layout

The analog front-end has been realized under SMIC 0.18 μm process. The die micrograph of the chip consumes an area of 1630*974 μm^2 , as shown in Fig 4.6.

Fig 4.6 Die micrograph of the chip

Fig 4.7 shows the implemented chip that has been bonded on the PCB.

Fig 4.7 Implemented chip bonded on the PCB

The chip we designed has around 28 pins. We give a pin summary here to explain the function of every pin.

Fig 4.8 Pin summary of the chip

VINN	Positive differential input
VINP	Negative differential input
CEXT1,CEXT2	External capacitor
VDD	Power supply
VDD_PAD_A33	Pad power supply
ITOP_CTRL	Bandwidth control of 1 st stage
VOUTP	Positive output of 1 st stage
CP	Parallel capacitor of 2 nd stage
VOUTP	Positive output of 1 st stage
CN	Parallel capacitor of 2 nd stage
VOUTN	Negative output of 1 st stage
VOUT2	Output of 2 nd stage
BUFFER_CTRL	Bias of output buffer
GND_PAD_A33	Pad ground
VDC	Output DC voltage ctrl
AGND	Ground of the whole system
IIN	Injected current
VCM	Common mode feedback voltage
V12	1.2V DC bias
R_CTRL	Equivalent resistance ctrl of 1 st stage
V18	1.8V DC bias

4.3 Chip Testing

The testing of the analog front-end circuits includes not only the testing parameters of normal amplifier but also the measuring of biopotential signals like the real clinical use. For the testing environment constrains, we are not able to test EEG and EMG signals, we just try out best to test the ECG signals.

The testing scheme is shown in Fig 4.9. The input signal is generated by Audio Precision 2700 (AP2700) and the DC voltage supply is HP6224A. The output signal is sampled by Spectrum Analyzer or oscilloscope.

Fig 4.9 Testing schemes of the chip

4.3.1 Bias circuits

The voltage directly supplied by HP6224A is not that good, so we use addition voltage and current supply chip to offer a DC bias for the testing chip. The current and voltage supply is high-resistive to the exterior interference, thus offer a stable operating point for the interior testing chip.

(1) DC voltage supply

The MIC49150 is a high-bandwidth, low-dropout, 1.5A voltage regulator ideal for powering core voltages of low-power microprocessors, shown in Fig 4.10. The MIC49150 implements a dual supply configuration allowing for very low output impedance and very fast transient response. The MIC49150 requires a bias input supply and a main input supply, allowing for ultra-low input voltages on the main supply rail. The input supply operates from 1.4V to 6.5V and the bias supply requires between 3V and 6.5V for proper operation. The MIC49150 offers fixed output voltages from 0.9V to 1.8V and adjustable output voltages down to 0.9V.

The MIC49150 is configured shown in Fig 4.11. R_1 is a variable resistor to adjust the output voltage. C_0 - C_5 are decoupling capacitors and L_0 is a decoupling inductor, which are used to filter the unwanted signals.

Fig 4.10 Package of MIC49510

Fig 4.11 Circuit configuration for MIC19510

(2)DC current supply

The LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V, as shown in Fig 4.12. Current is established with one external resistor and no other parts are required. Initial current accuracy is $\pm 3\%$. The LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The LM334 is configured shown in Fig 4.13. Res_v1 and Res_v2 are variable resistors with dip J1 and J2 to adjust the injected current. In the testing schemes, we adjust it offer a current of 10uA with 3% accuracy, which is enough good for testing. Dip J3 can bypass the injected current to test the magnitude of the current.

Fig 4.12 Package of LM334

Fig 4.13 Circuit configuration for LM334

4.3.2 Designing of PCB board

The PCB board itself is a mixed signal circuits. In the designing process, though the chip we design does not work in a high-speed environment, there are still some critical principles we should conform to:

- (1) All the bypass capacitors should be placed near the devices. Use the surface mounted components as many as possible. Shorten the metal wires to decrease the parasitic capacitors.
- (2) Using a 0.1uF and 10uF to bypass the components.
- (3) Using multiple layer PCB boards to assure the integrity of signals.
- (4) The critical signal path should be placed in a symmetrical way to ensure high matching characteristics.
- (5) All the metal wires should be rounded, with no abrupt turns.

The implemented PCB is shown in Fig 4.14.

Fig 4.14 Implemented PCB

4.4 Measurement results

4.4.1 Transient test

A 100Hz 2mV V_{pp} input signal is generated by AP2700. The gain of the analog front-end is set to be 300(49.5dB). It can be shown the amplitude of the output signal is 600mV.

Fig 4.15 Transient response of a sinusoidal signal

4.4.2 AC response

An ac sweep signal from 0.1Hz to 10000Hz is generated by the AP2700. The output signal is also captured by AP2700. With the data manipulated by MATLAB, we can get one AC response curve for one gain configuration. Fig 4.16 shows four measured AC response with four different gains: 45.95dB, 51.38dB, 54.29dB, and 61.11dB. Additional gain could be achieved by continuously changing the VR of the HPCFA stage and external capacitor of the VBGA stage.

Fig 4.16 Measured variable gain of the front-end

Another ac response test is accomplished by changing C_{ext} of the HPCFA stage and gate voltage of M_{39} transistor in VBGA stage. The measured results clearly show that the bandwidth of the front-end can be varied in the following scope: 0.48-33.3Hz, 0.48-131.8Hz, 0.48-302Hz, 0.48-900Hz, 7-524Hz.

Fig 4.17 Measured variable bandwidth of the front-end

The bandwidth of the amplifier can be as low as 0.48Hz and as high as 2000Hz. Table 4.2.2 gives a spectrum scope of some widely used biopotential signals.

Application	Bandwidth
EEG	0.5-40Hz
ECG	0.5-150Hz
EMG	14-350Hz

Table 4.2.2 Spectrum of some widely used biopotential signals

We can find the bandwidth of the front-end includes the spectrums of ECG, EEG, EMG and EOG signals.

4.4.3 Performance summary and comparison

Table 4.4.3.1 gives the measured performance summary of the analog front-end. It should be mentioned here that for the testing conditions constrain, the CMRR and input-referred noise are just simulation results here. We will give a discussion on how to measure these two parameters in the next part.

Parameter	This work
Process	SMIC 0.18 μ m
Supply Voltage	3V
Power Consumption	32.1 μ W
Input referred noise	1.19 μ V _{rms} (0.48-2000Hz)
CMRR	137dB
High cut-off frequency (Changed by C _{ext})	>0.48Hz
Low cut-off frequency (Continuously tunable)	<2000Hz
Gain (Continuously tunable)	40-63dB

Table 4.4.3.1 Performance summary of the front-end

When comparing low-noise low-power amplifiers, NEF (noise efficiency factor) is always introduced to define the performance of an amplifier. The lower the NEF, the better the amplifier.

$$NEF = V_{in,rms} \sqrt{\frac{2I_{tot}}{\pi V_t 4kTB_w}} \quad (4-4-3-1)$$

After calculation, the NEF of this amplifier is around 2.97, which is the lowest among the references. (See table 4.4.3.2)

Process / μ m	Supply /V	Power / μ W	Input referred noise/ μ V _{rms}	NEF	CMRR /dB	Applications
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This work	0.18	3	32.1	1.19 (0.5Hz-2.5kHz)	2.97	153	ECG/EEG /EMG
Ref[21]	1.5	± 2.5	80	2.2 (0.5Hz-50kHz)	4.0	83	EEG
Ref[22]	0.5	± 1.5	485	0.86 (0.3Hz-150Hz)	N/A	117	ECG/EEG
Ref[23]	0.35	± 1.5	142	2.417 (0.3Hz-150Hz)	N/A	155	ECG/EEG /EMG
Ref[24]	1.5	± 1.7	27.2	3.6 (20-10kHz)	3.6	N/A	ECG/EEG/ ENAP

Table 4.4.3.2 Performance comparison of the front-end

4.5 Testing of ECG signals

We bought several electrodes and a 5-lead ECG measurement cables. Fig 4.18 shows the electrodes with gel on it. Fig 4.19 shows the 5 lead cables.(More details of the genesis and electrical event of the heart can be found in appendix)

Fig 4.18 Electrodes attached to the arms

Fig 4.19 5-lead ECG measurement cables

We used the right arm and left arm electrodes as the basic 3-lead ECG measurement schemes. Fig 4.20 shows the electrodes attached on the right arm and left arm.

Fig 4.20 Electrodes attached to the right arm and left arm

The 5-lead cables have a shielding layer around the signal path to protect the weak biopotential signals from the interference. The shielding layers are attached to the ground of the amplifier. Two input capacitors block the DC component of the input signals. The biopotential signal is ac-coupled to the input of the analog front-end. Two 1.5Mohm resistors are attached to 1.5V DC supply to offer a suitable DC operating point for the analog front-end. The detail circuit configuration is shown in Fig 4.21. The gain is set to be 60dB and the bandwidth is adjusted to 0.5Hz-150Hz.

Fig 4.21 Circuit configuration for ECG testing

When testing the output of the analog front-end, we do not get anything except noise. Instead of extracting ECG signal from human body, we use ECG simulator produced by Fudan biomedical engineering lab. The gain is set to be 52dB. The stimulator creates a 1mV V_{pp} ECG signals with artificial interference. The testing circuit is shown in Fig 4.22. It is not surprising that we successfully get the ECG signals. The gain is set to 52dB. The 50Hz interference is effectively reduced. All the P,

Q, R, S and T complexes are evident on the waveform, shown in Fig 4.23

Fig 4.22 ECG testing with ECG stimulator instead of human body

Fig 4.23 ECG waveform tested

A careful check of the comparison of these two testing schemes, we found where the problem is. The ECG simulator is indeed a combination of embedded system and a DA converter. The ECG signal with interference is stored in the embedded system with digital form. The output is analogized by the DA converter. The output impedance of the ECG stimulator is low compared to the input impedance of the analog front-end. Therefore, the ECG signal can be coupled to the front-end amplifier.

Fig 4.24 Blocks of ECG stimulator

On the country, when human body is attached, two resistors that connected to the 1.5V bias (which is around 1.5Mohm) make the input impedance of the analog front-end around 1.5M ohm. This impedance is too small compared the contact resistance of human body and electrode, which is always more than 10M ohms.

Fig 4.25 Analysis of error configuration of ECG testing circuits

We can modify the ECG testing circuits by two means. The first one is to implement a dual polarity voltage supply. In this way, we no longer need two resistors that offer the 1.5V voltage supply. The weak biopotential can be directly fed into the front-end circuits. The 0V input DC voltage can make the input transistors work in the saturation region. This is shown in Fig 4.26

Fig 4.26 Modified testing circuits without bias resistors

Another mean is to insert two buffers in front of the analog front-end. The buffers can couple the biopotential signals into the analog front-end with low output impedance. In this way, the two bias resistors are still big enough for the output resistance of the buffers.

Fig 4.27 Modified testing circuits with two output buffers

4.6 Discussion on the measurement of CMRR

The designed CMRR is higher than 120dB. It is a big problem how to measure such a high CMRR. According to some references, maybe we can try to test the CMRR in two ways:

(1) If the differential gain is set to 60dB, since the CMRR is more than 120dB, the common-mode gain is around -60dB. The spectrum analyzer is able to measure signals as low as -80dBm, maybe it is possible to measure the amplified common mode signal with the spectrum analyzer. But one thing should be considering here, the input impedance of the spectrum analyzer is about 50ohms. It is a must a buffer should be inserted at the output stages, or the rather big output impedance of the analog front-end will attenuate the weak common mode signals. The testing circuits is shown in Fig 4.28

Fig 4.28 One way to measure CMRR

(2) Another way to measure the CMRR which is more robust is shown in Fig 4.29 [25]. While the method can be used for dynamic characterization, we will use it from a static viewpoint. If all V_{set} voltages are increased by unit voltage, this will cause the output and power supply to the analog front-end (the black one in the Fig

xx) under test to be increased by unit voltage. As a result, a voltage V_i will appear at the input of the analog front-end. V_i is of the same magnitude of the common-mode unit voltage divided by the differential voltage gain of the front-end under test. This change can be measured by V_{os} , which is around $1000V_i$. If this value is designated as V_{os1} , doing the same thing, only to decrease the V_{set} by the same amount. This measure of V_{os} is designated as V_{os2} . The CMRR of the analog front end can be approximately as:

$$CMRR = 2000 / (V_{os1} - V_{os2}) \quad (4-6-1)$$

Fig 4.29 Another way to measure the CMRR of the front-end

Chapter 5 Conclusion and Future work

5.1 Conclusion

A continuously tunable gain and bandwidth analog front-end for ambulatory biopotential measurement system is presented in this paper.

Firstly, we give a brief introduction of the sources and characteristics of biopotential signals, especially for the ECG signals. The chemistry of the biopotential electrodes and the mechanisms behind the generation of the differential DC electrode offset voltages between the biopotential electrodes are also described. In addition, the interference theory is presented, describing the coupling of the common-mode signals from mains to the human-body that needs to be rejected by the analog front-end.

Then, we discuss different architectures of amplifier to implement such an analog front-end. The advantages and disadvantages are both compared. We propose a single 3V voltage supply analog front-end. The front-end is pure analog without interference from digital parts like chopping and switch capacitor circuits. The noise performance is not sacrificed by careful design of critical transistors. The system adopts only two stage amplifier architecture. The continuously gain and bandwidth achieved make the system better compatible with a variety of biopotential signals.

The critical points in the designing of layout are also presented. The chip is fabricated under SMIC 0.18 μ m CMOS process. Although the power consumption is only 32.1 μ W under 3V voltage supply, test results show that the chip can successfully extract biopotential signals.

Of course, there are still some problems in the testing process, like how to measure the ultra-high CMRR, ultra ultra-low noise of the chip, and how to get the ECG signals from human body. We give some use suggestions or maybe solutions in the last part of the whole paper.

5.2 Future work

Based on what we have achieved in this paper, the suggestions for future works are summarized as follows:

- (1) Redesigning a PCB board, either implementing a dual-polarity voltage supply or inserting a buffer before the input of the front-end. Retesting the ECG signals from human body and the ultra-high CMRR and ultra-low noise.
- (2) Reducing the power supply from 3V to 1.8V to further decrease the power

consumption of the front-end to make it better in performance.

- (3) Implementing an SAR architecture AD conversion behind the analog front-end to further digitize the signals for advanced processing.
- (4) Comparing the chip we design with the implemented commercial products.
- (5) Further medical validation is necessary especially on patients with disorders.

Appendix

Anatomy of Heart and Electrical Event of the Heart

Our heart is a muscular organ that acts like a pump continuously sending blood throughout our body [6]. The heart is at the center of the circulatory system, which is composed of blood vessels, such as arteries, veins and capillaries. Blood is carried in these vessels from and to all area of our body. An electrical system regulates our heart and contracts the heart's walls by means of electrical signals. Blood is pumped into our circulatory system when the walls contract. A system of inlet and outlet valves in our heart chambers work to ensure that blood flows in the right direction. Heart is important to our health and almost everything that goes on in our body. With the heart's pumping function, our blood carries the oxygen and nutrients to our organs to make it work properly. It also carries carbon dioxide to our lungs to be passed out of the body. If disease weakens our heart, it won't receive enough blood to work normally.

Fig A.1(a) shows the cross-section of our heart. It is divided into right side and left side by a septum. The heart has four chambers: a right atrium and ventricle and a left atrium and ventricle. It has four valves (the red dots in the figure) that regulate the flow of blood through the heart, its chambers and arteries.

The right side and left side of our heart work co-operationally to pump blood. The right side of our heart pumps blood from the heart to the lungs through the pulmonary artery. The left side of our heart pumps blood to other parts of our body through the aorta. This is shown in Fig A.1(b)

Fig A.1(a) Cross-section of our heart (b) Function of two sides of the heart

A pumping cycle begins when blood from our body that is now low in oxygen returns through the superior and inferior vena cava to fill our heart's right atrium.

When the right atrium is full with blood, it contracts, the tricuspid valve opens, and the blood is pumped into the right ventricle of our heart. This is called the atrial systole. When the right ventricle is full with blood, the tricuspid valve closes. This prevents blood from flowing back into the right atrium.

Fig A.2(a) Beginning of a pumping cycle (b) Atrial systole

When full with blood, our heart's right ventricle begins to contract. The pulmonary valve opens and blood is pumped into our pulmonary artery and on to our lungs. This is called ventricular systole. After that, the pulmonary valve quickly closes to prevent blood from flowing back into the right ventricle

Meanwhile, oxygen rich blood returns from the lungs through the right and left pulmonary veins and has fill our heart's left atrium.

Fig A.3(a) Ventricular systole (b) Left atrium filled with blood

Our heart's left atrium contracts, the mitral valve opens and blood is pumped into

the left ventricle. This occurs at the same time a new contraction is taking place in our heart's right atrium. When our heart's left ventricle is full with blood, the mitral valve closes. This prevents blood from flowing back into the left atrium.

When our heart's left ventricle contracts and the aortic valve between the left ventricle and aorta opens. The contraction pumps oxygen-rich blood into our aorta and onto the rest of our body. After that, the aortic valve quick closes to prevent blood from flowing back into the left ventricle. This occurs at the same time a new contraction is taking place in our heart's right ventricle. Meanwhile, our heart's atria have filled with blood and the cycle continues.

Fig A.4(a) Left atrium contracts (b) Left ventricle contracts and aortic valve opens

Our heart's electrical system controls all the events that happen when our hearts pump blood [7]. Each beat of our heart is set in motion by an electrical signal from within our heart muscle. The electrical activity is recorded by an electrocardiogram, known as ECG (or EKG), as shown in Fig B.1

FigB.1 Electrocardiogram that records our heart electrical activity

Each beat of our heart begins with an electrical signal from the sinoatrial node, also known as the SA nose. The SA node is located in our heart's right atrium. When

out heart's right atrium is full with blood, the electrical signal generated from SA node spreads across the cells of our heart's right and left atria. This signal causes the atria to contract or squeeze, shown in FigB.2 (a).

This pumps blood through the open valves from the atria into both ventricles. The P-wave on the EKG marks the contraction of our heart's atria, shown in FigB.2 (b).

Fig B.2 (a) Signal causes the atria to contract (b) P-wave on EKG

The signal arrives at the atrioventricular (AV) node near the ventricles. Here it is slowed for an instant to allow our heart's right and left ventricles to fill with blood. On and EKG, this interval is represented by the start of the line segment between the P and Q wave (marked in the FigB.3(a))

The signal is released and moves next to the bundle of His, which is located in our heart's ventricles. From the bundle of His, the signal fibers divide into left and right bundle branches, which run through out heart's septum. On the EKG, this is represented by the Q wave.

Fig B.3 (a) Line between P and Q wave (b) Q-wave on EKG

The signal leaves the left and right bundle branches through the Purkinje fibers that connect directly to the cells in the walls of our heart's ventricles. The signal spreads quickly across our heart's ventricles.

When the signal spreads across the cells of the ventricle walls, two ventricles contract simultaneously, but not at exactly the same moment. The left ventricle of our heart contracts an instant before the right ventricle. On EKG, the R wave marks the contraction of our heart's left ventricle and the S wave marks the contraction of our heart's right ventricle.

FigB.4 (a) Signal across ventricles (b) R-wave on EKG

The contraction of our heart's right ventricle pushes blood through the pulmonary valve to our lungs. The contraction of our heart's left ventricle pushes blood through the aortic valve to the rest of our body. As the signal passes, the walls of our heart's ventricles relax and await the next signal. On the EKG, the T wave marks the point at which our heart's ventricles are relaxing, shown in Fig. This process continues over and over.

Fig B.5 (a) T-wave on EKG (b) Repeat of the heart cycle

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