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Wire-bonded through-silicon vias with low capacitive substrate coupling

A C Fischer¹, M Grange², N Roxhed¹, R Weerasekera², D Pamunuwa²,
G Stemme¹ and F Niklaus¹

¹ KTH Royal Institute of Technology, Microsystem Technology Laboratory, School of Electrical Engineering, Osquldas väg 10, 100 44 Stockholm, Sweden

² Department of Engineering, Centre for Microsystems Engineering, Lancaster University, Lancaster LA1 4YW, UK

E-mail: andreas.fischer@ee.kth.se

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Abstract

Three-dimensional integration of electronics and/or MEMS-based transducers is an emerging technology that vertically interconnects stacked dies with through-silicon vias (TSVs). They enable the realization of circuits with shorter signal path lengths, smaller packages and lower parasitic capacitances, which results in higher performance and lower costs. This paper presents a novel technique for fabricating TSVs from bonded gold wires. The wires are embedded in a polymer, which acts both as an electrical insulator, resulting in low capacitive coupling toward the substrate and as a buffer for thermo-mechanical stress.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

In the past few years hybrid integration of IC and MEMS technology was dominated by 2D approaches, resulting in multi-chip modules (MCM), where different dies are integrated on a single substrate, and system-on-chip (SoC) solutions, where different functionalities are merged onto one die. CMOS and MEMS processing are both well-established and cost-efficient base technologies where each technology itself is typically characterized by short development times, low fabrication costs and high yields. Separate manufacturing of CMOS and MEMS chips and their integration to a system-in-package (SiP) in a final packaging step offer high versatility and low process costs, and thus is an attractive alternative to SoC solutions. In particular, 3D-integrated system-in-package (3D-SiP) solutions, which are based on vertical chip stacking, are a general trend in many integration approaches. Not only do 3D-SiPs decrease costs by reducing the volume and weight of the package, but they also improve system performance through enhanced signal transmission speed and lower power consumption, which is of importance for various demanding applications [1, 2]. This is due primarily to the shorter signal path lengths and lower capacitive, resistive and inductive parasitic components in the vias [3]. 3D-SiP implementations

require vertical interconnects through selected dies in the stack in order to connect their functional layers. Much development effort for the realization of reliable and cost-efficient TSVs is currently ongoing and the first commercially available devices such as MEMS inertial sensors and microphones, CMOS imagers and power LEDs successfully incorporate TSV technology [4–6].

The structure and hence the fabrication of TSVs can be roughly divided into three major elements: a dimensioned vertical hole through the substrate, a conductive core and a dielectric layer acting as an insulator between the conductor and the substrate. The exact design of the via and the fabrication process flow depends very much on the application.

Typical TSV diameters vary between a few microns [2, 9] and several hundreds of microns [12]. Basic via designs are either based on solid (figure 1(a)) or lined metallizations (figures 1(b) and (c)) as the vertical conductor. TSVs can have either straight (figure 1(b)) or tapered sidewall profiles (figure 1(c)) [7] as well as combinations of both [8]. Various methods for the formation of via holes exist and can be categorized into dry etching [1, 7–13], wet etching [8] and drilling processes [4]. The majority of TSVs have an aspect ratio between 1 and 10. The most common techniques and challenges for the fabrication of the main TSV structures are discussed in the following subsections.

Figure 1. Cross-sectional view of three common TSV designs. (a) Solid metal-filled TSV, (b) annular metal-lined TSV and (c) metal-lined TSV with tapered side wall profile.

1.1. Via holes

Deep reactive ion etching (DRIE) is by far the most commonly used technology to form the TSV hole. DRIE has an excellent process controllability and is capable of creating high aspect ratio vias (up to 110:1) with specific sidewall profiles and topographies. The etch rate of DRIE is aspect ratio dependent (ARDE) and may cause several topographic imperfections on the sidewalls such as scalloping, caused by alternating etch and passivation steps, which results in corrugated sidewalls. By using state-of-the-art DRIE equipment, these effects can be minimized [7] and adopted to the demands of subsequent insulation, barrier and seed-layer deposition steps.

Laser ablation is an emerging low-cost and high-speed process for drilling TSV holes, as it benefits from the absence of any lithographic process steps and is agnostic to different materials. This results in high process and design flexibility and thus lower overall costs compared to DRIE [4, 18]. Laser ablation, however, suffers from a high local thermal load, crystal defects and particle generation around the perimeter of the drilled via hole. Additional cleaning steps are therefore required and reliability issues may arise due to induced stress on pores and micro-cracks [19, 18].

1.2. Via insulator

Chemical vapor deposition (CVD) is a well-established CMOS process with moderate temperature requirements [1, 2, 7, 9] and is therefore the most commonly used method for a direct deposition of silicon dioxide or silicon nitride on the via sidewall. The use of organic dielectrics such as bisbenzocyclobutene (BCB) [11, 16], epoxy-based polymers [11, 12], silicone [11] or parylene [13] is becoming established as well. Polymers, especially low- k types with a lower relative permittivity compared to silicon dioxide, are very attractive for the realization of TSVs with improved electrical characteristics [12]. The relative permittivity of selected materials is listed in table 1. In addition, polymers can further act as a buffer for thermo-mechanical stress caused by coefficient of thermal expansion (CTE) mismatches [11, 14] as their Young's modulus is approximately two orders of magnitude lower as compared to silicon dioxide and silicon nitride.

1.3. Via conductor

The metallization step is the most critical and often most costly part of the via fabrication. Established processes are

Table 1. Relative permittivity of commonly used TSV insulation materials such as silicon nitride and oxide as well as emerging low- k insulators represented by the polymers benzocyclobutene (BCB) and the epoxy-based SU-8 and InterVia 8023.

Material	Relative permittivity ϵ_r
SiO ₂	3.9
Si ₃ N ₄	7
BCB 3000 series (Dow)	2.65 ^a
Parylene N	2.65 ^b
SU-8 2000 (Microchem)	3.2 ^c
InterVia 8023 (Dow)	3.2 ^d

^a 1–20 GHz. ^b 60 Hz–1 MHz. ^c at 10 MHz. ^d at 1 GHz.

electrodeposition of copper [8, 9, 11–14], CVD of tungsten [2], CVD of polysilicon [2, 7] and the use of low-resistivity silicon [10]. In particular, electrodeposition of copper, being a very well-established semiconductor process, is used by many research groups and implemented in most commercialized devices that contain TSVs. Electrodeposition of copper benefits from widely available tool vendor support and process maturity, as well as being amenable to processing at close to room temperature, but suffers due to its complexity in terms of process controllability, reliability and throughput [4]. In particular, high aspect ratio TSVs with void-free conductive metal cores are difficult to implement [9]. Alternative approaches to plating processes have therefore been investigated, such as filling with conductive metal pastes [1] as well as the use of solder balls [15] and the assembly of pre-fabricated wires [17].

Wire bonding is an extremely mature and cost-efficient back-end process for electrical interconnects due to its broad availability and high performance in terms of reliability and throughput. Wire-bonded stud-bumps can serve as an alternative to regular TSVs with low aspect ratios and have already been implemented in mass-produced devices such as CMOS image sensors [21]. The estimated cost per 100 000 stud-bumps is approximately 14 USD in high-volume production [20] and thus stud-bumping can be cost competitive to plating processes for applications with up to 100 000 I/Os per wafer. However, this method is restricted to via scenarios with low aspect ratios and thin via substrates as stud-bumps are comparably short.

Figure 2. CAD image with a cross-sectional illustration of the main elements of the wire-bonded TSV design. The metal core in the center of the via is a ball-bonded wire on a metal membrane and is surrounded by a polymer.

2. TSV design

The main novel feature of the presented TSV design is the metal core, which is wire bonded. Wire bonding easily enables the fabrication of high-quality and inherently void-free metal cores with high aspect ratios.

As depicted in figure 2, a wire is ball bonded to a metal membrane on the bottom of the via cavity. The remaining hollow space of the cavity is subsequently filled with a dielectric, which both acts as an insulator and provides mechanical support for the via core. Typical diameters of commercially available gold or copper wires used for ball/wedge-bonding are 12.5–50 μm . In order to be able to wire-bond at the bottom of the via cavity and to achieve a low capacitive coupling of the metal core to the substrate, a via hole diameter of 200 μm was chosen. Wire bonding on the bottom of via cavities with these dimensions requires special bond capillaries with reduced tip-diameters, which are commercially available and typically used for fine-pitch and deep-access wire-bonding applications.

For the proposed TSV design, the placement of the via metal core by wire bonding can take part prior to the application of the via insulation polymer. This is the opposite order as compared to most other TSV fabrication schemes where the via metal is gradually deposited after the via insulator. The proposed approach therefore does not require any additional high aspect ratio lithography and patterning of the insulation polymer.

3. TSV fabrication

The fabrication process for the TSVs is depicted in figure 3 and is based on 300 μm thick double-side polished 100 mm

Si substrates with a 2.5 μm thick silicon dioxide layer on both sides, which was created by thermal wet oxidation. The oxide acts both as a hard mask for the DRIE step and as an electrical insulator for the metal lines, which connect to the via on the front- and backside of the substrate. The oxide on the backside is initially thinned down to 400 nm by a wet blank buffered hydrofluoric acid (BHF) etch with front-side protection by a photoresist. A standard lithography and RIE process on the front side of the substrate removes the oxide and defines circular openings for the vias in the hardmask. An aluminum layer is sputtered on the unpatterned backside of the wafer (figure 3(b)). As the wire bonding will be later performed on a membrane of this layer, a thickness of 5 μm was chosen in order to withstand mechanical stresses during wire bonding. A Bosch DRIE process creates the via holes with straight side walls; the etch stops on the silicon oxide at the bottom of the cavity. A second blank BHF etch removes the thin layer of oxide on the aluminum membrane but not the thicker oxide layer on the front side of the substrate (figure 3(c)).

As depicted in figures 3(d) and 4, a bond capillary with a reduced tip-diameter for fine-pitch applications is used in order to be able to place the wire bond at the bottom of the cavity. The bond head moves down after the free-air-ball (FAB) formation by an electrical discharge. The ball bond is performed at room temperature with the help of force and ultrasonics. The bond head subsequently moves straight upward, generating a tail length of about 400 μm (figure 3(e)). A second electrical flame-off (EFO) cuts the wire on a spot above the upper substrate surface (figure 3(f)). This wire-bond sequence is repeated for every TSV and was performed with a semi-automatic wire bonder (Delvotec 5410) with a minor hardware modification in order to trigger a second EFO.

The via cavities are subsequently filled with the thermosetting polymer BCB CYCLOTENE[®] 3022-46 (figure 3(g)). In order to reduce the viscosity of the polymer, the substrate is placed on a hotplate with a temperature of 60 °C before the polymer is manually applied with a syringe. As the polymer is not spin-coated, the resulting polymer layer has a non-uniform thickness of the order of 100–150 μm . The subsequent hard-curing of the BCB is performed on a hotplate using the temperature profile according to the manufacturer's standard process procedures [22]. The curing procedure was performed in a vacuum environment at 0.02 mbar in order to prevent any void formation in the polymer. A grinding and polishing step of the front side removes the remaining gold of the bond wire and the BCB from the surface of the substrate (figure 3(h)). A final aluminum deposition on the front side contacts the gold core of the via. The lithographically defined patterning of both aluminum layers forms the signal lines leading to the TSV (figure 3(i)).

4. Experimental results

The wire-bonding and filling processes are the most crucial steps in the presented fabrication scheme and have therefore been extensively investigated. The wire-bonding process on a thin metal membrane has been developed with a set of bond

Figure 3. The fabrication scheme can be divided into three major tasks. First is the formation of the via hole by DRIE etching, second is the wire bonding of the conductive TSV core and last is the filling with the polymer.

Figure 4. Photograph of a fine-pitch bond capillary (SPT Roth Ltd, Switzerland) equipped with a 25 μm gold wire. Inset: magnification of the capillary tip, bond wire and free-air-ball (FAB), which is generated by an EFO. The free-air-ball is pulled up to the end of the capillary by a wire tensioning system prior to the ball bond, as shown in figure 3(d).

parameters optimized for room temperature conditions, low bond force and moderate ultrasonic power.

The formation of truncated bond wires with the help of a second flame-off showed the best results in terms of the straightness of the wire and overall process reliability. Other evaluated methods such as tearing the wire or cutting the wire with a micro-scissor had less successful outcomes.

The position of the ball bond on the Al membrane can be slightly off-center due to manual alignment of the bond position (figures 5 and 6). However, the risk for a short circuit between the silicon substrate and the gold wire, caused for example by a crooked wire that touches the silicon sidewall,

Figure 5. SEM image with tilted view on a 200 μm wide via cavity and a bonded Au wire with a diameter of 25 μm prior to the filling with BCB.

is minimal. This is due to a clearly defined movement of the bondhead and the fact that the via diameter is about an order of magnitude larger compared to the gold wire diameter. In addition, the conical shape of the bond capillary prevents a wire placement that is too close to the silicon sidewalls of the via, as depicted in figure 3(d). The manual alignment of the bond position with the used wire-bonding tool causes both the displacement of the ball-bond position and a comparable long process time of several tens of seconds per TSV. Both problems can be addressed by using fully automated wire bonders. State-of-the-art wire bonders offer high speed (typically 20 bonds s^{-1}) and high precision placement (typically $\pm 2 \mu\text{m}$) of the bond with the help of pattern recognition systems.

Figure 6. Tilted SEM images with a cross section of the bottom features of a finalized TSV. The cross-sectional opening was realized by FIB milling. (a) Backside of the substrate prior to the FIB milling. An imprint of the ball bond, which was performed on the other side of the membrane, is visible. (b) Cross section of the bonded wire with its features. (c) Close-up of the ball bond facing the Al membrane. The shrinkage of the BCB filling leads to a partial delamination of the Au/BCB interface.

Using gold as a conductor can be critical for certain components, such as CMOS-based integrated circuits, if the gold diffuses into the silicon. A barrier layer deposition on the sidewall of the via subsequently to the via hole formation prevents the diffusion of gold from the bond wire to the substrate for such components.

Void-free dielectric filling with BCB and its characteristics have been investigated with the help of focused ion beam (FIB) milling and subsequent inspection with a scanning electron microscope (SEM). The BCB filling did not show any visible air voids or defects after the complete hard curing procedure. However, a partial delamination at the Au/BCB interface, as shown in figure 6(c), was observed. In addition, a slight deformation of the aluminum membrane occurred. Both the delamination and the membrane deformation are likely to be caused by the shrinkage of the polymer during the curing process. The topography of the membrane was evaluated with an optical surface profilometer and showed a peak valley depth of about 10 μm . There was no visible damage such as cracks or holes in the membrane visible, which is an important criterion for potential hermeticity of the via structure.

4.1. Electrical characterization

A basic electrical characterization of six TSVs with a height of 300 μm and a Au core diameter of 25 μm was performed with a 4-point probe station and a digital multimeter. The measurements showed an average value of 86 m Ω for the via structure and its contact metallization on either side. Based on the proposed TSV design, other electrical characteristics have been simulated and are discussed in the following section.

Figure 7. Parasitic R and L extracted from field solver simulations of an isolated wire-bonded via for increasing via diameter compared to a conventional cylindrical copper TSV with a SiO_2 insulator thickness of 0.2 μm . Height = 300 μm , BCB diameter = 100 μm .

5. Parasitic extraction through simulation

The wire-bonded via structures are simulated in a quasi-static 3D electromagnetic field solver (Ansoft Q3D) in order to extract the parasitic resistance (R), capacitance (C) and inductance (L) for a range of geometries. The substrate permittivity is chosen to be 10 S m^{-1} for all cases. In order to be able to compare between technologies, a conventional TSV with similar dimensions but with a 0.2 μm thick SiO_2 insulator serves as a reference [24]. The wire-bonded Au vias are modeled without any front- and backside contact metallization layers but include the ball-bonded features, BCB filling, silicon substrate and oxide layers on both front- and backside. The contact metallization will add an additional capacitance to the via structure, but is specific to the design layout. Our simulations comprise sweeps of the physical dimensions of the vias to cover a wide range of the possible dimensions under realistic design constraints. Vias are simulated with heights of 50–750 μm , bond wire diameters of 15–50 μm , BCB diameters of 100–400 μm and center-to-center via pitches between 50 and 1000 μm . The complex geometry of the flattened ball bond as depicted in figure 2 has also been modeled, with the diameter of the compressed ball bond assumed to be three times the core diameter and the height to be 0.4 times the ball diameter.

Shown in figure 7 are the resistance and inductance of an isolated via for an increasing core diameter from 15 to 50 μm , and a fixed height of 300 μm . The small difference between resistance and inductance in the two types of vias is a result of the ball structure at the wire-to-substrate interface, which is required by the bonding process and results in a slightly non-cylindrical shape. In either case, the resistance and inductance are negligible for digital applications when compared to the output impedance of a CMOS driver, which is typically of the order of k Ω . The resistive and inductive parasitics inherent in both the wire-bonded and the conventional TSVs are favorable compared to long on-chip wires found in large

Figure 8. The simulated frequency dependence of the resistance and inductance of a single wire-bonded via between 100 MHz and 50 GHz. Core diameter = 25 μm , BCB diameter = 100 μm .

SoCs and off-chip wire bonds and traces for other multi-chip packages. This is mainly due to the short length and relatively large diameter of the vias. Conventional wire bonds for I/Os, which are of the order of mm in length, exhibit much higher parasitic inductance for example.

The parasitics of a single 25 μm diameter, 300 μm length wire-bonded via at a frequency range between 100 MHz and 50 GHz have also been extracted. The skin effect can cause a significant variation in the inductance and resistance of interconnect structures, particularly in I/O bond wires for IC packages. However, in the through-silicon wire-bonded vias the DC parasitics are relatively low due to shorter lengths (spanning a range of tens to hundreds of microns) compared to the millimeter lengths typical of I/O package bond wires. The frequency sweep is shown in figure 8. The inductance only shows a deviation of less than 5 pH but the resistance changes from 40 m Ω at DC to 250 m Ω at 50 GHz. For digital signaling, the change in resistance is still negligible but it must be considered for other applications.

In figure 9, we extract the parasitic capacitance of an isolated wire-bonded via for the same core radius as in figure 7 but for increasing height in isolation. The wire-bonded capacitance is again compared to a cylindrical via of equal height and core diameter with an SiO₂ barrier thickness of 0.2 μm , representing a conventional TSV process. The self-capacitance of the wire-bonded via is at least an order of magnitude less than the conventional TSV, which is a result of the larger dielectric barrier (BCB filling). Decreased capacitance results in smaller signal delays and reduced power in the interconnect.

To observe the effect of the BCB layer on the substrate coupling, the BCB diameter has been simulated from 1 μm , beyond the edge of the wire-bond ball (minimum distance) to a diameter of 500 μm . For this case, the wire-bond core diameter was fixed at 25 μm . The change in capacitance is minimal (see figure 10), such that the minimum pitch afforded by the wire bonder is the deciding factor in the BCB barrier thickness. The minor deviations of individual data points

Figure 9. Simulated isolated wire-bonded via C parasitics for increasing via length as compared to a conventional cylindrical TSV with a SiO₂ barrier thickness of 0.2 μm . Core diameter = 25 μm , BCB diameter = 100 μm .

Figure 10. Field solver extracted capacitance for an isolated wire-bonded via as the BCB barrier is increased from a thickness of 1 μm to a diameter of 500 μm . Core diameter = 25 μm , via length = 300 μm .

from the trend are a result of the simulation approaching finite-element meshing limits for the chosen geometry. As previously mentioned, there will be an additional capacitance from the metallization layers to provide via connectivity to the rest of the circuit; however, this will be relatively small and will be present for any through-silicon via (TSV) technology.

5.1. Crosstalk from coupled via structures

Most applications require two or more TSVs in close proximity to one other, when coupling effects are prevalent. To quantify the effect on signal integrity, the self- and coupling parasitics for vias of varying geometries and pitches have been

Figure 11. The electrical equivalent circuit for the simulation setup. A row of three wire-bonded vias is simulated and the relevant RLC parasitics, including capacitive and inductive coupling between vias, are extracted to represent a number of vias in a row.

extracted. The inductance and capacitance terms include the self-capacitance of the vias and the mutual coupling components to the neighbors. The higher density of more mature conventional TSV processes can result in increased coupling between neighboring vias in a row and an $n \times n$ bundle as documented by the authors in [23]. This is less of an issue with the wire-bonded technology due to the larger pitches and thicker insulation barriers; however, the coupling components between vias are still important for matching of driver impedances to interconnect characteristics.

A row of three vias, which is a representative unit of any number of vias in a row (see figure 11), has been simulated. The capacitive and inductive coupling between the center (victim) via and the two neighbors (aggressors) represent the principal parasitic components for a row structure. Capacitive coupling to non-adjacent vias is vanishingly small due to shielding, while the inductive coupling is significant between all three vias. Using this characteristic behavior, we can model N number of vias in a row by using the parasitics extracted from the three coupled structures. The total capacitance includes the capacitive coupling to both neighbors in addition to the self-capacitance of the center via. The coupling capacitance includes only the capacitance shared between the center via and a single neighbor.

Figure 12 plots the capacitance and inductance of the middle via including the coupling between a neighbor. As the pitch increases, the total capacitance of the via marginally increases, while the coupling slightly decreases with larger pitches. It is evident from this plot that the capacitive coupling to the neighboring vias does not change much as a result of the spacing. The larger BCB surrounding (as compared to a cylindrical TSV with $0.2 \mu\text{m}$, SiO_2 barrier) has a significant effect on dampening the capacitive coupling between the structures. This is particularly beneficial for signal integrity and allows more freedom in the placing of the vias.

The parasitic extraction simulations have been performed to outline general trends in the wire-bonded structures for a range of realistic geometries expected in a typical application using a via of this type. The wire-bonded vias exhibit favorable electrical characteristics, where resistance and self-inductance are similar to the conventional TSVs but the capacitance is over an order of magnitude lower. The relatively small parasitics

Figure 12. Simulated total capacitance of the via and coupling capacitance of two neighboring vias in a row as spacing is increased between the wire-bonded structures. Core diameter = $25 \mu\text{m}$, BCB diameter = $100 \mu\text{m}$. Shown is the capacitive and inductive coupling between the center via and a single neighbor.

of the wire-bonded TSV as compared to long on-chip wires or other multi-package I/O structures and traces can enable fast data rates at lower power with improved signal integrity as a result of the reduced coupling between the vias.

6. Discussion and conclusions

We have demonstrated a proof of concept for the fabrication of through-wafer TSVs with an aspect ratio of 1.5 by wire bonding. Smaller TSV diameters and higher aspect ratios are feasible but limited by the wire-bonding process. The usage of bond capillaries with smaller tip-diameters and/or thinner substrates should enable via diameters down to $100 \mu\text{m}$. The concept is therefore suitable for applications with a comparatively low via density and large TSV pitch. However, superior electrical characteristics in terms of low capacitive substrate coupling of the presented approach enable the utilization of TSVs for demanding applications with the requirement for low capacitive coupling, such as the heterogeneous integration of capacitive MEMS sensors and IC technology for example. The presented approach utilizes exclusively well-established standard processes and is therefore suitable for mass production. The presented metal core placement technology by wire bonding should be cost competitive depending on the volume for applications with less than 100 000 vias per wafer.

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