FABRICATION OF HIGH ASPECT RATIO THROUGH SILICON VIAS (TSVs) BY MAGNETIC ASSEMBLY OF NICKEL WIRES

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ABSTRACT

Three-dimensional (3D) integration of electronics and/or MEMS-based transducers is an emerging technology that vertically interconnects stacked dies using through silicon vias (TSVs). They enable the realization of devices with shorter signal lengths, smaller packages and lower parasitic capacitances, which can result in higher performance and lower costs of the system. This paper presents a novel low-cost fabrication technique for solid metal-filled TSVs using nickel wires as conductive path. The wires are placed in the via hole of a silicon wafer by magnetic self-assembly. This metal filling technique enables through-wafer vias with high aspect ratios and potentially eliminates characteristic cost drivers of the TSV production such as metallization processes, wafer thinning and general issues associated with thin-wafer handling.

INTRODUCTION

During the past decades the hybrid integration of IC and MEMS technology has been dominated by (2D) side-by-side approaches in Multi Chip Modules (MCM) and System on Chips (SoC) solutions. CMOS and MEMS processing are both well-established and cost-effective base technologies where each technology itself is typically characterized by short development times, low fabrication costs and high yields. The separated manufacturing of CMOS and MEMS chips and their integration to a System in Package (SiP) as a final packaging step offers a high versatility and low process costs and thus is an attractive alternative to System on Chip solutions, where different technologies are merged onto one die. Especially 3D-integrated System in Package (3D-SiP) solutions, which are based on vertical chip stacking, are a general trend in many integration concepts. This integration method does not only decrease the costs by reducing the package size, its volume and weight but also improves the systems performance in terms of enhanced transmission speed, lower power consumption and lower parasitic capacitances due to shorter signal lengths, which is of importance for various demanding applications [1, 2]. 3D-SiP concepts require vertical interconnects through certain chips of the stack in order to connect their functional layers. Large development efforts for the realization of reliable and cost-effective TSVs are currently ongoing and first commercially available devices such as MEMS inertial sensors and microphones, CMOS imagers and power LEDs successfully incorporate TSV technology.

The structure and hence the fabrication of TSVs can be roughly divided into three major elements: A hole going

through the substrate, a conductive core and a dielectric material acting as an insulator between the conductor and the substrate (Fig. 1). The exact design of the via and the fabrication process flow depends very much on the application, i.e. the via integration concept.

Figure 1: Cross sectional view on basic TSV designs. a) Solid metal filled TSV, b) annular metal-lined TSV and c) metal-lined TSV with tapered side wall profile.

The diameter of via structures varies typically between 5 to 150 μm . Basic via designs are either based on solid (Fig. 1a) or lined metallizations (Fig. 1b, c) as vertical conductor. The vias can have either straight (Fig. 1b) or tapered sidewall profiles (Fig. 1c) [3] as well as combinations of both of them [4]. The majority of TSVs have an aspect ratio between 1 and 10. The most popular process techniques and challenges for the fabrication of the main TSV structures are in the following briefly discussed:

Via Holes

Various methods for the formation of via holes exist and can be categorized into dry etching [1, 3, 4, 5, 6, 7, 8, 9], wet etching [4] and drilling processes. Deep Reactive Ion Etching (DRIE) is by far the most commonly used technology to form the TSV hole due to its excellent process controllability and its capability to create high aspect ratio vias (up to 110:1) and adopted sidewall profiles and topographies. The etch rate of DRIE is aspect ratio dependent (ARDE) and may cause several topographic imperfections on the sidewalls, e.g. scalloping, caused by alternating etch- and passivation-steps, resulting in corrugated sidewalls. With state-of-the-art DRIE equipment this effect can be minimized [3] and adopted to the demands of subsequent insulation/barrier and/or seed-layer deposition steps.

Via Insulator

Chemical Vapour Deposition (CVD) is a well-established CMOS process with moderate temperature requirements [1, 2, 3, 5] and is therefore most commonly used method to deposit silicon dioxide or silicon nitride as via insulator. Organic dielectrics [6] such as Bisbenzocyc-

clobutene (BCB) [7, 15], SU8 [8], epoxy [7], silicone [7] or Parylene [9] are also used. These polymers, especially low-k types with a lower permittivity compared to silicon dioxide, enable the realization of TSVs with superior electrical characteristics [8]. Further they can act as a buffer for thermo-mechanical stress caused by CTE mismatches [7, 10] as their Young's modulus is almost two orders of magnitude lower compared to silicon dioxide and silicon nitride.

Via Filling

The metallization step is the most critical and often most costly part of the via fabrication. Established processes are electrodeposition of copper [4, 5, 7, 8, 9, 10], CVD of tungsten [2] or polysilicon [2, 3] and the use of low-resistivity silicon [6]. Especially the electrodeposition of copper as a very well established semiconductor process is widely used by most research groups to form the conducting path. The process benefits from its good availability and processability at close to room temperature conditions but suffers from its complexity in terms of throughput, reliability and process controllability [11]. Especially high aspect ratio TSVs with void-free conductive TSV metal cores are difficult to implement [5]. Alternative approaches to plating processes are therefore investigated, such as the filling with conductive metal pastes [1], the use of solder balls [12] and wire-bonded gold cores [15].

CONCEPT

This paper presents a novel approach for the TSV metallization and insulation process, which enables high aspect ratio vias with an inherently void-free conductor and insulator. As depicted in Fig. 2, the filling of the via with a conductive material is not realized by a deposition of a metal but by an instant filling technique, which magnetically assembles pre-formed conductive via cores into the via holes. The via insulator is a polymer, which acts both as low-k electrical insulator and buffer against thermo-mechanically induced stress.

Figure 2: Via formation concept: a) The via hole is formed by DRIE stopping on a silicon dioxide layer. b) A conductive, ferromagnetic nickel core is placed in the via hole by magnetic assembly. c) The remaining hollow space in the via cavity is filled with the thermosetting polymer Bisbenzocyclobutene (BCB).

Magnetic Assembly

Magnetism as a non-contact force enables a controlled manipulation of ferromagnetic features over long-distances and is insensitive to the surrounding medium and independent of details of the surface chemistry. Magnetic fields can have high energy densities and can influence feature sizes from macro- to nano-scale. These advantageous characteristics are very attractive and have been reported in various assembly approaches [13].

Ferromagnetic nickel has a similar electrical resistivity compared to tungsten, but is approximately 3 to 4 times higher compared to gold and copper. The thermal coefficient of expansion (CTE) of nickel approximately is 25 % lower as compared to copper. Volume manufactured nickel wires with diameters down to 10 μm are commercially available and are typically used for chemically resistant woven filter cloth, screen printing masks and recently also for wire bonded interconnections in high-temperature packaging of SiC electronics [14].

Fig. 3 shows hundreds of straight nickel wires that are aligned along the magnetic field lines of a underlying permanent magnet. The wires have a diameter of 35 μm and a length of 350 μm . By moving the magnet the wires can be moved and steered to certain positions, either directly on a substrate or into through via holes in the substrate.

Figure 3: Behavior of nickel wires in a magnetic field: a) about 300 straight nickel wires (35 μm diameter, 350 μm length) without an applied field. b) a magnetic field of 1.1 T is generated by a cylindrical permanent magnet. It aligns the nickel wires along the field lines and perpendicular to the ground plane.

FABRICATION

The fabrication process for the TSVs is depicted in Fig. 4 and is based on 300 μm thick double-side polished 100 mm-substrates with a 2 μm thick silicon oxide layer on both sides, which was created by thermal wet oxidization at 1100°C. The oxide acts both as a hard mask for the DRIE step and as an electrical insulator for the metal lines, which will finally connect the via on the front- and backside of the substrate. A standard lithography on the front-side of the substrate defines the circular openings for the vias. The silicon dioxide is dry-etched by RIE (Fig. 4b). As depicted in Fig. 4c), a Bosch DRIE process creates via holes with straight side walls. The etch stops at the silicon dioxide on the bottom of the cavity. A subsequent thermal oxidation ensures an electrical insulation of the via sidewalls.

Figure 4: The fabrication scheme can be divided into three main steps. First is the formation of the via hole by DRIE etching, second is the magnetic assembly of the conductive TSV core and third is the filling with the dielectric.

In order to produce a large amount of nickel wires with a defined length of $350\ \mu\text{m}$, several long nickel wires were placed parallel to each other on a handle substrate and subsequently embedded in AZ4562 photoresist. The wires were then diced in perpendicular direction by a wafer saw. The polymer matrix is then dissolved in acetone and the wire pieces are extracted with the help of a filter tissue.

As depicted in Fig. 4e), an excess amount of the nickel wires is randomly placed on the front-side of the substrate. The magnetic field of a cylindric permanent magnet from below aligns the wires normal to the surface (Fig. 4f). The permanent magnet has a diameter of 5 mm and generates a magnetic field of 1.1 T. The magnet is mounted on a manually operated xy-stage and is placed in a distance of about 3 mm below the substrate. A lateral movement of the magnet by the xy-stage moves the wires and forces them into the via cavities (Fig. 4g). The insulation filling of the cavities is performed by a manual application of BCB CYCLOTENE® 3022-46 (Fig. 4h). The subsequent hard-curing of the BCB is performed on a hotplate according to the manufacturer's standard process procedures. The curing procedure was performed in vacuum environment in order to prevent any void formation in the polymer.

A grinding and polishing step removes remaining nickel and BCB from the surface of the substrate (Fig. 4i). A subsequent lithography and RIE of the silicon dioxide and BCB residues opens the contact area of the via on the back-side of the wafer, as depicted in Fig. 4j). A final aluminum deposition on both sides of the wafer contacts the nickel core of the via. The structuring of both aluminum layers forms the signal lines to the TSVs (Fig. 4k).

EXPERIMENTAL RESULTS

The filling rate of a 30×30 array of via holes with a pitch of $120\ \mu\text{m}$ by magnetic assembly was determined. The assembly was conducted by a manual movement of a permanent magnet according to the previously described procedure. About 80 % of the wires are filled in a time span of about 20 seconds, as depicted in Fig. 5. The subsequent decline of the fill rate depends very much on the via pitch and the length of the wire pieces, i.e. the excess length of the wires, which are assembled in the via holes (Fig. 6). The excess wire length acts as physical obstruction especially for low via pitches. This results in a negative impact on the movement of the remaining free wires. In addition, magnetizing effects between the wires result in clustering of many wires.

Figure 5: Fill rate of a 30×30 via hole array: About 80 % of the wires are filled in a time span of about 20 seconds. Due to the small array pitch and magnetizing effects of the nickel wires the fill rate decreases. Three sub-images show a top-view on the array at a time of 0, 10 and 140 sec.

Figure 6: SEM image of a 30×30 array with a pitch of $120 \mu\text{m}$ of nickel wires placed in the via hole prior to the filling of BCB. The minimum via hole diameter for a $35 \mu\text{m}$ wire was determined to be $40 \mu\text{m}$.

Both the void-free dielectric filling with BCB and nickel have been investigated by cross-section grinding and subsequent inspection with a scanning electron microscope (SEM) (Fig. 7). The filling with BCB could be successfully conducted without any visible air-voids or defects after the complete hard curing procedure. Also, the nickel wire is inherently void-free. There are no indications for delamination of the BCB and the via side walls or the via core, which might cause mechanical or electrical failures of the vias.

Figure 7: SEM image of a cross section of a TSV with an aspect ratio of 8. It shows both, a void-free metal core and a void-free BCB-fill. Note: As indicated in the drawing, the sample was tilted during the grinding process of the cross section, which leads to the apparent view of a non-constant via diameter.

The electrical characterization of the TSVs was performed with a 4-point probe station and a digital multimeter. The via-resistances were measured to unexpectedly high values between 3 and 50Ω , which are likely caused by high contact resistances to the metallizations.

CONCLUSIONS

We have demonstrated a proof of concept for the fabrication of TSVs with an overall aspect ratio of 8. Smaller TSV diameters and higher aspect ratios are feasible but limited by the smallest commercially available diameter of ferromagnetic wires, which is $10 \mu\text{m}$ for nickel. Main fabrication objectives of state-of-the-art TSVs such as reliable fabrication of high aspect ratio TSVs, void-free solid metallizations, sufficient thermo-mechanical stability and reduction of fabrication costs are addressed by the presented concept.

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