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This is the accepted version of a paper presented at *21st International Conference on Noise and Fluctuations, ICNF 2011; Toronto, ON; 12 June 2011 through 16 June 2011.*

Citation for the original published paper:

Malm, G., Olyaei, M., Östling, M. (2011)

Low-frequency noise in FinFETs with PtSi Schottky-barrier source/drain contacts.

In: *Proceedings of the IEEE 21st International Conference on Noise and Fluctuations, ICNF 2011* (pp. 135-138).

<http://dx.doi.org/10.1109/ICNF.2011.5994282>

N.B. When citing this work, cite the original published paper.

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Low-frequency Noise in FinFETs with PtSi Schottky-Barrier Source/Drain Contacts

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Abstract— Schottky-barrier source/drain (SB-S/D) is a promising solution for low-resistive contact formation in fully depleted SOI ultra-thin body (UTB) FETs, or FinFETs. In this study the low-frequency noise of FinFETs and UTB-FETs, with platinum-silicide based source/drain contacts with low barrier height was characterized. The barrier height was tuned by means of segregation of implanted As or B. In the linear region of operation the noise power spectral density of devices with different barrier heights was not significantly affected for a given drain current. This suggests that channel noise dominates the behavior and that the low effective Schottky barrier height in dopant segregated devices does not introduce additional noise.

Keywords—Schottky barrier source/drain, dopant segregation, low-frequency noise, ultra-thin body, FinFET, trigate, asymmetric FET

I. INTRODUCTION

Schottky-barrier source/drain (SB-S/D) is a promising solution for low-resistive contact formation in fully depleted SOI ultra-thin body (UTB) FETs, or FinFETs. By use of dopant segregation techniques the schottky barrier can be effectively lowered [1]. In this study we have characterized the low-frequency noise of FinFETs and UTB-FETs, with platinum-silicide (PtSi) based source/drain contacts with low barrier height for both electrons and holes. It was previously demonstrated that presence of a source/drain Schottky barrier significantly influences the low-frequency noise of UTB devices [2, 3]. For devices with a mid-bandgap Schottky barrier, using NiSi, an increase of more than one order of magnitude in the noise under saturation conditions was observed, compared to reference devices with ohmic contacts [2]. Also as PtSi was used, the large electron barrier resulted in a large noise amplitude in the measured IV-characteristics for n-channel operation [3]. A Monte Carlo simulation analysis of gate and drain current noise under saturation conditions showed the influence of the barrier height in particular on the drain current noise [4]. For the devices investigated here a small barrier of about 0.15 eV, to the conduction and valence band respectively, was achieved, resulting in excellent IV-characteristics for both n-channel and p-channel devices [5].

The paper is organized as follows. Devices with different barrier heights were systematically characterized by IV and noise measurements, starting by p-channel devices with no dopant segregation present and hence in these the barrier was

not modified. Next we discuss results, obtained from p-channel devices with lower barrier. Furthermore, the study includes devices with low-barrier source and high-barrier drain, which were characterized in a gated-diode configuration. Finally results on n-channel devices with low electron barrier are shown for both UTB devices and FinFETs.

II. EXPERIMENTAL

Dopant segregation with As or B was used to modify the effective Schottky barrier height of PtSi towards the silicon channel region at implantation doses of 5×10^{15} and $1 \times 10^{15} \text{ cm}^{-2}$ respectively. For each wafer only one type of implantation was performed. In some device layouts the implantation was masked for both source and drain or alternatively only the drain was un-implanted. All contacts were formed using PtSi followed by the various implantations so no ohmic type of contacts was available. The substrate doping for all wafers was p-type $1 \times 10^{15} \text{ cm}^{-3}$ and hence n-channel devices work in inversion while p-channel devices work in accumulation. A silicon body thickness of 30 nm enabled simultaneous fabrication of UTB and FinFET devices. Using this fabrication scheme the FinFETs become trigate devices with gates on top and on the sidewalls of the fin. The fin dimensions width and height were 30 nm and 24 nm respectively and the gate length for most devices in this study was 90 nm. Longer channel devices were also measured in some cases. UTB devices had widths ranging from 6 to 25 μm and the width of FinFETs was scaled by the number of fins, two or four respectively. Noise measurements were obtained using a transimpedance amplifier (Femto DLCP200, gain setting $\times 10^4 \text{ V/A}$) and a battery powered bias network. In the linear operation region a fixed 50 mV drain-source voltage (V_{DS}) was applied. It was also possible to use the internal biasing of the amplifier to measure at varying V_{DS} and to get noise data in saturation.

III. RESULTS

Devices with no dopant segregation were initially characterized to establish a reference noise level for SB-S/D devices, with a Schottky barrier to the valence band present. The expected barrier height of PtSi towards silicon is approximately 0.19 eV. The IV-characteristics, shown in Fig. 1., revealed a variation in drain current (I_D) and sub-threshold behavior across different dies and also a slight

asymmetry as source and drain were interchanged. From previous analysis the variation could be related to the actual position of the PtSi to the channel interface [6]. It can also be observed that devices with a lower on-current have a slightly more pronounced ambipolar behavior, indicating higher hole barrier and lower electron barrier. Compared to the reference device, where boron segregation resulted in a lower effective barrier, it is also clear that the Schottky barrier limits the maximum current. Assymmetric devices, with dopant segregation for the source contact only, were included in the test structure layout on these wafers. Devices for p-channel operation, i.e. with B implantation at the source and unimplanted PtSi at the drain showed poor yield and we believe that gate current noise was dominant in these devices. Therefore these results are not further discussed.

Figure 1. IV-characteristics at V_{DS} of 50 mV for UTB p-channel FETs (no segregation, high barrier), ($L=90$ nm, $W=25$ μm) measured in forward and reverse source/drain configuration. Highlighted curve (circle symbols) represents typical device and bias points used in noise study. A reference low barrier device (square symbols, $W=6$ μm) is included for comparison.

The noise power spectral density S_{I_D} (PSD) was measured as function of drain current, from weak to strong inversion, as illustrated in Fig. 2. The threshold voltage (V_T) was estimated to around -0.5 V, but the shape of the IV-characteristics makes it difficult to give an exact value, due to the Schottky barrier present. The frequency dependence of the noise spectra was always close to $1/f$, no GR-type of noise was observed in this part of the spectrum (1-100 Hz). Since we focus on additional low-frequency noise, arising from the Schottky barrier, we have so far not investigated the effect on the thermal noise floor, which in principle should reflect a higher series resistance in these types of devices.

Figure 2. Power spectral density vs. gate voltage V_{GS} for UTB p-channel FETs (no segregation, high barrier), ($L=90$ nm, $W=25$ μm).

As shown in Fig 3, the normalized PSD S_{I_D}/I_D^2 exhibited relatively small variation when source/drain configuration was reversed. A closer look at the data for a drain current around 0.3 μA gives an estimation of a ratio of about 1:2 for the forward and reverse configuration respectively. Results from other devices fall within a similar range and support this observation. Also, the noise power order of magnitude is comparable, but somewhat higher than for the reference low barrier device. For the latter device the increased noise level at high drain current is attributed to the influence of series resistance or possibly gate current noise. A curve fitting of the relation $S_{I_D} \propto 1/I_D^\beta$ to the measured data, for both high and low barrier devices, reveals an exponent $1 < \beta < 2$. This points to number fluctuations in the channel carriers as the dominant noise source.

Figure 3. Normalized noise power spectral density vs. drain current at 10 Hz in forward and reverse source/drain configurations for UTB p-channel FETs (no segregation, high barrier), ($L=90$ nm, $W=25$ μm). Reference device with dopant segregation (low barrier), ($L=90$ nm, $W=6$ μm)

Figure 4. IV-characteristics at V_{DS} of 50 mV for two asymmetric FETs ($L=90$ nm, $W=25$ μ m) measured at different V_{GS} and V_{DS} polarities, to highlight the ambipolar behavior.

In the next section we discuss results for diode type of measurements, to highlight the influence of the Schottky barrier. Devices with As-implantation at the source (resulting in a low electron barrier) and un-implanted PtSi at the drain (resulting in low hole barrier/ high electron barrier) showed a very distinct ambipolar behavior, i.e. both hole and electron conduction can occur in the channel, see Fig. 4. To highlight this behavior, operation for both positive and negative V_{GS} and V_{DS} polarities is reported. The IV-data suggest that noise measurements could be done in four conceptually different configurations. For large positive V_{DS} the device essentially acts as a gated Schottky diode, while for large negative V_{DS} , saturated p-channel MOSFET operation can be obtained, but the current is severely limited and noise measurements become difficult. Note that the lowest gate bias, indicated by marker symbols, corresponds to what we refer to as ‘n-channel’ operation while for the other bias points the channel is in accumulation. The PSD is a weak function of gate voltage and the results are shown for two nominally identical devices (A & B) in Fig. 5.

Figure 5. Noise power spectral density vs. gate voltage at 10 Hz for UTB FETs with dopant segregation at source only, ($L=90$ nm, $W=25$ μ m).

We also show results for the same devices measured for varying V_{DS} at a fixed gate voltage in accumulation, see Fig. 6. It is found that the noise level is essentially controlled by the voltage applied to the Schottky drain-to-channel junction.

Figure 6. Noise power spectral density vs. drain voltage in accumulation ($V_{GS} \sim -1.8$ V) at 10 Hz for UTB FETs with dopant segregation at source only, ($L=90$ nm, $W=25$ μ m).

Finally, results are demonstrated from n-channel devices, both UTB wide channels and narrow channel FinFETs, with optimized low S/D barrier for electrons, using implantation and segregation of As. The IV data of short and long channel devices, shown in Fig. 7, present no evidence of a Schottky barrier and hence the noise properties are also expected to resemble behavior for normal FETs with ohmic source/drain contacts. It was found that UTB n-channel devices had significantly lower noise than the p-channel counterparts and were difficult to measure, due to strong short channel effects, resulting in a threshold voltage close to 0 V. For long channel ($L=0.5$ μ m), results are shown in both linear and saturation region in Fig. 8. These measurements suggest that noise is actually lower at sufficiently high V_{DS} , this could be related to the influence of Schottky barriers at S/D.

Figure 7. IV-characteristics of UTB n-channel FETs, no evidence of Schottky type S/D. Strong short channel effects observed for $L=90$ nm devices.

Figure 8. Normalized noise power spectral density vs. drain current at 10 Hz for UTB n-channel FETs, for linear and saturation drain bias conditions.

Figure 9. Normalized noise power spectral density at 10 Hz for FinFETs with As-dopant segregation ($L=90$ nm, $W=120/240$ nm respectively for 2 or 4 fins).

For the FinFETs, shown in Fig. 9, the device-to-device uniformity is good and scaling with number of fins is observed. The IV data for FinFETs also showed ohmic behavior and no evidence of Schottky S/D contacts was seen. However in comparison to UTB devices the noise levels are high, as expected for the case where conduction occurs on fin sidewall channels, which is an inferior interface compared to standard

(100) wafer surface. While these devices were effectively trigate the channel sidewall area is larger than the top gate area and is expected to dominate noise as well as IV-characteristics, including a positive V_T -shift.

IV. CONCLUSIONS

The low-frequency noise of UTB-FETs and FinFETs with platinum-silicide based source/drain contacts with low barrier height was characterized. In the linear region of operation the noise power spectral density of devices with different barrier heights was not significantly affected for a given drain current. This suggests that number fluctuation channel noise dominates the behavior and that the low effective Schottky barrier height in dopant segregated devices does not introduce additional noise. The dopant segregation technique was proven to effectively give low barrier n-channel devices, both UTB and FinFETs with lower noise than comparable p-channel devices. Comparison of noise data in linear and saturation region suggest that the influence of the Schottky barrier is more pronounced at lower drain bias voltage.

ACKNOWLEDGMENT

We acknowledge Valur Guðmundsson and Per-Erik Hellström for the processing of the devices in this study. The work was supported by the Swedish Science Council (VR) under contract 2008-5465, and ERC advanced investigator grant OSIRIS (91069) to M. Ö.

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